# High-performance zinc oxide transistors and circuits fabricated by spray pyrolysis in ambient atmosphere

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Research on solution processible semiconducting materials is rapidly making progress towards the goal of providing viable alternatives to silicon-based technologies for applications where lower-cost manufacturing and new product features such as mechanical flexibility and optical transparency are desired. One family of materials that has been the subject of intense research over the past twenty years is organic semiconductors.<sup>[1]</sup> Use of organic materials offers the prospect of low manufacturing cost combined with some desirable physical characteristics such as ease of processing and mechanical flexibility. Despite the impressive progress achieved in recent years a number of obstacles, especially poor air-stability, device performance that is insufficient for a variety of applications and device to device variability, have to be overcome before the advantageous manufacturability, and hence the economic benefits associated with organic semiconductors, can be fully exploited.

While research in the area of organic materials and devices has been intensifying, a different class of semiconducting materials, namely metal oxide semiconductors (MOxS), has emerged as possible alternative technology.<sup>[2]</sup> Metal oxides incorporate important qualities that are currently absent from organic-based semiconductors. For instance, they generally exhibit higher carrier mobilities which are already sufficient for use in optical displays, such as current-driven organic light-emitting diode (OLED) based displays. An additional advantage of MOxS relevant to many electronic applications is the superb optical transparency resulting

from their wide bandgap. The latter makes oxide semiconductors particularly interesting for use in transparent electronics<sup>[3]</sup> as well as in backplanes for the next generation of current-driven displays.<sup>[4,5]</sup>

For application in see-through electronics, in particular, transparent thin-film transistors (TFTs) with high switching speeds and low power consumption are required.<sup>[6]</sup> So far the opacity of amorphous silicon and the insufficient performance of organic semiconductors have impeded the development of such devices. In this respect, MOxS materials simultaneously fulfil the requirements for optical transparency and high charge carrier mobility. In addition, they provide excellent chemical stability combined with mechanical robustness.<sup>[7]</sup> A further advantage associated with MOxS is the diverse range of techniques that can be employed for thin-film deposition.<sup>[7]</sup> These include, sputtering,<sup>[8-10]</sup> pulsed-laser deposition (PLD),<sup>[11]</sup> metalorganic chemical vapour deposition (MOCVD),<sup>[12,13]</sup> as well as solution processing methods such as dip coating,<sup>[14]</sup> spin coating<sup>[15-18]</sup> and spray pyrolysis (SP).<sup>[19-21]</sup> Solution processing, in particular, offers a number of advantages, which are well known from the area of organic electronics, with the most important being the prospect of easy patterning on large area substrates. In most cases, however, control over the morphology of solution processed films is difficult and leads to low device yield and hence increased manufacturing cost. Therefore, the promise of oxide semiconductors as an enabling technology is only likely to be realised when a combination of simple processing and high performance can be achieved.

Here, we demonstrate the use of a simple deposition technique, namely spray pyrolysis, for the fabrication of high-performance low-voltage metal oxide electronics. The method is compatible with large area deposition and could potentially address both the issue of manufacturing cost and high operating voltages. To demonstrate this we realise high mobility (15 cm<sup>2</sup>/Vs) n-channel thin-film transistors based on zinc oxide (ZnO) deposited at substrate temperatures in the range 200-500°C. Semiconductor deposition is performed entirely in ambient atmosphere without any special precautions. It is established that the as-deposited ZnO films are of high quality and uniformity. Another key finding of this work is the compatibility of spray pyrolysis with a number of solution processible self-assembled monolayer (SAM) dielectrics. By combining SP with soluble SAM dielectrics, we are able to demonstrate ZnO transistors operating at voltages below |1.5| V. These transistors are used to fabricate unipolar inverter circuits with excellent operating characteristics, including low-voltage operation and negligible hysteresis. The SP method is simple and compatible with a wide range of precursor materials, facilitating for example the incorporation of suitable dopants (i.e. atoms or molecules) without the need for the stringent experimental conditions typically required by other deposition methods.

Among the many metal oxide semiconductors known<sup>[10,22-26]</sup> the II-VI group compound ZnO has attracted most interest because of its non-toxicity<sup>[17]</sup> and exceptionally high electron mobility.<sup>[13,27,28]</sup> In its crystalline form at room temperature, ZnO is characterised by a wide bandgap (~3.4 eV) and high optical transparency.<sup>[19]</sup> The highest field-effect mobility reported to date for polycrystalline films of ZnO is in the order of 30 cm<sup>2</sup>/Vs and is obtained from transistors fabricated at room temperature using sputtering.<sup>[28]</sup> Solution processed ZnO TFTs, on the other hand, yield lower mobilities that are typically in the order of 5 cm<sup>2</sup>/Vs.<sup>[18]</sup> Solution processing was also employed for the deposition of ZnO nanorods<sup>[29,30]</sup> as well as nanowires.<sup>[31]</sup> The highest electron mobilities obtained in these latter reports were in the range of 1-4 cm<sup>2</sup>/Vs.

In this work we employed SP for the deposition of ZnO thin films under ambient atmosphere. The relevant experimental details can be found in the *Experimental* section. Figure 1 shows the molecular structure of the precursor zinc acetate dihydrate and the schematic layout of our spray pyrolysis apparatus. The absorption spectra of ZnO films deposited at different substrate temperatures ( $T_S$ ) are displayed in Figure 2a. Films deposited at  $T_S \ge 200$  °C exhibit a clear absorption onset at around 370 nm, corresponding to an optical bandgap of approximately 3.35 eV. This is in good agreement with earlier reported values.<sup>[2,19,20]</sup> The surface morphologies of ZnO films deposited on SiO<sub>2</sub> substrates were studied by close-contact atomic force microscopy (AFM). Representative images are shown in Figure 2b. As can be seen, films deposited at  $T_s = 200^{\circ}C$  exhibit smooth surfaces with amorphous-like characteristics. Increasing the substrate temperature to values higher than 200°C, however, leads to ZnO films with rougher surfaces. This is probably because higher  $T_s$  lead to the formation of larger ZnO crystallites resulting in a rougher surface. Another contributing factor is that at higher  $T_s$  the solution droplets have less time to distribute into homogeneous films due to faster solvent evaporation.

To investigate the suitability of the SP method for the fabrication of functional devices we constructed a number of ZnO TFTs employing different device architectures. Details on the fabrication and electrical characterisation procedures are given in the Experimental section. Figure 3a displays the transfer and output characteristics obtained from a bottom-gate, topcontact (BG-TC) ZnO transistor (channel length and width of  $L = 60 \mu m$ , and W = 2 mm, respectively) fabricated by SP at 400 °C employing Al source/drain (S/D) electrodes. A schematic diagram of the device architecture is shown in the inset of Figure 3a. Excellent transport characteristics are obtained with maximum electron mobilities on the order of 15 cm<sup>2</sup>/Vs. Bottom-gate, bottom-contact (BG-BC) transistors employing gold S/D electrodes were also fabricated. Figure 3b shows the transfer and output characteristics obtained from a bottom-(BG-BC) ZnO transistor fabricated 400°C gate, bottom-contact at employing photolithographically defined gold S/D electrodes ( $L = 7.5 \mu m$ , W = 10 mm).

Figure 4a displays the electron mobilities extracted from the BG-TC and BG-BC transistors as a function of ZnO deposition temperature (T<sub>S</sub>). Table 1 summarises the various performance parameters of the transistors. A general observation is that the electron mobility for both transistor configurations increases with increasing deposition temperature in agreement with earlier reports.<sup>[32,33]</sup> Such an increase can be attributed to the improved crystallinity of ZnO films<sup>[21]</sup> and is consistent with the increased surface roughness shown in the AFM images in Figure 2b. Improved crystallinity is expected to yield larger domains and fewer grain boundaries present in the ZnO film both of which should lead to an increase in electron mobility with processing temperature. The highest mobility value obtained is on the order of 15 cm<sup>2</sup>/Vs and is obtained from BG-TC ZnO TFTs. It is to be noted that this value is among the highest electron mobilities reported to date for transistors based on solution processed MOxS films. To our knowledge the only values higher than 15 cm<sup>2</sup>/Vs have been reported only recently.<sup>[15,34,35]</sup>

Another interesting observation is the lower mobility values obtained from BG-BC ZnO transistors. This effect is attributed, partly, to the significant energy offset present between the Fermi level of the gold S/D electrodes ( $E_F = 5.1 \text{ eV}$ ) and the conduction band of ZnO (~4.4 eV) (the offset is much less pronounced in BG-TC devices where aluminium electrodes with a work function of 4.2 eV are employed). In addition to the energy offset, Göpel et al. also demonstrated that the Schottky barrier at the non-reactive Au-ZnO interface is qualitatively different from that of the rather reactive Al-ZnO interface.<sup>[36]</sup> This may also explain the differences in charge transport across the interface. In an effort to match the chemical properties of ZnO and the S/D electrodes, we fabricated ZnO TFTs using tin oxide S/D electrodes deposited also by SP (data not shown). Ohmic injection characteristics were obtained suggesting that SP is suitable not only for the deposition of the semiconducting layers but also for the deposition of transparent conductive electrodes. A further worth noting observation is the weak dependence of  $\mu_{e(s)}$  on temperature. This can clearly be seen in the Arrhenius plot of saturation mobility  $[\mu_{e(s)}]$  versus temperature (T) shown in Figure 4b. A plausible explanation for this effect is the band-like nature of the electron transport in ZnO deposited by SP. However, further work is needed in order to elucidate the exact transport mechanism.

The implementation of high-performance MOxS based integrated circuits not only requires TFTs with high carrier mobilities but also low operating voltages. In an effort to reduce the operating voltage of our ZnO transistors we have utilised phosphonic acid based ultra-thin gate dielectrics.<sup>[37,38]</sup> The molecular structure of the n-octadecylphosphonic acid (ODPA) employed is shown in Figure 5a. Experimental details of the deposition of ODPA onto an Al-AlO<sub>x</sub> bottom gate can be found in the Experimental section. Figure 5b shows pictures of water droplets on the Al-AlO<sub>x</sub> surface before and after treatment with ODPA. The significant changes in the water contact angle from  $\theta_{AIO_x} = (40 \pm 2)^\circ$  to  $\theta_{ODPA} = (105 \pm 2)^\circ$  confirm the presence of the hydrophobic monolayer. Interestingly, we find that high contact angles are preserved even after heat treatment of the samples at 400-450°C in N<sub>2</sub>. Detailed surface energy measurements reveal that the surface characteristics of Al-AlO<sub>x</sub>-SAM electrodes do not change significantly for annealing periods of up to 10 minutes. Hence, it can be concluded that phosphonic acid groups bond very strongly to AlO<sub>x</sub> and the insulating alkyl chains are not removed during annealing. Another important observation is that SAM functionalisation is found to drastically reduce the leakage current between the Al-AlO<sub>X</sub> electrode and an evaporated top aluminium electrode as shown in Figure 5c. Impedance measurements carried out on the same devices yield a geometric capacitance in the range 450-600 nF/cm<sup>2</sup> (obtained between 0.01 and 1 kHz). These results are consistent with previously reported values by Klauk et al., and from our group.<sup>[37,39]</sup>

To prepare low-voltage oxide transistors and integrated circuits employing SAM dielectrics we deposited ZnO on Al-AlO<sub>x</sub>-ODPA gate electrodes by SP followed by the evaporation of aluminium S/D contacts. Figure 6a-b shows the transfer and output characteristics of a SAMbased ZnO TFT ( $T_s = 400^{\circ}$ C), with channel length and width of 60 µm and 1 mm, respectively. The transistors exhibit excellent operating characteristics with minimum hysteresis. The device structure is shown in the inset of Figure 6a. As-prepared transistors exhibit n-channel characteristics with operating voltages of less than 1.5V. Table 2 summarises the performance parameters of SAM-based ZnO TFTs fabricated at different  $T_s$ . The extracted electron mobilities are comparable to values obtained from BG-TC transistors employing SiO<sub>2</sub> gate dielectric (see Table 1). To prove that the ODPA SAM layer plays a key role in reducing the leakage current to the gate electrode, we have also fabricated ZnO TFTs employing bare Al-AlO<sub>x</sub> gates. Surprisingly, operational transistors can be obtained even when functionalisation of the Al-AlO<sub>x</sub> gate with ODPA is omitted (data not shown). We attribute this to the unique matching of the two important chemical processes, (i) conversion of the zinc acetate dihydrate solution to ZnO, and (ii) further oxidisation of the surface of the aluminium gate electrode to AlO<sub>x</sub>. However, we note that low-voltage ZnO transistors without ODPA exhibit significantly higher gate leakage current, significantly lower on/off ratios (<10<sup>2</sup>) and reduced electron mobilities as compared to ODPA-based ZnO TFTs.

Using n-channel SAM-based ZnO transistors we have realised the first low-voltage unipolar oxide logic gates on glass. The transfer curves of a representative unipolar voltage inverter measured in air are shown in Figure 6c. The inset figure displays the circuitry of the inverter comprising two low-voltage ZnO transistors (TFT 1 and TFT 2) using 60 µm design rule (i.e., channel length). The circuit operates at voltages below 2 V and shows the correct logic function with signal gain >1. These results clearly demonstrate the potential of combining simple and low-cost deposition techniques for the fabrication of high performance transistors and logic circuits. These SAM-based ZnO transistors and circuits operate at lower voltages than state-of-the-art amorphous silicon TFTs and could arguably be considered as an alternative to amorphous and polycrystalline silicon in many electronic applications.

In conclusion, the present results demonstrate the possibility of combining two very simple deposition techniques, namely spin/dip coating of SAM-dielectrics and spray pyrolysis of MOxS, for the fabrication of high performance transistors and integrated circuits. Moreover, the compatibility of solution-processable SAM-dielectrics and large-area compatible spray pyrolysis deposition should be applicable to other metal oxides and can, therefore, be considered a major step towards low-cost, high-performance transparent electronics.

## Experimental

*Transistor fabrication:* Bottom-gate, bottom-contact (BG-BC) transistors were fabricated on heavily doped silicon (Si<sup>++</sup>) wafers employing a 200 nm thick SiO<sub>2</sub> gate dielectric. Gold source/drain (S/D) contacts were then patterned using standard photolithographic techniques. The SiO<sub>2</sub> surface was passivated using vapour deposited hexamethyldisilazane (HMDS). Bottom-gate, top-contact (BG-TC) transistors were fabricated on Si<sup>++</sup> wafers, acting as the gate electrode, employing a 200 nm thick SiO<sub>2</sub> dielectric. Aluminium (Al) S/D electrodes were thermally evaporated under high vacuum through a shadow mask following the deposition of ZnO films by spray pyrolysis. Low-voltage SAM-based transistors were fabricated as follows. Aluminium gate electrodes were thermally evaporated under high vacuum onto glass substrates. Gate electrodes were then exposed to oxygen plasma (5 min) prior to immersion of the samples in a 5 mM solution of octadecylphosphonic acid (ODPA) in isopropanol for 2 h. Substrates were then rinsed with isopropanol and dried in a furnace under N<sub>2</sub> at 140 °C. ZnO was then deposited by spray pyrolysis at different substrate temperatures. Finally, aluminium source/drain electrodes were thermally evaporated under high vacuum (10<sup>-6</sup> mbar).

*Transistor characterisation:* Device characterisation was performed under different conditions including; (i) under high vacuum ( $10^{-5}$  mbar), (ii) under inert atmosphere ( $N_2$ ), and (iii) under ambient atmosphere at room temperature. Electrical measurements were carried out using an Agilent Semiconductor Parameter Analyzer 4156C. Electron mobility was then extracted from the transfer curves in the saturation regime using the gradual channel approximation<sup>[40]</sup>

$$\mu_{e,sat} = \frac{L}{C_i W} \cdot \frac{\partial^2 I_D}{\partial V_G^2} \tag{1}$$

$$\mu_{e,lin} = \frac{L}{C_i W V_D} \cdot \frac{\partial I_D}{\partial V_G}$$
(2)

In Eq. 1  $C_i$  is the geometrical capacitance of the dielectric layer and L and W are the length and width of the transistor channel, respectively. The subthreshold slope *S* was calculated as the inverse slope of the transfer curve using

$$S = \frac{\partial V_G}{\partial (\log_{10} I_D)} \tag{3}$$

*ZnO deposition by spray pyrolysis:* A 0.2 M precursor solution of zinc acetate dihydrate  $(Zn(CH_3COO)_2 \cdot 2H_2O)$  was prepared in methanol. The substrates were kept at 200-500 °C on a hotplate, while aerosols of the solution were sprayed intermittently onto the substrates employing a conventional airbrush, held at a vertical distance of 20-30 cm (see Figure 1b). After a period of 12 seconds the spraying process was interrupted for 45 seconds to allow for the vapour to settle onto the sample before the cycle was repeated.

*UV-Vis and AFM characterization:* Optical absorption of the ZnO films on quartz substrates was measured at wavelengths between 250 nm and 800 nm in a UV-Vis absorption spectrometer. Height profile images of the ZnO surfaces were obtained using an atomic force microscope (Pacific Nanotechnology).

### Acknowledgements

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# Tables

T <sub>s</sub> [°C]	μ <sub>e(S)</sub>	V <sub>T</sub>	S	I <sub>ON</sub> /I <sub>OFE</sub>
0[-]	[cm²/Vs]	[V]	[V/dec]	
BG-BC usin	ig gold S/D elec	trodes		
(L = 10-40 µ	um, W = 10-20 r	nm)		
200	0.11	16	2.0	10 <sup>5</sup>
300	0.7	15	2.8	10 <sup>6</sup>
400	1.1	19	2.0	10 <sup>6</sup>
500	2	19	2.1	10 <sup>6</sup>
BG-TC usin	g aluminium S/[		ndee	
	W = 1 - 2  mm		Jues	
<u>200</u>	0.13	13.8	5.5	10 <sup>4</sup>
300	3.7	11.8	3.4	10 <sup>5</sup>
400	15	13.3	2.9	10 <sup>6</sup>
500	11.9	10.0	3.0	10 <sup>6</sup>

Table 1. Performance parameters of ZnO transistors based on SiO<sub>2</sub> dielectric.

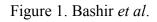
Table 2. Performance parameters of low-voltage BG-TC ZnO transistors based on  $AlO_x$ -SAM dielectrics. The channel length (L) of the TFTs was kept constant and equal to 60  $\mu$ m while the width (W) was varied within 1-2 mm.

T <sub>S</sub> [°C]	μ <sub>e(S)</sub> [cm²/Vs]	ν <sub>τ</sub> [V]	S [mV/dec]	$I_{\rm ON}/I_{\rm OFF}$
200	0.27	0.6	270	10 <sup>3</sup>
400	7.6	0.0	320	10 <sup>3</sup>
500	8.3	0.3	290	10 <sup>3</sup>

# **Figure captions**

- Figure 1. a) Chemical structure of the zinc acetate dihydrate precursor used. b) Schematic representation of the spray pyrolysis apparatus employed for the deposition of ZnO films under ambient conditions.
- Figure 2. a) Absorption spectra of ZnO thin films deposited at substrate temperatures (T<sub>S</sub>) in the range 200-500°C. b) Close contact atomic force microscopy (AFM) images of ZnO films deposited onto SiO<sub>2</sub> substrates at 200, 300 and 400°C.
- Figure 3. a) Transfer and output (inset) characteristics obtained from a bottom-gate, topcontact (BG-TC, see inset) transistor based on ZnO employing Al S/D contacts (L =  $60 \ \mu\text{m}$ , W = 2 mm). The ZnO layer was deposited by spray pyrolysis in air at T<sub>S</sub> =  $400^{\circ}$ C. b) Transfer and output (inset) characteristics obtained from a bottom-gate, bottom-contact (BG-BC, see inset) transistor based on ZnO employing Au S/D contacts (L = 7.5  $\mu$ m, W = 10 mm). Similarly, ZnO was deposited by spray pyrolysis in air at T<sub>S</sub> =  $400^{\circ}$ C.
- Figure 4. a) Electron mobility calculated in saturation for BG-TC and BG-BC ZnO transistors versus T<sub>s</sub>. b) Arrhenius plot of electron mobility (calculated in saturation) in a BG-TC ZnO transistor (T<sub>s</sub> = 500°C, L = 60  $\mu$ m, W = 1.5 mm) as a function of temperature.
- Figure 5. a) Chemical structure of the n-octadecylphosphonic acid molecule used as self-assembled monolayer (SAM) gate dielectric. b) Images of water droplets on the surfaces of Al-AlO<sub>x</sub>, Al-AlO<sub>x</sub>-SAM and Al-AlO<sub>x</sub>-SAM after annealing at 400°C in N<sub>2</sub>. The high contact angles of >105° measured for Al-AlO<sub>x</sub>-SAM surfaces following thermal annealing clearly demonstrate the thermal stability of ODPA monolayers. c) Leakage current density versus biasing voltage.
- Figure 6. (a) Transfer characteristics and (b) output characteristics measured from a lowvoltage ODPA-based ZnO transistor. Inset in (a) shows the BG-TC transistor

architecture employed (L = 60  $\mu$ m, W = 1 mm). ZnO was deposited by spray pyrolysis in air at T<sub>S</sub> = 400°C. b) Transfer characteristics of a unipolar voltage inverter comprising two low-voltage ODPA-based ZnO transistors (i.e. TFT 1 and TFT 2) measured at different  $V_{DD}$ . Inverter characterisation was performed in ambient atmosphere. Inset in (c) shows the circuitry of the unipolar inverter (using 60  $\mu$ m design rule).



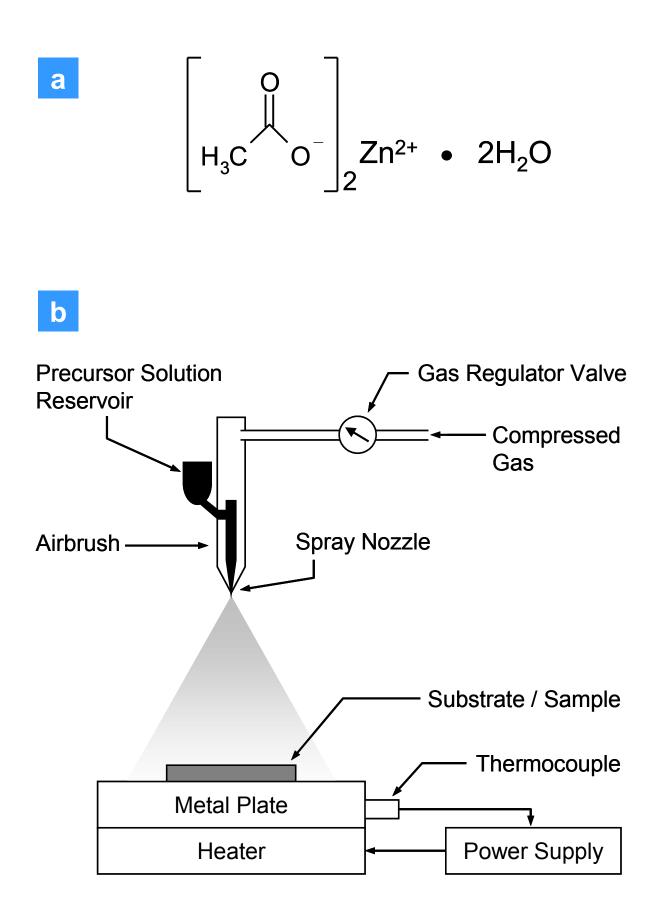


Figure 2. Bashir et al.

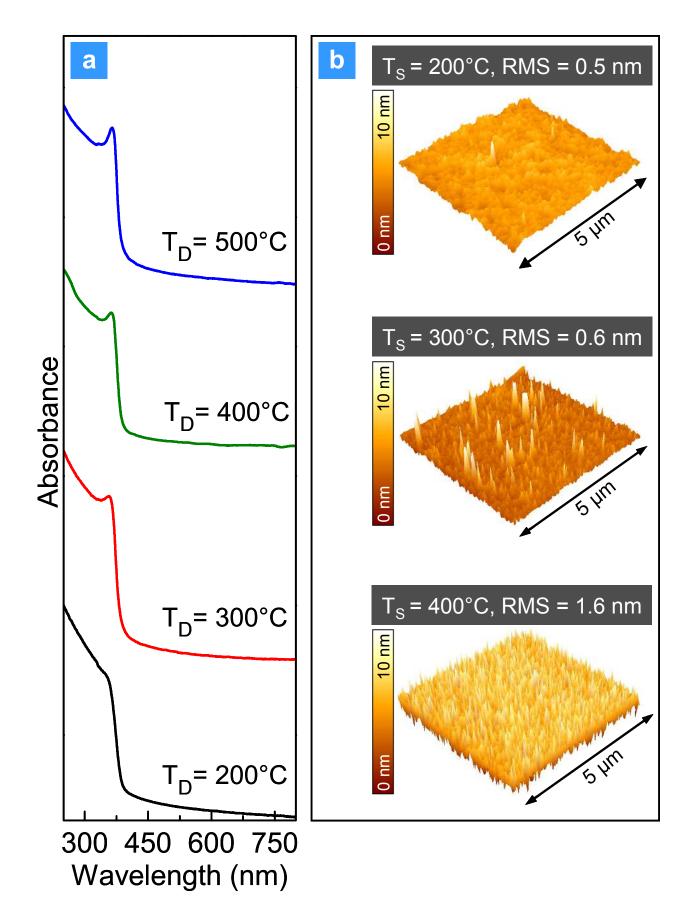


Figure 3. Bashir et al.

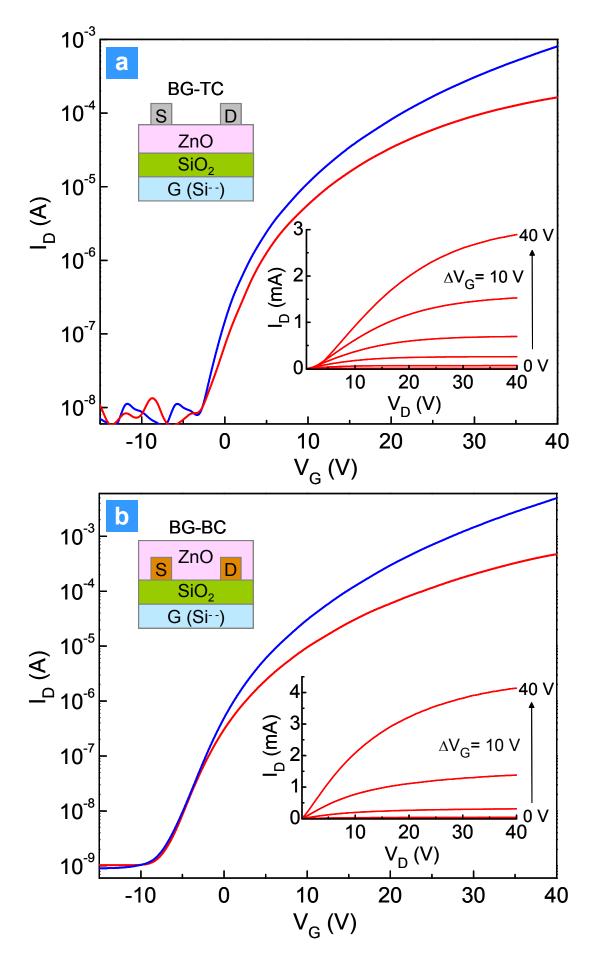


Figure 4. Bashir et al.

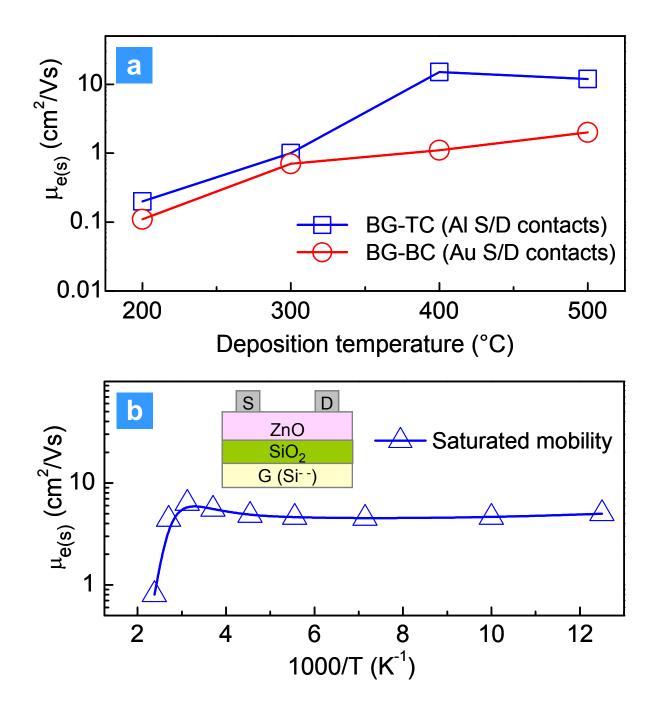


Figure 5. Bashir et al.

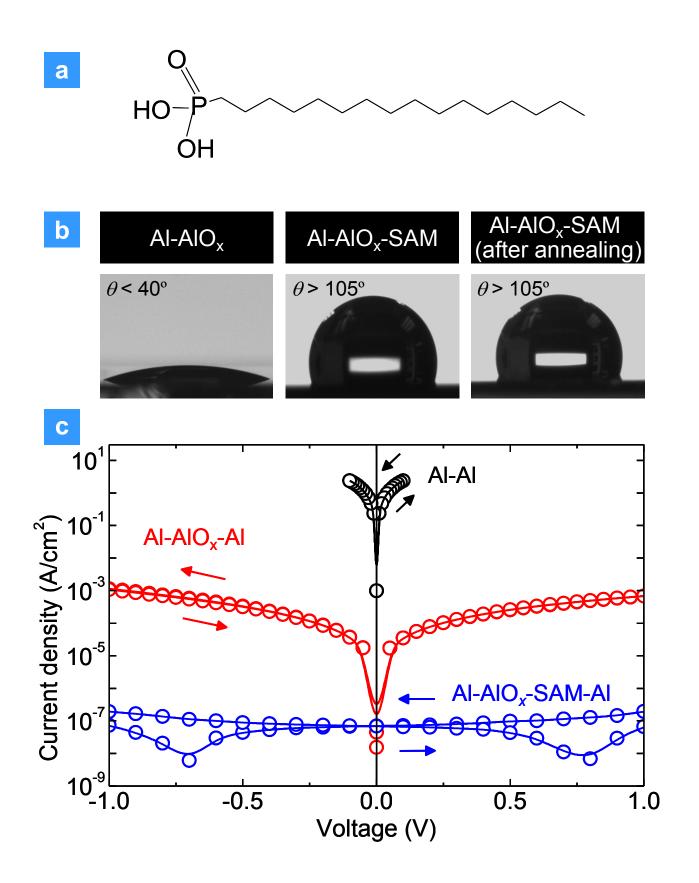


Figure 6. Bashir et al.

