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High Power Current Sensorless Bidirectional 16-Phase Interleaved DC-DC Converter for Hybrid Vehicle Application

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Abstract—A new 16-phase interleaved bidirectional dc/dc converter is developed featuring smaller input/output filters, faster dynamic response and lower device stress than conventional designs, for hybrid vehicle applications. The converter is connected between the ultracapacitor (UC) pack and the battery pack in a multisource energy storage system of a hybrid vehicle. Typically, multiphase interleaved converters require a current control loop in each phase to avoid imbalanced current between phases. This increases system cost and control complexity. In this paper, in order to minimize imbalance currents and remove the current control loop in each phase, the converter is designed to operate in discontinuous conduction mode (DCM). The high current ripple associated with DCM operation is then alleviated by interleaving. The design, construction, and testing of an experimental hardware prototype is presented, with the test results included. Finally, a novel soft switch topology for DCM operation is proposed for future research, to achieve zero-voltage switching (ZVS), or zero-current switching (ZCS) in all transitions.

Index Terms—Battery, discontinuous conduction mode, energy storage system, multiphase interleaved dc-dc converter, PHEV hybrid electric vehicle, soft switching, ultracapacitor.

I. INTRODUCTION

THE TRANSITION from internal combustion engine (ICE) vehicles to pure electric vehicles (EVs), or hybrid electric vehicles (HEVs) is very attractive and desirable, but there are still some serious issues with regard to energy storage technology. The lithium-ion battery is the most commonly used energy storage device in current hybrid vehicles, because of its high power and energy density. However, it has over-heating issues, limited life cycle, and durability limitations, especially under high power conditions. In contrast, the ultracapacitor has the advantages of a long life cycle, high output power and high reliability. Thus, the combination of batteries and ultracapacitors as an energy storage unit is a potential solution to improving vehicle performance, battery lifetime, and durability [1], [2]. It also offers excellent performance in both high acceleration

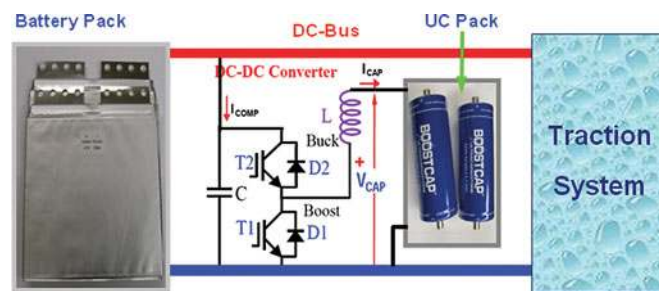


Fig. 1. Typical topology of a battery and ultracapacitor energy storage system.

and regenerative braking. The typical topology of a battery and ultracapacitor energy storage system is shown in Fig. 1. The battery pack is parallel connected with the ultracapacitor pack through a bidirectional dc/dc converter [3], [4]. One objective of the design is that the converter has to achieve a high power density with low current/voltage ripple, particularly on the battery side. Moreover, the converter has to meet basic automotive industry requirements, such as high efficiency, low cost, low EMI, and compact component size. Several different circuit designs for high power applications have been published [5]–[10]. Most of these designs require large inductors/transformers and devices with high voltage/current ratings. The volumes of these components are generally large [7]–[10], or the designs have the disadvantage of limited voltage ratio [5], [6]. A multiphase interleaved dc/dc converter is adopted as a good solution for the application with high power and high current with low current ripple.

Interleaving techniques have been widely used in power converters in recent years [9], [11]–[16]. Typical benefits of interleaving techniques include reduced device stress by separating power into each discrete phase, reduced filter size by increasing effective frequency, and alleviation of the effects of current ripple. The interleaving technique also enables other beneficial technology changes, such as replacement of aluminum electrolytic or polymer organic capacitors by film or ceramic capacitors, which improves the equivalent series resistance, power density, and reliability in a rugged thermal environment.

However, most of the published papers require a current control loop in each phase to achieve balanced phase currents and to improve dynamic response [13], [16]–[18]. The cost, weight, and control complexity grows when the number of phases increases, which limits the total number of phases to be considered. The optimum number of phases will be another issue that has to be considered [12], [19], [20]. The imbalance current

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mainly depends on duty cycle differences, inductance value differences, and parasitic resistance differences among different phases, all of which integrate over time in a continuous conduction mode converter. In order to minimize imbalance currents and eliminate current control loops, some authors designed a synchronous converter working in continuous conduction mode (CCM) [14], [15]. However, the inductor current falls to a negative value during every switching cycle, which would lead to a higher current ripple per phase and lower efficiency, especially for light load conditions.

This paper proposes the design of a 16-phase interleaved power converter operating in discontinuous conduction mode (DCM) that improves the current balance without using current control loops, which can simplify control system and reduce cost. This also allows the circuit to use a larger number of phases, which decrease power stress on each device and reduce filter size requirements. Therefore, compared to traditional dc/dc converters with current control, the proposed method is a cost-effective approach.

The design also features fast dynamic response since the phase current is reset to zero at every switching cycle. To verify the proposed approach, a 45-kW hardware prototype has been constructed and tested with experimental results presented.

II. INTERLEAVING DC/DC CONVERTER IN DCM

A. Interleaved Converter Topology and Operation

The multiphase interleaved dc/dc converter is a circuit topology where basic converter circuits are placed in parallel between input and output. The number of phases is in relation to efficiency, cost, volume, and control complexity. This paper adopts 16 phases based on a previous research [12]. Also, a 16 phase design will result in moderate current flow in each phase. Therefore, switches and filters will be smaller and easy to obtain/build. The optimization of the number of phases is a critical issue and will be further investigated in a separate paper. The schematic diagram of the 16-phase interleaved dc/dc converter is shown in Fig. 2. An ultracapacitor pack is placed on the low-voltage side with voltage range 86.4 to 172.8 V, and a battery pack is placed on the high-voltage side with a voltage range of 192 to 268.8 V. The battery voltage working range in this paper is designed to be compatible with 2004 Toyota Prius specifications. The high-voltage side is also connected with the traction system or load. When the demand power is larger than the battery pack rated power, the ultracapacitor pack releases power for acceleration and the converter operates in boost mode. When the ultracapacitor pack is not fully charged and the regenerative braking power is larger than the battery pack rated power, the ultracapacitor pack absorbs power from regenerative braking and the converter operates in buck mode.

The switch gate signals and inductor currents are shown in Fig. 3. The gate signals for the phases are exactly shifted by $360^\circ/N$ (N is the number of phases, here $N = 16$). All phase currents have the same waveform, except that they are shifted $360^\circ/N$. The ripple in the low voltage side current i_L , which is the sum of all low side phase-currents, is significantly reduced

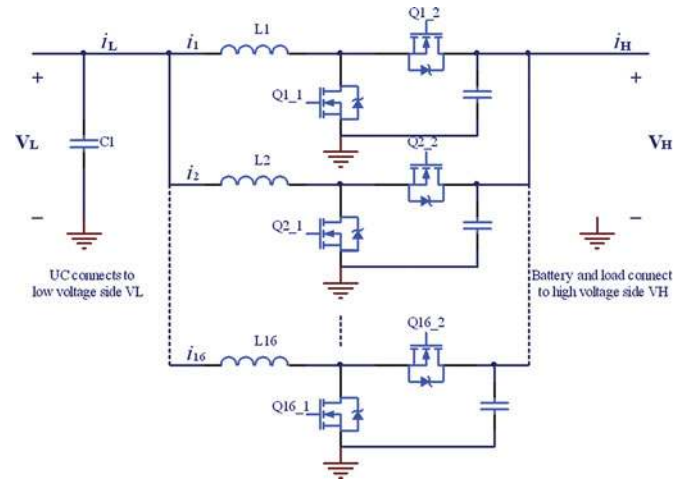


Fig. 2. Power stage of a 16-phase bidirectional DC/DC converter.

due to harmonic elimination. Furthermore, the frequency of the ripple in i_L is increased to $N \cdot f_s$ (f_s is the switching frequency).

Because of lower current ripple and less harmonic content, the size of the filter capacitance on the low voltage side can be reduced, or even removed. The filter capacitance on the high side is composed of N capacitors. Each one is placed physically close to its phase, in order to reduce the parasitic inductance between the switch and the capacitor. Each phase processes only $1/N$ of the total power, which, therefore, reduces the stress on the switching devices.

B. Synchronous DC/DC Converter in DCM

This proposed design is working in DCM so that the system has a small imbalance current and fast response, since the inductor current is reset to zero at every switching cycle. Moreover, the inductance requirement for each phase is small in DCM. The converter current is related with duty ratio directly in DCM, which could simplify the control system.

In boost operation mode, the duty ratio of the main switch (low side switch, e.g., Q1_1) is a function of output current, and can be calculated by the following equation:

$$D_{\text{boost}} = \sqrt{\frac{2L f_s I_H (V_H - V_L)}{N \cdot V_L^2}} \quad (1)$$

where L is the inductance in each phase, f_s is the switch frequency, I_H is the average current on the high voltage side, V_H is the voltage on the high voltage side, V_L is the voltage on the low voltage side, and N is the number of phases.

In a synchronous converter in CCM, the duty ratio D' of the freewheeling MOSFET equals \bar{D} with necessary dead time. In DCM, the freewheeling MOSFET has to be turned OFF by zero current detection on the inductor current, or the on-time is estimated by the control stage. In this paper, the on-time of the freewheeling MOSFET is estimated by the following equation in boost mode

$$D'_{\text{boost}} = \frac{D_{\text{boost}} \cdot V_L}{V_H - V_L} \quad (2)$$

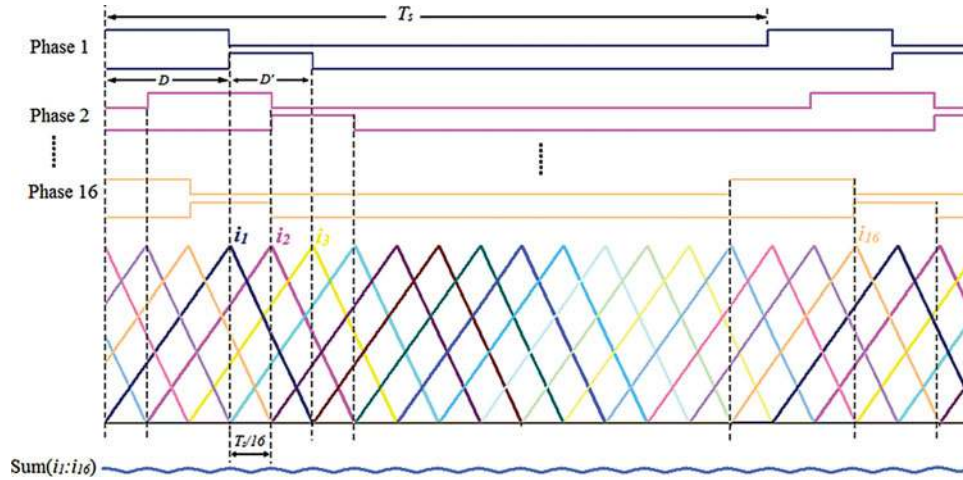
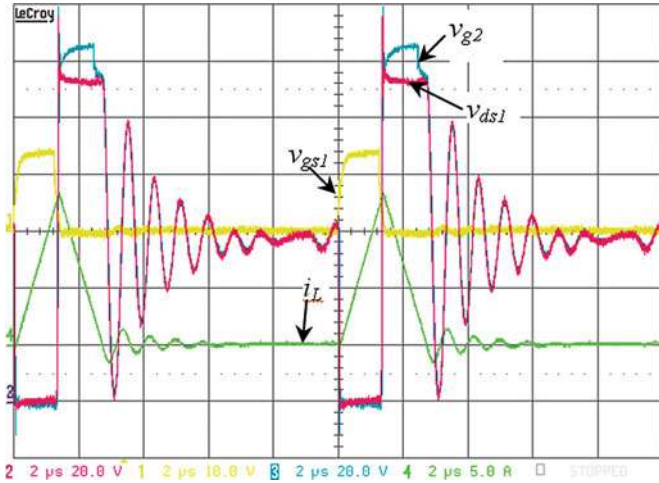
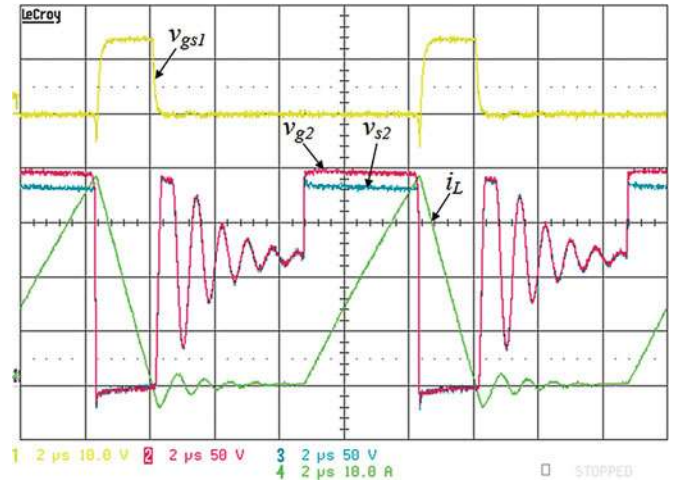


Fig. 3. Gate signals and inductor currents waveforms.


 Fig. 4. D' estimation result in boost converter (see v_{g2}).

 Fig. 5. D' estimation result in buck converter (see v_{gs1}).

In buck operation mode, the duty ratio functions for the main switch and freewheeling MOSFET are calculated by (3) and (4), respectively

$$D_{\text{buck}} = \sqrt{\frac{2Lf_s I_L V_L}{N \cdot V_H (V_H - V_L)}} \quad (3)$$

$$D'_{\text{buck}} = \frac{D_{\text{buck}} \cdot (V_H - V_L)}{V_L}. \quad (4)$$

Figs. 4 and 5 show the results of D' estimation by (2) for the boost converter and (4) for the buck converter. These results show the slave switch turns OFF close to where the inductor current reaches zero and thus the D' estimation equations work well in the real system. After the inductor current falls to zero, the circuit experiences some voltage oscillations due to the influence of the inductor and parasitic capacitances of the switches. These voltage oscillations cause only very small losses in each phase, since all devices are turned OFF and the current is almost zero. Furthermore, they do not overstress the devices. The oscillations can be reduced by adding an RC snubber circuit

between each switch and transfer losses caused by oscillation from switch to the snubber circuit. However, when observed from input and output of the whole converter with the proposed interleaving techniques, these oscillations will not be apparent, even if snubber circuits are not added.

From the above equations, it is noted that the imbalance current depends primarily on duty ratio differences and inductance differences. However, in DCM mode, the imbalance current is very small since each phase current starts from zero at every switching cycle. A 1% difference in duty cycle will cause a 2% increase of current imbalance in theory. In CCM mode, however, a 1% difference in duty cycle can cause an unacceptable current imbalance (for example, 84% imbalance current in [12]) over time. In order to minimize the difference in each duty cycle, digital controllers, such as field-programmable gate arrays (FPGA), can generate many signals simultaneously with high accuracy [21]. The phase shift techniques are also implemented in the digital controller.

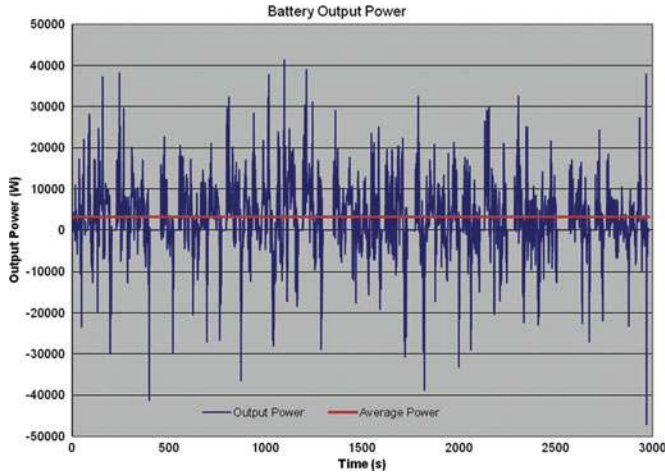


Fig. 6. Battery power requirement during urban driving for battery power alone system.

C. Control Stage Design

There are two control stages in this energy storage system: power distribution control stage and the converter control stage.

The power distribution control stage determines the power distribution between ultracapacitor power and battery power. While a vehicle is driving, especially in urban conditions, the power requirement changes frequently. A simulation-based battery power requirement model has been built with battery power requirement shown in Fig. 6 [23]. The simulation was based on local driving conditions in urban an area of Lincoln, Nebraska, using a 2004 Toyota Prius data with assumption of Lithium-ion battery presented in this paper. Detailed modeling and calculation of the battery power requirement is available in [23].

In order to improve the battery lifetime and meet the overheating limitation, the ultracapacitor provides/absorbs most peak power and the battery is kept at almost constant power. Thus, it is important to ensure the ultracapacitor stores enough power to release during acceleration, and has enough room to absorb power during braking. A system control strategy has been designed to keep the ultracapacitor voltage in a range at different vehicle speeds as in reference [24] and shown in Fig. 7. According to the ultracapacitor voltage, the battery SOC and the traction demand power, the control system gives out the demand power for dc/dc converter.

The converter control stage will generate the driving signals for the 16 phases according to dc/dc converter demand power, that is, in total 32 gate signals need to be generated. Using digital control, these pulses can be timed to a high accuracy level such that the differences of duty ratio between each phase are very small and the imbalance current can be minimized. Thus, a current control loop in each phase can be removed and the complexity of control circuit can be reduced. The main switch duty ratio can be calculated by (1) in boost mode and (3) in buck mode in the open-loop control system. Also, the control can be achieved by a simple proportional-integral controller (PI) in the closed-loop control system. The duty ratio of freewheeling

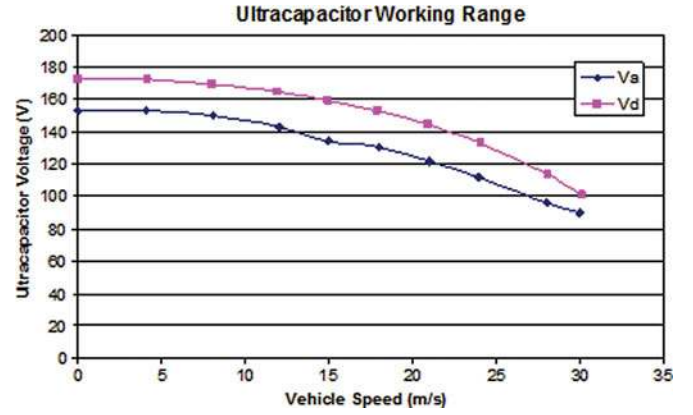


Fig. 7. Ultracapacitor voltage working range at different vehicle speed (between V_a and V_d). V_a is the voltage to ensure that ultracapacitor can provide enough power for acceleration; V_d is voltage to ensure that ultracapacitor has enough room to absorb power during braking.

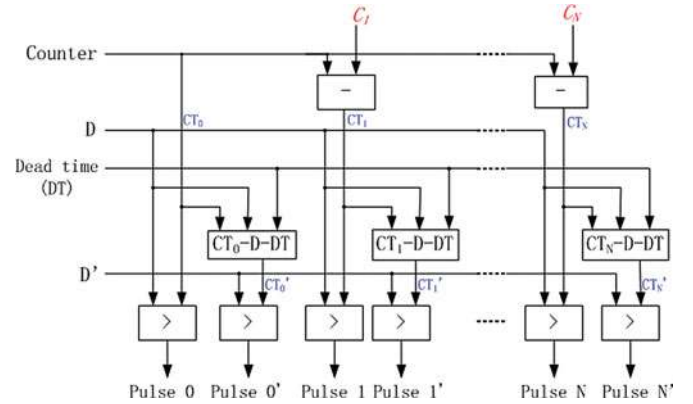


Fig. 8. Phase-shifter structure implemented in an FPGA.

transistor is calculated by (2) in boost mode and (4) in buck mode. Each driving signal is shifted from the previous one.

The gate signals are generated by making a comparison between the duty cycle and the counter. Each phase has its own counter. The phase shift is achieved by controlling the value of the counter. The phase-shifter structure is shown in Fig. 8. There is a main counter, with the calculation of other counters based on it (see CT_0 in Fig. 8). For the main switch in each phase, these subordinate counters are the value of the main counter minus some constants to get subordinate counter values, and then each is compared to the duty cycle. The main switch counter CT_i and constants C_i to be added are:

$$CT_i = CT_0 - C_i \quad (5)$$

$$C_i = \frac{i \cdot C_p}{N + 1} \quad (6)$$

For the slave switch of each phase, the counter value can be calculated as

$$CT'_i = CT_i - D - DT \quad (7)$$

where, i is the phase number, $(N+1)$ is the number of the phase, C_p is the resolution of the period which is equal to the range of the counter, and DT is the dead time.

TABLE I
CORE LOSS CALCULATION FOR DIFFERENT CORE MATERIALS

Core material	μ	l_e (cm)	A_e (cm ²)	V_e (cm ³)	Turns N	B_{pk} (mT)	Core Loss (W)
Xflux (Powdered)	135	10.74	1.99	21.3	6.0	132.9	63.9
-66 (Powdered)	130	33.1	5.24	173	6.2	49.6	88.2
3F3 (Ferrite)	1660	12.7	2.80	35.5	6.6	86.95	2.0
3C94 (Ferrite)	1770	12.7	2.80	35.5	6.5	87.85	1.6

TABLE II
DC/AC RESISTANCE AND WINDING LOSS CALCULATIONS

R_{dc} (m Ω)	R_{ac} (m Ω)	P_{dc_loss} (W)	P_{ac_loss} (W)
1.383	16.60	1.42	13.8

The FPGA NI 7831R real-time system, used in this converter, has a 40 MHz on-board frequency generator with a high duty cycle resolution (400 different duty cycles for 100 kHz switch frequency).

D. Inductor Design

The inductors used in this interleaved dc/dc converter have low inductance value, but work at high frequency with high current ripple. Therefore, the inductor losses become a main issue during design. The inductor losses mainly include core loss and winding loss. The core loss is related to the core material used, and has been calculated for different core materials at rating power ($L = 5 \mu\text{H}$, $I_L = 32 \text{ A}$, $f = 100 \text{ kHz}$, $V_L = 87 \text{ V}$, $V_H = 268 \text{ V}$), shown in Table I. A 1.5 mm air gap is adopted for ferrite core material during calculation.

According to Table I, the core loss of ferrite core materials is much lower than the powdered core materials. Therefore, the ferrite core 3C94 has been chosen for inductors in the dc/dc converter.

Winding losses mainly include dc winding losses and ac winding losses. DC resistance can be calculated according to wire length; ac resistance is estimated according to [22]. Resistance values and winding losses are calculated at the above condition, and the results are shown in Table II.

When ferrite core material is chosen, using a single concentrated airgap, the gap induced eddy current loss in the conductors has to be considered, especially for inductors working at high current ripple and high frequency. Any winding turns positioned close to the gap will most likely exist within the high flux density of the fringing field and huge eddy current losses can occur in those few turns close to the gap, which can cause severe localized heating problems, even leading to the failure of the inductor. To reduce the gap-loss and avoid the winding heating, the following actions were taken during experiment hardware design: 1) using Litz wire winding to reduce ac winding loss; 2) keeping the windings positioned close to the air gap to a single layer; and 3) keeping other windings a little distance from

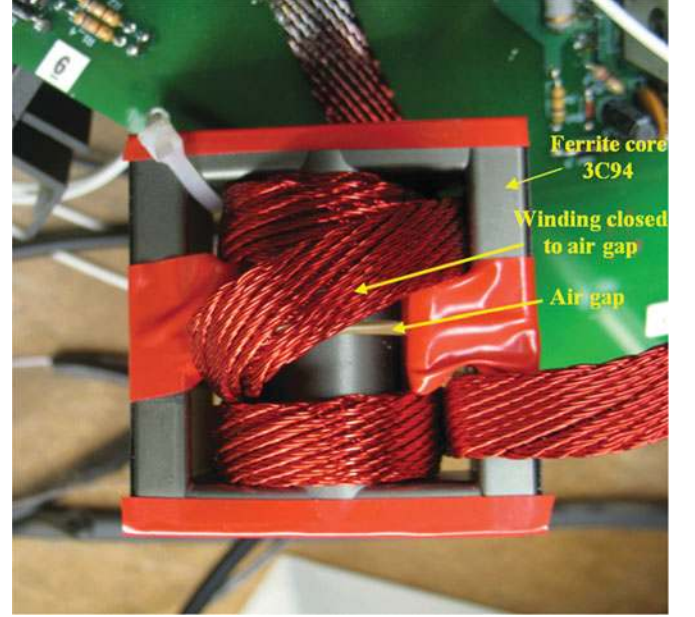


Fig. 9. Photo of a hand-wound inductor.

air gap. Fig. 9 is a photo of a hand-wound inductor in the dc/dc converter circuit. The bobbin has been eliminated to save space in the board.

E. Power Loss Analysis

Power losses of multiphase dc/dc converter, similar to traditional single phase of dc/dc converter, mainly include inductor loss, switch device loss and input/output capacitor loss. Input/output capacitor loss should be considered in whole system, and total capacitor loss would be lower than signal phase. In this paper, most of losses are from main switch due to high peak current in DCM in each phase. The inductor loss has been discussed in the previous section. This section focuses on MOSFET losses in a boost converter.

Conduction losses are defined by the $R_{DS(on)}$ of the MOSFET. The losses can be estimated by the following

$$P_{cond} = I_{RMS}^2 \cdot R_{DS(on)}. \quad (8)$$

Here the I_{RMS} is the triangular current through the MOSFET, not the output current of the converter.

The low side MOSFET loss during switch turned ON is negligible because it has zero-current switching in DCM; the loss during switch turned OFF is the main loss in the whole system due to high peak current in each phase. It can be estimated by following

$$P_{sw(off)} = \frac{V_H \cdot I_{pk}}{2} \cdot t_{sw_off} \cdot f_{sw} \quad (9)$$

I_{pk} is the inductor peak current, t_{sw_off} is the transition time from switch on to off, and f_{sw} is the converter switching frequency.

The switching loss of high side MOSFET is negligible, because it has almost zero-voltage switching when turned ON due to the conduction of its body diode and zero-current when turned OFF due to DCM.

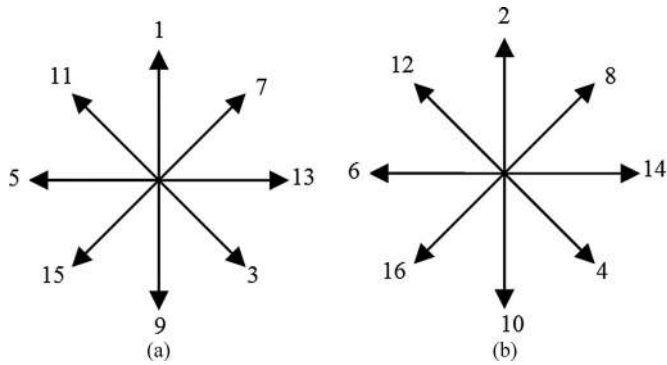


Fig. 10. Physical phases position with optimized order for two boards. (a) Physical positions of odd phases. (b) Physical positions of even phases.

There is a dead time between low side MOSFET turned OFF and high side MOSFET turned ON. The inductor current goes through the diode, which is parallel with high side MOSFET. The calculation of the diode power loss can be taken by using the following parameters: forward voltage drop of the body diode V_D , the source to drain body diode current I_{SD} , the dead time t_D and switching frequency f_{sw}

$$P_{DT} = V_D \cdot I_{SD} \cdot t_D \cdot f_{sw}. \quad (10)$$

The losses in MOSFET also include reverse recovery loss, output capacitor loss, and gate drive loss. These losses are much smaller than switching loss.

F. PCB Board Topology

In order to minimize imbalance current among phases, the structural differences between phases should be minimized. The heat sink and inductor occupy a large volume in each phase. Therefore, it would be congested if all 16 phases were placed on a single circuit board. The 16 phases are separated into two boards with each board having 8 phases, distributed as a star-shape with optimized phase order. Fig. 10 shows the physical phase positions of two boards with phase numbers labeled. One board hosts the odd phases and is ordered with minimized parasitics. The other board hosts the even phases and is also ordered with minimized parasitics. The capacitors in each high voltage side are composed of 16 film capacitors, with each one placed close to its phase, to reduce harmonics in the circuit. The star-shaped distribution is used to maintain the same physical distances for each phase. The optimized phase order not only keeps each phase under the same operation condition but also allows precise harmonic elimination and current ripple reduction in the high side capacitor.

III. EXPERIMENT AND RESULTS

Based on the above design methodology, a 16-phase bidirectional dc/dc converter without current control loops has been built and tested. The converter is connected with resistance load instead of propulsion motor in the experiment. A photo of the 16-phase prototype is shown in Fig. 11(a), which is composed of two circuit boards with each one hosting an 8-phase converter, shown in Fig. 11(b).

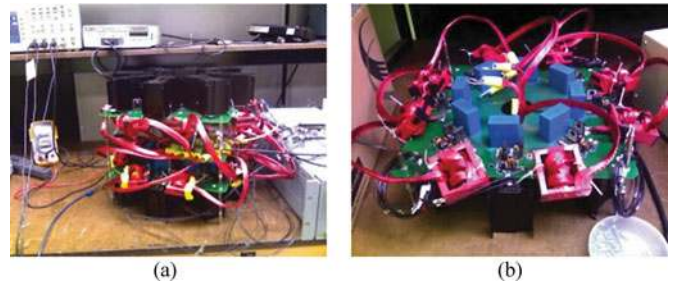


Fig. 11. Photos of prototype interleaved dc/dc converter. (a) 16 phases on two boards. (b) 8 phases on one board.

In the experimental hardware design, the following components have been used: Power MOSFET IRFP4242; Gate driver FAN7390; Inductor $5 \mu\text{H}$, ETD54 core, and 3C94 material with Litz wire winding; low side capacitor $30 \mu\text{F}$; and high side capacitor $240 \mu\text{F}$ (composed of 16 film capacitors of $15 \mu\text{F}$ each). The gate control signal has been implemented by applying an FPGA board (National Instrument NI-7831R FPGA, 40 MHz) programmed by a PC. The complete converter power rating is 45 kW and the switching frequency is 100 kHz.

The imbalance currents are mainly caused by the differences in inductance and duty ratio among each phase. Fig. 12 shows the inductor current of each phase and the total current before/after the capacitor filter. The differences in current of each phase are primarily caused by the differences in manufacturing of the individual inductors. The differences in the duty ratio between phases are very small because of the high accuracy of the driving signals generated by the FPGA. The results show that based on the proposed design discussed above, the imbalance current among these phases is very small. Based on the test results, it is concluded that in general a 1% difference in inductance causes a 2% or less current imbalance. The ripple of total current from 16 phases before filtering is much smaller than that of individual phase currents. Therefore, it is possible to get a lower ripple current in the low side of the converter using a small capacitor filter.

To validate the effectiveness of this approach, an external 0.5% and 1% extra duty cycle has been applied to Phase 14 to compare the inductor current with and without an incremented duty cycle condition. Figs. 13–15 and Table III show the results of this experiment. Phase 15, without an extra duty cycle, is chosen to compare with Phase 14 in Table III since the inductance in these two phases is very close. The results show that the current imbalance is still acceptable and the performance is very good even with an extra 1% duty cycle. Normally, the differences in the duty ratio in an FPGA are very small, typically less than 0.25% in this application.

The power rating for this dc/dc converter is 45 kW with 2.82 kW in each phase. Due to equipment limits, only a 5.5 kW experiment can be carried out in the laboratory. The efficiency, as a function of input power for one stage boost/buck converter, is shown in Fig. 16, operating up to rated power of 2.82 kW. The efficiency of buck converter is a little higher than that of boost converter. The efficiency values for 2 phases, 8 phases, and 16 phases of boost converter is shown in Fig. 17, up to

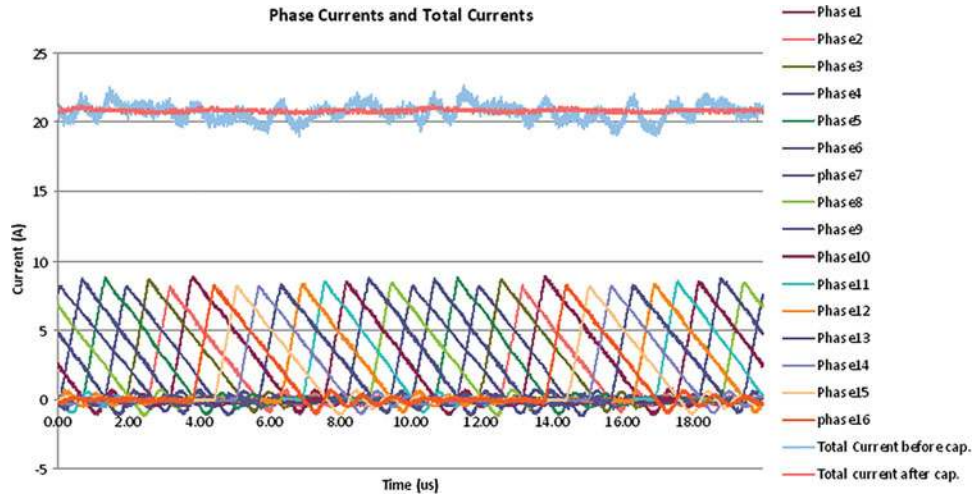


Fig. 12. Inductor current of each phase and their total current with/without capacitor filter.

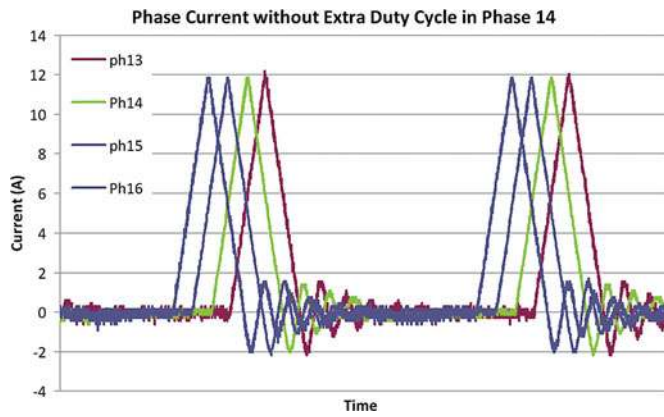


Fig. 13. Phase current without extra duty cycle in Phase 14.

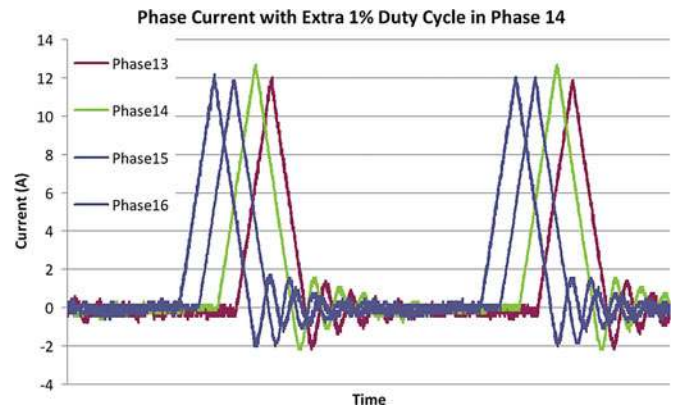


Fig. 15. Phase current with extra 1% duty cycle in Phase 14.

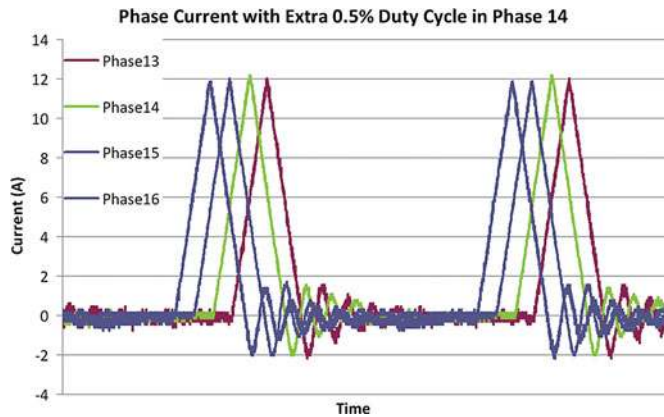


Fig. 14. Phase current with extra 0.5% duty cycle in Phase 14.

5.5 kW. The efficiency for 16 phases is high and there is a trend that indicates that the efficiency will be higher if more power were taken from it. The loss analysis is provided in Table IV for the 16-phase boost converter. Most of the losses are from low side MOSFETs in the boost converter and over 90% of these losses are from switching losses, due to the large peak current

TABLE III
IMBALANCE CURRENT INDUCED BY DIFFERENTIAL DUTY RATIO

Extra duty ratio in Phase 14	Average current in Phase14 (A)	Average current in Phase15 (A)	$1-I_{14}/I_{15}$
0%	1.32	1.31	0.8%
0.5%	1.38	1.32	4.5%
1%	1.48	1.33	11%

in the inductor and high switching frequency. The input/output capacitor losses are categorized as “Other Losses.”

Two phases of the boost converter operating at 5.4 kW level have been tested, with the results shown in Fig. 18. The low side voltage is 172.8 V and the high side voltage is 236 V. The peak inductor current, I_L , is 50.3A. V_{ds1-1} and V_{ds2-1} are drain-source voltages in the low side of MOSFETs in two phases. There are high voltage spikes in those waveforms due to high di/dt values. The efficiency for the two-phase boost converter is 94.9% at 5.4 kW.

Sixteen phases of the boost converter operating at 5.1 kW have been tested with the results shown in Fig. 19. The low side voltage is 163 V and the high side voltage is 195 V. The peak inductor current, I_L , is 14.22 A. The efficiency is 95.3%.

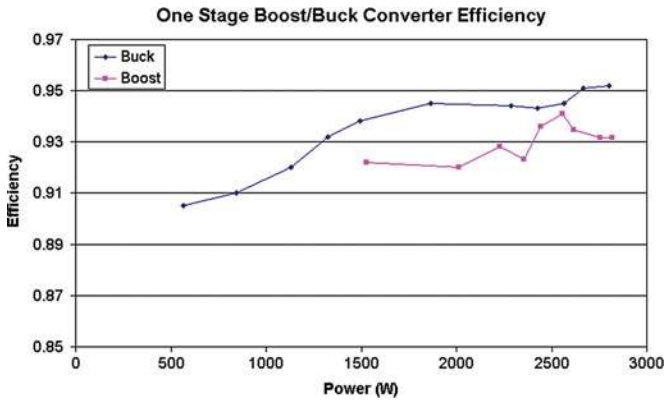


Fig. 16. One stage boost/buck converter efficiency at various input powers.

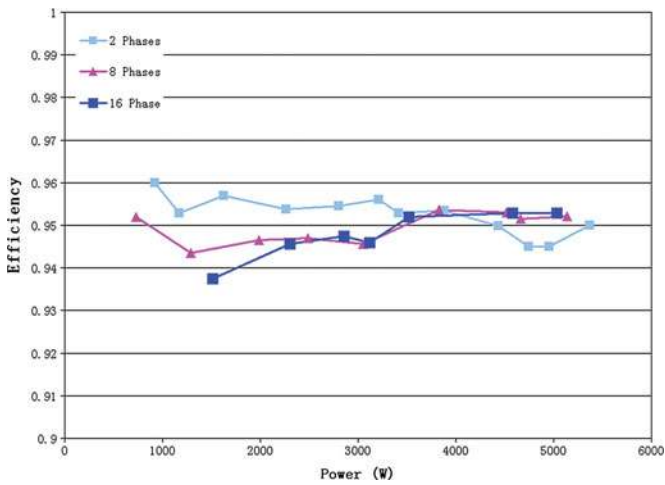


Fig. 17. Efficiency of boost converter with 2, 8, and 16 phases versus various input powers.

TABLE IV
LOSS DISTRIBUTION OF 16-PHASE BOOST CONVERTER OPERATED AT 100 kHz WITH 5.1 kW INPUT POWER

	Low side MOSFETs	High side MOSFETs	Inductors	Oscillation circuit losses	Other Losses
Losses (W)	139.2	32.0	14.5	15.6	35.0
% of Total Losses	59%	13.5%	6.1%	6.6%	14.8%

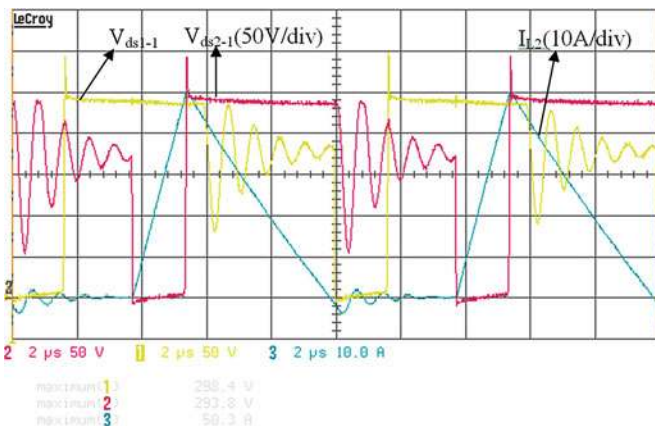


Fig. 18. Low side MOSFET voltage V_{ds1} and inductor current of two-phase boost converter at 5.4 kW.

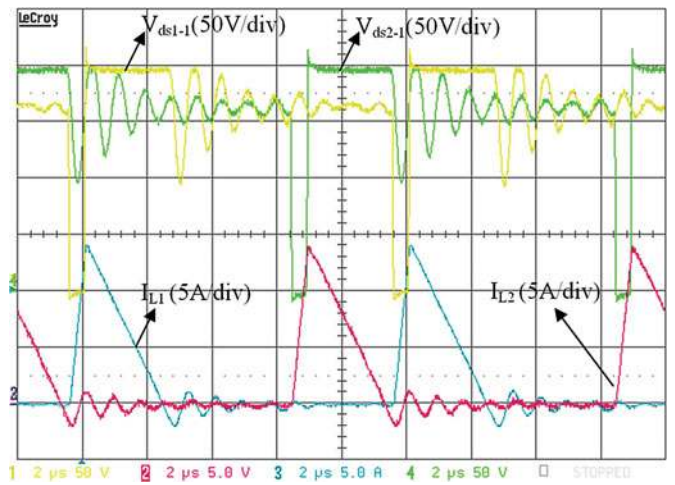


Fig. 19. Low side MOSFET voltage V_{ds1} and inductor current of 16-phase boost converter at 5.1 kW.

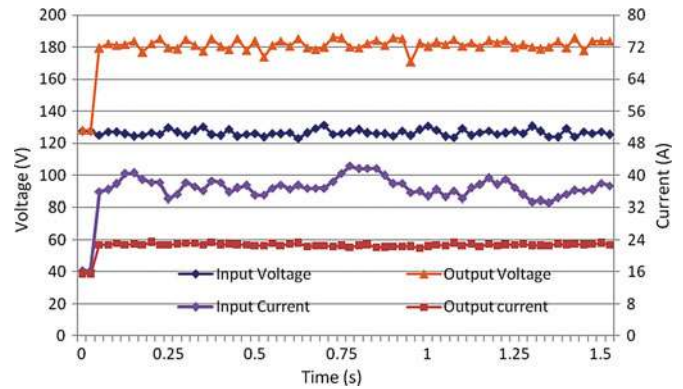


Fig. 20. Experiment results for 16-phase boost converter connected with ultracapacitor.

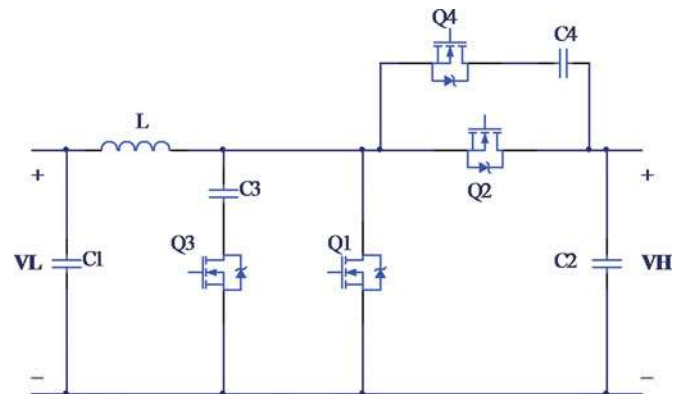


Fig. 21. Proposed ZVS/ZCS soft switch topology.

The ultracapacitor pack has been connected to the low voltage side of the 16-phase dc/dc converter, and the high voltage side is connected to a resistive load. The test results are shown in Fig. 20. The input/output voltage and current data are collected by the NI DAQ USB 6008. The input power is around 4.8 kW.

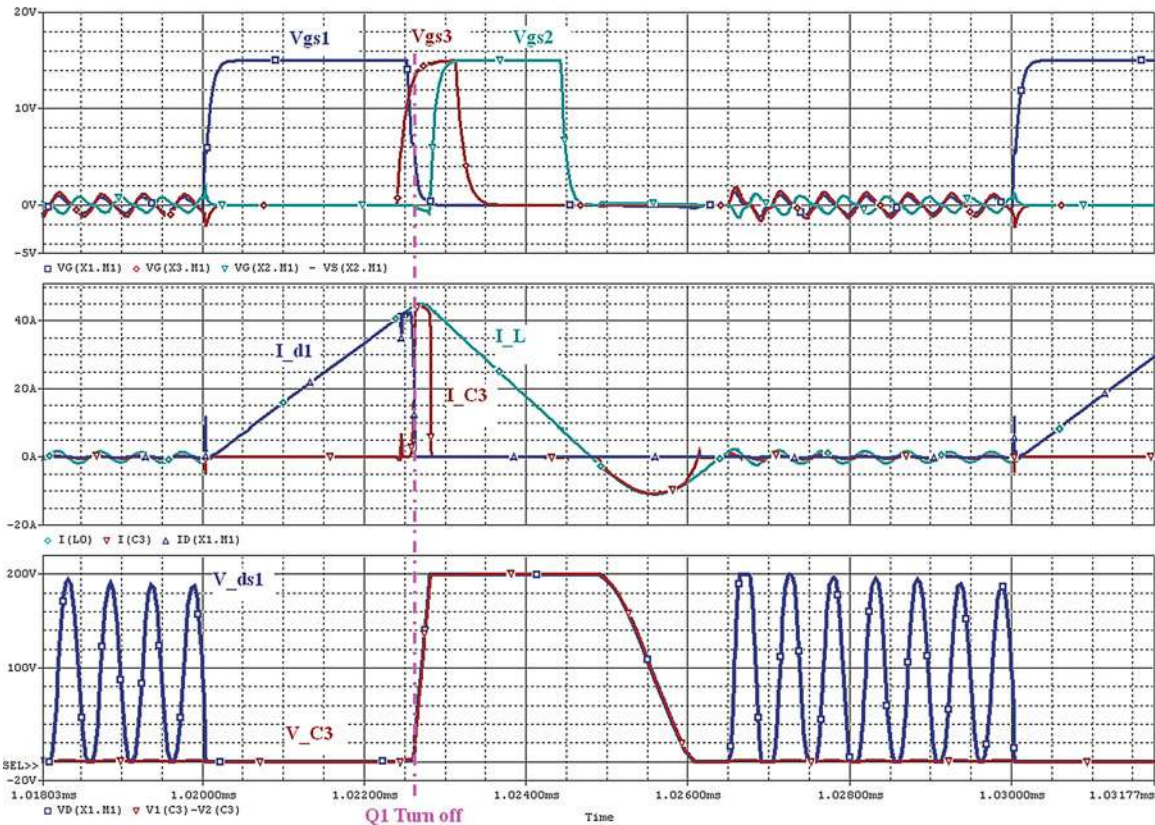


Fig. 22. Simulation results of the boost mode.

IV. ZVS/ZCS SOFT SWITCHING FOR DCM OPERATION

DCM operation has the advantage of zero current turn-ON. However, this operation significantly increases turn-OFF losses because the main switch is turned OFF at more than twice the average inductor current value. This drawback not only increases power losses but also induces current/voltage parasitic ringing. Soft switching techniques provide a solution for this problem. A topology is proposed to achieve ZVS turn-OFF in the DCM mode, as shown in Fig. 21.

To verify the theoretical analysis of the proposed topology, a simulation model was built in PSpice for a one-stage converter using the following design specifications: $L = 5 \mu\text{H}$, $C_3 = C_4 = 47 \text{ nF}$ and a switching frequency $f_s = 100 \text{ kHz}$, $V_L = 90 \text{ V}$ with $R_{\text{load}} = 51 \Omega$ which is connected to VH for boost mode operation. The switches used in this simulation are MOSFET IRFP4242's manufactured by International Rectifier, Inc. The simulation results are shown in Fig. 22.

In the boost mode, there are two different operation modes compared with the hard switched topology: the period of transition from Q1 turn-OFF to Q2 turn-ON and the period of the series LC resonance (inductor L and capacitor C_3) after the inductor current has reached zero. The auxiliary switch Q3 turns ON before the main switch turns OFF, so that Q1 turns OFF at zero voltage due to the capacitor C_3 . Q3 turns OFF before the high side switch Q2 turns OFF. After the inductor current I_L falls to zero, the inductor L and capacitor C_3 compose a series LC resonant circuit, until C_3 voltage V_{C3} falls to zero, and then V_{C3}

will be clamped at zero. All switches in this circuit are turned ON and OFF at zero voltage or zero current or both. The circuit has a similar operation in the buck converter mode.

A 400 W hardware prototype was designed, built, and tested to verify the proposed soft switch and evaluate its performance. A 16.8 nF capacitor and IRFP4242 MOSFET are used in the circuit. The frequency for main switch is 100 kHz. The control signal is generated by the FPGA.

The result is shown in Fig. 23 operating in boost mode without a snubber and external gate resistor. The input voltage is 50 V and the output voltage is 120 V. The efficiency is 92%. Similar operation for hard switching was also tested and compared with soft switching. Fig. 24 shows the experimental results for the hard switch topology with a gate resistor of 2.7 ohm. The efficiency is 91.5% for hard switching. Comparing soft switching with hard switching, the efficiency does not improve significantly, due to the losses in auxiliary circuit. However, the spike voltage and high frequency voltage ringing of soft switching have been reduced, even without an external gate resistor. The noise of the soft switching gate signal is also smaller than that of hard switching signal.

The proposed method can also improve efficiency, reduce the heat sink size for the main switch and allow reduction of both di/dt and dv/dt by increasing the gate drive resistor. In addition, the soft switching circuit can reduce the voltage overshoot during the main switch turn-OFF. Since the losses in the auxiliary switches are very small, it is not necessary to use a heat sink for

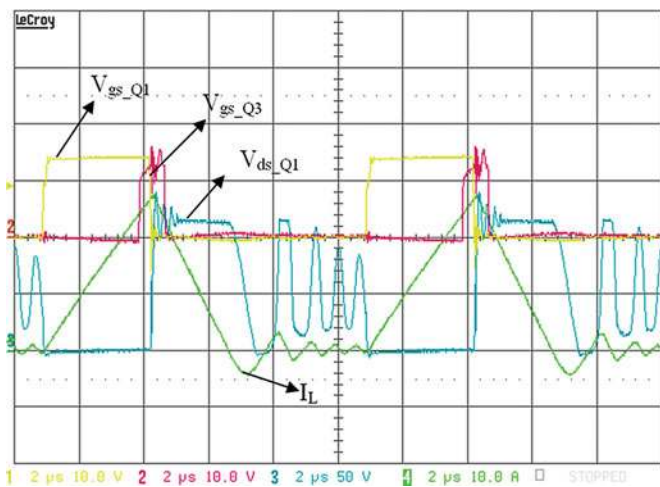


Fig. 23. Experiment result for proposed soft switch with $R_g = 0$ ohm.

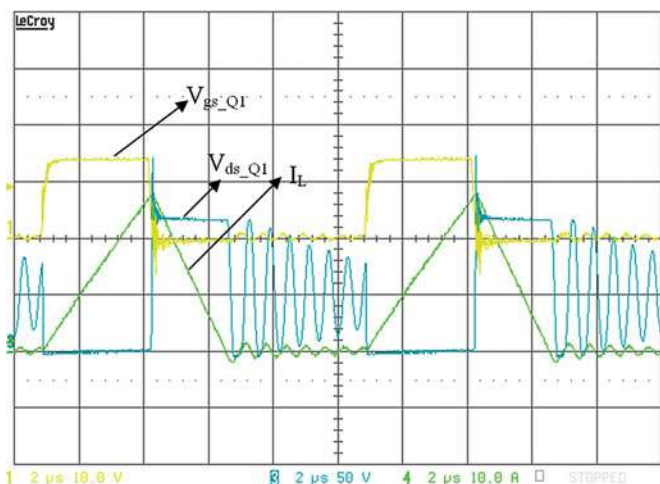


Fig. 24. Experiment result for hard switch with $R_g = 2.7$ ohm.

them. This proposed method is under investigation in ongoing research.

V. CONCLUSION

In the proposed design, the imbalance current among phases, caused by difference of duty ratio and component mismatch, is small and acceptable based on DCM operation, thus the current control loop in each phase can be removed. This allows cost-effective converters with a high number of phases. Another advantage of DCM operation is that it can reduce the inductance in each phase. The high current ripple in each phase associated with DCM operation can be alleviated by interleaving. By interleaving techniques, the power and current can be separated in each phase, and the device stress can be reduced. The current ripple is also reduced, particularly on the battery side, which might improve the battery lifetime. The proposed method makes it possible to increase the switching frequency and reduce filter size requirements, which can give benefits through smaller volume, lower cost, and higher safety. Moreover, high efficiency can be achieved with a proper design. The proposed design is

generic and is also applicable for other applications. Finally, a novel ZVS/ZCS soft switch topology for DCM operation is proposed and simulated to show its operability and improved performance, with respect to issues such as switching losses and voltage overshoot.

REFERENCES

- [1] Z. Amjadi and S. S. Williamson, "Novel control strategy design for multiple hybrid electric vehicle energy storage systems," in *Proc. Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 597–602.
- [2] A. W. Stienecker, T. Stuart, and C. Ashtiani, "A combined ultracapacitor-lead acid battery storage system for mild hybrid electric vehicles," in *Proc. 2005 IEEE Conf. Veh. Power Propulsion*, Sep. 2005, p. 6.
- [3] G. Guidi, T. M. Undeland, and Y. Hori, "An optimized converter for battery-supercapacitor interface," in *Proc. IEEE Power Electron. Spec. Conf. (PESC)*, Jun. 2007, pp. 2976–2981.
- [4] Z. Amjadi and S. S. Williamson, "Review of alternate energy storage systems for hybrid electric vehicles," in *Proc. 2009 IEEE Electr. Power Energy Conf. (EPEC)*, Oct. 2009, pp. 1–7.
- [5] F. H. Khan and L. M. Tolbert, "5 kW multilevel dc-dc converter for hybrid electric and fuel cell automotive applications," in *Proc. 42nd IEEE IAS Annu. Meet. Conf. Record*, Sep. 2007, pp. 628–635.
- [6] W. Qian, F. Z. Peng, and L. M. Tolbert, "Development of a 55 kW 3X dc-dc converter for HEV systems," in *Proc. IEEE Veh. Power Propuls. Conf., (VPPC)*, Sep. 2009, pp. 433–439.
- [7] R. L. Steigerwald, R. W. De Doncker, and H. Kheraluwala, "A comparison of high-power dc-dc soft-switched converter topologies," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1139–1145, Sep./Oct. 1996.
- [8] G. Franceschini, E. Lorenzani, M. Cavatorta, and A. Bellini, "3boost: A high-power three-phase step-up full-bridge converter for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 173–183, Jan. 2008.
- [9] D. P. Urciuoli and C. W. Tipton, "Development of a 90 kW bi-directional dc-dc converter for power dense applications," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2006, p. 4.
- [10] D. Aggeler, J. Biela, and J. W. Kolar, "A compact, high voltage 25 kW, 50 kHz dc-dc converter based on SiC JFETs," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo., (APEC)*, Feb. 2008, pp. 801–807.
- [11] S. Waffler, J. Biela, and J. W. Kolar, "Output ripple reduction of an automotive multi-phase bi-directional dc-dc converter," in *Proc. IEEE Energy Convers. Congr. Expo., (ECCE)*, Sep. 2009, pp. 2184–2190.
- [12] O. Garcia, P. Zumel, A. de Castro, and A. Cobos, "Automotive dc-dc bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 578–586, May 2006.
- [13] M. Pepper, K. Mansfield, J. Elmes, K. Rustom, R. Kersten, M. Qahwash, and I. Batarseh, "Bi-directional DCM DC to DC converter for hybrid electric vehicles," in *Proc. Power Electron. Spec. Conf., (PESC)*, Jun. 2008, pp. 3088–3092.
- [14] J. Zhang, J.-S. Lai, R.-Y. Kim, and W. Yu, "High-power density design of a soft-switching high-power bidirectional dc-dc converter," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1145–1153, Jul. 2007.
- [15] O. Garcia, P. Zumel, A. de Castro, P. Alou, and J. A. Cobos, "Current self-balance mechanism in multiphase buck converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1600–1606, Jun. 2009.
- [16] J. A. A. Qahouq, "N-phase efficiency-based current sensing auto-tuning controller," in *Proc. Appl. Power Electron. Conf. Expo., (APEC)*, Feb. 2009, pp. 274–279.
- [17] B.-S. Min, N.-J. Park, and D.-S. Hyun, "A novel current sharing technique for interleaved boost converter," in *Proc. Power Electron. Spec. Conf., (PESC)*, Jun. 2007, pp. 2658–2663.
- [18] X. Zhou, P. Xu, and F. C. Lee, "A novel current-sharing control technique for low-voltage high-current voltage regulator module applications," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1153–1162, Nov. 2000.
- [19] M. Gerber, J. A. Ferreira, I. W. Hofsjager, and N. Seliger, "Interleaving optimization in synchronous rectified dc/dc converters," in *Proc. 35th IEEE Annu. Power Electron. Spec. Conf. (PESC)*, Jun. 2004, vol. 6, pp. 4655–4661.
- [20] Y. Louvriev, P. Barrade, and A. Rufer, "Weight and efficiency optimization strategy of an interleaved DC-DC converter for a solar aircraft," in *Proc. 13th Eur. Conf. Power Electron. Appl., (EPE)*, Sep. 2009, pp. 1–10.
- [21] A. de Castro, T. Riesgo, O. Garcia, and J. Uceda, "A methodology to design custom hardware digital controllers for switching power

- converters,” in *Proc. 35th IEEE Annu. Power Electron. Spec. Conf., (PESC)*, Jun. 2004, vol. 6, pp. 4676–4681.
- [22] L. H. Dixon, “Eddy current losses in transformer windings and circuit wiring,” Texas Instruments, 2003.
- [23] L. Ni, D. Patterson, and J. L. Hudgins, “Preliminary design, simulation and modeling of a series hybrid commuter vehicle with a minimal IC engine,” in *Proc. IEEE Veh. Power Propuls. Conf. (VPPC)*, Sep. 2007, pp. 754–758.
- [24] L. Ni, “Energy storage and management for a small series plug-in hybrid electric vehicle,” Ph.D. Dissertation, Dept. Elect. Eng., Univ. of Nebraska-Lincoln, NE, 2010.

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