IEEJ Journal of Industry Applications
Vol.8 No.4 pp.694–703 DOI: 10.1541/ieejjia.8.694

Paper

High Power Density SiC-Based Inverter with a Power Density of 70 kW/liter or 50 kW/kg

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(Manuscript received June 30, 2018, revised Dec. 25, 2018)

This paper presents a high power density silicon carbide (SiC)-based inverter, with a two-level voltage-source structure having forced air cooling, which provides a high volumetric power density of 70 kW/liter or 50 kW/kg in gravimetric terms. In order to achieve a power density greater than that of conventional inverters, the losses must be reduced or the cooling performance must be improved. Small light-weight SiC MOSFET power modules with directly soldered foil fins having good thermal conductivities, are developed in this study. The antiparallel SiC Schottky barrier diodes (SBDs) are removed from the modules to improve the power density. Gate drivers are developed to reduce the switching losses and switching time. A prototype of the proposed high power density inverter, which includes the developed power modules and proposed gate driver, is fabricated. The volume and weight of the prototype inverter are approximately 0.5 liter and 660 g, respectively. Experimental results confirm that the prototype inverter can operate continuously with an output power up to 35 kW. Therefore, the power density of the prototype inverter is approximately 70 kW/liter or 50 kW/kg. The efficiency of the prototype inverter is found to be more than 98%. Hence, the measures undertaken in this study have been verified to improve the power density of the inverters. The proposed high power density inverters can be applied in future aircraft and other electric vehicles.

Keywords: SiC, gate drive, MOSFET, high power density, inverter

1. Introduction

The purpose of this research is to achieve high power density for future applications such as aircraft or other electric vehicles. High power density converters have attracted huge interest for application in next-generation power electronic systems such as aircraft and other electric vehicles. The research and development of higher power density converters have accelerated with the emergence of devices based on silicon carbide (SiC) and gallium nitride (GaN).

The next generation aircraft such as more electric aircraft (MEA) and all electric aircraft (AEA) need light-weight high power density converters [(1)–(8)]. Three-phase ac-dc-ac 10 kW converters capable of providing power densities of 3.03 kW/liter and 3.59 kW/kg, with SiC junction field-effect transistors (JFETs) and Schottky barrier diodes (SBDs) have been developed, which excludes controller and housing [(1)]. Although dc/ac converters capable of providing a power density of 4 kW/kg are available, filtering and cooling systems in aircraft may reduce the power density to 2 kW/kg [(2)]. Water-cooled three-phase SiC 50 kW inverters using novel gate drivers capable of switching at 100 kHz have been reported; these are capable of producing power densities up to 26 kW/kg, excluding filters [(5)]. A water-cooled three-phase SiC 50 kW inverter capable of producing 6.49 kW/kg, considering filters, is achieved by design optimization [(6)].

The power density was predicted to reach approximately 30 kW/liter around 2015 [(9)]. Technologies related to high power density converters have been investigated comprehensively in (10), and power density limits of 26 to 44 kW/liter are calculated for several types of converters. Applying higher switching frequencies is promising choice to reduce volume of passive components. An 8.5 kW/liter forced-air-cooled 10 kW rectifier and a 10 kW/liter water-cooled rectifier are achieved at a switching frequency of 400 kHz. An 18.5 kW/liter water-cooled converter is achieved by applying higher switching frequencies up to 2.5 MHz [(11)]. However applying higher switching frequencies increases the switching losses and requires new materials for the magnetic components or larger heat sinks. Therefore, an LCL filter design suitable for aircraft applications is studied in (7) and (8), and cooling concepts for the magnetic parts are investigated in (12). The use of active ripple energy storages to reduce the dc capacitors is studied in (13).

Operating SiC power devices at higher temperatures such as 200°C than silicon devices has been applied to improve the power density, in (14) and (15). A 1.37 kW/liter and 1.41 kW/kg liquid-cooled 5 kW three-phase inverter has been developed in (14). A 40 kW/liter air-cooled three-phase inverter without electromagnetic interference (EMI) filters has

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been developed in (15). A printed metal power module with integrated cooling using additive manufacturing is developed in (16).

In 2014, Google and IEEE launched a competition called the Little Box Challenge (LBC), in which the participants attempted to develop the world's smallest 2 kW single-phase air-cooled inverters with EMI filters. The developed inverter concepts and technologies are comprehensively investigated in (17), (18), and (19). Power densities ranging from 3.41 kW/liter to 13.18 kW/liter have been achieved by the participants [17]. The participants have achieved high power densities by applying SiC on GaN devices, and employing active power decoupling (APD), and higher switching frequencies. The APD methods used in LBC have been compared in (20), which highlighted the importance of APD in improving the power densities. A tradeoff study on the cooling system and output filter volume in a GaN-based inverter has been conducted for design optimization, in (21). A 13.18 kW/liter air-cooled inverter has been developed with a 7-level multilevel GaN inverter switching at 120 kHz and APD, in (22). A 6.22 kW/liter air-cooled inverter has been developed with GaN inverter switches at 100 kHz and APD, in (23). A 6.1 kW/liter air-cooled inverter has been developed with SiC inverter switching at 45 kHz and active ripple filters, in (24).

According to the latest research reports on high power density converters, many researches have tried to (a) apply SiC and GaN devices to reduce losses, (b) employ higher switching frequencies to reduce the sizes of the magnetic components, (c) operate under higher temperatures to enhance the output power, using the same cooling systems, (d) apply APD to reduce the sizes of capacitors, (e) improve cooling systems to reduce the sizes of cooling systems, and (f) optimize the design to reduce the tradeoffs between the component volume and weight. The latest inverters have achieved the high power density predicted in (9), such as 40 kW/liter in (15), 13.18 kW/liter in (22), and 26 kW/kg in (5). The inverter developed in this study achieves 70 kW/liter and 50 kW/kg, and features SBD-less SiC power modules with direct soldered foil fin and low-loss gate driver.

Small and light-weight SiC MOSFET power modules have been developed in this study. The antiparallel SiC SBDs are removed from the modules to improve the power density, while some commercialized power modules have antiparallel SiC SBDs. A gate driver is developed to reduce the switching losses and improve the power density. The authors have already reported on the design and evaluation of high power density inverters using the developed modules in a previous work [25]. The effects of removing the antiparallel SiC SBDs from the SiC-based inverters are introduced in (26). Removing the antiparallel SiC SBDs not only reduces the size but also improves the speed and low-noise switching capabilities. However, removing SBDs can risk deteriorating the long-term reliability of SiC-MOSFETs [27]; therefore, some commercialized SiC MOSFET modules still contain anti-parallel SiC-SBDs. However, recent research has indicated that the latest devices can endure a 1,000 h stress test without deterioration [28]. The proposed gate driver has been comprehensively evaluated in (29). The proposed gate driver can reduce the switching losses and delay time. However, comprehensive thermal evaluation results are not included in the previous reports.

This paper presents additional evaluation of the thermal characteristics of developed module and further studies of influence of the approaches proposed to achieve higher power density on the power density. The proposed approaches are small light-weight SiC-MOSFET power modules with direct soldered foil fins, removing antiparallel SiC SBDs, and the proposed gate driver.

Section 2 introduces the developed power modules and evaluation results. Section 3 shows the influence of removing antiparallel SiC SBDs on the power density. Section 4 evaluates the influence of the proposed gate driver on the power density. Section 5 introduces the developed inverter and experimental results. Finally, section 6 provides the conclusions.

2. SiC Power Modules

2.1 Prototype of Power Modules Prototypes of small and light-weight SiC power modules have been developed. Figure 1 shows cross sectional structure of the prototype power module. Figure 2 shows some photographs of the prototype power module. The prototype power modules have two arms, with eight paralleled 1200 V/ 80 mΩ SiC MOSFET chips in each arm. A copper heat sink is directly soldered to the copper base plate of the substrate. Typical conventional

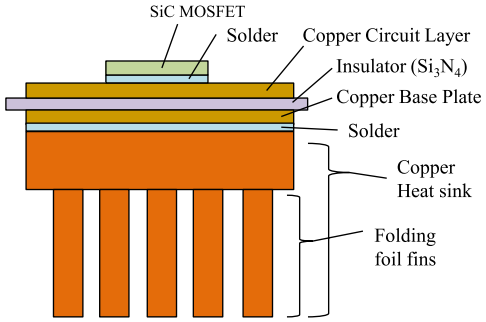
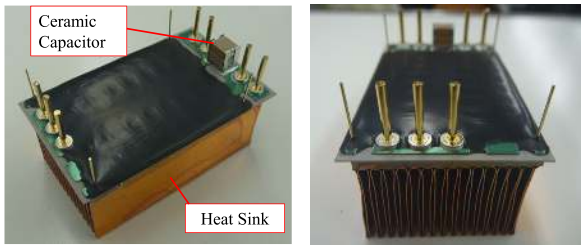
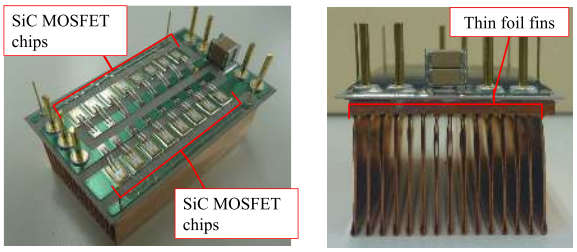


Fig. 1. Cross sectional structure of the prototype power module

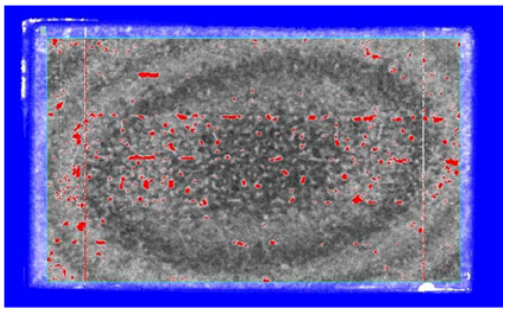


(a) Prototype power module (53 mm × 32 mm × 31 mm, 52 cc, 95 g)



(b) Internal structure (c) Direct soldered heat sink strucure

Fig. 2. Photographs of the prototype power module



Ultrasonic inspection (Void proportion 2.7%)

Fig. 3. Direct soldering layer evaluation

Table 1. Specifications of heat sink

Item	Prototype Power Modules
Heat Sink Size (approx.)	30 mm × 50 mm × 20 mm = 0.03 liter
Heat Sink Weight (approx.)	75 g
$R_{th(f\text{-}a)}$ per Module	0.44 K/W (measured from inverter evaluation tests)
Fan Size per Module (approx.)	0.03 liter (prototype inverter has 2 fans and 3 modules, 45 cc/fan)
Fan Weight per Module (approx.)	40 g (prototype inverter has 2 fans and 3 modules, 60 g/fan)
Fan	9GA0412P3K01 (SANYO)
CSPI (*V*) (Cooling System Performance Index per liter)	37 W/K*liter (include cooling fan)
CSPI (*G*) (Cooling System Performance Index per kg)	19 W/K*kg (include cooling fan)

structures have thermal interface materials (TIMs) such as silicon grease instead of a solder layer, between the copper base plate and heat sink. Both the solder layers under the chips and under the copper base plates are reflowed simultaneously; therefore, the proposed structure is easy to manufacture and has a lower number of reflow soldering processes. Figure 3 shows the ultrasonic inspection results of the direct soldering layer; the void distribution is shown in red. The void proportion rate is 2.7%.

The specifications of the heat sink are presented in Table 1. While heat sinks made of extruded aluminum material are widely applied in power converters, the power modules developed in this work have light-weight heat sinks with folded thin copper foils. The prototype power modules exhibit significantly improved thermal conductivity and power density for a high aspect ratio of the folded thin foil structure. The measured thermal resistance from the heat sink to ambient air $R_{th(f-a)}$ is approximately 0.44 K/W. The volumetric and gravimetric cooling system performance index (*CSPI*) are 37 W/K*liter and 19 W/K*kg, respectively, which take into account the cooling fans also. For comparison, highly optimized heat sinks such as the 17.5 W/K*liter aluminum heat sink, 21.6 W/K*liter copper heat sink, and 30.9 W/K*liter double-side cooling copper heat sink are studied in (10). The *CSPI* are defined as in (1) and (2).

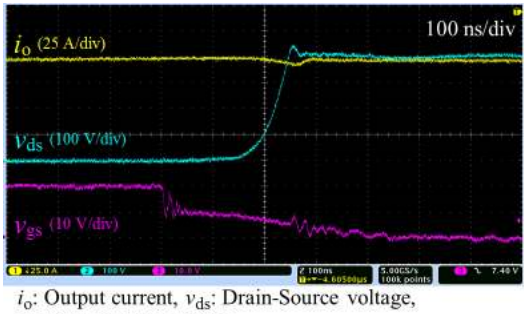
$$CSPI(V) = \frac{1}{R_{th\_cs} \times Vol_{\_cs}} \quad \cdots\cdots (1)$$

$$CSPI(G) = \frac{1}{R_{th\_cs} \times W_{\_cs}} \quad \cdots\cdots (2)$$

R_{th_cs} is the thermal resistance of the cooling system [K/W].

$Vol_{\_cs}$ is the volume of cooling system, including the volumes of the heat sinks and cooling fans or pumps.

$W_{\_cs}$ is the weight of cooling system, including the weights of the heat sinks and cooling fans or pumps.



i_o: Output current, v_{ds}: Drain-Source voltage, v_{gs}: Gate-Source voltage.

Fig. 4. Turn-off waveforms of the prototype power module, output current I_o = 100 A, DC input voltage V_{dc} = 400 V, voltage source of gate driver V_{cc} = 18 V

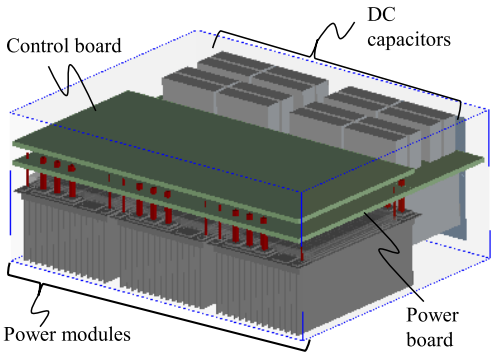
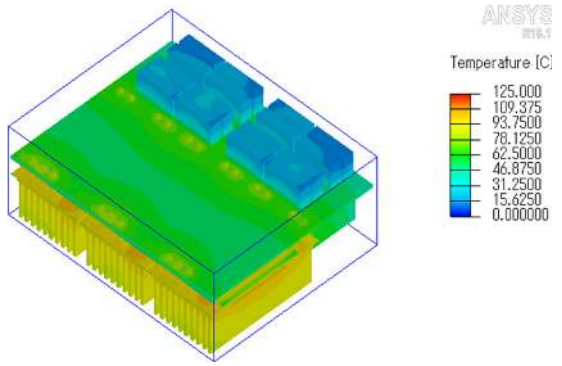


Fig. 5. 3D-FEM simulation model of prototype power modules and inverter

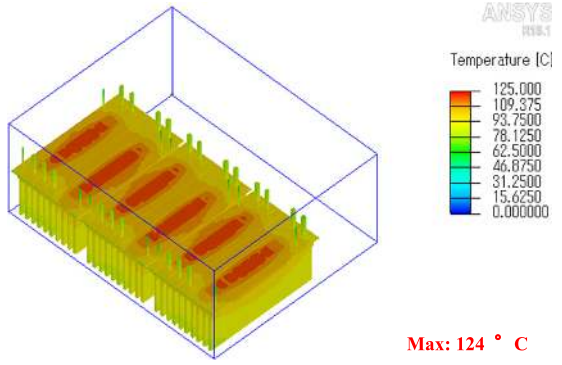
The power modules have ceramic capacitors between the DC input terminals, to reduce the inductance of the commutation loop as shown in Fig. 2. Figure 4 shows the switching waveforms of the turn-off transient at 400 V/100 A, at room temperature (approximately 25°C). The voltage overshoot is approximately 50 V with almost no oscillations. The stable switching capability of the developed power modules is confirmed by the experimental results.

2.2 Thermal Characteristic Evaluation This section presents the results of the thermal characteristic evaluation of the prototype power modules. 3D-FEM simulations have been performed to compare the thermal characteristics of the proposed and conventional power modules. Figure 5 shows the prototype inverter model used in the 3D-FEM simulations. The inverter has three power modules, the power board which includes gate drivers, control board, DC capacitors, and cooling fans. The power modules with conventional structures consist of excluded aluminum heat sink and TIM (G-767, Shinetsu-Silicon). The inverter loss is assumed to be 500 W and the ambient temperature is set as 17°C, which are the same values in the experiments that will be described in the following section.

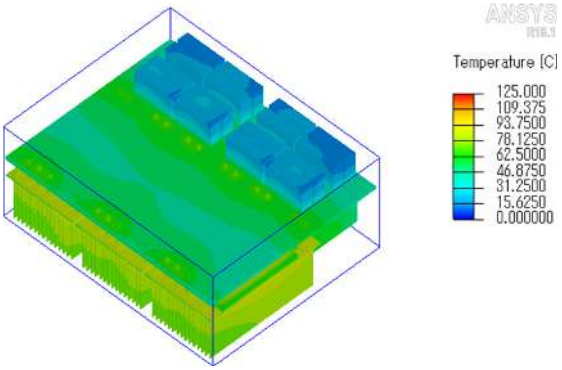
Figure 6 shows the simulation results. Figures 6(a) and (b) show the thermal contributions of the conventional modules and Figs. 6(c) and (d) show the thermal contributions of the proposed modules. The maximum chip temperatures are 124°C for the conventional power modules and 103°C for the proposed power modules. The proposed power module structure reduces the maximum chip temperature by approx-



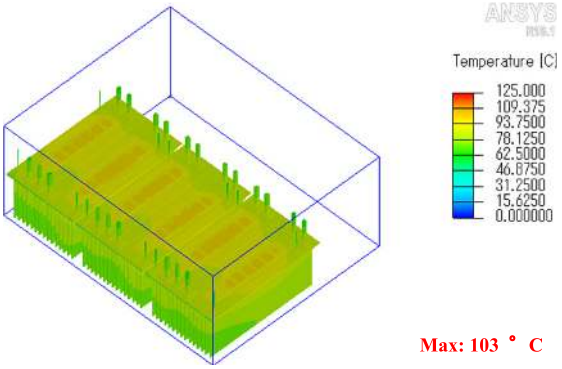
(a) Inverter with the power modules with conventional structure



(b) The power modules with conventional structure



(c) Inverter with the proposed power modules



(d) The proposed power modules

Fig. 6. 3D-FEM simulation results with ANSYS Icepack

imately 16% compared to the conventional power modules.

Table 2 shows the thermal resistances extracted from the simulation results. The thermal resistance from the SiC MOSFET chips to the ambient air, $R_{\text{th(j-a)}}$, is approximately 1.28 K/W per arm, for the conventional structure. The $R_{\text{th(j-a)}}$ of the proposed structure is approximately 1.03 K/W per arm.

Table 2. Power module thermal conductivity evaluation

Item	Conventional	Proposed
Heat Sink	Aluminum extruded fin	Copper folding foil fin
TIM (Thermal Interface Material)	G-765 (Shinetsu Silicon)	Direct solder structure
$R_{\text{th(j-c)}}$ per arm	0.04 K/W	0.04 K/W
$R_{\text{th(c-f)}}$ per arm	0.10 K/W	0.01 K/W
$R_{\text{th(f-a)}}$ per arm	1.15 K/W	0.98 K/W
$R_{\text{th(j-a)}}$ per arm	1.28 K/W	1.03 K/W (19% smaller than conventional)
Maximum Output Power Capability P_{max} (The following assumptions are made. Inverter efficiency 98% Ambient temperature 25 ° C Max chip temperature 125 ° C)	22.9 kW	28.5 kW (24% increase from conventional)

Therefore, it can be observed that the proposed structure reduces the thermal resistance by approximately 19%. The direct-soldered heat sink structure reduces the thermal resistance from the baseplate to the heat sink, $R_{\text{th(c-f)}}$, by approximately 90%.

2.3 Influence on Power Density The prototype power modules have smaller thermal resistances than the conventional modules. The calculated maximum inverter output power capabilities are shown in Table 2. The evaluation conditions are assumed to be as follows, inverter efficiency is 98%, ambient temperature is 25°C, and maximum allowable chip temperature is 125°C. The maximum output power capability P_{max} of the inverter with the prototype power module is calculated using (3). It is observed that P_{max} is enhanced by approximately 24%, compared to that of the inverter with the conventional power module structure. Therefore, it can be concluded that the developed power module improves the power density by approximately 24%.

$$P_{\text{max}} = \frac{\eta}{100-\eta} \times \frac{\Delta T_{\text{max}}}{R_{\text{th(j-a)\_arm}}} \times 6 \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

P_{max} is the maximum output power capability.

η is the efficiency of the inverter.

$R_{\text{th(j-a)\_arm}}$ is the total thermal resistance from the chip to the ambient, per arm.

ΔT_{max} is the acceptable chip temperature increase from the ambient.

3. Effects of Removing SiC SBDs

3.1 Characteristics of Inverters without SBDs A comprehensive evaluation of the effects of removing the antiparallel SiC SBDs has been described in (26). Table 3 shows a summary of the advantages and disadvantages of removing the antiparallel SiC SBDs. The forward voltage drops of the body diodes of the SiC MOSFETs, V_{F}, are larger than those of the antiparallel SiC SBDs. However, the synchronous rectification method is widely used in MOSFET-based inverter applications. Therefore, the body diode conductive loss drawback during only dead time is not critical for MOSEFT-based inverters.

SiC SBDs do not have recovery current at turn-off; they just have a small charge current due to stray capacitances. The body diodes of SiC MOSFETs exhibit the recovery phenomenon during turn-off if the antiparallel SiC SBDs are removed, and the recovery current and loss increase as the

Table 3. Advantages and disadvantages of removing SiC SBDs

Item	With SBDs (Conventional)	Without SBDs (Proposed)
Forward Voltage Drop of Diode V_F	1 V (approx.)	3 V (approx.)
Recovery Current	Small	Body diode recovery current increases as temperature increases
Output Capacitor C_{oss}	Large	Small
Stray Resistance R_S	Small	Large
Resonant Frequency at Switching	Low	High
Damping Factor	Small	Large
Cost	---	Small
Size	---	Small
Loss	Small conductive losses while SBDs are on	Small switching losses
Noise	---	Small
Reliability	Good	Needs to be checked.

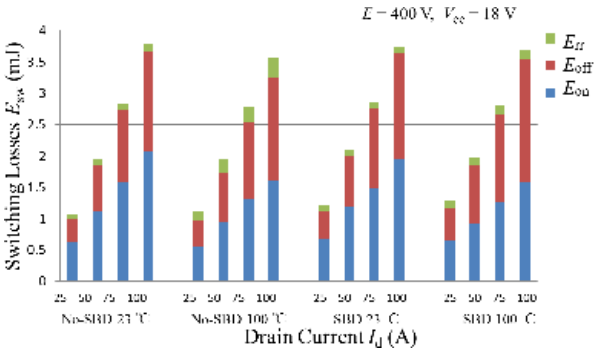


Fig. 7. Experimental results of switching losses, voltage source for gate driver V_{cc} = 18 V, DC input voltage V_{dc} = 400 V, gate resistance for turn-on $R_{g(on)}$ = 3.9 Ω, gate resistance for turn-off $R_{g(off)}$ = 6.8 Ω

temperature increases. This drawback should be evaluated. Figure 7 shows the experimental results of the switching-loss comparisons of SiC MOSFETs with and without antiparallel SiC SBDs. The experiments have been done using the same gate drive circuit for both SiC MOSFETs (with and without anti-parallel SiC SBDs). The total switching losses of the SiC MOSFETs without antiparallel SiC SBDs are slightly smaller than those of SiC MOSFETs with antiparallel SiC SBDs. The recovery losses without SBDs become larger at higher temperatures; however, the recovery losses of the body diodes are small enough even at high temperatures. The smaller output capacitances of the SiC MOSFETs without antiparallel SiC SBDs make the turn-off losses smaller. The switching loss differences between SiC MOSFETs with and without antiparallel SBDs are negligible, in this study.

The SiC power modules without antiparallel SiC SBDs have smaller output capacitances and larger stray resistances than those with antiparallel SiC SBDs. These parasitics make the damping factors of SiC MOSFETs without antiparallel SiC SBDs larger than those of SiC MOSFETs with SBDs. The switching ringing is reduced by removing the antiparallel SiC SBDs, because of the larger damping factors. Small ringing makes the switching faster and switching losses smaller. Effective fast switching improves the inverter efficiency and leads to a smaller heat sink, which indicates a higher power density. Small ringing can also reduce the sizes of the noise filters such as EMI filter. However, the recovery loss and influence on EMI issues should be considered carefully for use in high-temperature applications.

Table 4. Normalized loss and power density

Item	SiC MOSFETs With SBDs	SiC MOSFETs Without SBDs	SiC MOSFETs Without SBDs
Paralleled Chip	5	5	8
Total Chip Size	1	≈ 0.6	≈ 1
Conductive Loss P_{cond}	1	≈ 1	≈ 0.6
Switching Loss P_{sw}	1	≈ 1	≈ 1
Inverter Total Loss P_{inv}	1	≈ 1	≈ 0.7
$R_{th(j-a)}$ per arm	1	≈ 1.6	≈ 1
Expected Power Density (Per power module and cooling system)	1	≈ 1	≈ 1.42

3.2 Influence on Power Density Removing the antiparallel SiC SBDs reduces the SiC chip size by approximately 40%. In this study, a 13.64 mm^2 SiC MOSFET chip and 9.73 mm^2 SiC SBD chip are used. The developed power modules have additional SiC MOSFET chips, occupying the space resulting from the removal of the antiparallel SiC SBDs.

Table 4 shows the normalized loss and power density of the prototype power module. The calculations are done with the following conditions: DC input voltage V_{dc} = 400 V, output current I_o = 80 A_{rms}, and switching frequency f_{sw} = 20 kHz. SiC MOSFETs have low switching loss characteristics; therefore, their conductive losses are dominant, especially, at higher outputs. Removing the antiparallel SiC SBDs and adding SiC MOSFETs reduce the inverter conduction loss and enhance the power density. As shown in Table 4, removing the antiparallel SiC SBDs does not enhance the power density. Although the total chip size reduces by removing the SBDs, the total loss does not decrease. Therefore, removing antiparallel SiC SBDs alone will result in requiring the same size cooling systems. Adding additional SiC MOSFET chips in the space obtained by removing antiparallel SiC SBDs plays an important role; it reduces the conductive loss by approximately 40% for the same thermal conductivity. The total inverter loss is reduced by approximately 30% for the calculation conditions used in this study. Therefore, the proposed inverter enhances the maximum output power and improves the power density.

4. Proposed Gate Driver

4.1 Switching Performance of the Proposed Gate Driver The authors have proposed a low loss gate driver in a previous work [27]. This section briefly reviews the performance of the proposed gate driver. Figure 8 shows the switching characteristics of SiC MOSFETs with the proposed gate driver. The SiC MOSFET under test is a 1200 V/100 A all SiC power module with antiparallel SiC SBDs (BSM120D12P2C005, ROHM). The proposed gate driver reduces the switching losses by approximately 12% compared to the conventional one.

4.2 Influence on Power Density The proposed gate driver reduces the inverter loss by approximately 2%. This

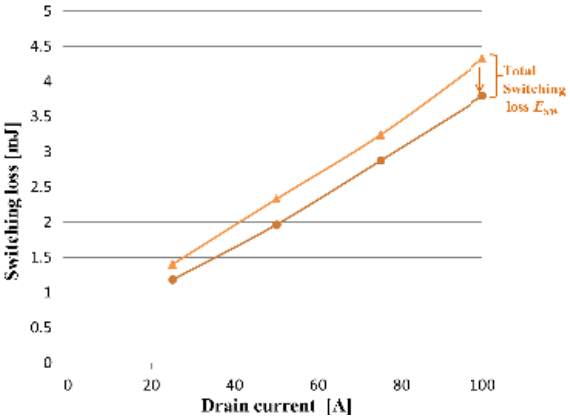


Fig. 8. Switching loss reduction with the proposed gate driver

(a) Whole package of inverter

(b) Internal structure of the inverter

Fig. 9. Photographs of the prototype inverter

2% loss reduction leads to a 2% smaller or lighter heat sink with same *CSPI*. The calculation conditions are as follows, SiC power module is BSM120D12P2C005, V_{dc} = 400 V, I_o = 80 A_{rms}, f_{sw} = 20 kHz.

5. High Power Density Inverter

5.1 Prototype Inverter Figure 9 shows photographs of the prototype inverter. The inverter consists of three of the developed power modules, the developed gate drivers, control board, DC capacitors, and two cooling fans inside the package. The prototype inverter does not contain current sensors. The inverter volume is approximately 0.5 liter (104 mm × 110 mm × 45 mm), and its weight is approximately 660 g. Figure 10 shows the circuit diagram of the developed inverter. The inverter is two-level three-phase voltage-source inverter. Figure 11 shows the volume and weight distributions of the prototype inverter. The cooling system comprising heat sinks and fans is responsible for approximately 35% of the volume distribution and 53% of the weight distribution.

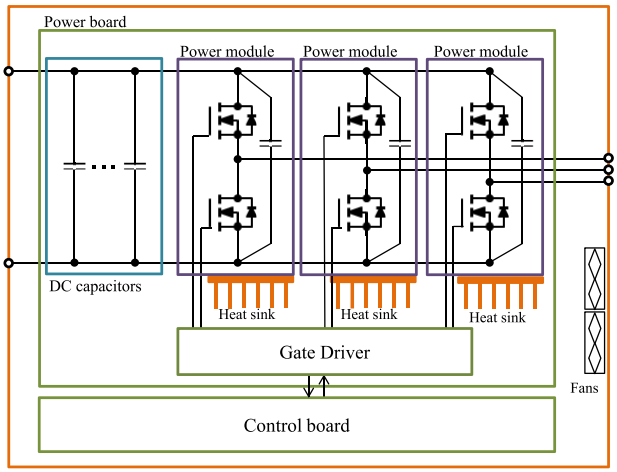
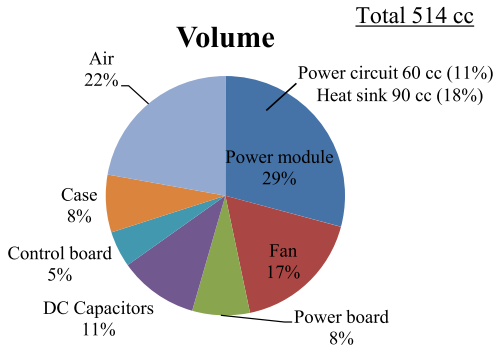
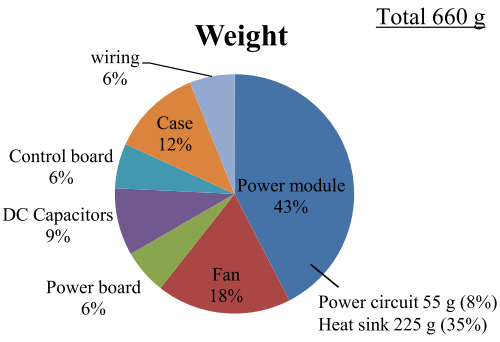


Fig. 10. Circuit diagram of the developed inverter



(a) Volume distribution



(b) Weight distribution

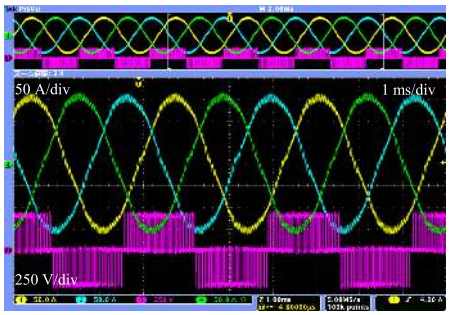
Fig. 11. Volume and weight distributions of the prototype inverter

Fig. 12. Test setup for inverter performance evaluation

5.2 Performance of the Inverter This section shows some experimental results to evaluate the prototype inverter performance. Figure 12 shows the test setup for the experiments. The basic experimental conditions are as follows: DC input voltage V_{dc} = 400 V, output AC frequency f_{ac} = 300 Hz, switching frequency f_{sw} = 20 kHz, load inductance ~100 μH, and load resistance ~1.57 Ω at 25°C.

Figure 13 shows the test results of the evaluation of the

(a) Maximum output power and efficiency



(b) Output current and voltage waveforms

Fig. 13. Maximum continuous output power, efficiency, and output waveforms

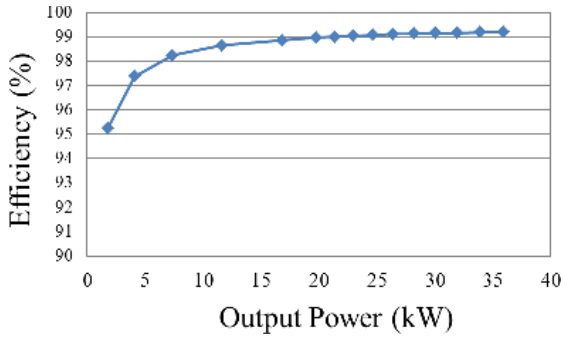
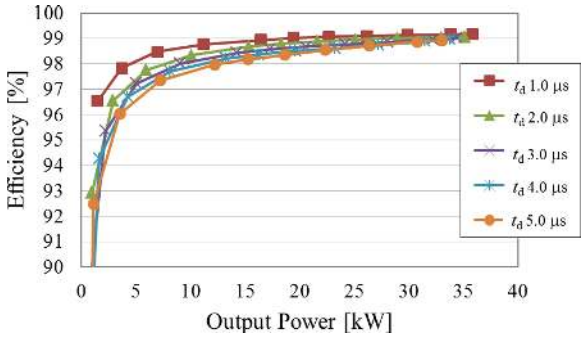
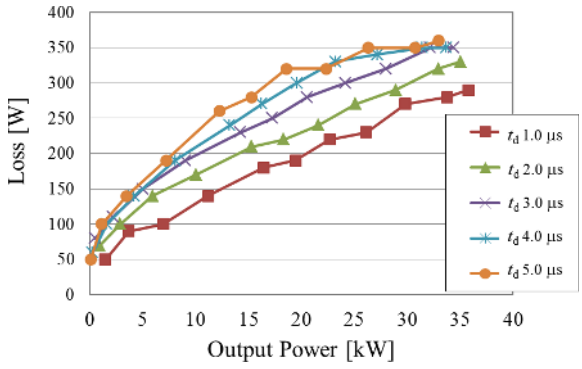


Fig. 14. Efficiency of the developed inverter



(a) Inverter efficiency



(b) Inverter loss

Fig. 15. Influence of dead-time length

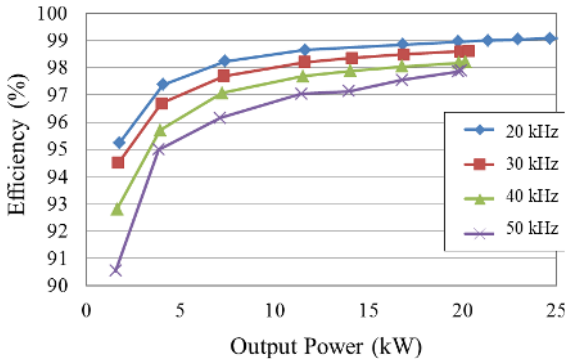


Fig. 16. Influence of switching frequencies

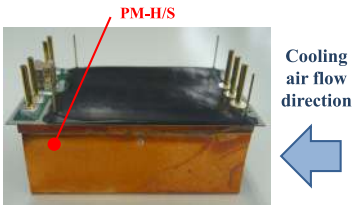
maximum continuous output power of the developed inverter. Figure 13(a) shows the value measured with a power meter HIOKI 3390, which is captured after the heat sink temperature has been saturated enough. The maximum continuous output power is more than 35 kW and the inverter efficiency is more than 98%. As shown in Fig. 13(b), the developed inverter works stably and does not suffer from switching noise. Figure 14 shows the inverter efficiency for various outputs. The developed inverter works effectively with more than 98% efficiency for a wide range of outputs.

Figure 15 shows the evaluation results of the influence of dead time length. Figure 15(a) shows the inverter efficiency and Fig. 15(b) shows the inverter loss. The results confirm that shortening the dead time improves the inverter efficiency and reduces the inverter loss. Shortening the dead time also reduces the conductive losses of the body diodes in synchronous rectification. This effect is stronger for inverters without antiparallel SiC SBDs than for inverters with antiparallel SiC SBDs, because the forward voltage drops of SiC MOSFET's body diodes are larger than those of SiC SBDs. The fast turn-off capability of the proposed gate driver has the advantage of reducing the dead time.

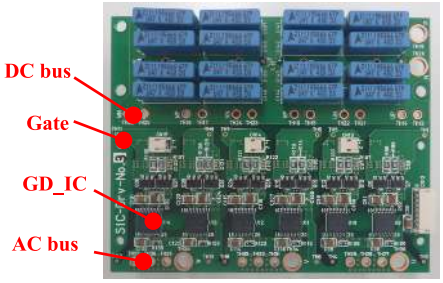
Figure 16 shows the inverter efficiency for various switching frequencies ranging from 20 kHz to 50 kHz. The prototype inverter can work efficiently with more than 97% efficiency even at 50 kHz. The maximum output power for a switching frequency of 50 kHz is 20 kW.

5.3 Thermal Performance Evaluation This section shows some experimental results of the evaluation of the thermal performance of the prototype inverter, and some simulation results of the evaluation of the SiC MOSFET chip temperature, which is difficult to measure in inverter experiments. The basic experimental conditions are as follows: DC input voltage $V_{dc} = 400$ V, output AC frequency $f_{ac} = 300$ Hz, switching frequency $f_{sw} = 20$ kHz, load inductance ~100 μH, and load resistance ~1.57 Ω at 25°C.

Figure 17 shows the measurement points for thermal evaluation. Figure 17(a) shows the measurement point for measuring the power module heat sink temperature. The measurement point is set on the leeward side of the heat sink. Figure 17(b) shows the measurement points on the power board. The measurement points are set adjacent to the power module terminals; DC bus, AC bus, and gate terminals. Figure 18 shows the thermal performance evaluation test results. The

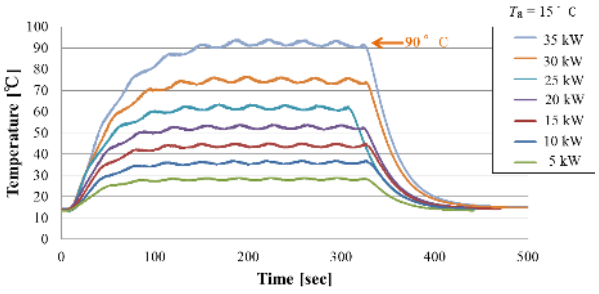


(a) Measurement point of power module heat sink temperature

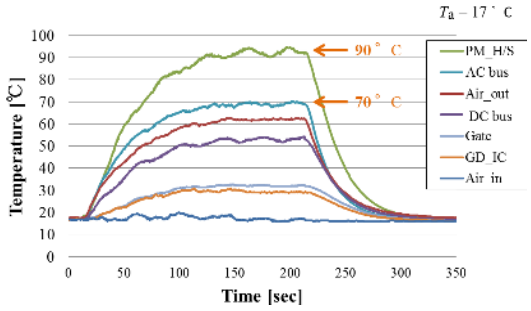


(b) Measurement points on power circuit board

Fig. 17. Thermal measurement points for measuring with thermocouples

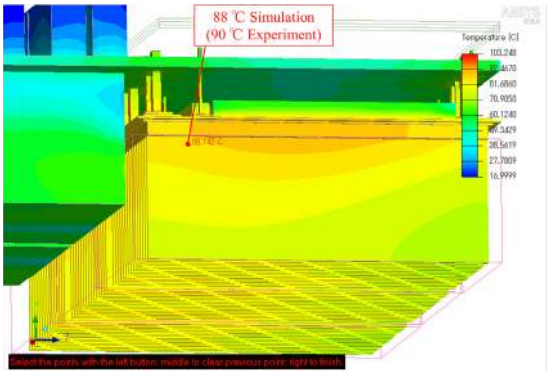


(a) Heat sink temperature

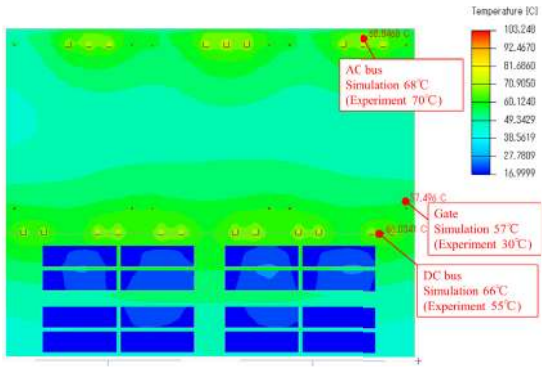


(b) Measurement point temperatures on power circuit board; output power is 35 kW

Fig. 18. Thermal performance evaluation test results



(a) Heat sink temperature



(b) Measurement point temperatures on power board

(c) MOSFET chip temperature distribution

Fig. 19. Thermal simulation results

heat sink temperatures for different inverter output conditions are presented in Fig. 18(a). The maximum heat sink temperature reaches 90°C for an output of 35 kW. Figure 18(b) shows the temperatures at measured points on a power board. The highest temperature point is on the AC bus, at approximately 70°C, and the second highest one is on the DC bus, at approximately 55°C.

The experiments confirm that there is no thermally critical point on the power board and that the cooling system provides sufficient cooling performance.

Figure 19 shows the simulation results of the evaluation of the SiC MOSFET chip temperatures. The simulation model used in this study is already shown in Fig. 5. The simulation conditions are as follows, inverter loss = 500 W which is extracted from the experimental results shown in Fig. 13(a); ambient temperature T_a = 17°C, which is set to be the same as the condition for the experiment shown in Fig. 18(b). The simulation results for a heat sink temperature of 88°C are in good agreement with the experimental results for 90°C, as shown in Fig. 19(a) and Fig. 18. The simulation results are in good agreement with the experimental results, for the measurement points on the power board, as shown in Fig. 19(b). The gate terminal temperature has a larger error than the other points, which is considered to be due to the modeling error of the thin printed circuit pattern and pins for gate signals. Figure 19(c) shows the MOSFET chip temperature distribution. MOSFET chips on the center-located power module and leeward side chips exhibit higher temperatures. The maximum MOSFET chip temperature is 103°C, according to the simulation results. As the evaluation points around the power modules exhibit good agreement between the simulation and experimental results, the simulation results for the MOSFET chip temperature can be assumed to be sufficiently accurate.

6. Conclusion

This paper presents the development of SiC-based high power density inverters, with experimental results demonstrating that the prototype inverter can achieve a power density of 70 kW/liter and 50 kW/kg, which is more than double the value predicted [9]. The prototype inverter can operate with efficiency higher than 98%.

The following three approaches are used to achieve high power density, and their validity has been confirmed.

1) SiC-MOSFET power modules, which have direct soldered copper foil fins, are proposed and developed. The impact of the proposed power module structure on power density has been evaluated. The developed power modules enhance power density by approximately 24%. The measured *CSPI* of the prototype power modules are 37 W/K*liter and 19 W/K*kg.

2) Removal of the antiparallel SiC SBDs is proposed to enhance the power density. The impact of removing SiC SBDs on the power density has been evaluated. Removing antiparallel SiC SBDs enhances the power density by approximately 40%.

3) A low-loss gate driver for SiC MOSFETs has been proposed [27]. The impact of the proposed gate driver on power density has been evaluated. The proposed gate driver reduces the switching and inverter losses by approximately 12% and 2%, respectively. Therefore, the prototype inverter can use a 2% smaller cooling system, achieving higher power density.

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