Open access • Journal Article • DOI:10.1109/TPEL.2011.2155671

High-Power Modular Multilevel Converters With SiC JFETs — Source link

Dimosthenis Peftitsis, Georg Tolstoy, Antonios Antonopoulos, Jacek Rabkowski ...+4 more authors

Published on: 01 Jan 2012 - IEEE Transactions on Power Electronics (IEEE Press)

Topics: Silicon carbide

Related papers:

- An innovative modular multilevel converter topology suitable for a wide power range
- Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters
- New transformerless, scalable Modular Multilevel Converters for HVDC-transmission
- Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters
- Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters

Share this paper:

View more about this paper here: https://typeset.io/papers/high-power-modular-multilevel-converters-with-sic-jfets-1vt8nvtwzx

High-Power Modular Multilevel Converters with SiC JFETs

Dimosthenis Peftitsis[1], *Student Member*, Georg Tolstoy[1], *Student Member*, Antonios Antonopoulos[1], *Student Member*, Jacek Rabkowski[1,3], *Member*, Jang-Kwon Lim[1,2], Mietek Bakowski[2], Lennart Ängquist[1], *Member* and Hans-Peter Nee[1], *Senior Member*

[1]Electrical Machines and Power Electronics Lab (EME)
School of Electrical Engineering
Royal Institute of Technology (KTH)
Teknikringen 33, SE-10044 Stockholm, Sweden
E-mail: dimost@kth.se

[2]Departement of Nanoelectronics, Acreo AB
Electrum 236, SE-164 40 Kista, Sweden

[3]Institute of Control and Industrial Electronics,
Warsaw University of Technology,
Koszykowa 75, 00-662 Warsaw, Poland

Abstract -- This paper studies the possibility of building a Modular Multilevel Converter (M2C) using Silicon Carbide (SiC) switches. The main focus is on a theoretical investigation of the conduction losses of such a converter and a comparison to a corresponding converter with silicon insulated gate bipolar transistors. Both SiC BJTs and JFETs are considered and compared in order to choose the most suitable technology. One of the sub-modules of a down-scaled 3 kVA prototype M2C is replaced with a sub-module with SiC JFETs without anti-parallel diodes. It is shown that diode-less operation is possible with the JFETs conducting in the negative direction, leaving the possibility to use the body diode during the switching transients. Experimental waveforms for the SiC sub-module verify the feasibility during normal steady-state operation. The loss estimation shows that a 300 MW M2C for high-voltage direct current transmission would potentially have an efficiency of approximately 99.8 % if equipped with future 3.3 kV 1.2 kA SiC JFETs.

Index Terms – Silicon Carbide, Modular Multilevel Converter, SiC JFETs, Diode-less operation, High Voltage Direct-Current Transmission

Corresponding author:

Dimosthenis Peftitsis

Email: dimost@kth.se

Tel: +46-8-790-6627

Tel: +46-76-582-3884

Address: Electrical Machines and Power Electronics/KTH-The Royal Institute of Technology, Teknikringen 33, SE-100 44, Stockholm, SWEDEN.
This paper has been previously presented at the Energy Conversion Congress and Exposition 2010 (ECCE-2010) in Atlanta in September 2010.

High-Power Modular Multilevel Converters with SiC JFETs

Abstract -- This paper studies the possibility of building a Modular Multilevel Converter (M2C) using Silicon Carbide (SiC) switches. The main focus is on a theoretical investigation of the conduction losses of such a converter and a comparison to a corresponding converter with silicon insulated gate bipolar transistors. Both SiC BJTs and JFETs are considered and compared in order to choose the most suitable technology. One of the sub-modules of a down-scaled 3 kVA prototype M2C is replaced with a sub-module with SiC JFETs without anti-parallel diodes. It is shown that diode-less operation is possible with the JFETs conducting in the negative direction, leaving the possibility to use the body diode during the switching transients. Experimental waveforms for the SiC sub-module verify the feasibility during normal steady-state operation. The loss estimation shows that a 300 MW M2C for high-voltage direct current transmission would potentially have an efficiency of approximately 99,8 % if equipped with future 3.3 kV 1.2 kA SiC JFETs.

Index Terms – Silicon Carbide, Modular Multilevel Converter, SiC JFETs, Diode-less operation, High Voltage Direct-Current Transmission

I. INTRODUCTION

For high-power converters with ratings above 10 MW substantial attention is paid to the efficiency. The driving factor is not only the problem to remove the heat caused by the losses, but also the cost for the energy losses, as this cost is usually accounted for when evaluating the total cost for the converter in these applications [1]. A very promising converter topology in this power range is the modular multilevel converter (M2C) [2]-[5], which can provide excellent output waveforms without impairing efficiency. In fact, efficiencies in the range of 99.5 % have been indicated for High-Voltage Direct-Current (HVDC) converters [1]. No other Voltage Source Converter (VSC) topology for HVDC application has shown such high efficiencies. This holds for two-level VSCs, diode-clamped multilevel VSCs and capacitor-clamped multilevel VSCs. Additionally, the two latter suffer from very complicated high-voltage design problems [1]. The reason for the high efficiency of the M2C is that very low switching frequencies can be used, e.g. 150 Hz for a converter operating at a fundamental frequency of 50 Hz. At such low switching frequencies, the on-state losses dominate. The question, therefore, arises what can be done in the future to reduce these losses and to increase the efficiency even more. A very tempting solution is to use silicon carbide (SiC) switches [6]-[8], which potentially could have substantially lower conduction losses than current silicon Insulated Gate Bipolar Transistors

(IGBTs). Replacing the Si IGBT with a SiC counterpart is possible but not necessarily uncomplicated. A Si n-channel IGBT is fabricated starting with a p-type substrate. Such substrates are also available in SiC, but the resistivity is far too high for to be used in components aiming for high-power applications [9]-[11]. Another problem with fabricating a SiC IGBT is to form a good and stable gate oxide layer enabling low channel resistivities [9], [11]. Finally, the SiC IGBT is a bipolar component, and as such it is prone to suffer from parameter degradation due to stacking faults. Even if all these problems are dealt with by many highly qualified scientists, it does not seem likely that SiC IGBTs are on the market within 10 years. Nevertheless, several excellent attempts have been made to fabricate laboratory-scale SiC IGBTs with blocking voltages of 5 kV [10], 7.5 kV [12] and 10 kV [13]. Keeping the fabrication problems of SiC IGBTs in mind, however, the two most realistic switch candidates are the SiC Junction Field Effect Transistor (JFET) and the SiC Bipolar Junction Transistor (BJT) since these two devices are already in series production [8], [14]-[19]. The voltage and current ratings of the devices are, however, not sufficiently high for application in HVDC converters, but with the rapid development in this field it is not unrealistic to foresee substantially increased ratings within 5 years. Additionally, the devices in [8], [14]-[19] have not been tested extensively in commercial products. This would be a reasonable next step before considering application in HVDC converters. Unfortunately, both devices are challenging from a systems perspective. The SiC JFET, on the one hand, is a normally-on component if it is optimized for minimum on-state losses [16]. The SiC BJT, on the other hand, requires a continuous base current as long as the collector current flows [15], [21]. This is a serious drawback in high-voltage applications, since supply transformers for the base-drive circuit are very costly in high-voltage applications, and since the base current is required when the voltage across the BJT is almost zero. With this in mind, the SiC JFET seems to be the most promising candidate. Additionally, no anti-parallel diodes are necessary if the JFETs are operated as diodes when the valve current is negative [22]-[23]. Consequently, a certain amount of the cost increase imposed by the, potentially costly, SiC devices can be reduced at the same time as the complexity is reduced and the availability can be increased. In the present paper the possibility to use SiC JFETs in high-power M2Cs will be explored. The investigation will be made partly as analytical considerations, especially the loss and efficiency estimations, and partly experimentally on an existing M2C prototype.

II. Description Of The M2C Converter

A. *Main Principles*

The M2C converter was proposed by Marquardt and Lesnicar in 2003 [24], while several other research groups have investigated a variety of different aspects dealing with this converter [3], [25]-[27]. In fact, the basic circuit, using voltage sources instead of capacitors, was already proposed by Alesina et al. in 1981 [28]. The main advantage of this multilevel design seems to be the very low switching frequency in comparison to the conventional 2-level converters [1]. The low switching

frequency causes lower switching losses and the dominant part of the total converter losses is the conduction losses of the devices. An estimation of the power losses and the efficiency as well of a realistic, high-power converter which totally consists of SiC JFETs, are presented in Section VI.

A schematic of a three-phase M2C is shown in Figure 1(a). Each phase-leg consists of two arms: the upper and the lower one connected in series. The vital part of this converter is the sub-modules which are connected in series in each arm and in series with a small inductor L_{ARM}. This inductor is connected in order to take up the voltage difference, which is produced when a submodule is switched in or out. A schematic of a single sub-module is presented in Figure 1(b) consisting of two switches with two antiparallel diodes and the capacitor bank. In this figure the switches are drawn as MOSFETs (as in the laboratory prototype), but for a full-scale converter typically high-voltage IGBTs would be chosen.

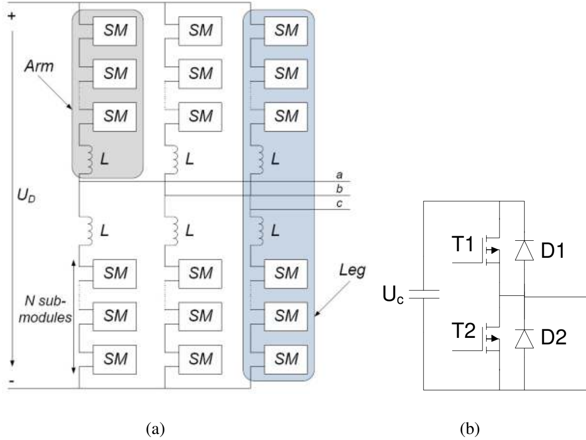

Fig. 1: (a) Schematic of the M2C, (b) Single sub-module.

From the operation point of view, the maximum number of the voltage levels on the output depends on the number of the sub-modules per arm, N. The output voltage is created by the insertion and bypassing of the sub-module capacitors according to a switching pattern created by the modulator. It is important to make sure that the individual capacitor voltages U_c of the sub-modules are properly balanced. Additionally, the sum of all capacitor voltages of the upper arm must be kept the same as that of the lower arm. Finally, the circulating currents in the arms must be controlled. Several control methods dealing with the issues mentioned above have been suggested for the M2C. In this investigation, however, a simple, yet well-performing, open-loop method has been chosen.

B. *Open-loop control*

In order to investigate the behavior of the M2C when one of the sub-modules is replaced with the SiC counterpart, a simple control method is utilized. This control method is the so-called open-loop control for the M2C converter [29]. A closed-loop

control system requires measurement of the total arm voltages as well as those of all sub-modules, which implies a high amount of exchanged data between the controller and the modulator, especially for converters with a high number of sub-modules. On the other hand, the open-loop system estimates the total capacitor voltage, namely the stored energy in the arm, by measuring other quantities, easier to interface with the controller. The open-loop control system is fully described in [29].

III. Expected Performance Improvements with SiC Switches

Due to the rapid development and improvement of the SiC material, device fabrication techniques, design aspects of the devices and various relative issues, the SiC power devices have come closer to the commercialization stage [19]-[20], [22], [30]. Power semiconductor switches built in SiC (e.g. SiC JFETs, SiC BJT and SiC MOSFETs) are already offered as restricted prototype samples by some companies for evaluation, while SiC Schottky diodes are commercially available since a few years ago [31]. High temperature operation of SiC devices (>200°C), lower switching losses, higher current density and smaller device area for the same blocking capability as the Si counterparts are counted as the advantages of SiC versus Si. Recent research results have indicated that both SiC JFETs and SiC BJT potentially may play very important roles in future multi-megawatt power converters that are used for power transmission and high-power motor drives. This can be also verified by comparing the conduction losses for SiC JFETs and SiC BJTs. It is obvious from [17] that JFETs have lower specific on-state resistance than BJTs at the same current density and blocking voltages up to 4-5 kV.

State-of-the art on-state resistances for the SiC JFET have been reported to be lower than 2mΩ.cm^2 for 1200V designs [16], [32], while the currents density of the already developed SiC JFETs exceeds 200A/cm^2 and might overpass this value in the future [16]. On the other hand, both the complicated gate-drive circuits (negative pinch off voltage requirement to turn the JFET off) and the high cost of the existing SiC JFET technology constitute drawbacks that impede commercial use.

Compared to the SiC JFET, the SiC BJT, which has slightly higher on-state resistance (in the range of 4.5mΩ.cm^2 for 1200V design), requires the simplest base-drive configurations, but also a substantially higher base current than the JFET, which should be supplied when the load current flows. Moreover, in order to achieve very short turn-on times, a high-peak current is required to be supplied from the base-drive circuit.

From the drive power consumption point-of-view, the SiC JFET gate power depends on the switching frequency, while the BJT base power consumption is almost constant at low switching frequencies [33]. However, since the switching frequency is very low for the targeted high-power M2Cs, the power consumption of the JFET gate driver will be substantially lower than that for the SiC BJT. Thus, the SiC JFET seems to be a better candidate for this.

Additionally, the ability of high temperature operation of the SiC switches leads to the reduction of the cooling-systems volume. Practically this means less cooling systems for the same power level as the corresponding Si devices, because the SiC

chips can become hotter. This issue also counts to the reduction of the total size and cost of a converter. On the other hand, high temperature packaging for SiC devices is still under development and not that cost-effective.

An additional advantage of SiC JFETs is the possibility of diode-less operation [22]-[23]. This means that no anti-parallel diodes are required in order to pave way for negative load currents, as the JFET conducts also in the negative direction. Since very low voltage drops are anticipated, the body diode of the JFET will not be forward biased during normal operation, except during short transients during the switching between the upper and lower JFETs. This also contributes not only to the total cost and size reduction of the converter, but also to the conduction losses reduction since the reverse current flows through the channel and not through the body diode.

Taking into account the comparison between SiC JFETs and SiC BJTs, it seems that using JFETs might be more efficient for multi-megawatt M2C converters, because of the lower on-state losses. Note also that the switching frequency of the M2C converter is significantly low, thus the contribution of the switching losses on the total converter losses is expected to be slightly lower. A problem with commercially available JFETs is that the ratings are not sufficiently high for application in HVDC converters. In order to have high production yields, chip sizes are comparably small today. In the future, however, the chip sizes are anticipated to be increased significantly with the same production yield due to improvements in material quality and fabrication processes. The development towards larger chip sizes will probably be accelerated by the demand for high voltage (>4.5 kV) switches as these require larger areas for edge terminations. Therefore, higher current ratings will be promoted by two separate development treads. It is, therefore, the opinion of the authors that sufficient current ratings for HVDC converters (approximately 1200 A) could probably be anticipated within 10 years.

IV. Sub-Module Design With SiC Switches

The sub-modules of the lab prototype are all identical in size and appearance and have been implemented with silicon MOSFETs except one, which instead is implemented with two SiC JFETs. As a result of the different switches used, the ratings of the prototype will be scaled down, in order to match the ratings of the lowest rated devices. The current and voltage ratings of the SiC JFETs and Si MOSFETs that are used for the down-scaled prototype and the on-state resistances as well are shown in Table I. The rated power of the original MOSFET 3-phase converter is 10 kVA. However, as the current rating of the SiC JFETs used is almost 3 times lower compared to the Si MOSFETs, the converter rating when using the SiC JFETs will be reduced 3 times. The voltage rating of each sub-module of the prototype converter is limited by the voltage rating of the Si MOSFET. If the voltage rating of the sub-module should be chosen with respect to the voltage rating of the available 1200 V SiC JFETs, a substantially higher voltage rating of the sub-module would be used. However, since the MOSFETs are only rated 300 V this is not possible without having sub-modules with different voltage ratings.

TABLE I
RATINGS OF THE SWITCHING DEVICES

	SiC JFET	Si MOSFET
Voltage rating	Vds = 1200 V	Vds = 300 V
Current rating @ 25°C	Id = 15 A	Id = 46 A
On-state resistance @ 25°C	Ron = 100 mΩ	Ron = 46 mΩ

The MOSFET Printed Circuit Board (PCB) has been modified in such a way that it is possible for the normally-on SiC JFETs to be driven. The differences between the two sub-modules can be seen on the block-diagrams in Figure 2, while both the MOSFETs and the SiC JFETs lab prototype boards are shown in Figure 3. As shown in this Figure, the design of the two sub-modules looks almost identical. A number of essential changes have been done in order to control the normally-on SiC JFETs. For the down-scale prototype the SiC JFETs are connected without any anti-parallel diodes in the same way as the MOSFETs [22]. On the other hand in multi-megawatt M2C converters using SiC JFETs without external, anti-parallel diodes will be a great advantage in comparison to the IGBTs which require external diodes. The difference between the SiC JFETs and Si MOSFETs sub-modules deals with the gate-drive circuit. The MOSFET is a normally-off device, which requires a positive gate-source voltage in order to conduct the current, whereas the SiC JFET is a normally-on switch which needs a negative gate-source voltage. This voltage should be lower than the device pinch-off voltage, in order to keep the JFET turned-off. The gate-drive design is a standard one for the SiC JFETs and has been derived from [34]. The driver is supplied from 24 V integrated dc/dc converter and the gate-source voltage when the JFET is blocking equals to the pinch-off voltage, while it is equal to 0 V when it is conducting. The signals to the SiC JFET sub-module are communicated through fiber-optics from the main controller. To minimize the losses for the sub-module the blanking time should be very small. Thus, the body diode will conduct only for very short time during the transition and after this the reverse current will flow through the channel of the SiC JFET. For this implementation the blanking time is set to 100 ns for both turn-on and turn-off of each device. Doing so, the reverse conduction losses are minimized, since the voltage drop across the channel is lower than the one across the body diode [23], [39].

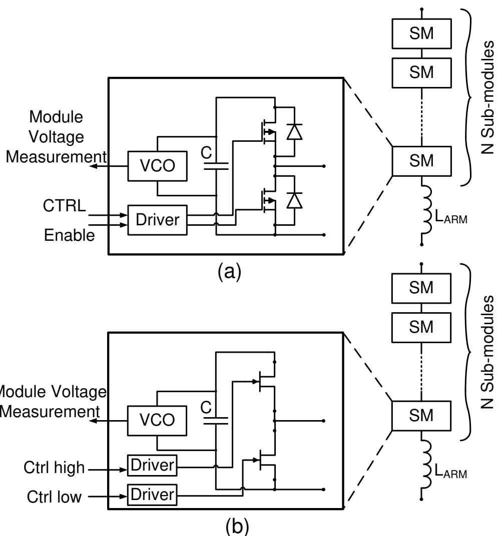

Fig. 2: (a) Sub-module design with Si MOSFETs, (b) sub-module design with SiC JFETs.

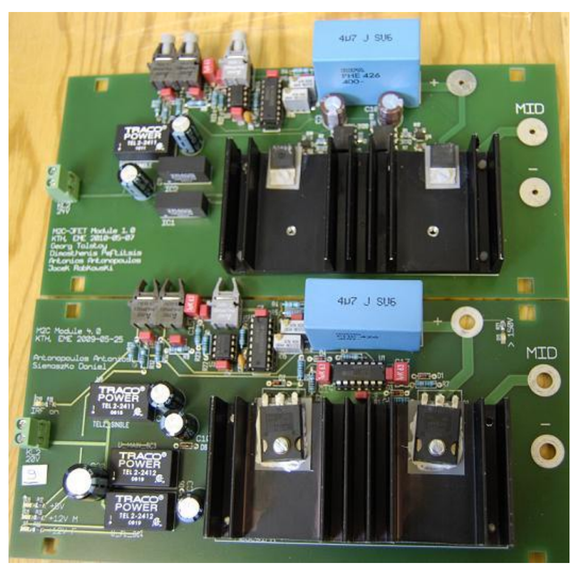

Fig. 3: SiC and Si sub-module boards.

The main energy storage unit of the sub-module is an external capacitor mounted outside the PCB. In order to reduce the influence of stray inductances, a small film capacitor is placed directly on the board suppressing high-frequency transients while switching. The sub-module capacitor voltage is measured and converted into a pulse train with a frequency determined by a voltage controlled oscillator (VCO). Tuning the VCO to a sufficiently high frequency allows an accurate measurement by the FPGA in a short period of time. In this experimental set-up all the VCOs are tuned to produce a 500 kHz digital pulse train when the sub-module capacitor voltage is at its nominal value.

V. Experimental Results

Even though the M2C converter aims to be used for high power applications (HVDC transmission, high power motor drive systems etc), a down-scaled prototype was built in the lab. It consists of 5 sub-modules per arm, which means 10 sub-modules per phase, all built with Si MOSFETs. In a large-scale converter each phase will consist of a significantly larger number of sub-modules, as will be discussed in Section VI. Naturally, it will be more complicated to build and control a large-scale converter, as there is a need to control a significantly larger number of signals, but the M2C concept implies quite good scalability as the topology is modular. On the contrary, in a large scale converter, the greater number of levels per phase will create waveforms of much higher quality than the results shown by the downscaled laboratory prototype. However, even when experimenting only with 10 sub-modules per phase-leg, it is possible to draw safe qualitative conclusions about the shape of the voltages and currents flowing in and out of the converter. The aim then of this paper is to verify the feasibility of using SiC JFETs in such a converter. Thus, one of the Si sub-modules was replaced by a SiC counterpart as shown in Figure 4. Table II summarizes the ratings of the so established 3 kVA M2C prototype including the SiC JFET sub-module.

Note that the measurements for Figures 8, 9 and 10 have been done by using a PC-based data acquisition system, while all the others by using a normal oscilloscope. This is because the access on the SiC JFETs sub-module was easier by using the oscilloscope probes rather than building a separated PCB for measurements of the JFET voltage and current. Hence, the sampling rate of those two instruments is different and therefore the current in Figure 8 is clearer than the one in Figure 5.

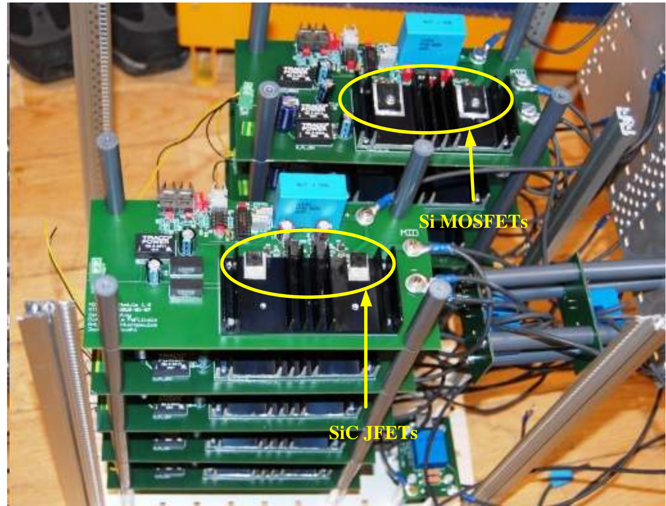

Fig. 4: Phase-leg of the lab prototype showing the SiC and the Si sub-modules.

The low switching frequency of the M2C seems to be one of its greatest advantages. As a result of the low switching frequency, the switching losses are also very low, and thus only the conduction losses play the most important role on the efficiency of such a converter. Figure 5 verifies this statement, showing the drain to source voltage, V_{ds} of the lower SiC JFET

(connected between midpoint and negative bus of the sub-module). The voltage across the upper arm, on which the sub-module with the SiC JFETs is connected, is illustrated in the same figure and the upper arm current as well. It is obvious that the JFET is switching 7 times during the 2 time periods that are shown. A closer view of the upper arm and the drain-source voltages shows exactly the time intervals that the SiC sub-module is either inserted or bypassed (Figure 6). When the lower JFET is turned-off, the upper one is on and the capacitor is inserted, providing an additional voltage level on the output voltage and vice-versa.

TABLE II
RATINGS OF THE PROTOTYPE

Rated Power	S = 3 kV A
Input Voltage	U_D = 500 V
Carrier frequency	fs = 1 kHz
Rated RMS current	I_N = 5.7 A
Number of sub-modules per arm	N=5
Sub-module capacitor voltage	U_c=100V
Sub-module capacitance	C=3.3mF
Arm inductance	L_{ARM}=3.3mH
Output voltage frequency	f_0=50Hz
Modulation index	m=0.9

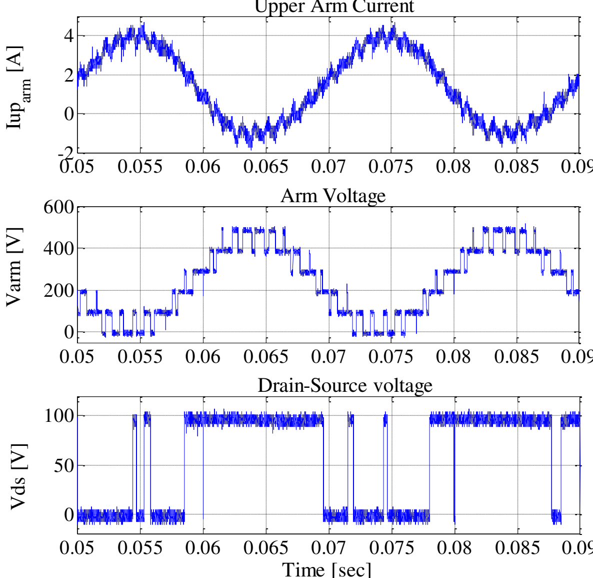

Fig. 5: Upper arm current and voltage, and drain-source voltage of the lower JFET (sampling frequency 50 kHZ).

The operation of the two SiC JFETs on the sub-module is complementary and this can be proven in Figure 7 that shows the drain currents of the two SiC JFETs which correspond to the switching states that are shown in Figure 5. With the chosen control method, the switching states are not identical for each time period, but they depend on the capacitor charge and the

sorting algorithm. This can be verified for the SiC sub-module in Figure 7. The three-phase output currents during normal steady-state operation are shown in Figure 8, while the same Figure also shows the upper and the lower arm currents of the SiC sub-module corresponding phase-leg and the circulating current as well. It can be seen that the circulating current is approximately dc-current equal to one third of the total input dc-current of the converter. Typical steady-state waveforms of the line-line and the three-phase output voltages for the M2C are shown in Figure 9, verifying at least the feasible operation with the SiC sub-module.

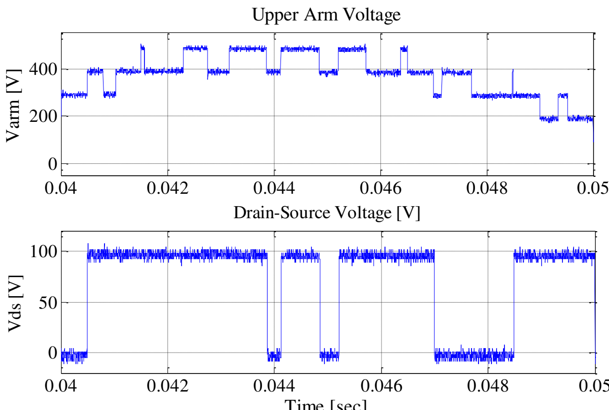

Fig. 6: Insertion and bypass of the SiC sub-module (sampling frequency 50 kHZ).

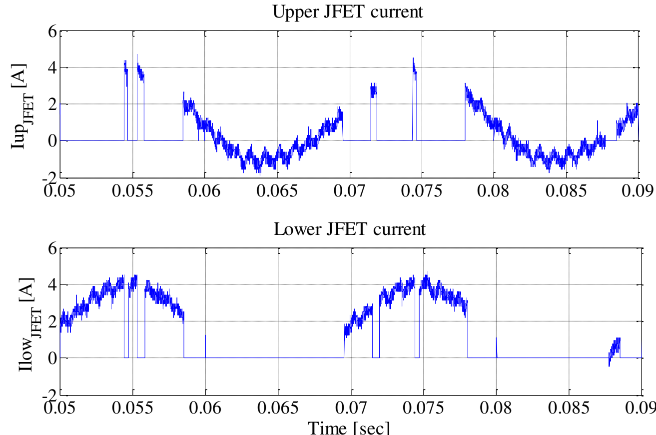

Fig. 7: JFETs switching currents (sampling frequency 50 kHZ).

Figure 10 presents the voltages across the capacitors of the phase-leg on which the SiC sub-module is connected. These 10 voltages look similar to each other even for the SiC sub-module, also proving that it normally operates as the Si ones do.

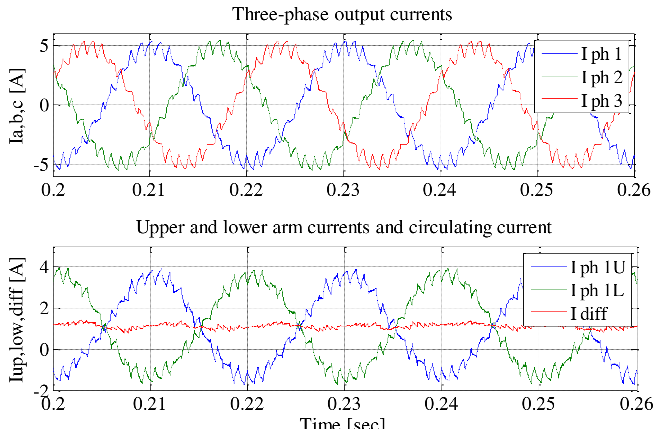

Fig. 8: Three-phase output and arm currents during steady-state operation (sampling frequency 10 kHZ).

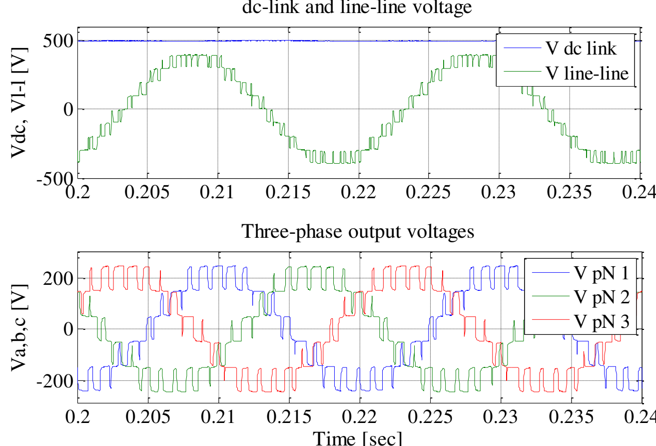

Fig. 9: dc-link, line-line and three-phase output voltages during steady-state operation (sampling frequency 10 kHZ).

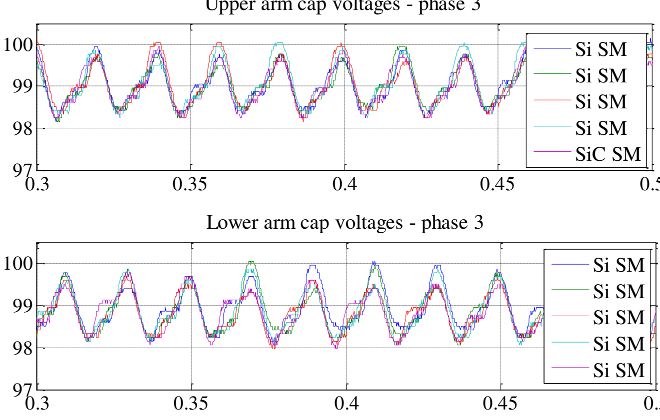

Fig. 10: Capacitor voltages for a whole phase-leg during steady-state operation (sampling frequency 5 kHZ).

VI. Power Loss Estimation For A High-Power Converter

A. High-power SiC JFETs

The power loss estimation has been done assuming two different cases of high-voltage, high-current, normally-on SiC JFETs

with the ratings 3.3 kV/1.2 kA and 4.5 kV/1.2 kA respectively. The threshold voltage has been set equal to -50 V. Although it seems to be unrealistic device cases today, it is likely to fabricate such high-power switches in the future. Therefore, the JFET data that are used for the loss estimation are only simulation results using the Medici software. A current density of 200 A/cm^2 and a switching speed of di/dt=500 A/μs is assumed for the simulations. Table III shows the obtained on-state resistance and the switching-on and off energies as well at 150°C for both JFET cases. As shown in Table III, even though the switching energies for the two SiC JFET cases are similar, the on-state resistance of the 4.5 kV JFET is significantly higher, because this device is closer to the theoretical limits of the unipolar SiC devices [17].

TABLE III
SIC JFET ON-STATE RESISTANCE AND
SWITCHING ENERGY AT 150°C

	3.3 kV SiC JFET	4.5 kV SiC JFET
On-state resistance	Ron = 7.8 mΩ.cm^2	Ron = 29 mΩ.cm^2
Turn-on energy	Eon = 68 mJ	Eon = 57 mJ
Turn-off energy	Eoff = 75 mJ	Eoff = 74 mJ

B. Power losses

In order to estimate the power losses and the efficiency for a 300 MW three-phase M2C that totally consists of SiC JFETs without any externally connected anti-parallel diodes, a number of assumption have been done:

- The losses on the auxiliary and control circuits have been neglected since they are low enough compared to the conduction and switching losses. However, in practice these losses should be included.
- The inductor power losses are also neglected for the present study.
- Each sub-module consists only of two SiC JFETs, thus there are no parallel or series connected devices.
- Since the voltage rating of each SiC JFET is 3.3kV, a voltage of 1.8kV is assumed across the capacitor of each sub-module. Similarly, a voltage of 2.4 kV is assumed across the capacitor when 4.5 kV devices are used.
- Taking into account the capacitor voltage and a dc-link voltage of V_{dc}=300 kV, a number of n=167 levels per arm are considered for the 3.3 kV device case, while a number of n=125 sub-modules for the case of 4.5 kV SiC JFETs.
- The circulating current that is shown in Figure 8 is assumed to be pure dc-current in order to calculate the RMS current flows through the switches.
- The power flow is positive. This means that power is flowing from the dc to the ac side.
- The average switching frequency is 200 Hz as in the measurements. Considering the 50 Hz frequency of the output voltage, this practically means that each of the devices is switching only 4 times during the time period.

- The conduction power losses on the body diode are also neglected due to the very narrow blanking time that was used.
- The upper and the lower SiC JFETs have the same ratings and they are conducting complementary to each other.

Following all the assumption given above, Figure 11 shows the power losses of the SiC M2C converter for various output powers when 3.3kV SiC JFETs are used, while Figure 12 the losses for 4.5 kV SiC JFETs case. It is obvious that for both device cases, the switching losses are really low compared to the conduction losses. Despite the lower number of sub-modules when 4.5 kV devices are used, the power losses are higher caused by the higher on-state resistance. Additionally, the total power losses at 350 MW output power with 3.3 kV devices are only 30% of the corresponding losses with 4.5 kV JFETs. Thus, by using 3.3 kV devices, the volume of the cooling system will be smaller.

Finally, the total efficiency of the SiC M2C converter for both SiC JFET cases is presented in Figure 13. It is high as expected for the SiC JFETs and comparing to the IGBT M2C case presented in [1], the efficiency here exceeds at least 0.3% the corresponding IGBT M2C one, when the output power is 350 MW.

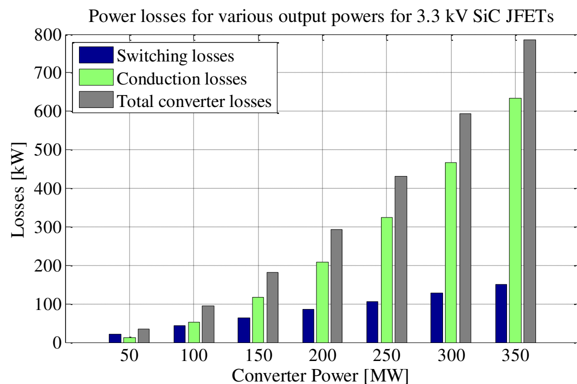

Fig. 11: Power losses for different output power levels with 3.3 kV SiC JFETs.

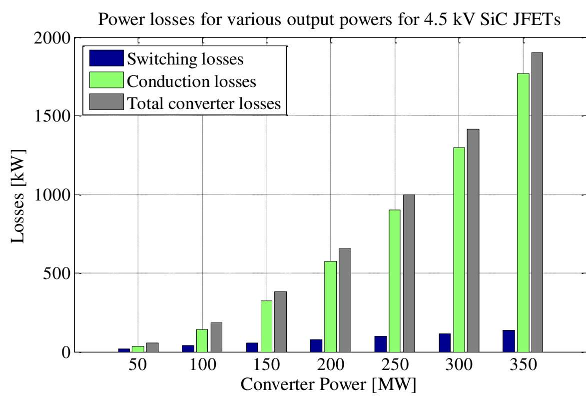

Fig. 12: Power losses for different output power levels with 4.5 kV SiC JFETs.

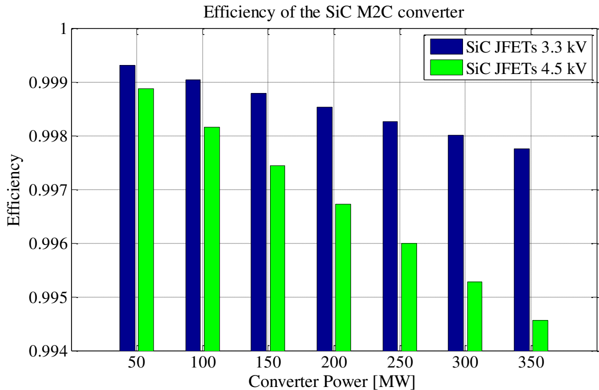

Fig. 13: Comparison of the SiC M2C efficiency for both device cases.

VII. CONCLUSION

This paper investigates the possibility to build multi-megawatt converters using SiC switches. As comparing the use of SiC BJTs and JFETs in such a converter, it is concluded that the SiC JFET seems to be a better solution than the BJT. This is due to the fact that the JFET is a voltage controlled device while the BJT is current controlled and requires a high base current when it is conducting load current.

Based on the discussion between the two SiC switches, one sub-module of a down-scaled 3 kVA M2C with 30 sub-modules was built with SiC JFETs and the experimental results show that it operates as well as the sub-modules with Si MOSFETs. Various steady-state operation waveforms are shown and verify the whole concept and is proved that such an idea is feasible in the future.

Due to the high temperature operation of the SiC devices, cooling requirements for the power devices can be reduced. Consequently the volume, weight and cost for the whole cooling system can be reduced. This paper has also shown that the diode-less operation of the SiC sub-modules is feasible since the SiC JFET that are considered have an integrated body-diode.

Furthermore, the conduction losses have been calculated for SiC-based M2Cs assuming high-power SiC JFETs and it is shown that the losses can be reduced considerably compared to the Si case, while the total efficiency is increasing at least 0.3%. For high-voltage direct current transmission an M2C is found to have an efficiency of approximately 99.8 %.

REFERENCES

[1] S. Allebrod, R. Hamerski, and R. Marquardt, “New Transformerless, Scalable Modular Multilevel Converters for HVDC-Transmission”, in *Proc. Power Electronics Specialist Conference 2008,* Rhodes, June 2008, pp.174-179.

[2] M. Glinka, and R. Marquardt, “A New AC/AC Multilevel Converter Family”, *IEEE Trans. on Industrial Electronics*, Vol. 52, No. 3, June 2005, pp. 662-669.

[3] M. Hagiwara, and H. Akagi, “Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters”, *IEEE Trans. on Power Electronics*, Vol. 24, No. 7, July 2009, pp. 1737-1746.

[4] M. Saeedifard, and R. Iravani, “Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System”, *IEEE Trans. on Power Delivery*, Vol. 25, No. 4, October 2010, pp. 2903-2912.

[5] G.P. Adam, O. Anaya-Lara, G.M. Burt, D. Telford, B.W. Williams, and J.R. McDonald, “Modular Multilevel inverter: pulse width modulation and capacitor balancing technique”, *IET Power Electronics*, Vol. 3, Issue. 5, September 2010, pp. 702-715.

[6] N. Kaminski, “State of the art and the future of wide band-gap devices” , in *Proc. 13th European Conference on Power Electronics and Applications, EPE '09,* 2009 , Page(s): 1 – 9

[7] J.W. Kolar, U. Drofenik, J. Biela, L. Haldwein, H. Ertl, T. Friedli, and S.D. Round, “PWM converter power density barriers”, in *Proc. Power Conversion Conf. (PCC),* Nagoya, Apr. 2007, pp.9-29.

[8] J. Richmond, S. Leslie, B. Hull, M. Das, A. Agarwal, and J. Palmour, “Roadmap for megawatt class power switch modules utilizing large area silicon carbide MOSFETs and JBS diodes”, in *Proc. IEEE Energy Conversion Congress and Exposition ECCE 2009* , Page(s): 106 – 111

[9] Singh, R.; Sei-Hyung Ryu; Capell, D.C.; Palmour, J.W.; , "High temperature SiC trench gate p-IGBTs,", *IEEE Transactions on Electron Devices*, vol.50, no.3, pp. 774- 784, March 2003

[10] Sui, Y.; Wang, X.; Cooper, J.A.; , "High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC,", *IEEE Electron Device Letters*, vol.28, no.8, pp.728-730, Aug. 2007

[11] Friedrichs, P.; Rupp, R.; , "Silicon carbide power devices - current developments and potential applications," in *Proc. European Conference on Power Electronics and Applications, 2005*

[12] Qingchun Zhang; Jun Wang; Jonas, C.; Callanan, R.; Sumakeris, J.J.; Sei-Hyung Ryu; Das, M.; Agarwal, A.; Palmour, J.; Huang, A.Q.; , "Design and Characterization of High-Voltage 4H-SiC p-IGBTs,", *IEEE Transactions on Electron Devices*, vol.55, no.8, pp.1912-1919, Aug. 2008

[13] Das, M.K.; Callanan, R.; Capell, D.C.; Hull, B.; Husna, F.; Richmond, J.; O'loughlin, M.; Paisley, M.J.; Powell, A.; Qingchun Zhang; , "State of the Art 10 kV NMOS Transistors," in *Proc. 20th International Symposium on Power Semiconductor Devices and IC's, 2008. ISPSD '08.*, vol., no., pp.253-255, 18-22 May 2008

[14] P. Friedrichs, “Unipolar SiC Devices: Latest Achievements on the Way to a New Generation of High Voltage Power Semiconductors”, in *Proc. Power Electronics and Motion Control Conference 2006,* IPEMC 2006, 14-16 Aug. 2006

[15] M. Domeij, C. Zaring, A.O. Konstantinov, M. Nawaz, J-O. Svedberg, K. Gumaelius, I. Keri, A.Lindgren, B. Hammarlund, M. Östling and M. Reimark, "2.2 kV SiC BJTs wth low Vcesat fast switching and short-circuit capability", in *Proc. International Conference on SiC and Related Materials 2009 (ICSCRM 2009),* 11 – 16 October 2009, Nuremberg, Germany.

[16] J.-K. Lim, M. Bakowski, and H.-P. Nee, "Design and gate drive considerations for epitaxial 1.2 kV buried grid N-on and N-off JFETs for operation at 250°C", in *Proc. International Conference on Silicon Carbide and Related Materials 2009*, Nürnberg, Oct. 2009.

[17] M. Bakowski, "*Status and prospects* of SiC power devices", *IEEJ Trans. on Industry Applications*, Vol.126, No.4, pp.391-399, 2006.

[18] P. Friedrichs, H. Mitlenher, R. Kaltschmidt, U. Weinert, W. Bartsch, C. Hecht, K.O. Donke, B. Weis, and D. Stephani, "The vertical silicon carbide JFET – a fast and low loss solid state power switching device", in *Proc. 9-th European Conference on Power Electronics and Applications Conf. Record, EPE 2001*

[19] P. Friedrichs, "Silicon Carbide Power semiconductors – New opportunities for high efficiency", in *Proc. 3rd IEEE Conf. On Industrial Electronics and Applications ICIEA 2008*, 1770-1774

[20] I. Sankin, D.C. Sheridan, W. Draper, V. Bondarenko, R. Kelley, M.S. Mazzola, and J.B. Casady, "Normally-Off SiC VJFETs for 800 V and 1200 V Power Switching Applications" , in *Proc. 20th International Symposium on Power Semiconductor Devices and IC's, ISPSD '08.* , Page(s): 260 – 262

[21] H.-S. Lee, M. Domeij, C.-M. Zetterling, R. Ghandi, M. Ostling, F. Allerstam, and E. O. Sveinbjornsson, "1200 V 4H-SiC BJTs with a Common Emitter Current Gain of 60 and Low On-resistance", in *Proc. International Conference on SiC and Related Materials 2007 (ICSCRM 2007),* Lake Biwa Resort, Otsu, Japan, October 14 – 19, 2007.

[22] B. Ållebrand, and H.-P. Nee, "On the possibility to use SiC JFETs in Power Electronic circuits", in *Proc. Proceedings of the European Conference on Power Electronics and Applications (EPE),* August 2001.

[23] B. Ållebrand, and H.-P. Nee, "On the choice of blanking times at turn-on and turn-off for the diode-less SiC JFET inverter bridge", in *Proc. of the European Conference on Power Electronics and Applications (EPE),* August 2001.

[24] A. Lesnicar, and R. Marquardt, "An Innovative modular multilevel converter topology for a wide power range", in *Proc. Power Tech Conference Proceedings*, 2003 IEEE Bologna, page(s): 6 pp. Vol.3

[25] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Proc. European Power Electronics Conference (EPE),* Barcelona, Spain, September 8-10, 2009.

[26] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, “Pulse width modulation scheme for the modular multilevel converter”, in *Proc. of 13th European Power Electronics and Applications Conference,* EPE 2009, Barcelona, 8-10 Sept. 2009.

[27] C. Oates, “A methodology for developing ‘Chain link’ converters”, in *Proc. of 13th European Power Electronics and Applications Conference, EPE 2009*, Barcelona, 8-10 Sept. 2009.

[28] A. Alesina, and M. G. B. Venturini, “Solid-State Power Conversion: A Fourier Analysis Approach to Generalized Transformer Synthesis”, *IEEE Trans. on Circuits and Systems*, vol. CAS-28, NO. 4, April 1981

[29] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, “Inner control of modular multilevel converters – an approach using open-loop estimation of stored energy,” in *Proc. International Power Electronics Conference (IPEC),* Sapporo, Japan, June 21-24, 2010.

[30] Q. Zhang, A. Burk, F. Husna, R. Callanan, A. Agarwal, J. Palmour, R. Stahlbush, and C. Scozzie, “4H-SiC bipolar junction transistors: From research to development - A case study: 1200 V, 20 A, stable SiC BJTs with high blocking yield” , in *Proc. 21st International Symposium on* Power Semiconductor Devices & IC's, ISPSD 2009, Page(s): 339 – 342

[31] R. Rupp, M. Treu, S. Voss, F. Bjork, and T. Reimann, "2nd Generation" SiC Schottky diodes: A new benchmark in SiC device ruggedness”, in Proc. *IEEE International Symposium on* Power Semiconductor Devices and IC's ISPSD 2006.

[32] S. Harada, M. Kato, K. Suzuki, M. Okamoto, T. Yatsuo, K. Fukuda, and K. Arai, “1.8 mΩcm^2, 10 A Power MOSFET in 4H-SiC”, in *Proc. International* Electron Devices Meeting, IEDM '06, 2006 , Page(s): 1 – 4

[33] J-K Lim, G. Tolstoy, D. Peftitsis, J. Rabkowski, M. Bakowski, and H-P. Nee, “Comparison of total losses of 1.2kV SiC JFET and BJT in DC-DC converter including gate driver”, in *Proc. European Conference on Silicon Carbide and Related Materials 2010, ECSCRM 2010*, 29 August-2 September 2010, Oslo, Norway.

[34] S. Round, M. Heldwein, J.W. Kolar, I. Hofsajer, and P. Friedrichs , “A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter”, in *Proc. Conference Record of the Fourtieth IAS Annual Meeting - Industry Applications Conference*, 2005, Volume 1, 410 – 416

[35] J.Callaway, Y. Wang, R. Burgos, T.P. Chow, F. Wang, and D. Boroyevich, “Evaluation of SiC JFETs for a Three-Phase Current-Source Rectifier with High Switching Frequency”, in *Proc. Twenty Second Annual IEEE Applied Power Electronics Conference*, APEC 2007, 345 – 351

[36] W.T. Franke, and F.W. Fuchs, **“**Comparison of switching and conducting performance of SiC-JFET and SiC-BJT with a state of the art IGBT**”,** in *Proc. European Conference on Power Electronics and Applications, EPE 2009*, Barcelona, Spain, 2009.

[37] R. Kelley, A. Ritenour, D. Sheridan, and J. Casady, "Improved two-stage DC-coupled gate driver for enhancement-mode SiC JFET", in *Proc. Twenty-Fifth Annual IEEE* Applied Power Electronics Conference and Exposition (APEC), 2010, Page(s): 1838 – 1841

[38] M.A. Huque, R. Vijayaraghavan, M. Zhang, B.J. Blalock, L.M. Tolbert, and S.K. Islam, "An SOI-based High-Voltage, High-Temperature Gate-Driver for SiC FET", in *Proc. Power Electronics Specialists Conference PESC 2007,* Page(s): 1491 - 1495

[39] G. Tolstoy, D. Peftitsis, J. Rabkowski, and H-P. Nee, "Performance tests of 4,1x4,1mm^2 SiC JFET for DC/DC boost converter application", in *Proc. European Conference on Silicon Carbide and Related Materials 2010*, ECSCRM 2010, 29 August-2 September 2010, Oslo, Norway.

[40] B. Ållebrand, "On SiC JFET converters: components, gate-drivers and main-circuit considerations", *Doctoral Thesis, KTH, Stockholm*, Sweden, 2005

[41] R. Burgos, Z. Chen, D. Boroyevich, and F. Wang, "Design considerations of a fast 0-Ω gate-drive circuit for 1.2 kV SiC JFET devices in phase-leg configuration ", in *Proc. Energy Conversion Congress and Exposition ECCE 2009,* Page(s): 2293 - 2300

[42] D.Aggeler, J. Biela, and J.W. Kolar, "Controllable dυ/dt behaviour of the SiC MOSFET/JFET cascode an alternative hard commutated switch for telecom applications", in *Proc. Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010* , Page(s): 1584 - 1590

[43] T. Friedli, S.D. Round, and J.W. Kolar, "A 100 kHz SiC Sparse Matrix Converter", in *Proc. IEEE Power Electronics Specialists Conference PESC 2007*, 17-21 June 2007, 2148 – 2154

[44] D. Aggeler, J. Biela, and J.W. Kolar, "A compact, high voltage 25 kW, 50 kHz DC-DC converter based on SiC JFETs", in *Proc. Applied Power Electronics Conference 2008*, 24-28 Feb. 2008 pp. 801 – 807

[45] J. Rabkowski, and R. Barlik, "Three-phase inverter with SIC JFETs and Schottky diodes", in *Proc. 16th International Conference Mixed Design of Integrated Circuits & Systems, MIXDES '09,* 2009 , Page(s): 181 - 184

[46] R. Lai, F. Wang, Puqi Ning, Di Zhang, Dong Jiang, R. Burgos, D. Boroyevich, K.J. Karimi, and V.D. Immanuel, "Development of a 10 kW high power density three-phase ac-dc-ac converter using SiC devices", in *Proc. European Conference on Power Electronics and Applications, EPE 2009*, Barcelona, Spain, 2009

[47] T. Friedli, S.D. Round, D. Hassler, and J.W. Kolar, "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter", *IEEE Trans. on Industry Applications,* Volume: 45 , Issue: 5 , 2009 , Page(s): 1868 - 1878

[48] M. Chinthavali, H. Zhang, L.M. Tolbert, and B. Ozpineci, "Update on SiC-based inverter technology ", in *Proc. Brazilian Power Electronics Conference, 2009*, Page(s): 71 - 79

[49] H. Zhang, and L.M. Tolbert, "Efficiency of SiC JFET-Based Inverters", in *Proc. 4th Industrial Electronics and Applications ICIEA 2009,* Page(s): 2056 - 2059

[50] K. Takao, T. Shinohe, S. Harada, K. Fukuda, and H. Ohashi, "Evaluation of a SiC power module using low-on-resistance IEMOSFET and JBS for high power density power converters" , in *Proc. Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010* , Page(s): 2030 - 2035