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High power vector summation switching power amplifier development

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HIGH POWER VECTOR SUMMATION SWITCHING POWER AMPLIFIER DEVELOPMENT

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ABSTRACT

A time sequence of square waves is summed to provide minimum distortion high power voltage sinusoids. The phase difference is varied to control the resultant summed amplitude. Frequency and phase modulation is achieved through digital control of the individual square waves.

1. INTRODUCTION

The U. S. Navy operates strategic Very Low Frequency (15-30 kHz) communication stations which transmit megawatts of power. These stations are now relatively outdated, inefficient, and costly to maintain. Motivation exists to replace these stations with a more efficient and less costly to maintain technology. To fulfill these needs, current switching power technology is being investigated in the 15-50 kHz frequency range and at power levels of 500 kW to 2 MW. Although all known switching regulator configurations have complementary power amplifier configurations, the lesser known approach of vector summation was chosen. With vector summation only one switching transition is required to process unregulated DC input to AC output power. The high efficiency, digital control of modulation, and fault tolerance are advantages of this approach.

2. VECTOR SUMMATION

The basis of the approach consists of a series connection of a number of bridge driven power transformers. The output of each transformer is a square wave whose value is either +V, -V, or 0. Each transformer's square wave is slightly out of phase with the others although the duty ratio is approximately the same for all. The resultant voltage is a minimum harmonic distortion stepped sinusoidal waveform as shown in Figure 1. This waveform is the series sum of the secondaries of eight transformers. Several aspects of this waveform deserve attention. First the turn-on and turn-off times of each step are determined by Fourier analysis for minimum harmonic distortion. Second, as each bridge's step contribution is the same magnitude (+V or -V), it is possible to insure that each of the square waves is also of approximately the same duration. The situation in which the individual square waves have a longer duration at the base of the sinusoid and progressively shorter durations towards the peak should be avoided to prevent distortion and equalize power processing. Instead it is possible to obtain the same resultant voltage waveform by turning off the first bridge to be turned on at the first down step of the sinewave or point A of Figure 1.

STEP VOLTAGE NUMBER	TURN ON (DEG)	TURN OFF (DEG)
1	3.6	110.4
2	10.8	125.7
3	18.2	136.6
4	25.9	145.8
5	34.2	154.1
6	43.4	161.8
7	54.3	169.2
8	69.6	176.4

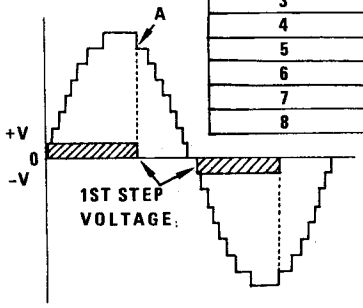

Figure 1. Fourier Analysis Results and Sinewave Construction.

The second square wave is turned off at the second down step of the output sinusoid and so on. This method of sinusoid generation results in a range of individual positive and negative on-time duty ratios of 28% to 32%.

Once a single stepped voltage sinusoid is obtained, a second identical sinusoid is constructed and summed with the first sinusoid. The amplitude resultant of this vector summation sinusoid is controlled by varying the phase difference of the two sinusoids. The magnitude of this resultant is simply given by $2V\cos\theta/2$ where V is the amplitude of each sinusoid and θ is the phase difference.

3. POWER CIRCUITRY

The basic bridge power circuitry is shown in Figure 2. The transistor drive diagrams illustrate the timing required to produce the bridge output waveform shown. When transistors A and B are conducting, the positive voltage step is produced. Transistor A turns off earlier than transistor B, ending the positive step. As transistor B is still on, the transformer's primary is essentially shorted via B and transistor D's snubber diode for currents in the direction indicated. The energy stored in the transformer's leakage inductance can be released without distortion. Also, secondary load current flowing from the series connected secondaries will likewise be shorted in the primary minimizing distortion. If the secondary load current is opposite that shown, a path for primary current flow exists between C and D's snubber diodes and the supply V. The distortion induced in the secondary winding is essentially limited to the supply voltage V during this brief condition. Approximately 4 microseconds after transistor A has been turned off, D is turned on, which insures A and D do not simultaneously conduct to short the supply voltage. During this time with B and D on, the primary is shorted and distortion minimized. Four microseconds after B turns off C can be turned on, and the negative pulse begins. The cycle repeats in a similar manner for the negative pulse.

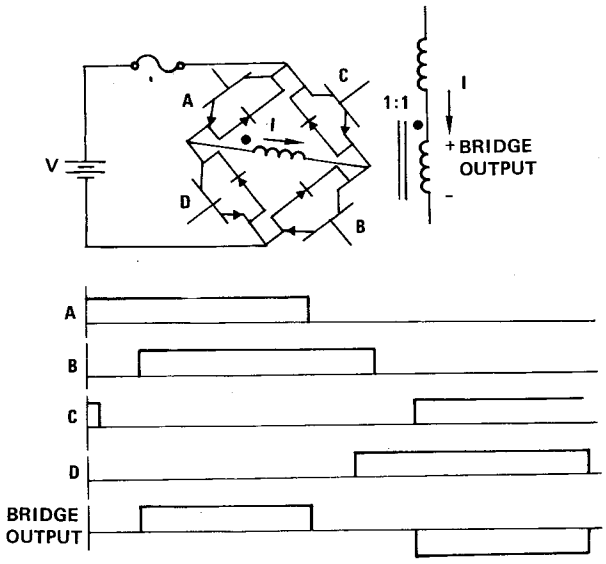

Figure 2. Power Bridge Drive Signals and Output Waveform.

The series connected secondaries of the transformer sum the individual square waves to produce the sinewave shown in Figure 3. The first harmonic's amplitude of this waveform is measured with an FFT and is found to be 22 dB down from the fundamental's amplitude. A further reduction of distortion is possible by increasing the number of steps employed to construct the sinusoid.

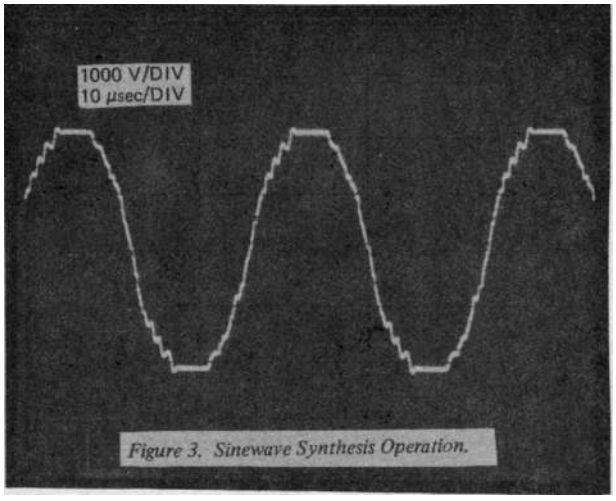

Figure 3. Sinewave Synthesis Operation.

The actual implementation of the power switches employed in the 30 kW breadboard is shown in Figure 4. The Darlington transistor pair Q3 and Q4 are chosen as the main power switches for several reasons. First, the circuit losses are reduced as compared to a single transistor configuration. Second, the inner transistor Q3 prevents the main power switch Q4 from being overdriven. This reduces Q4's storage time and results in a shorter turn-off time. Q3 may be overdriven at light load, but since Q3 handles much less power than Q4, its storage time is also less significant. The base drive transformer T1 performs three functions: conductive isolation, base drive current to the Darlington during the "on" time, and reverse bias during the "off" time due to its flyback action.

When transistor Q1 is turned on, +15 volts are applied across the primary of T1, which induces +5 volts across each of the secondary windings because of a 3:1 step-down ratio. The secondary winding NS1 provides the necessary base drive to the power Darlington, and winding NS2 charges to capacitor C4 through D2. The capacitor charge in C4 will be used to speed up the turn-off of Q4 at the instant of turn-off. C3, C5, and C6 are used for speeding up the turn-on of the transistors. Darlington base resistors R11 and R12 provide a path for diverting noise signals from the base of the Darlington to avoid false triggering. Q2 is cut off during this period because of the reverse bias of its base emitter by the forward voltage drop of D2.

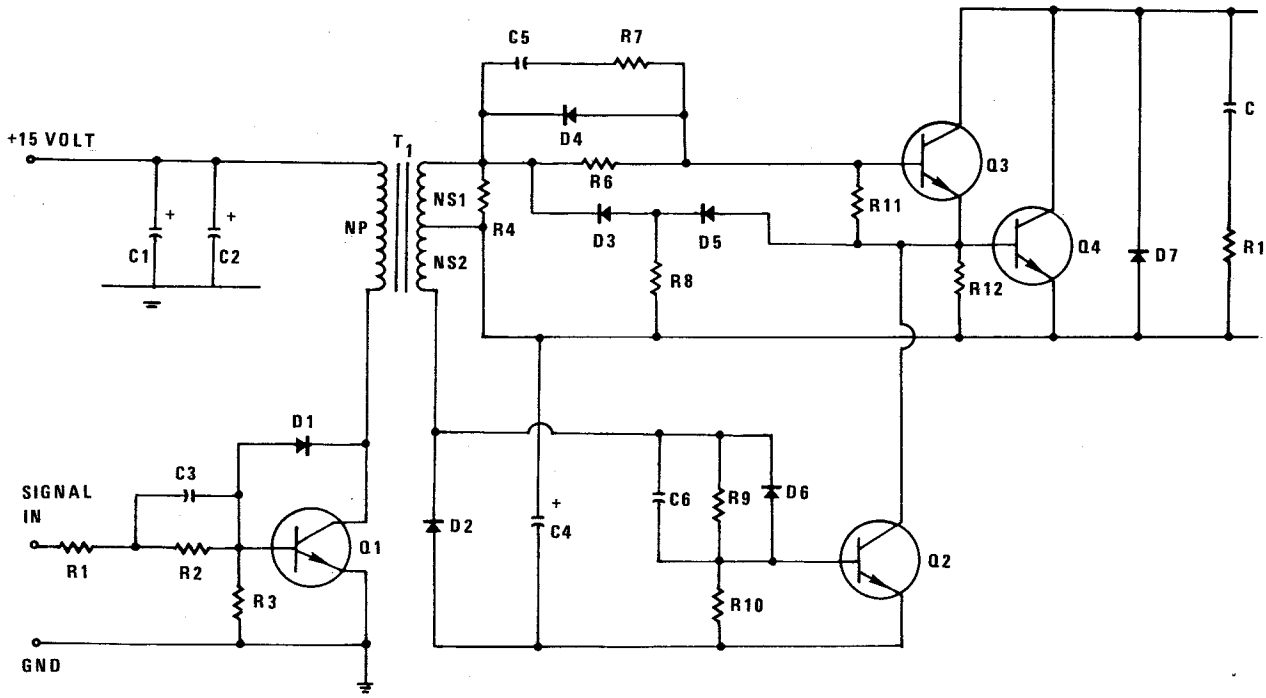

Figure 4. Base-Drive Circuit and Darlington Pair Power Switch.

When Q1 is turned off, the energy stored in T1 is released through several paths. Path 1 (NS2, C6, base-emitter of Q2 and C4) turns on Q2 so that base-emitter of Q4 is reverse-biased by the voltage across C4. This speeds up the sweep out of minority charge and rapidly turns off Q4. Path 2 (C4, emitter-base of Q4, and collector-emitter of Q2) provides reverse bias to the base-emitter Q4. Path 3 (NS1, base-emitter of Q4, and D5, D3, or base-emitter Q3 and D4) sweeps out the minority charge in Q3 and Q4. D3 and D5 provide a discharge path for the B-E junction of Q4 in case Q3 has already been reverse-biased. The combined forward voltage drop of D3 and D5 also insures that B-E junction of Q3 is adequately reverse-biased. Resistors R4 and R8 provide shaping of the transformer secondary voltage waveforms. The values of R4 and R8 are chosen to provide reverse-bias voltage to the power transistor for the entire "off" period. Diode D4 speeds up the turn-off of the Darlington. D6 similarly speeds up turn-off of Q2.

4. BASE DRIVER SIGNAL GENERATION

The control and versatility of the vector summation approach to power amplification lie in the generation of the base drive signals. Figure 5 describes the hardware employed to generate these signals. The ROMs contain the basic bridge switch information to digitally construct a complete sinewave cycle. Since the ROMs are 256 x 8 devices, there are 256 addresses or 256 points within the sinusoid at which a bridge power switch may be turned on or off. The actual turn-on or turn-off points are determined by the Fourier analysis mentioned earlier. The clock frequency is 256 times the desired output sinusoid frequency. As there are eight bits per address, each ROM contains enough switch drive information for eight "A" or "B" transistors in the lead or lag phases. The lead and lag phases each have a separate ROM base drive circuit to permit phase shifts. Although each is driven by a common clock, the addresses of the lead and lag ROMs may be different because of the correction clock pulses supplied to the ALU. The correction clock pulses are either generated by a feedback loop in closed loop operation or manually supplied through a control box in open loop operation. In either case the number of clock pulses added to the lead phase is subtracted from the lag phase and vice versa. This avoids a phase shift in the output sinusoid during corrections.

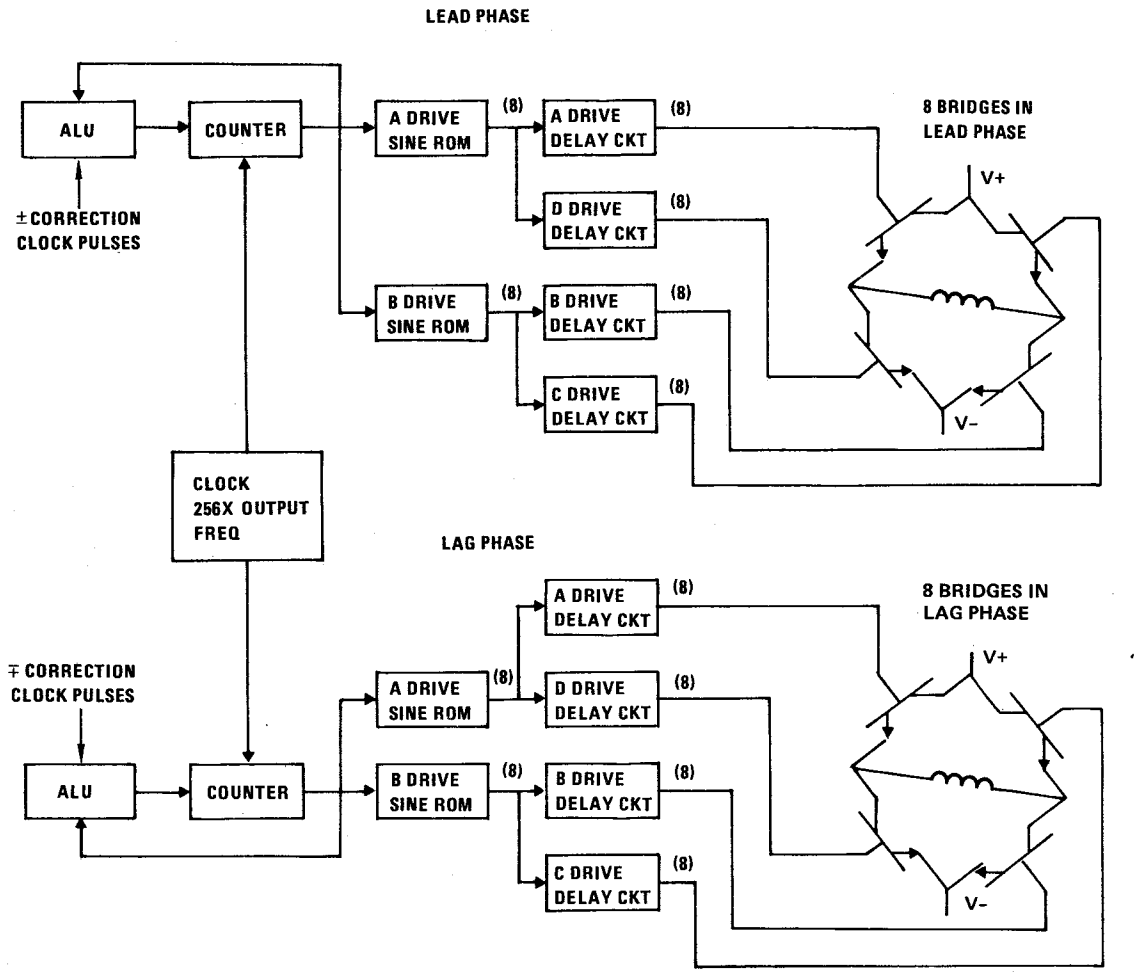

Figure 5. LEAD/LAG Base Drive Signal Generation.

Although a counter could address four separate ROMs for the A, B, C, and D transistors in the lead and lag phases this is not done because of a problem encountered during phase changes. An approximate 4 microsecond delay must exist between turning on and off the A and D or B and C power transistors of the bridges. Without delay circuitry a short occurs when a correction initiates an immediate conduction reversal of the A and D or B and C power switches on the next system clock pulse. The delay circuitry employed to solve this problem allows one of the transistors to turn-off immediately but delays the other transistor's turn-on time by 3.5 microseconds. A beneficial consequence of this approach is that two sets of transistor-base drives can be generated from the same ROM.

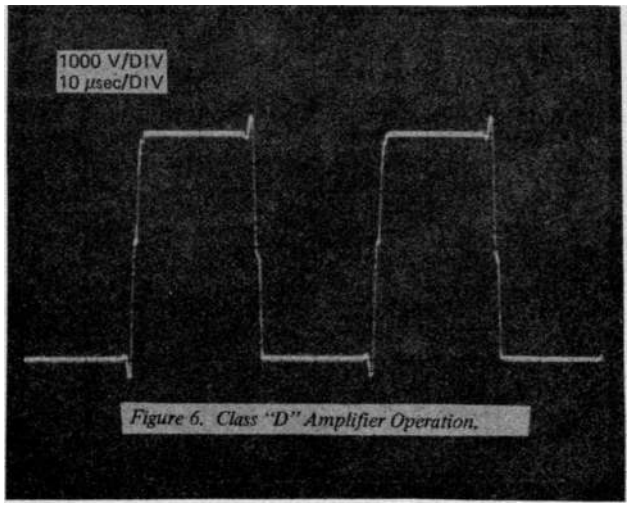

Figure 6. Class "D" Amplifier Operation.

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.SUBCKT STAGE 1 2 3 4  5 6  7 8  10
*ONE STAGE     A B C D  +P-  +S-  VDC
.SUBCKT SNUB 1 2 3
.MODEL TN6655 NPN( BF=43 C2=2 NE=1.245 IK=7.6 BR=1 IS=10PA
+CJC=700PF MC=.44 PC=.41 CJE=1UNF ME=.34 PE=.56
+RC=.74 RB=.11 TF=16NS TR=50US )
Q1  1 2 3 TN6655
RSH  2 3  14
.MODEL D10 D(IS=10PA)
DX  3 1 D10
CX  1 4  .5NF
RX  4 1 75
.ENDS SNUB
*
XA 10  1  5 SNUB
XB  6  2  8 SNUB
XC 10  7  6 SNUB
XD  5  4  0 SNUB
*
LP  5  6  1MH
KT  LP LS .973
LS  7  8 1MH
.ENDS STAGE
*
*
I11 99  11 PULSE( 1A 0A 12US 1US 1US 23US 40US )
I12 15  12 PULSE( 0A 1A .6US 1US 1US 16.9US 40US )
I13 99  13 PULSE( 0A 1A 20.4US 1US 1US 16.9US 40US )
I14 15  14 PULSE( 0A 1A 19.1US 1US 1US 16.9US 40US )
*
I21 99  21 PULSE( 1A 0A 17.8US 1US 1US 23.1US 40US )
I22 24  22 PULSE( 0A 1A 1.4US  1US 1US 16.9US 40US )
I23 99  23 PULSE( 0A 1A 21.4US 1US 1US 16.9US 40US )
I24 25  24 PULSE( 0A 1A 16.9US 1US 1US 16.9US 40US )
*
I31 99  31 PULSE( 1A 0A 15.0US 1US 1US 23.2US 40US )
I32 34  32 PULSE( 0A 1A  2.2US 1US 1US 16.8US 40US )
I33 99  33 PULSE( 0A 1A 22.2US 1US 1US 16.9US 40US )
I34 35  34 PULSE( 0A 1A 19.2US 1US 1US 16.8US 40US )
*
I41 99  41 PULSE( 1A 0A 16.1US 1US 1US 23.1US 40US )
I42 44  42 PULSE( 0A 1A  3.1US 1US 1US 16.9US 40US )
I43 99  43 PULSE( 0A 1A 23.1US 1US 1US 16.9US 40US )
I44 45  44 PULSE( 0A 1A 20.2US 1US 1US 16.9US 40US )
*
I51 99  51 PULSE( 1A 0A 16.9US 1US 1US 23.1US 40US )
I52 54  52 PULSE( 0A 1A  3.9US 1US 1US 16.9US 40US )
I53 99  53 PULSE( 1A 0A  .5US  1US 1US 23.1US 40US )
I54 55  54 PULSE( 0A 1A 20.0US 1US 1US 16.9UU 40US )
*
I61 99  61 PULSE( 0A 1A 0.9US  1A 1A 16.9US 40US )
I62 64  62 PULSE( 0A 1A 5.0US  1A 1A 16.9US 40US )
I63 99  63 PULSE( 1A 0A 1.9US  1A 1A 23.1US 40US )
I64 65  64 PULSE( 0A 1A 22.9US 1A 1A 16.9US 40US )
*
I71 99  71 PULSE( 0A 1A 1.7US  1A 1A 16.9US 40US )
I72 76  72 PULSE( 0A 1A 6.3US  1A 1A 16.8US 40US )
I73 99  73 PULSE( 1A 0A 3.1US  1A 1A 23.2US 40US )
I74 75  74 PULSE( 0A 1A 21.7US 1A 1A 16.9US 40US )
*
I81 99  81 PULSE( 0A 1A 2.5US  1A 1A 16.9US 40US )
I82 86  82 PULSE( 0A 1A 7.0US  1A 1A 16.8US 40US )
I83 99  83 PULSE( 1A 0A 4.8US  1A 1A 23.2US 40US )
I84 85  84 PULSE( 0A 1A 22.5US 1A 1A 16.8US 40US )
VDC  99  0  200V
X1 11 12 13 14 15 16 10 20 99 STAGE
X2 21 22 23 24 25 26 20 30 99 STAGE
X3 31 32 33 34 35 36 30 40 99 STAGE
X4 41 42 43 44 45 46 40 50 99 STAGE
X5 51 52 53 54 55 56 50 60 99 STAGE
X6 61 62 63 64 65 66 60 70 99 STAGE
X7 71 72 73 74 75 76 70 80 99 STAGE
X8 81 82 83 84 85 86 80 90 99 STAGE
*
RL 10  0  90
V0  0 90 0.PROBE
*
.TRAN  .5US  150US UIC
.PLOT TRAN V(10)
.FOUR  25KHZ  V(10)
.OPTIONS METHOD=GEAR RELTOL=.01 ITL5=50K LIMPTS=1001 TRTOL=5.0
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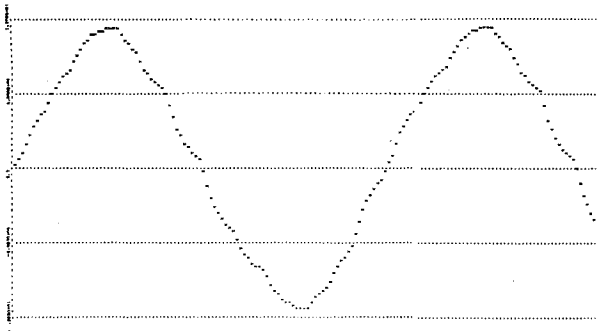

Figure 7. SPICE Runstream and Output Voltage.

This approach to base drive signal generation allows for flexibility in output voltage waveform and modulation. Shifting from one clock frequency to another induces frequency modulation of the output. Amplitude modulation results from varying the lead and lag sinusoid phase angle. The output voltage waveform shape may easily be changed by employing a differently programmed set of ROMs in place of the sine drive ROMs. Power amplifier class "D" operation is easily simulated by programming the ROMs to provide in-phase square waves from all the bridges. When this is done the waveform of Figure 6 results. Class D operation also exerts the maximum power processing capability of the amplifier for a given source voltage and load. In actual transmitter operation the square wave is applied to a high Q resonant antenna load. Appreciable sinusoidal current is drawn and radiated at only this resonant frequency.

5. COMPUTER MODELING

The basic power circuitry of the vector summation power amplifier has been modeled on SPICE. Information regarding the predicted Fourier harmonic distortion of the stepped sinusoid; and power processing efficiency as a function of frequency, lead/lag phase angle and power level is obtained. Also modeled are the effects of operating into a high Q antenna resonant load and various fault conditions. Figure 7 shows the SPICE run stream modeling the basic power circuitry for the eight bridges of the lead or lag phase. Also shown in Figure 7 is the resultant sinusoidal voltage waveform. The program is brief despite the number of components involved because the redundant nature of the power circuitry allows good use of SPICE's subcircuit models.

6. FAULT TOLERANCE

Fault tolerance techniques are an extremely important part of any high power solid state power amplifier. As power levels and the quantity of power processing circuitry are increased, the need for fault tolerance becomes more pronounced. The primary fault of concern is the failure of the power switches. If a bridge power switch fails open or closed, it will cause the bridge fuse or circuit breaker protecting the high power supply to open. In the case where a switch fails closed, the fuse will open the next time the other switch on the same side of the bridge is closed. Should a power switch fail open, the bridge's transformer will eventually be driven to saturation by the remaining pair of functioning switches. When this happens, the fuse will also open. The major concern is that the amplifier should be able to continue operation in this case without major degradation of the output waveform. However the secondary load current induced by the other active bridges could find an open circuited primary in these cases if the failed

bridge's power switches are not functioning. The degradation of the output sinusoid in this case is significant.

To alleviate this problem, the effect of shorting the transformer's primary upon the bridge fuse opening is being investigated. This effectively removes the bridge from the power circuitry and the degradation of the output waveform is minimal. One additional benefit of this approach is that in-operation repair of the power amplifier may be possible. If the bridge's power circuitry is mounted on removable racks or cards, removal and replacement of the faulty switches may be possible while the amplifier is operating.

In addition the feasibility of spare on-line power bridges is being investigated. In this case the spare bridge's transformer secondary winding is series connected with the other transformers, but its primary is normally shorted. Also, the power switch drives are normally inhibited. The detection of a fault in another bridge causes the fault bridge's primary to be shorted and its switch drives removed. These switch drives are then applied to the on-line spare bridge and its primary short removed. In this manner the spare bridge replaces the faulted bridge.

7. POWER LEVEL SCALING

Power scaling is of immediate interest. The goal is to produce power amplifiers capable of processing several megawatts of power with solid state switches. A number of approaches are possible and are being given consideration. The number of voltage steps or bridges employed in the construction of the sinewave can be increased. This has the additional benefit of decreasing the harmonic distortion under normal and bridge fault conditions. The number of bridge power switches in parallel can be increased. This may be readily accomplished with FETs but is still quite possible with bipolar transistors. Design and construction of a 30 kW bridge are presently underway. Also under design and construction is the power transformer combiner approach. Here the power handling capability of a lead/lag power generation unit is fixed. A particular power level is achieved by operation of multiple lead/lag power units in parallel and effectively summing their power outputs with a combiner transformer. The primary windings of the combiner transformer are connected to the outputs of the individual lead/lag power units and the secondary winding sources the load.

8. SUMMARY

The vector summation approach to high power amplification offers a number of significant advantages especially in transmitter applications. Very high efficiencies and the potential to use unregulated DC input power are possible. Modulation flexibility exists. It is possible to shift from sinewave synthesis to class D operation by changing the base drive ROMs employed. Amplitude modulation is accomplished by varying the lead/lag phase angle separation and frequency modulation through varying the system clock frequency. Sinewave synthesis provides a low harmonic distortion output not possible with class D amplifier approaches. This decreases antenna resonating circuitry requirements and permits other modes of transmitter operation such as frequency hopping. Lastly, fault tolerance approaches are inherently practical because of the redundant nature of power circuitry.

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