High Precision Low Temperature Coefficient Current Reference with Resistor Compensation

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***Abstract*—In order to improve temperature characteristics and precision of current reference, a novel resistor compensated current reference based on bandgap voltage reference with trimming network is proposed in this paper. By introducing the combination of 2nd order resistor and transmission gate whose temperature characteristics compensate that of bandgap voltage reference, lower temperature coefficient has been achieved. This circuit is implemented using HHNEC 0.35um BCD process with 3.3V power supply. Simulation results for the proposed current reference show the worst temperature coefficient of 15.25ppm/°C and the best temperature coefficient of 5ppm/°C over a temperature range from -45°C to 85°C. With trimming network, an output current variation of 1.4‰ is achieved among process corners. On the premise of not introducing high-order curvature compensated to bandgap which increase circuit complexity, this circuit put forward a new thought for the design of current reference.**

Keywords-Current reference, Resistor compensation, Trimming network, Temperature coefficient

I. INTRODUCTION

Current reference is a basic building block in analog circuit. The implementation of analog-mixed circuit such as current-steering data converters, loop-powered data converters[1], etc. needs stable bias current which is derived from current reference. With layout techniques to improve matching, reference current can be accurately mirrored and multipled by current mirrors, then bias other components in analog circuit. So it is of great significance to design a high precision low temperature coefficient current reference.

It has been admitted that the current reference does not exist alone but has to consist of a bandgap voltage reference (BVR) and one or two resistors. With curvature correction and resistor trimming technology, the temperature coefficient (TC) of BVR could be kept under 2ppm/°*C* [2][3][4]. But the corresponding low TC current references have been rarely covered. The major difficulty is the lack of resistor that is independent to temperature[5], which means the bandgap voltage reference is not virtually irrelevant to temperature when designing low TC current reference. By compromising parts of BVG temperature coefficient to cooperate with resistor, we obtain better current reference. Based on study of traditional current reference, we propose a novel resistor-compensated current reference to achieve better temperature coefficient. By adding resistor trimming network to the circuit, high precision is expected to be fulfilled.

II. TRADITIONAL CURRENT REFERENCE

In order to get current reference from BVR, a resistor is needed[6]. The best way converting voltage to current is using amplyfier. The schematic of traditional current reference has been shown in Figure.1. The circuit uses an amplifier in a negative feedback loop to drive the voltage across resistor R euqal to bandgap reference voltage V_{REF}. The current I_{OUT} flowing through current regulator MOS *P* is forced to be exactly the same with current flowing through resistor *R*. The major error comes from input offset voltage of amplyfier *AMP*.

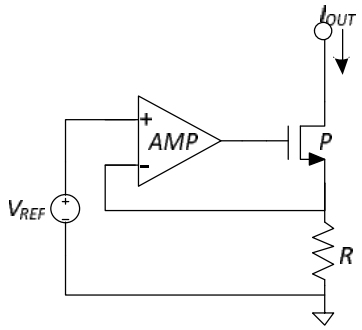

Figure 1. Traditional current reference

When voltage reference V_{REF} and the resistor *R* are all ideal, output current can be expressed as $I_{OUT}=V_{REF}/R$. But the integrated resistors which are related to temperaure and process make current reference highly sensitive to temperature change and process variation. This problem can be solved perfectly by using off-chip hybrid resistor[7], but hybrid resistor is costly and cannot be implemented in off-chip-resistor-prohibited system. Hosung Chun proposed a method that can reduce the effect of resistor value variations by combining different kinds of integrated resistor together in series[8]. Each kind of integrated resistor has its own process parameter independent to others. When the process changes, different kinds of resistor can compensate each other to achieve stable resistence.

The methods mentioned above make current reference more precise, but they all ingored the resistor's own temperature characteristics which affect temperature characteristics of current reference. One way to solve this problem is adding I_{PTAT} and I_{CTAT} current to compensate

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high-order term in current reference[9]. Ming-Dou Ker[10] reports utlizling the difference of temperature-dependent currents generated from the parasitic n-p-n and p-n-p bipolar junctions to obtain temperaure-independent current reference. All these methods ignore the resistor temperature characteristics and require complex circuits implementation.

Temperature characteristics of 1st order compensated BVR are slightly parabolic shape, where output voltage has a nearly zero temperature coefficient at peak. As the current reference is the output voltage of BVR divided by the resistor, therefore we conside to design a resistor whose temperature characteristics compensate the curve of BVR to achieve better TC current reference. The compensation theory is shown in Figure.2.

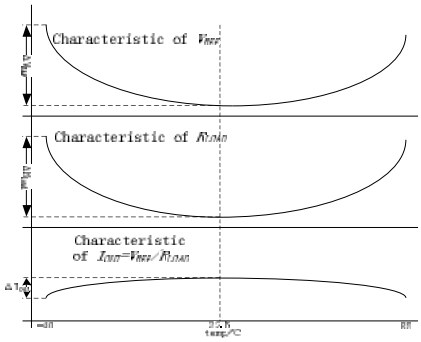

Figure 2. The theory of resistance compensation

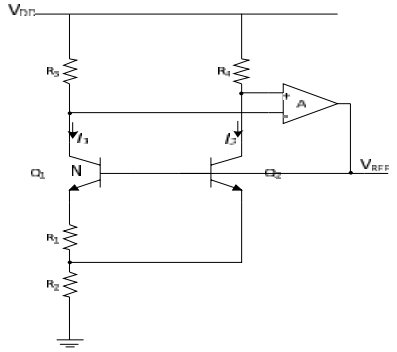

Figure 3. Circuit architecture of Brokaw BVR

III. CHARACTERASTICS OF BANDGAP VOLTAGE REFERENCE

A voltage reference with zero temperature coefficient can be achieved by adding the negative TC of V_{BE} to positive TC V_{PTAT} weighted by K, since the voltages referenced to V_{BE} and V_{PTAT} have opposite temp coefficient.

$$V_{REF} = V_{BE} + K \times V_{PTAT} \tag{1}$$

Based on theory above, many BVR circuits have been proposed. Among them, the Brokaw bandgap[11] is widely used in high precision data convertors for its simplicity, ability to operate at low supply voltages and easing of scaling the output voltage above the silcon bandgap voltage. The circuit archtecture of Brokaw BVR is shown in Figure.3.

In this circuit, amplifier A in deep negative feedback loop enforces the voltage across resistor R_3, R_4 to be the same voltage. If R_3 is equal to R_4, the bias currents I_1 and I_2 flowing through collector of n-p-n bipolar Q_1 and Q_2 are identical. Assuming the current gain of n-p-n bipolar is large enough that base current of n-p-n bipolar can be ignored, we obtain:

$$V_{REF} = V_{BE2} + (I_1 + I_2)R_2 \tag{2}$$

Because the emitter area of Q_1 is N times larger than that of Q_2, with the same biased current the value of V_{BEQ1} is smaller than V_{BEQ2}. The difference bewteen these two voltage is the proportional to absolute temperature voltage(V_{PTAT}). Dividing V_{PTAT} by resistor R_1 we get the expression I_{PTAT}:

$$I_{PTAT} = \frac{V_{BE2} - V_{BE1}}{R_1} = \frac{V_T \ln \frac{I_{C2}}{I_{S2}} - V_T \ln \frac{I_{C1}}{I_{S1}}}{R_1} = \frac{V_T}{R_1} \ln \frac{I_{C2} I_{S1}}{I_{C1} I_{S2}} = \frac{kT}{R_1 q} \ln N = \frac{\beta}{R_1} \cdot T \tag{3}$$

Where V_{BE2} is the forward voltage drop across the base emitter junction of bipolar Q_2. The relationship between V_{BE} and temperature is a nonlinear property, Tsividis studied *Temp-*V_{BE} characteristic of bipolar and gave the euqation as[12]

$$\begin{aligned} V_{BE} &= V_{g0} - \left(\frac{T}{T_0}\right) \cdot \left(V_{g0} - V_{BE}(T_0)\right) - (\eta - \alpha) \frac{kT}{q} \ln\left(\frac{T}{T_r}\right) \\ &= V_{g0} - \left[\frac{V_{g0} - V_{BE}(T_0)}{T_0} - \frac{k(\eta - \alpha)}{q} \cdot \ln T_0\right] \cdot T - \left[\frac{k(\eta - \alpha)}{q}\right] \cdot T \ln T \\ &= \alpha_0 - \alpha_1 T - \alpha_2 \cdot T \cdot \ln T \end{aligned} \tag{4}$$

Where V_{g0} is the bandgap voltage of silicon at *0°K*, η is a constant depending on process, α is the order of tempature dependence of collect bias current, when the current flows through bipolar is small and proportational to absolute temperaure $\alpha = 1$, otherwise $\alpha = 1$. In (4), the term of *TlnT* can be expanded by Taylor series, we obtain: $TlnT \approx T^2/2 - 1/2$, rewrite (4):

$$V_{BE} = \left(\alpha_0 + \frac{\alpha_2}{2}\right) - \alpha_1 T - \frac{\alpha_2}{2} T^2 \tag{5}$$

Substitude (3) (5) into (2), we can get the expression of Brokaw BVR:

$$\begin{aligned} V_{REF} &= V_{BE} + V_{PTAT} = \left(\alpha_0 + \frac{\alpha_2}{2}\right) - \alpha_1 T - \frac{\alpha_2}{2} T^2 + 2\beta \frac{R_2}{R_1} \cdot T \\ &= \left(\alpha_0 + \frac{\alpha_2}{2}\right) + \left(\alpha_1 - 2\beta \frac{R_2}{R_1}\right) T - \frac{\alpha_2}{2} T^2 \end{aligned} \tag{6}$$

Expression (6) indicates that the temperature characteristics of 1st order compsenstaed Brokaw BVR has parabolic shape. The location of the peak voltage of V_{REF} is a function of the ratio of R_1 to R_2. This relationship can be derived by first recognizing that V_{REF} peaks at T_0, where

$dV_{REF}/dT=0$. Solving this equation for T, substituting T with T_0, and solving for R_1/R_2, yields the resistor ratio that will place the peak of V_{REF} at any specified T_0. [13] The equation is:

$$\frac{R_2}{R_1}=\frac{\alpha_1-\alpha_2 T_0}{2\beta} \tag{7}$$

T_0 where $dV_{REF}/dT=0$ is called the "Magic Temperature". From the nature of parabola, only when the magic temperature point locates in the middle of full temperature range, can we get the minimum difference of V_{REF} to achieve the best temperautre coefficient in the condition of 1st order compensate.

IV. DISSCUSSION ON RESISTOR COMPENSATION

In CMOS process, the resistance varies with the temperature and the voltage applied on it. SPICE models use parameter TCR and VCR to represent temperature coefficient and voltage coefficient respectively. In SPICE models, resistance is defined as[14]

$$R_{eff}=R_{SH0}\frac{L}{W_{eff}\,pf}\times vc_{coeff}\times\left[1+TCR1\cdot T+TCR2\cdot T^2\right] \tag{8}$$

Where pf is the numbers of multiple fingers, L is the length of resistor, W_{eff} is the effective width deducting beak effect, R_{SH0} is sheet resistance measured at $0°C$. The R_{SH} is proportinal to resistivity ρ which is a temperature dependent variable[15], SPICE uses a quadratic to model the temperature dependence of a resistor, $TCR1$ is the 1st order temperature coefficient whereas $TCR2$ is the 2nd order temperature coefficient. If we choose the resistor with 2nd order temperature coefficient in process whose temerature characteristics match Brokaw BVR temperature characterisitcs, it is possbile to achieve lower temperature coefficient current reference. In practice, due to process limitation, it is difficult to find a resistor whose temperature characteristics perfectly match that of BVR. We should compensate this 2nd order resister to make it matches with the BVR better.

The simplest way of compensating 2nd order resistor is to connect 1st order resistor connecting in series. The resistance of 1st order resistor compensated hybird resistor can be expressed as:

$$R=R_{1st}+R_{2nd}=R_1\cdot\left(1+TCR1_1\times T\right)+R_2\cdot\left(1+TCR1_2\times T+TCR2_2\times T^2\right)$$
$$=R_2TCR2_2\left(T+\frac{R_1TCR1_1+R_2TCR1_2}{2R_2TCR2_2}\right)^2+C \tag{9}$$

The temperature characterisitcs of 1st order resistor compensation is parabolic. The curve needed to compensate Brokaw BVR can be obtained by adjusting the ratio of R_1 to R_2. But this method consumes large layout area and cannot be compatible with trimming technology which guarantees the precision of current reference. Transmission gate(TG) consisting of NMOS and PMOS whose resistance is the MOS on-resistance is a better choice. In switching state, the resistance of TG is defined as the ratio of drain-source voltage(V_{DS}) to drain current I_D:

$$R_{ON}\equiv\frac{V_{DS}}{I_D}=\frac{L\cdot t_{ox}}{\mu_n\cdot\varepsilon_{ox}\cdot W\cdot\left(V_{GS}-V_T\right)} \tag{10}$$

Where V_T is the threshold of MOS which has a linear relationship with temperature, μ_n is the mobility of electron whose temperature characteristic is proportional $T^{1.5}$. Simulation results show that the on-resistance of TG approximately has a linear relationship with temperature[16]. Therefore ratio of width to length of MOS in TG can be adjusted so that the temperature characteristics of TG compensated hybrid resistor match that of the Brokaw BVR, which is the similar to 1st order resistor compensated method. Compared with 1st order resistor compensation, layout area can be reduced by using TG. More importantly TG can be used in digital trimming circuit to improve the precision of current reference.

V. PROPOSED CIRCUIT ARCHITECTURE

The schematic of proposed CMOS current reference is shown in Figure.4. The core circuit consists of two parts: 2.5V bandgap voltage reference and 32uA current reference. By means of an operational amplifier and transistors, a stable voltage reference V_{REF} generated by Brokaw BVR is applied across a compensated resistor which consists of a 2nd order resistor and a TG connecting in series, resulting in a current. Bandgap reference biasing circuit and start-up circuit are also added to make current reference a complete system.

The core of 2.5V Brokaw BVR consists of Q_8, Q_9, R_6, R_7. The error amplifier which consists of P_5, P_6, Q_{11}, Q_{12} and R_8 enforces collectors of Q_8, Q_9 to have equal potential. The 2.5V Brokaw BVR is supplied by current source composed of P_7 and Q_{10}. Compared with voltage supply, current supply can improve the current reference's PSRR by obtaining feedback current from BVR rather than a voltage. R_9 and R_{10} are used to boost the output voltage of BVR. Ignoring the input offset of error amplifier we know $V_{REF}=V_1(1+R_{10}/R_9)$, where $V_1=1.25$ is the Brokaw BVR output voltage. Making $R_{10}=R_9$, we obtain 2.5V voltage reference V_{REF}.

In 32uA current reference circuit, P_{10}, P_{11}, Q_{14}, Q_{15}, Q_{16}, R_{15} and P_{12}, N_3 compose of a two-stage amplifier used to increase the output resistance of current reference. Bias circuit consists of P_8, P_9, Q_{13}, R_{14} and N_2, and the bias voltage is supplied by 1.25V bandgap bias which consists of P_3, P_4, Q_5, Q_6 and R_2, R_3. The two-stage amplifier is in deep feedback state, so voltages apply on differential pairs(V_+ and V_-) are forced to be equal: $V_+=V_-=V_{REF}\bullet R_{14}/(R_{11}+R_{14})$. If $R_{11}=R_{17}$, then we have:

$$I_{out}=\frac{V_{REF}-V_+}{R_{17'}}=\frac{V_{REF}}{R_{11}+R_{14}} \tag{11}$$

The Brokaw BVR has a zero-state when there is no current in the circuit at start-up. Therefore start-up circuits are introduced to avoid zero-state at start-up. P_1, Q_1, Q_2, Q_3 and R_1 compose the 1.25V bandgap bias start-up circuit. P_1

is a long channel PMOS used as MOS resistor. When the power is on, start current flows through P_1, Q_2 to the core of 1.25V Brokaw BVR. Once the BVR is on, the ΔV_{BE2} becomes less than 0.7V turning off the Q_2.The start-up process is over. 2.5V BVR start-up circuit consists of P_2, Q_4, Q_7. 1.25V bandgap bias provides a start-up current flowing through P_2 and Q_4 to the core of 2.5V BVR.Similarly, once 2.5V BVR is on, the ΔV_{BE7} becomes lower than 0.7V turning off the start-up circuit of 2.5V BVR.

VI. SIMULATION RESULTS AND ANALYSIS

Based on HHNEC035um BCD process, the current reference circuit is simulated with HSPICE. Figure.5 shows the current reference output I_{OUT} versus temperature at TT corner. At TT corner the maxim value of current is 32.01uA at 22.5°*C*, and it has the minimum value 31.97uA at -40°*C* and 85°*C*. The curve is totally a parable shape as expected with the TC of 11.25ppm/°*C*. Figure.6 shows the 2.5V BVR output V_{REF} versus temperature, the zero-drift point is around 22.5°*C*, the TC of BVR is 7.057ppm/°*C*. We get the resistance versus temperature from $R_{LOAD}=V_{REF}/I_{OUT}$, as shown in Figure.7. From the curve, we found that the transmission gates compensate the 2nd order resistor perfectly. The total power dissipation is 0.42mW at 3.3V voltage supply.

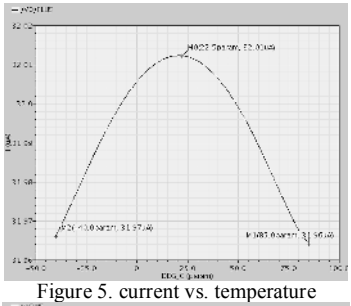

Figure 5. current vs. temperature

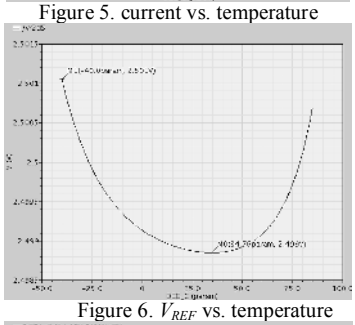

Figure 6. V_{REF} vs. temperature

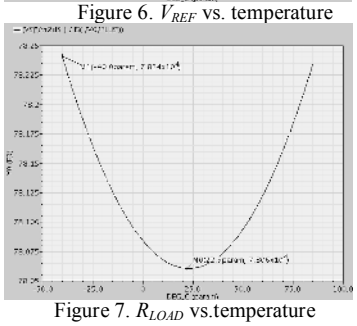

Figure 7. R_{LOAD} vs.temperature

Because the resistance varies ±20% with process changing, digital trimming technology was introduced to guarantee the precision requirement. With transmission gates, the R_{14} in Figure.4 was divided into serval binary weighted segements. The transmission gates are controlled by serial shift register composed of d-flip-flops connecting in series. The schematic diagram is shown in Figure.8. The ratio of *W* to *L* of each transmission gate must be set carefully, so that the temperature characteristic of each segements match the temperature characteristic of BVR.

During the simulation, we set the processes of resistor independent to other device. After trimming, the current reference outputs(I_{OUT}) and bandgap output voltages(V_{REF}) at 9 corner are presented in Tab.1:

The worst temperature coefficient (TC) of current reference which is about 15.25ppm/°*C* appears in fast-fast corner of other device and typical resistor process corner. In the case of slow-slow of other device where the temperature characteristic of resistor matches V_{REF} better, although the TC of V_{REF} is worse, the TC of I_{OUT} is better and can achieve as low as 5ppm/°*C*.

VII. CONCLUSION

The resistor compensated accurate current reference with digital trimming technology is proposed. Under the condition of not introducing high order compensation to bandgap, we use the combination of transmission gate and 2nd order resistor compensating the tepmerature characteristic of Brokaw bandgap reference. To calibre the process violation, the serial shift registers change the value of resistor network which controls the temperature coefficient and magnitude of the reference current perfectly. Simulation result showed the worst temperature coefficient of 15.25ppm/°*C* for the reference current across a temperature range from -40°*C* to 85°*C* and the maximum output reference variation of 1.5‰ among nine process corners.

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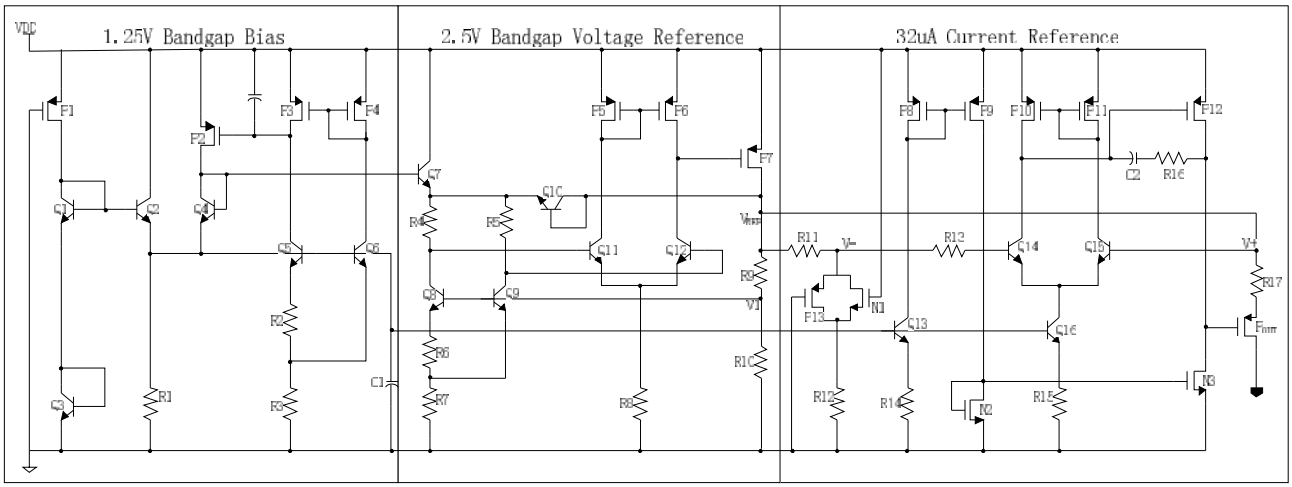

Figure 4. Proposed circuit archicture

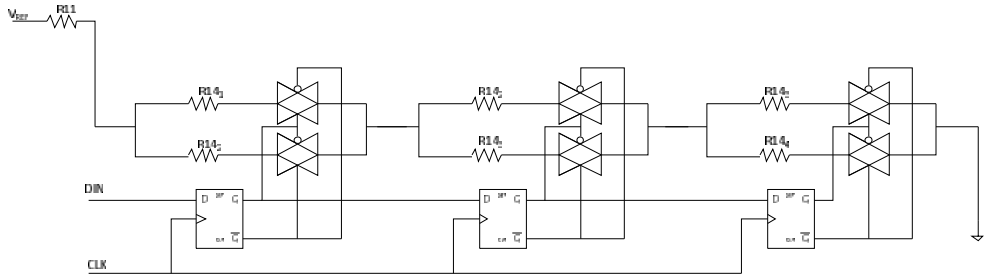

Figure 8. The trimming network

TABLE I. OUTPUT OF CERRENT REFERENCE AND BVR AT 9 CORNERS

other device corner	resistor corner	V_{REF} min	V_{REF} max	I_{OUT} min	I_{OUT} max	I_{OUT} precision	I_{OUT} TC
TT	TT	2.4988	2.5011	31.965	32.013	1.0‰	11.25
TT	MAX	2.4984	2.5006	31.969	32.029	0.9‰	15.00
TT	MIN	2.4982	2.5016	31.979	32.035	1.1‰	14.00
FF	TT	2.4968	2.5000	31.970	32.031	1.0‰	15.25
FF	MAX	2.4988	2.5012	31.963	32.020	1.1‰	14.25
FF	MIN	2.4984	2.5028	31.987	32.047	1.4‰	15.00
SS	TT	2.4984	2.5033	31.987	32.007	0.4‰	5.000
SS	MAX	2.5000	2.5047	31.998	32.019	0.6‰	5.250
SS	MIN	2.4978	2.5034	31.990	32.019	0.6‰	7.250