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High-precision transfer-printing and integration of vertically oriented semiconductor arrays for flexible device fabrication

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ABSTRACT

Flexible electronics utilizing single crystalline semiconductors typically require post-growth processes to assemble and incorporate the crystalline materials onto flexible substrates. Here we present a high-precision transfer-printing method for vertical arrays of single crystalline semiconductor materials with widely varying aspect ratios and densities enabling the assembly of arrays on flexible substrates in a vertical fashion. Complementary fabrication processes for integrating transferred arrays into flexible devices are also presented and characterized. Robust contacts to transferred silicon wire arrays are demonstrated and shown to be stable under flexing stress down to bending radii of 20 mm. The fabricated devices exhibit a reversible tactile response enabling silicon based, nonpiezoelectric, and flexible tactile sensors. The presented system leads the way towards high-throughput, manufacturable, and scalable fabrication of flexible devices.

High performance electronics on flexible substrates have been gaining attention from research communities due to the attractive properties of flexible substrates such as transparency and biocompatibility [1]. The potential for multilayer systems on flexible films enabling diverse functionality such as computing, sensing, imaging, energy harvesting/storage, lighting, display and communications along with the market for handheld and wearable consumer electronics, has also been a driver for research in this area [2]. The incorporation of such devices into existing applications, however, will require breakthroughs in nanoscale crystal growth with controlled size, reduced defect and impurity densities, and large mobility; an understanding of the fundamentals of the nano–micro–macro interface, organic–inorganic interface and

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thermomechanical deformation; and most importantly, an integrative manufacturing platform for high-speed, cost-effective, lightweight, and large area production of flexible electronic systems for conformal and deformable surfaces.

Flexible devices benefit greatly from the incorporation of inorganic single crystalline nano- and micro-scale semiconductor materials as they offer high mobilities and benefit from the expertise of the semiconductor industry while allowing for flexibility due to the material discontinuity and increased bending strength [3, 4]. Vertically oriented arrays of one-dimensional (1D) inorganic semiconductor nanowires (NWs) and microwires (MWs) have shown promise for many devices such as photoelectrochemical cells [5, 6], photoanodes and cathodes [7, 8], and thermoelectric devices [9, 10]. These devices would benefit from integration onto flexible substrates. However, crystalline semiconductor arrays generally require growth on crystalline mother substrates and high temperature processing, precluding the direct use of temperature sensitive flexible substrates. Therefore, processing and integration techniques subsequent to growth are required to fabricate devices which benefit fully from the combination of single crystalline semiconductor arrays and flexible substrates.

Many techniques for detaching NW and MW arrays from mother substrates and their aligned lateral reassembly onto substrates compliant with flexibility and processability have appeared in the literature with examples like contact printing [2, 11], solution processes [12, 13], and elastomeric stamp based transfer printing (TP) techniques such as "dry" TP [1, 14, 15]. Of these lateral techniques, dry TP processes are attractive for controllably assembling arrays onto flexible substrates as they are deterministic and have the required precision to maintain the ordered array architecture and uniform end-to-end registration [16], properties which are advantageous for the fabrication of small scale devices [17]. However, the compatibility of dry TP with vertically oriented arrays has not been demonstrated, an important consideration as vertical orientations offer longer optical absorption paths, as well as several design, processing, and scaling benefits [18].

Several methods for transfer printing of vertical arrays have been demonstrated including techniques utilizing steps such as polymer infiltration and mechanical separation of arrays [19–21]. Methods for direct TP of vertical arrays, akin to dry TP for lateral arrays, could potentially lead to wide adaptability. However, this approach requires high precision to overcome the challenge of maintaining the array orientation, planarity, and end-to-end registration without contact of the wire's lateral surface with the transfer substrate. Unlike TP of lateral arrays where stabilization is achieved by van der Waals forces facilitated by the large lateral contact area, vertical arrays will not stand directly on the surface of transfer substrates by making contact to the individual tips. However, placing a thin polymer layer on top of transfer substrates can allow for stabilization of the array tips, holding the array in its vertical orientation while aiding in separating the array from the mother substrate.

Previously, we reported on a TP method for vertical silicon (Si) MWs arrays where the arrays were embedded into polymer layers on transfer substrates [22, 23]. However, this technique was based on a manual transferring method and therefore it lacked precision and control which limited the method to arrays with low density and small areas. In particular, this method was limited to MWs with a maximum achievable transferable area of ~25 mm^2. Herein, a TP method is presented based on a high precision mechanical tooling system capable of accurate control over planarities, array displacements, and temperatures, significantly extending the scope of TP processes to meet all of the requirements for vertical arrays. Precision control allows for the vertical end-to-end registration to be maintained and is crucial to enable transfer of vertically oriented arrays with a wide range of aspect ratios, geometries, areas and densities. The successful TP of various vertical arrays is presented along with a complementary device fabrication scheme used to create flexible devices enabled by the transferred arrays. The system presents a way towards high-throughput, manufacturable, and scalable fabrication of flexible devices as it is based on an archetypical mechanical tooling system capable of facilitating large area TP of virtually any arbitrary semiconductor array.

The high precision vertical transfer printing (hpVTP) process consists of a controlled application of force in two consecutive steps. The process utilizes a thermoplastic polymer layer which can be controllably changed between a fluidic (viscoelastic) and solid (elastic) state by temperature changes to above or below the glass transition temperature (T_g), respectively. This allows arrays to be controllably embedded (embossed) into the polymer in the fluidic state and rigidly held in the solid state. Figure 1 shows a schematic representation of the hpVTP mechanism and the system that we built for this process. First, an arbitrary vertical array (Fig. 1(a)), which is attached to a mother substrate, is aligned above the transfer substrate (glass, metallic, or Si) onto which a polymer layer (poly(methyl methacrylate) (PMMA) Microchem 950PMMA) has been previously spin coated and heated above the T_g. The alignment is achieved by affixing the mother substrate, array side down, and the transfer substrate, polymer side up, to vacuum chucks on the vertical embossing tool (Fig. 1(b)). The array is then embedded into the polymer with a controlled depth (10 nm resolution piezo actuator) while the applied force is monitored by a load cell attached to the end of the piezo actuator. The applied pressure is obtained from the applied force by dividing by the array contact area. The embedding depth is recorded during this process as the overall displacement of the piezo actuator as it extends. The planarity is precisely controlled and the embossing process is automated and adjusted in real time via computer control systems. During this embedding process, the polymer ($T > T_g$) exhibits viscoelastic properties and therefore embedding is accomplished

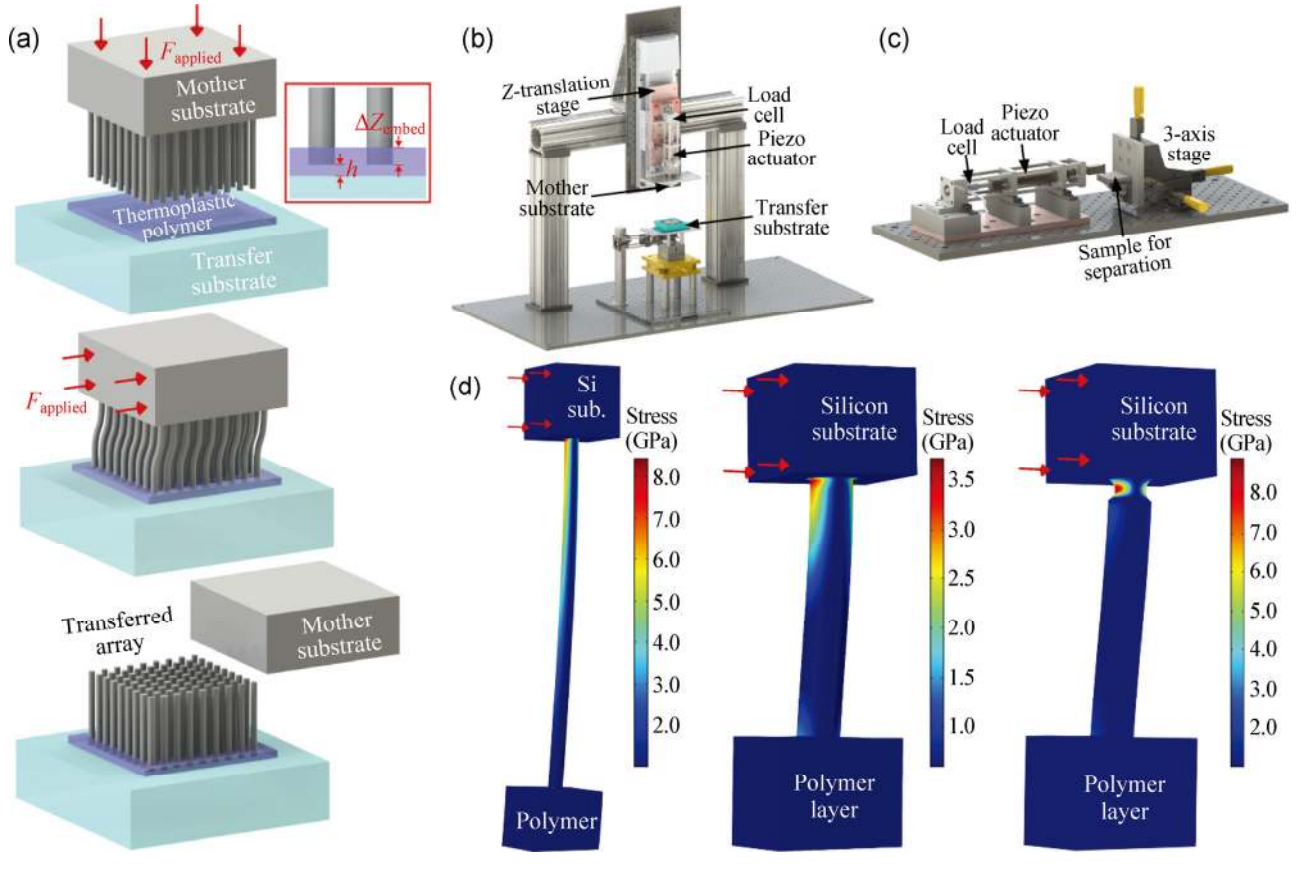

Figure 1 (a) Illustration of the high precision vertical transfer printing (hpVTP) process. An array of crystalline semiconductor nano or microstructures is embedded into a thermoplastic polymer (fluidic polymer, $T > T_g$) layer on a transfer substrate with (b) the vertical embossing tool. The array is then separated from the mother substrate using (c) the lateral separation tool (solid polymer, $T < T_g$). The mother substrate is then polished and reused for further processing. (d) Stress simulations elucidating the mechanics during lateral separation. The stress concentration is large enough to facilitate separation at the array root location.

by increasing displacement steps utilizing low stress (~0.1 MPa). Each step is held for a period of time longer than a few multiples of the polymer relaxation time to allow for viscous force relaxation due to thermal motion and redistribution of polymer chains [24]. Each step increases the vertical embedding displacement to a higher desired value as the polymer relaxes and the internal feedback mechanism of the tool measures the displacement and adjusts it to the desired value. This process allows for mechanical equilibrium to be reached so that the embedding depth can be accurately determined. Precision control over the embedding depth simultaneously controls the portion of the array that remains protruding from the polymer after transfer, parameters which are optimized for post transfer device fabrication steps. After embossing, the system is cooled below the T_g to solidify the polymer and bind the tips of the array onto the transfer substrate.

The next step involves applying a force, orthogonal to the embossing direction, utilizing the lateral separation tool (Fig. 1(c)). The transfer substrate is fixed during this step, but the mother substrate is displaced laterally while the vertical distance to the transfer substrate is maintained by affixing it to the tool's pressing surface. Here, the polymer is in a solidified state ($T < T_g$) exhibiting no stress relaxation allowing quasi-continuous force ramping by increasing lateral displacements (10 nm steps). The force gradually increases until failure occurs at the root location of the crystalline array and the stress is abruptly relaxed, consequently separating the array from the mother substrate and leaving it firmly attached to the transfer substrate. Due to the robust adhesion, mechanical stability, and slight stretchability of the PMMA, the polymer/NW composite immediately relaxes back to an unstressed state after failure, robustly maintaining the array integrity, spacing, and alignment.

An important aspect of the hpVTP process is the ability to separate the mother substrate from the array directly at the root. In order to elucidate the mechanics and determine if the process could achieve this goal, stress simulations were conducted using the COMSOL Multiphysics® solid mechanics simulation package, as depicted in Fig. 1(d). For each case, a lateral force was applied (red arrows) to a Si substrate which contained a protruding NW or MW facing downward and embedded into a polymer layer. The PMMA polymer layer has a fixed motion constraint on its lower surface, simulating the rigidly localized transfer substrate, while the Si substrate has a roller constraint on its top surface to allow for lateral displacement without rotational motion (see Electronic Supplementary Material (ESM) for simulation details). The Si NW–polymer interface is considered to have a perfect interface and the NW–PMMA interfacial shear strength is high enough so that this assumption is valid [22]. PMMA has roughly two orders of magnitude lower modulus than Si so it can stretch to allow for stress relaxation of the array tips while the array roots experience a high stress level. In the first diagram, representing a Si NW, the concentration at the root is large enough to facilitate separation as the maximum stress is a factor of two larger than the failure strength reported for Si microstructures [25], and >10% higher than that reported for vapor–liquid–solid (VLS) Si NWs (see ESM) [4]. For MWs the stress is also concentrated at the root as shown in the second diagram in Fig. 1(d). However, creating a notch at the root (as discussed below) further localizes the stress, as shown in the third diagram. For the MW without the notch, the maximum stress is roughly equal to reported failure strengths [25], while for the notched MW, the maximum stress is larger by a factor of two. The separation mechanics also determine the overall chip area which can be transferred by each application of the hpVTP process. For VLS Si NWs, a maximum transferrable area of ~6 in^2 is expected for the observed separation force requirements and array area densities (see ESM).

Results from the hpVTP process have been obtained for many different material types and geometries. Figure 2 shows results obtained for two types of Si NWs. For the case of NWs grown via a VLS process, the array prior to transfer can be seen in Fig. 2(a). VLS NWs were grown using Au thin film catalysts on (111) Si wafers in a FirstNano EasyTube 3000 cold wall CVD reactor (SiH_4 precursor, 680 °C). Figure 2(b) shows a large area scanning electron microscopy (SEM) image of the array embedded into the polymer layer after the hpVTP process where the initial parallel alignment, uniform end registry, and array pitch is

maintained. This can also be seen more clearly in Figs. 2(c) and 2(d) which show higher magnification images of the transferred VLS NWs. A small portion of the NWs are misaligned during growth which leads to some deviations from perfect parallel alignment and spacing after transferring. This deviation also leads to a small portion of the NW tips being nonplanarized and therefore not embedded properly during the embedding step. These NWs are not transferred and therefore lower the overall transfer yield by roughly 5%. The root ends of the VLS NWs are slightly wider than the rest of the NW and the wider end can be seen as the exposed top end of the NWs after transfer in Fig. 1(d), indicating that the NWs were separated directly at the root location. A transferred area of ~1 in^2 is typically achieved for each application of the hpVTP process with VLS NWs.

Figure 2(e) shows electroless NWs prior to the hpVTP process. In this case, the NWs are an extension of mother substrate with robust crystal continuity. Electroless NWs were fabricated from unpatterned (100) Si wafers by exposure to 0.02 M $AgNO_3$/5 M HF solution. These arrays also have a larger areal density than the VLS NWs, but despite these properties the hpVTP process produces good results as presented in Figs. 2(f) and 2(g).

The hpVTP process works equally well for low aspect ratio arrays. Figure 3 shows the results for 1D Si microwires (MWs) and quasi-2D Si microwalls (MWAs). Figures 3(a) and 3(b) show the MWs on the mother substrate before transferring with a slightly notched root end, where extra material was etched away (overetched). These MWs were fabricated by deep reactive ion etching (DRIE) (Bosch process) after photolithographical patterning on (100) n-type Si wafers ($n = 10^{18}$ cm^{-3}). The overetching process was carried out by extending the last etching step. Figure 3(c) shows the separation point at the root location after transfer. Figures 3(d)–3(g) show transferred MWs embedded in the polymer from various angles where the MW array–polymer composite can be seen to be highly flexible if removed from the transfer substrate (Figs. 3(d) and 3(e)). Similarly, for MWA arrays, the array prior to and after transfer can be seen in Figs. 3(h) and 3(i), respectively. MWA arrays were prepared by KOH etching from SiN_x patterned (110) Si wafers. The root location of the MWAs has a continuous notch caused by overetching which facilitated TP of the walls which had lengths of hundreds of μm. The overetching was done by oxidation, RIE to remove oxide between the walls and subsequent etching of the exposed area in $HF:HNO_3:CH_3COOH$ solution (2:15:5). The transferred MWA arrays embedded in the transfer polymer are depicted in Figs. 3(j) and 3(k). For MWA arrays, an extra consideration for the wall orientation must be observed as the separation force

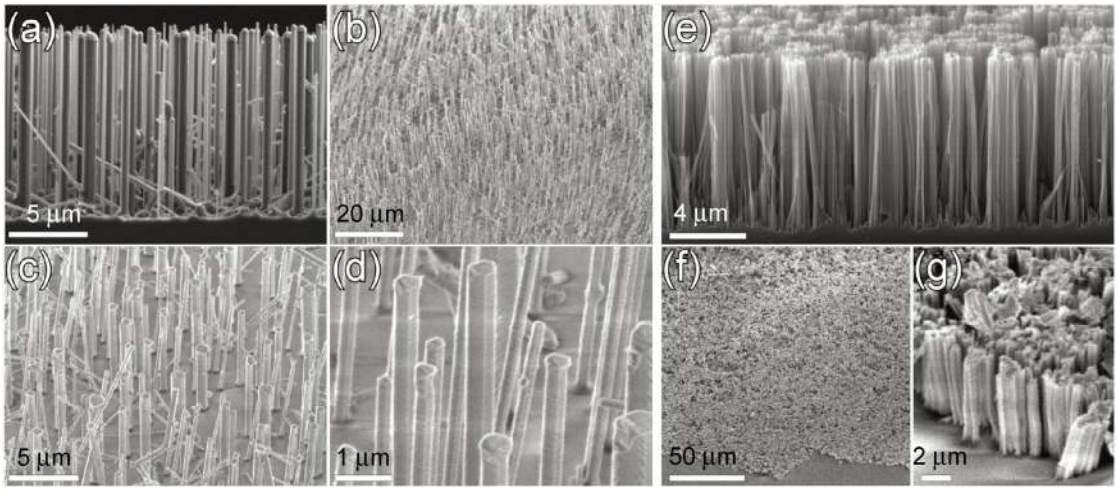

Figure 2 SEM micrographs of the high precision vertical transfer printing (hpVTP) process for nanowire (NW) arrays. (a) VLS Si NWs on the mother substrate prior to the hpVTP process. (b)–(d) Large area and high magnification images of transferred VLS NWs embedded in polymer with maintained initial array properties. (e) Electroless Si NWs on the mother substrate prior to transfer. (f) and (g) Large area and high magnification images of transferred electroless NWs.

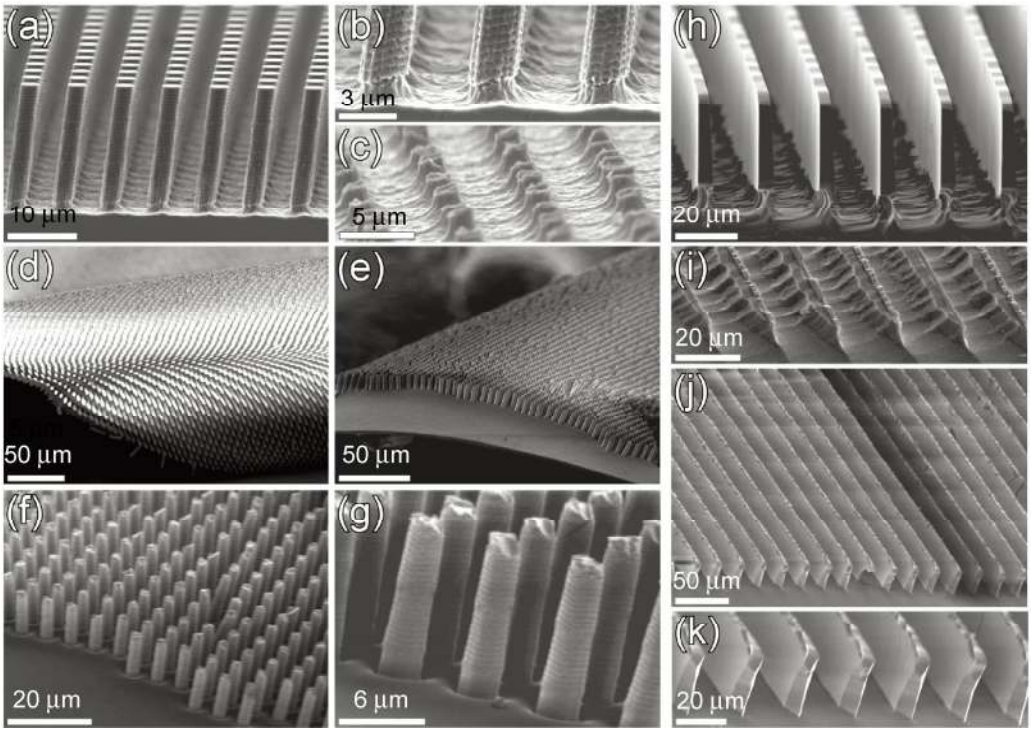

Figure 3 High precision vertical transfer printing (hpVTP) of microwires (MWs) and microwalls (MWAs). (a) Si MW arrays as etched on the mother substrate. (b) and (c) Root location of the MWs on the mother substrate before and after transfer printing, respectively. (d)–(g) Large area and high magnification images of a transferred MW array embedded in polymer. (h) Si MWA arrays as etched with a notch (overetch) at the root location. (i) MWA root location after transfer. (j) and (k) Large area MWA array transferred into polymer, low and high magnification images, respectively.

must be perpendicular (normal) to the vertical face of the MWAs. For both MWs and MWAs, the top exposed end of the transferred arrays can be seen to have geometry consistent with the notched end. For all of the demonstrated array types, the initial array pitch, alignment and end-to-end registry are robustly maintained throughout the hpVTP process, which is helpful for any subsequent fabrication and integration steps.

A wide variety of techniques can be used to create devices from the transferred arrays following the general hpVTP method. The transfer polymer layer was selected for its selective solubility in acetone, allowing it to act as a sacrificial layer. Figure 4(a) outlines an example of a device fabrication method. Top and bottom ensemble contacts are required for an ideal vertical device, so an insulating layer is needed to electrically isolate each end of the array. The insulating layer additionally serves as flexible encapsulating support for the array. Therefore, the first step was to spin coat a different insulating polymer (stable in acetone) over the array. Either polyurethane, prepared by dissolving commercial beads in dimethylformamide, or polydimethylsiloxane (PDMS) (Dow Corning Sylgard® 184 silicone elastomer 1:10) mixed with hexane (60:40 hexane:PDMS wt.%), was used for this step. These insulating layers were spin coated at high speeds (~3,000 rpm) onto the transferred arrays. The first contact was then deposited after planarizing the array–polymer top surface by removing any remaining polymer and the native oxide using reactive ion etching (RIE) and dilute HF, respectively. The contacts (aluminum (Al), 0.3–1 μm) were deposited by shadow mask in a CHA Industries E-beam evaporator or Kurt J. Lesker Lab 18 RF/DC Sputtering System. At this point, the array was sufficiently stabilized to be placed into an acetone bath where the transfer polymer was dissolved, lifting off the encapsulated array. The device was then adhered to a thin copper film (contact down) using silver epoxy

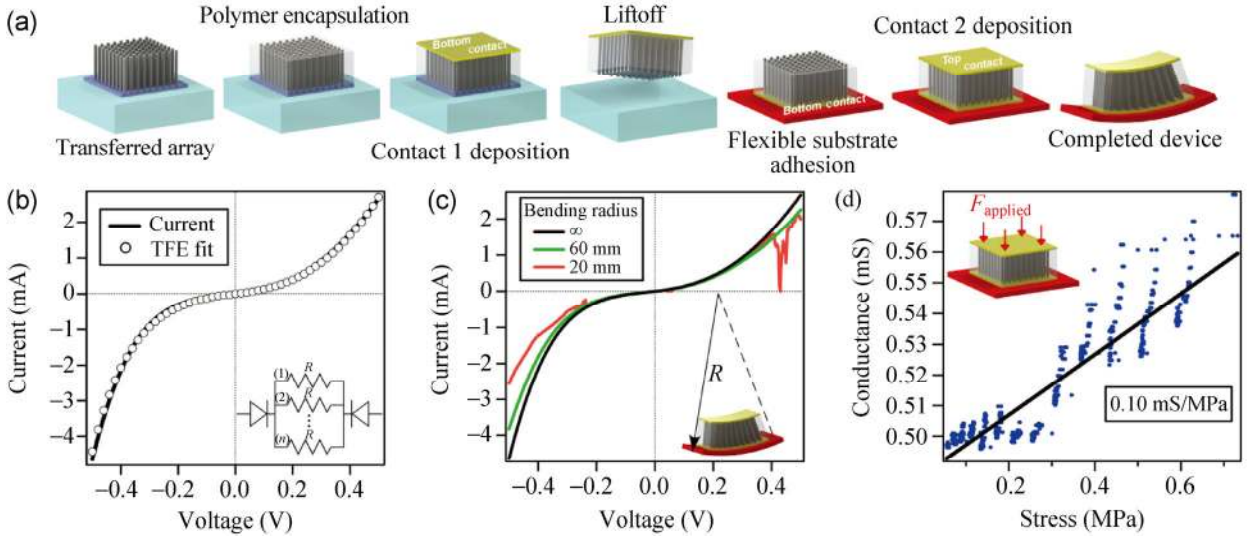

Figure 4 (a) Fabrication scheme for flexible devices following transfer printing of vertical arrays. (b) *I*–*V* curve for a flexible Si wire device showing symmetric and non-linear characteristics. A fit to the data is also shown based on a metal–semiconductor–metal back-to-back Schottky model with a thermionic-field emission (TFE) current mechanism (circuit model in inset). (c) Electrical characteristics for flexible devices at various bending radii. (d) Tactile characteristics of flexible devices, showing a reversible increase in conductivity with applied vertical stress.

and sealed to a flexible polyimide substrate using further insulating polymer before deposition of the second (top) contact to complete the flexible device.

Flexible Si MW array devices were prepared following the outlined procedure with n-type Si (10^{18} cm^{-3}) and Al (1 μm) top and bottom contacts. Characterization results for these devices are shown in Figs. 4(b)–4(d). The *I*–*V* characteristics were nonlinear and symmetrical confirming the ability of the hpVTP process and fabrication steps to make robust contact to both sides of the array. To help understand the *I*–*V* characteristics, a metal–semiconductor–metal system with back-to-back Schottky contacts was used as a circuit model (Fig. 4(b) inset). The current densities and voltage drops at the contacts were calculated by solving a set of nonlinear equations assuming a thermionic-field emission (TFE) current mechanism (see ESM for details) [26]. The nonlinear *I*–*V* curve and the fit to the data are presented in Fig. 4(b) where the goodness of the fit confirms the TFE mechanism, which is expected for the doping level, temperature, and metal–semiconductor interfaces present [26]. While these devices exhibited nonlinear characteristics, we expect that future devices could be produced with low-resistance ohmic contacts by depositing metal layers onto the tips of the array and annealing the interface prior to the hpVTP process, as this procedure can reduce the unintentional barrier at the metal–semiconductor interface [26, 27].

The mechanical properties of the fabricated devices allowed testing of the electrical characteristics of the device under flexing stress. Little change to the *I*–*V* curve was observed down to bending radii of roughly 20 mm, beyond which breakdown was noticed. The breakdown most likely occurred at the MW–metal interface, as the strain at this interface increases with decreasing bending radius and the devices exhibited repeated flexing cyclability while above the 20 mm limit without noticeable failure [28]. Additionally, the bending strength of the encapsulation polymer and Si MWs far exceed the stresses experienced for this radius (see ESM).

The devices also exhibited a reversible increase in conductivity with applied vertical stress (Fig. 4(d)) with a reproducible sensitivity $S = dG/dP$ of 0.10 mS/MPa, over tens of cycles. These characteristics are suitable for tactile sensor applications as the sensitivity is within one order of magnitude of demonstrated piezoelectric NW tactile devices [29]. While it is difficult to definitively determine the mechanism governing

the tactile response, the most likely explanation is based on the nature of the MW–metal contact since piezoresistive effects in Si are too small to account for the observed change [30]. As seen in Fig. 3(f), a small portion (~5%–10%) of the transferred MWs have a slanted top surface slightly lower than the remaining MWs, due to a crystallographic slip plane which exists at the Si (111) plane, allowing for slip in the [110] direction [31]. These MWs do not planarize effectively during the RIE steps and will have a very thin polymer interfacial layer mostly covering the tip. While the majority of the array with conformal contact would not be affected by applied stress, tunneling current through the slanted MWs could reversibly change as the interfacial layer is compressed.

In conclusion, we have demonstrated a general method for transfer printing of arbitrary arrays of 1D and 2D crystalline semiconductors that maintains the initial array properties and could be adapted to arrays of virtually any crystalline semiconductor material. We also introduced a complementary fabrication scheme for integrating transferred arrays into flexible devices which demonstrated the ability to make robust and flexible contacts to transferred arrays. The fabricated devices also exhibited pressure sensitive conductivity making them useful as low cost tactile sensors. Since devices fabricated with the hpVTP method are limited mainly by the initial array properties, a broad range of flexible and functional electronic and optoelectronic devices can be realized with this method. We expect that this fabrication method for substrate-less devices can be scaled up and adapted to create universal platforms for heterogeneous material integration and for the fabrication of large area flexible solar cells, sensors, conformable electronic devices, and many others in the "macroelectronics" regime.

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