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High pulsed current density β-Ga_2O_3 MOSFETs verified by an analytical model corrected for interface charge

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We report on Sn-doped β-Ga_2O_3 MOSFETs grown by molecular beam epitaxy with as-grown carrier concentrations from 0.7×10^{18} to $1.6 \times 10^{18}\,cm^{-3}$ and a fixed channel thickness of 200 nm. A pulsed current density of >450 mA/mm was achieved on the sample with the lowest sheet resistance and a gate length of 2 μm. Our results are explained using a simple analytical model with a measured gate voltage correction factor based on interface charges that accurately predict the electrical performance for all doping variations. [http://dx.doi.org/10.1063/1.4979789]

β-Ga_2O_3 has recently emerged as a promising semiconductor for high-power, high-voltage device applications because of its ultra-wide bandgap of ~4.8 eV and the corresponding expected critical breakdown field of ~8 MV/cm.[1,2] β-Ga_2O_3 also has the advantage of a native substrate that can be synthesized in bulk by melt growth techniques with Sn and compensating Fe and Mg impurity doping.[3–5] Further, homoepitaxial channel conductivity for field effect transistor (FET) device applications has been demonstrated by Sn and Si doping using both molecular beam epitaxy (MBE) and metalorganic vapour phase epitaxy (MOVPE).[6,7] Disadvantages include low thermal conductivity[8] and high hole effective mass.[9] Depletion-mode metal-semiconductor FETs and Si-implanted metal-oxide-semiconductor FETs (MOSFETs) have been demonstrated with current densities exceeding 25 and 40 mA/mm, respectively.[2,10] Further, a depletion-mode MOSFET exceeding 750 V with a field plate and an enhancement-mode fin-array MOSFET up to 600 V were recently reported.[11,12] Finally, Green *et al* measured a lateral gate-drain critical field strength >3.8 MV/cm on a β-Ga_2O_3 MOSFET surpassing bulk GaN and SiC theoretical limits.[13]

While high blocking voltages have been achieved, insight into the high-current density potential of Ga_2O_3 MOSFETs has been largely unexplored. In this letter, we compare n-type β-Ga_2O_3 MOSFETs with various Sn channel concentrations and accurately predict the I-V performance using a simple electrostatic model that includes the gate oxide-gallium oxide interface charge voltage. The model which does not include self-heating effects or gate and drain dispersion is validated by isothermal pulsed I-V measurements with quiescent voltages and sweep parameters chosen to minimize dispersion effects. Agreement between measured and theoretical values for knee voltage (V_{knee}) and saturated drain current (IDSS) over a wide range of Sn doping concentrations is verified. A MOSFET with the highest channel charge-mobility (N_d-μ) product achieved a pulsed current density of 478 mA/mm at a gate voltage of +4 V, much higher than previously reported DC values of 60 mA/mm for MOSFETs on homoepitaxial materials[13] and 90 mA/mm for ion-implanted MOSFETs,[11] and second only to nanomembrane devices which achieved 610 mA/mm at a high forward gate bias of +120 V.[14] This indicates the performance of the material system if self-heating due to the low thermal conductivity can be mitigated by cooling techniques or less thermally stressful applications. MOSFETs were fabricated on single crystal β-Ga_2O_3 grown by MBE on commercially available Fe-doped (010) semi-insulating substrates.[6] Sn-doping was performed during the epitaxial growth, and carrier concentrations from 0.7×10^{18} to $1.6 \times 10^{18}\,cm^{-3}$ were measured after growth using electrochemical capacitance-voltage (C-V) measurements. Table I includes these values as N_d *As Grown* and also summarizes the measured data for all the samples as described further below.

A schematic process flow for the MOSFET is shown in Figure 1. Mesa isolation of the active channel was conducted using a BCl_3 inductively coupled plasma (ICP) dry etch and verified by profilometer measurements. Source and drain ohmic contacts were formed using an evaporated Ti/Al/Ni/Au metal stack and annealed for 60 sec in a nitrogen ambient at 470 °C.[10] All the contacts were ohmic and the contact resistance (R_C) ranged from 10.7 to 80.0 ohm-mm as measured by the circular transfer length method (TLM)[15] and shown in Table I. A 20 nm thick gate dielectric layer of HfO_2 was deposited by plasma-enhanced atomic layer deposition (ALD) at 250 °C without any surface pre-treatment. The gate dielectric was selectively removed in the ohmic pad regions by CF_4 reactive ion etching (RIE). Interconnects and 2-μm long gates were patterned and deposited simultaneously using a 20/480 nm Ti/Au metal stack.

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TABLE I. β-Ga_2O_3 MOSFET sample summary.

N_d As Grown[a]	V_{knee}[c]	IDSS[d]	V_{off}[c]	N_d post process[a]	μ_{eff}[b]	$IDSS_{mod}$[d]	$IDSS_{mod}$ ΔV_G[d]	$V_{knee\ mod}$ ΔV_G[c]	R_C[e]
0.70×10^{18}	13.0	19	−9.6	2.50×10^{17}	74.5	36.5	20.5	12.9	80.0
1.00×10^{18}	33.9	111	−18.8	4.84×10^{17}	58.3	136.1	111.2	35.8	32.0
1.30×10^{18}	53.7	235	−24.5	6.29×10^{17}	52.4	258.8	235.4	54.7	14.0
1.60×10^{18}	69.6	381	−30.8	7.88×10^{17}	51.0	404.6	381.4	71.0	10.7

[a]cm^{-3}.
[b]$cm^2/V \cdot s$.
[c]V.
[d]mA/mm.
[e]Ohm-mm.

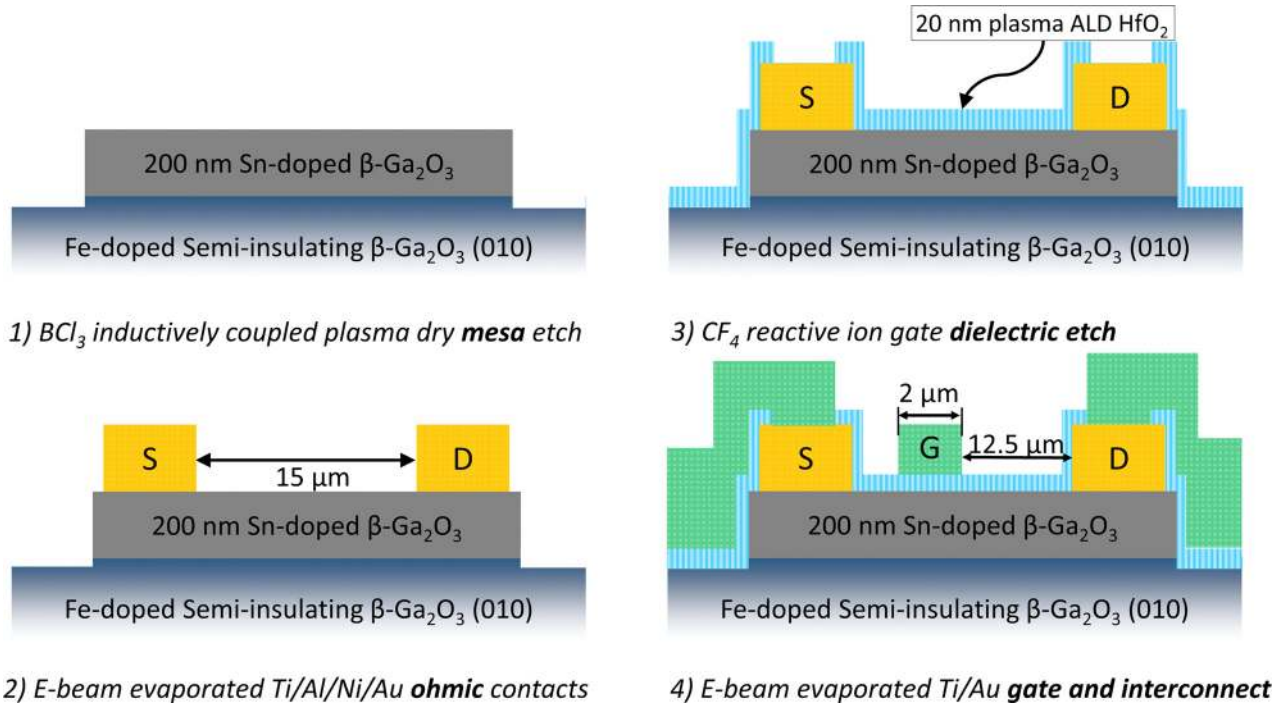

FIG. 1. β-Ga_2O_3 MOSFET process flow.

All device electrical testing was conducted on self-isolating ring-type FETs with a gate-source spacing of 0.5 μm and a total source-drain spacing of 15 μm (12.5 μm G-D spacing). The total gate width was 422 μm. All the structures were fabricated on a single 10×15 mm sample for each doping level. Figure 2 shows a static log transfer curve (I_D -V_{GS}) for the highest current density MOSFET with good transistor operation including a high on/off ratio of $>10^8$ which was typical of all the devices measured regardless of the carrier concentration. Sister devices routinely achieved breakdown voltages >400 V for a 10.5 μm gate-drain spacing and were limited by the failure of the gate dielectric.

Pulsed-IV measurements were conducted on MOSFET devices using an AMCAD system to provide a pulsed drain voltage and a Keysight E5270a to provide static gate bias. The pulse width was 200 ns with a quiescent drain bias of 0 V and a low duty-cycle of 0.001 percent to minimize thermal effects. The pulsed measurement used represents an ideal environment where gate and drain dispersion and self-heating effects can be ignored to evaluate the β-Ga_2O_3 MOSFET under ideal conditions and assess the material system. Figure 3 shows a pulsed-

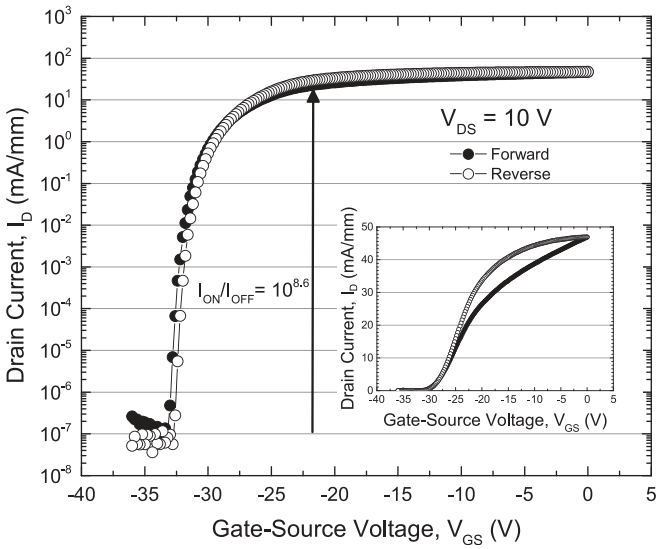

FIG. 2. DC log transfer curve for a high current density β-Ga_2O_3 MOSFET showing good transistor operation. The inset shows a linear plot of the transfer curve showing significant gate dispersion between forward and reverse curves.

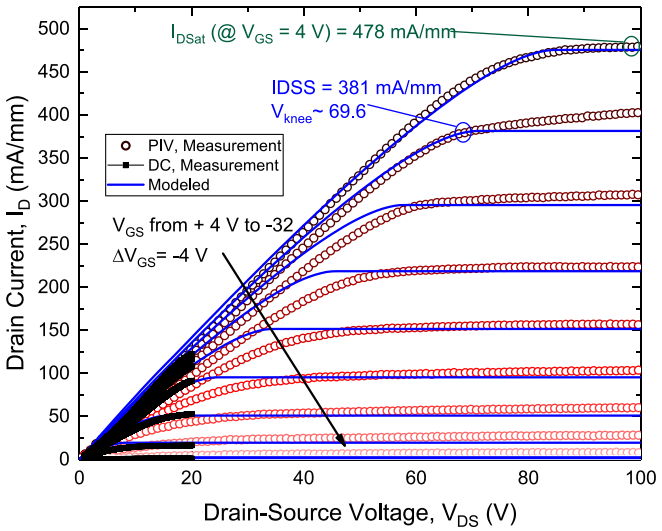

FIG. 3. Pulsed family of drain current curves (symbols) for a high current density β-Ga_2O_3 MOSFET. The maximum current density measured was 478 mA/mm. The device operates very close to theoretical values shown using an analytical electrostatic model (blue lines). Gate dispersion was avoided by measuring from the on to off states. A static measurement limited to $V_{DS} = 20$ V and $V_{GS} = 0$ V is also shown with a maximum current of 118 mA/mm @ $V_{DS} = 20$ V and $V_{GS} = 0$ V, which agrees with the pulsed measurement (120 mA/mm @ $V_{DS} = 20$ V and $V_{GS} = 0$ V) and the model.

IV and static family of curves (I_D -V_{DS}) for the highest current density device. We extracted the knee voltage, V_{knee}, and the saturated drain current at $V_G = 0$ V, IDSS, from the inflection point in the pulsed-IV family of curves as shown in Figure 3. V_{knee} and *IDSS* are recorded for all the samples in Table I.

Capacitance-voltage (C-V) measurements were performed on lateral C-V structures with diameters of 75, 100, and 125 μm using a B1505a equipped with a multi-frequency capacitance measurement unit and needle probes. A representative C-V curve for each sample is presented in Figure 4. Measurements were performed at frequencies that provided smooth C-V characteristics (100 kHz or 1 MHz), and

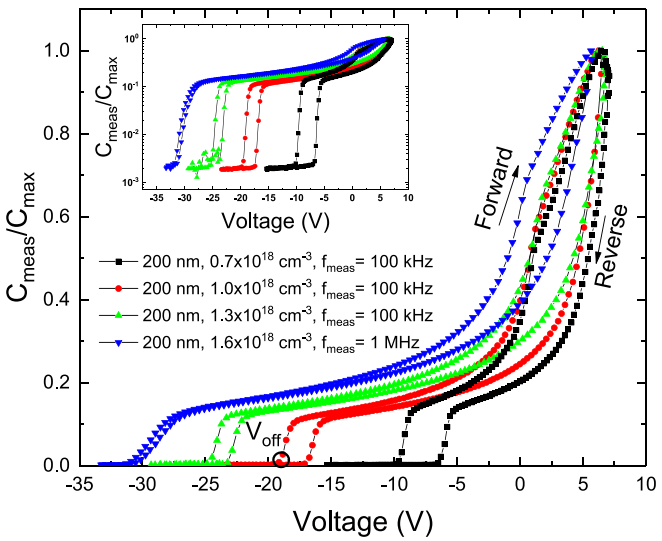

FIG. 4. Normalized capacitance vs. voltage, C-V, for MOS structures on MBE grown β-Ga_2O_3 layers with varying target doping and an active layer thickness of 200 nm. The inset shows log scale plots of the same. The inflection point used to determine V_{off} is shown for one device. All the samples had HfO_2 gate dielectric.

measurement differences at frequencies between 1 kHz and 1 MHz were confirmed to have a negligible effect on the experimental results. We used the C-V measurement data to determine the off-state gate voltage, V_{off}, from the inflection point where the C-V curve (and therefore the available drift carriers) is minimized. This inflection point is shown for one device in Figure 4, and V_{off} is recorded for all the samples in Table I. The measured V_{off} is the gate voltage required to deplete the entire active layer:

$$V_{off} = V_{FB} - dqN_d\left(\frac{d}{2\epsilon_s\epsilon_0} + \frac{1}{C_{ox}}\right), \quad (1)$$

where V_{FB} is the flat-band voltage, d is the active layer thickness, q is the electron charge, N_d is the average active ionized dopant concentration in the active layer, $\epsilon_s\epsilon_0$ is the static dielectric constant of β-Ga_2O_3, and $C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$ is the oxide capacitance per unit area.

Obtaining exact values for V_{FB} and N_d from measurements is difficult because of interface trap charges at the Ga_2O_3-HfO_2 interface and non-uniform carrier concentration in the active layer after fabrication as shown in Fig. 5. To simplify our calculations, we use the measured value of V_{off} from C-V data, substitute the ideal value of the flatband voltage:

$$V_{FB} = \Phi_M - \Phi_S = \Phi_M - \left(\chi_S + \phi_t \ln\left(\frac{N_C}{N_d}\right)\right), \quad (2)$$

where Φ_x is the work function of the metal or semiconductor, ϕ_t is the thermal voltage, χ_S is the electron affinity of Ga_2O_3, and N_C is the effective density of states in the conduction band, and then solve for N_d iteratively starting from the maximum value of $V_{FB} = \Phi_M - \chi_S$ in (1). The result obtained is an average of N_d through the active layer thickness of each sample, and it is recorded in Table I as N_d *Post Process*. The difference between the carrier concentration before and after the fabrication results from the depletion of carriers at the epitaxy-substrate interface during processing and surface effects at the gate oxide-gallium oxide interface. The average value extracted from V_{off} agrees reasonably with average values extracted from post-process C-V profiling (Figure 5); however, C-V profiling is unreliable near the gate oxide-gallium oxide interface.

To verify the MOSFET current density, we used simple electrostatic model equations for the depletion region. We first acknowledge that the β-Ga_2O_3 MOSFET never creates a conducting inversion layer. Then, we started with the basic equation for the drain current[16]

$$I_D = -QWv = -QW\mu E(y) = -QW\mu\frac{dV}{dy}, \quad (3)$$

where v is the carrier velocity, W is the gate width, E(y) is the lateral electric field at a point under the gate (y is the direction along the gate length), V is the potential at a point along the channel, and μ is the average carrier mobility. Then, assuming that the total channel charge per unit area, Q, is equal to the charge in the un-depleted portion of the channel and using the depletion approximation where

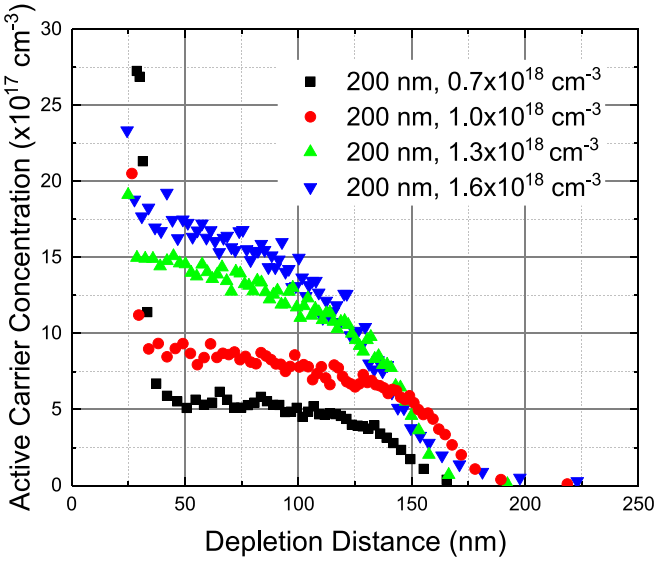

FIG. 5. Depletion distance dependent carrier concentration through the channel thickness for β-Ga_2O_3 homoepitaxial layers after MOSFET fabrication extracted from capacitance vs. voltage measurements using the slope of $1/C^2$-V to extract carrier concentration and a depletion and gate oxide capacitor in series to extract the distance from the gate oxide-gallium oxide interface. The result shows the difficulty in characterizing the gate oxide-gallium oxide interface (near 0 nm) and the epi-substrate interface (near 200 nm) using C-V profiling after fabrication.

$$x_{dep}(y) = \sqrt{\frac{2\epsilon_s\epsilon_0\Psi_s(y)}{qN_d}} \tag{4}$$

is the depletion distance and

$$\Psi_s(y) = V_{FB} - V_G + V(y) - V_{ox} \tag{5}$$

is the surface potential, we can integrate (3) from source to drain to obtain

$$I_D = I_o\left\{V_{DS}\left(d + \frac{\epsilon_s\epsilon_0}{C_{ox}}\right) + \sqrt{\frac{8\epsilon_s\epsilon_0}{9qN_d}}[V_o]\right\}, \tag{6}$$

where

$$I_o = \frac{qN_d\mu W}{L} \tag{7}$$

$$V_o = (A^2 - V_{GS} + V_{FB})^{3/2} - (A^2 - V_{GS} + V_{FB} + V_{DS})^{3/2}, \tag{8}$$

$A = \frac{\sqrt{2\epsilon_s\epsilon_0 qN_d}}{2C_{ox}}$, and V_{ox} is the voltage drop across the gate oxide. Equation (6) is valid in the depletion region only ($V_{off} < V_{GS} < V_{FB}$). We also modeled the effect of access resistance in the un-gated regions at the source and drain by implementing (6) in VerilogA in series with source and drain access resistors in the TINA circuit simulator.[17,18] Each access resistor was the sum of the measured R_C and the resistance for the ungated region based on R_{SH} and lateral device geometry (Figure 1).

The measured value of R_{SH} was also used with N_d calculated above to determine the effective mobility from the N_d-μ product. This mobility is included in Table I as μ_{eff} and agrees with the expected value from sister epitaxial growth. Finally, N_d, V_{FB}, and μ_{eff} are used in (6) to estimate the drain current under isothermal, ideal-interface-state conditions. Additional parameters used in the model are shown in Table II. The modeled value of IDSS using (6) is included in Table I as $IDSS_{mod}$.

TABLE II. Model values.

Parameter	Value
ϵ_s	10.0 Ref. 19
ϵ_{ox}	22.3 meas[a]
N_C	3.72×10^{18} cm^{-3} Ref. 20
Φ_M	4.33 eV Ref. 21
χ_S	4.0 eV Ref. 20

[a]Measured on MIM caps.

While our devices operate close to theoretical values under pulsed conditions, the drain current is still reduced by surface potential dependent negative charges at the gate oxide-gallium oxide interface[22] that effectively reduce the gate voltage applied by:[16]

$$\Delta V_G = \frac{-\Delta Q_{it}(V_G)}{C_G(V_G)}, \tag{9}$$

where $\Delta Q_{it}(V_G)$ is the interface charge difference between a device with filled and empty gate oxide-gallium oxide interface traps and C_G (V_G) is the total capacitance seen by the gate at a given gate voltage. In (9), we used the fact that the surface potential in (5) depends only on the gate voltage to replace Ψ_S with V_G. Based on the assumption that the time constant of traps is slower than the AC signal, and that interface traps are filled and empty for reverse and forward C-V sweeps, respectively, we calculate ΔV_G from the charge difference between the two curves in Figure 4 and the measured C_G at every point. We then replace V_{GS} with V_{GS}-ΔV_G in (6) to obtain the values for $IDSS_{mod}$ ΔV_G and $V_{knee\ mod}$ ΔV_G in Table I. We also include the accumulation mode by solving (6) with $V_{GS} = V_{FB}$ and adding an accumulation current:

$$I_{Dacc} = \mu C_{ox} V_{DS}\frac{W}{L}(V_{GS} - \Delta V_G - V_{FB}). \tag{10}$$

In doing so, we note that effects of the normal field on μ_{eff} have not been evaluated, and further investigation is required. In our case, where the normal field is very small, however, this addition to our model accurately predicts the I-V curve for $V_G = +4$ V. The result is shown in Figure 3 for our highest current density device. Similar agreement was observed for all but the lowest doped samples. As the doping level was decreased, the assumption that V_{off} is not significantly affected by interface trapped charges breaks down, and (1) using the ideal value of V_{FB} miscalculates N_d. In other words, as the doping concentration (or active layer thickness) is reduced, the magnitude of V_{off} (Ψ_S) is not sufficient to drive out negative interface trapped charges, and ΔV_G affects not only (6) but also (1). N_d calculated from (1) becomes dependent on V_G and transfer characteristics of the analytical model become inaccurate without additional advanced measurement techniques. With thin or lightly doped devices, the interface charge effect on ΔV_G and V_{FB} is significant. In fact, thin enhancement-mode devices have been reported[14] with $V_{off} > +75$ V exceeding the band-gap-

electron-affinity sum for β-Ga_2O_3 and indicating significant thickness of the gate oxide-gallium oxide interface trap layer. In these difficult cases, Hall measurements can be used to determine μ_{eff}, but techniques must be developed to overcome anomalies at the gate oxide-gallium oxide interface to accurately determine N_d and V_{FB}.

In conclusion, we have shown the measured and analytically modeled effects on device performance as a function of Sn doping concentration. A μ_{eff} of $> 50\ \frac{cm^2}{V \cdot S}$ was maintained for a device with $N_d = 7.8 \times 10^{17}\ cm^{-3}$, resulting in record-high pulsed current density for homoepitaxially grown β-Ga_2O_3 MOSFETs. The agreement between our simple MOSFET model with a gate-charge correction and the measured data highlights the importance of doping levels and interface optimization for future β-Ga_2O_3 MOSFET designs.

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