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High quality crystalline silicon surface passivation by combined intrinsic and n-type hydrogenated amorphous silicon

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We investigate the influence of thermal annealing on the passivation quality of crystalline silicon (c-Si) surfaces by intrinsic and n-type hydrogenated amorphous silicon (a-Si:H) films. For temperatures up to 255 °C, we find an increase in surface passivation quality, corresponding to a decreased dangling bond density. Due to the combined chemical and field effect passivation of the intrinsic/n-type a-Si:H layer stack, we obtained minority carrier lifetimes with a value as high as 13.3 ms at an injection level of 10^{15} cm^{-3}. For higher annealing temperatures, a decreased passivation quality is observed, which is attributed to hydrogen effusion. © *2011 American Institute of Physics*. [doi:10.1063/1.3662404]

Silicon heterojunction (SHJ) solar cells, consisting of hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si), form a potentially inexpensive alternative to standard p-n homojunction c-Si solar cells.[1–4] In homojunction c-Si cells, the p-n junction is formed by the thermal diffusion of dopants, for which temperatures around 900 °C are required. In case of a-Si:H/c-Si based heterojunction solar cell processing, temperatures below 200 °C are used, as the p-n junction is formed by depositing a thin doped a-Si:H layer on a c-Si wafer. This lower temperature processing (1) decreases the thermal budget of the production process, (2) limits thermal degradation of the c-Si, and (3) enables the use of thinner wafers ($<100 \mu$m), avoiding warpage issues associated with traditional high temperature processing.

Surface passivation of c-Si is a key requirement in optimizing the performance of SHJ solar cells. The preparation of SHJ solar cells involves the deposition of a passivating thin intrinsic a-Si:H film before depositing the doped emitter layer on the front side and the back surface field (BSF) layer on the rear side. This way, the open circuit voltage (V_{OC}) of these structures can be increased to values exceeding 700 mV.[2,3] Sanyo[1] has introduced this concept in 1992 and, due to its excellent results, inspired many other groups worldwide to focus on this concept.

The passivating properties of intrinsic a-Si:H have been widely studied,[5–8] and excellent results have been obtained by various laboratories using different deposition techniques. In SHJ cells, however, the influence of the doped layers on the quality of passivation is also very crucial. For the BSF structure, a combined layer stack consisting of intrinsic and n-type a-Si:H is used for n-type c-Si wafers. The role of the intrinsic film is to obtain a low defect density at the a-Si:H/c-Si interface (chemical passivation), whereas the role of the n-type film is to repel minority charge carriers from the interface, thereby further reducing recombination losses. This latter process is generally referred to as field effect passivation.

In this letter, we study the surface passivation of layer stacks, consisting of a thin intrinsic a-Si:H layer (thickness $\sim$5 nm), and an n-type a-Si:H layer (thickness $\sim$20 nm) as used in SHJ solar cells. Such a layer stack can be expected to lead to excellent surface passivation of c-Si, as it leads to combined chemical and field effect surface passivation. To this purpose, we deposit this layer stack on both sides of an n-type c-Si wafer and measure the injection level dependent minority carrier lifetime after annealing at different temperatures. Subsequently, these minority carrier effective lifetime data are fitted to a recombination model to identify the influence of the dangling bond density and the surface charge density at the a-Si:H/c-Si interface on the passivation quality.

We use $\sim$275 μm thick phosphorous doped n-type $\langle 111 \rangle$ oriented double-side polished (DSP) float zone (FZ) c-Si wafers ($\rho \sim$2.5–3 Ω cm). Prior to a-Si:H deposition, the wafers are dipped in hydrofluoric acid (HF) for 3 min (1% diluted in H$_2$O) to make them hydrophobic. The a-Si:H layers are made by rf PECVD (plasma enhanced chemical vapor deposition) at 13.56 MHz in a high vacuum multichamber system, called Process Equipment for Advanced Silicon Thin Film Applications (PASTA).[9] For each dopant type of a-Si:H (n-type, p-type, or intrinsic), a different process chamber is used to avoid cross-contamination. The intrinsic a-Si:H films are deposited from pure SiH$_4$ at a process pressure of 1.08 mbar, a power density of 30 mW/cm^2 and a substrate temperature of 130 °C. The n-type a-Si:H films are fabricated using a gas mixture consisting of SiH$_4$, H$_2$, and PH$_3$ at gas flow ratio of 4:1:0.02, a power density of 21 mW/cm^2, and a substrate temperature of 195 °C. The intrinsic a-Si:H films have a thickness of 5 nm, whereas the n-type a-Si:H films have a thickness of 20 nm. These are the thicknesses that are also used in practical SHJ solar cells. The layer stacks are deposited on both sides of the c-Si substrates. Between the depositions on the two sides, the wafers are flipped in air, without performing a second HF dip.

To test the influence of the annealing temperature on the passivation properties of the intrinsic/n-type a-Si:H layer stack, the samples are isochronally annealed at stepwise increased temperatures. This is done in 11 steps, starting at

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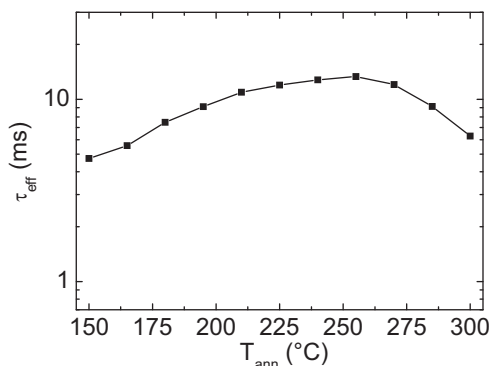
FIG. 1. Minority carrier effective lifetime at an injection level of $10^{15}\,cm^{-3}$ for different annealing temperatures.

150 °C and ending at 300 °C, with 15 °C increments, each step lasting for 1 h in a N_2 ambient. After each step, the samples are characterized by means of quasi steady state photoconductance (QSSPC) measurements,[10] using the quasi-transient mode and the generalized mode.[11] From these measurements, the injection level dependent minority carrier lifetime can be determined. From these lifetime data, both the dangling bond density and the surface charge density at the a-Si:H/c-Si interface can be extracted, by fitting them to several recombination models, i.e., Refs. 12–14. In this letter, the model developed by Leendertz *et al.* is used.[14]

The minority carrier lifetimes at an injection level of $10^{15}\,cm^{-3}$ of the best sample after the different annealing temperatures are depicted in Figure 1. A drastic improvement in passivation quality can be observed for temperatures up to T = 255 °C. For higher T, a decrease is observed. At annealing temperatures between 210 °C and 270 °C, very high carrier lifetimes, in excess of 10 ms at $10^{15}\,cm^{-3}$, are obtained, peaking at 255 °C. The minority carrier lifetime at this temperature is equal to $\tau_{eff} = 13.3$ ms at $10^{15}\,cm^{-3}$; superior to values reported thus far in the literature for c-Si passivated by a-Si:H. The injection level dependent minority carrier lifetime of this sample is shown in Figure 2. Other high lifetimes by a-Si:H containing layer stacks have, for instance, been obtained by Koyama *et al.*[15] for layer stacks consisting of a-Si:H and a-SiN$_x$:H deposited by hot-wire CVD (9.7 ms at $10^{15}\,cm^{-3}$). For intrinsic a-Si:H, lifetimes
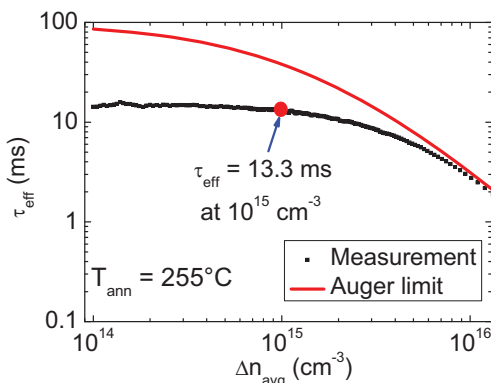

FIG. 2. (Color online) Injection level dependent minority carrier lifetime after thermal annealing at T = 255 °C, leading to an effective lifetime as high as 13.3 ms at $10^{15}\,cm^{-3}$ (indicated by the red dot in the figure) together with the Auger limit according to Ref. 17.
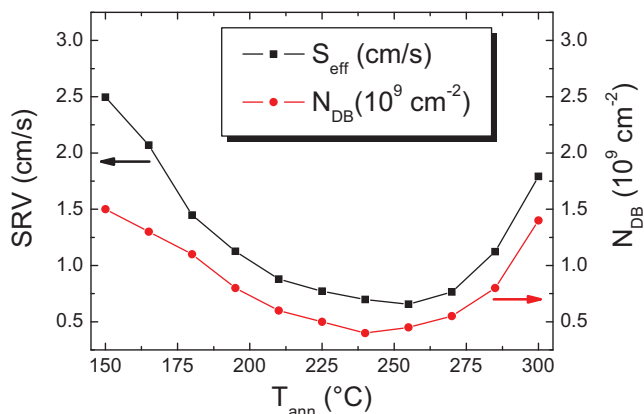

FIG. 3. (Color online) SRV corrected for Auger recombination, as well as N_{DB} versus anneal temperature. The SRV values are specified at an injection level of $10^{15}\,cm^{-3}$, whereas the N_{DB} values are determined from the whole measured injection level range.

around 10 ms at $10^{15}\,cm^{-3}$ have been obtained by the authors of this work,[8] as well as by De Wolf *et al.*[16]

As can be seen from Figure 3, we measured even higher minority carrier lifetime values at lower injection levels (exceeding 15 ms for injection levels below $1.5 \times 10^{14}\,cm^{-3}$). At higher injection levels, the minority carrier lifetime is limited by Auger recombination.[17] To identify the passivation mechanisms leading to this excellent carrier lifetime, we fit our data to the recombination model developed for a-Si:H/c-Si heterostructures by Leendertz *et al.*[14] For the bulk c-Si wafer, Auger recombination has been taken into account according to Ref. 17. From these fits, the dangling bond density (N_{DB}) as well as the charge density (Q_S) at the a-Si:H/c-Si interface can be extracted. The N_{DB} value indicates the quality of the chemical passivation, whereas Q_S assesses the field effect passivation. From our data, we deduce a strong qualitative correlation between surface recombination velocity (SRV) and N_{DB}, while Q_S has the same value for all data points. The value of Q_S is similar to values reported by Olibet *et al.*[13] for the same type of surface passivating a-Si:H layer stacks. In Figure 3, the SRV at an injection level of $10^{15}\,cm^{-3}$ (corrected for Auger recombination) as well as N_{DB} are plotted versus the annealing temperature. Both parameters obviously show the same trend, indicating that the improved surface passivation upon thermal annealing is caused by a reduction in dangling bond density at the a-Si:H/c-Si interface, whereas the surface charge density remains at a constant value, indicating that the charge persists during the thermal annealing process.

Our results from the annealing experiments can be explained as follows: a-Si:H growth at low temperature results in defective material, as the hydrogen is not properly equilibrated throughout the material during deposition, due to its low diffusion coefficient.[18] a-Si:H films that are deposited at relatively low temperatures typically possess a higher void density, porosity, and fraction of hydrogen that is bonded as multihydrides (Si-H$_{n>1}$),[6,18,19] leading to higher defect densities and reduced passivation quality.[19,20] The recombination effect has been observed to be stronger if these multihydrides are present close to the a-Si:H/c-Si interface, and less detrimental if they occur in the a-Si:H layers further away from the interface.[19] Thermal annealing enables

the hydrogen to become mobile,[18,19] diffuse towards the a-Si:H/c-Si interface, and equilibrate bulk and surface defect densities in the a-Si:H.[7,18] This mechanism strongly reduces the defect density at the a-Si:H/c-Si interface and, therefore, improves the passivation quality.[6,8] If the deposition temperature is too high (T > 255 °C in the present case), the passivation quality again decreases due to hydrogen effusion from the intrinsic a-Si:H film.[21,22] Effusion of hydrogen occurs at lower temperatures for doped a-Si:H films than for intrinsic a-Si:H.[21]

In summary, we have obtained high quality c-Si surface passivation by applying a layer stack consisting of intrinsic and n-type a-Si:H, yielding combined chemical and field effect passivation. Annealing at temperatures up to 255 °C has been demonstrated to reduce surface recombination, leading to an effective lifetime as high as 13.3 ms at an injection level of 10^{15} cm^{-3}. Modeling of the injection level dependent minority carrier lifetime data shows that this reduced surface recombination correlates with a reduced dangling bond density at the a-Si:H/c-Si interface, which is ascribed to dangling bond saturation. Annealing at higher temperatures leads to an increased dangling bond density, caused by hydrogen effusion. The surface charge density at the a-Si:H/c-Si interface, however, is not affected; the charge persists during thermal annealing, which partly explains the high lifetime results.

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