High-Resolution ADC Linearity Testing Using a Fully Digital-Compatible BIST Strategy

Hanqing Xing, *Student Member, IEEE*, Hanjun Jiang, *Member, IEEE*, Degang Chen, *Senior Member, IEEE*, and Randall L. Geiger, *Fellow, IEEE*

***Abstract*—This paper proposes a digital-compatible built-in self-test (BIST) strategy for high-resolution analog-to-digital converter (ADC) linearity testing using only digital testing environments. The on-chip stimulus generator consists of three low-resolution and low-accuracy current steering digital-to-analog converters (DACs), which are area efficient and easy to design. The linearity of the stimuli is improved by the proposed reconfiguration technique. ADCs' outputs are evaluated by simple digital logic circuits to characterize the nonlinearities. The proposed BIST strategy is capable of characterizing ADC transition levels one by one with small hardware overhead. The testing performance is not sensitive to the mismatches and process variations, so that the analog BIST circuits can easily be reused without complex self-calibration. Simulation and experimental results show that the proposed circuitry and BIST strategy can test the INL_k error of 12-bit ADCs to a ± 0.15 least significant bit (LSB) accuracy level using only 7-bit linear DACs.**

***Index Terms*—Analog-to-digital converters (ADCs), built-in self-test (BIST), deterministic dynamic element matching (DDEM), embedded test, integral nonlinearity (INL), static linearity testing.**

I. Introduction

ALONG with the continuous advance in the integration level of the CMOS technology, more and more new applications in signal processing, communications, and instrumentation tend to add more functionality to a single silicon chip. Analog and mixed-signal (AMS) circuits are deeply embedded with other core semiconductor technologies, such as logic, memory, input–output, and radio frequency. The accessibility and observability of the circuit nodes are inevitably reduced because of the limited number of pins available for testing. Meanwhile, the performance of AMS circuits keeps improving to satisfy the demands of the new applications. As a result, testing these circuits becomes increasingly demanding and costly [1].

An analog-to-digital converter (ADC) is one of the most extensively used mixed-signal circuitries. As the interface between the analog and digital signals, ADCs quantize the received analog signal and generate the digital outputs for later signal processing. The performance of ADCs then directly determines the performance accuracy of the whole system. Testing of the ADCs is indispensable for almost all those systems to validate the design and to reduce the rejected parts.

The AMS circuits can be tested in different ways to achieving satisfactory test performance with low test cost. Almost all the solutions incorporate automated test equipment (ATE) and device interface boards (DIB). The most common way is to use an AMS ATE tester with an analog DIB. The tester needs to have much better performance than the circuits under test (CUTs) in accuracy, speed, noise, and so on. The DIB should carefully be designed for each type of CUT according to their unique electrical and mechanical testing requirements. For high-resolution testing, the eligible AMS ATE will prohibitively be expensive for its extremely high performance. The test cost then will considerably be high. With the CUTs deeply embedded in the system, this method has difficulties to maintain signal integrity due to the loss of the node accessibility and observability. Then, the test accuracy is reduced. To lower the cost, it is preferred to use cheap but low-performance testers. In [2], the authors use a much cheaper digital ATE tester in AMS testing by adding the necessary analog functionality on the DIB. However, designing such a DIB is quite elaborate and time consuming. More important, the signal integrity issue still remains. A possible solution to the signal integrity problem is the built-in self-test (BIST) technique, which offers the on-chip stimulus and response verification capabilities for testing by adding some functionality circuits on-chip with the CUT. Therefore, no analog signal needs to be applied or processed off-chip, and only digital testers and digital DIBs, which provide simple digital connections, are necessary for testing. The testing cost can further be reduced by having more CUTs tested in parallel since BIST could often decrease the number of connections for testing.

BIST has been proposed for a long time as a solution to lowering test cost and improving test accuracy. However, unlike the widely used digital BIST, "analog/mixed-signal BIST techniques are lagging. No proven alternative to performance-based analog testing exists and more research in this area is needed [1]." The reason is that, although BIST simplifies the test setup, it increases the circuit complexity and silicon area. To provide satisfactory testing performance for high-resolution AMS circuits, BIST circuits tend to be very complicated and large. Furthermore, conventional high-performance analog circuits are subject to mismatch and process variation errors. BIST circuits then have to be tested and calibrated. The efforts of

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H. Xing, D. Chen, and R. L. Geiger are with the Department of Electrical and Computer Engineering, Iowa State University, Ames, IA 50011 USA (e-mail: xinghq@iastate.edu).

H. Jiang is with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China (e-mail: jianghanjun@mail.tsinghua.edu.cn).

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testing the BIST circuits often make the whole BIST idea nonrealistic. As a result, the practical BIST circuits should have high performance but should be small, easy to design, and insensitive to mismatch and process variation.

In this paper, we present a BIST solution to measuring ADCs' linearity performance. The method is fully compatible with digital testing environments using only digital testers and straightforward connections. On-chip circuitry for testing is able to provide high testing performance under the process variation and mismatch with small silicon area and minimal design effort. No complex self-calibration is required. The rest of this paper is organized as follows: Section II briefly discusses ADCs' linearity specifications and the needs of implementing ADCs' linearity BIST. Section III describes the structure and the performance of the proposed on-chip source generator. In Section IV, the proposed test structure and BIST strategy are presented. Simulation and experimental results are shown in Sections V and VI, respectively. Finally, Section VII concludes this paper.

II. BIST of ADC Linearity Performance

The nonlinear errors in an ADC are usually characterized by measuring the differential nonlinearity (DNL) and the integral nonlinearity (INL) of its transition levels [3]. DNL is the maximum deviation in the code bin widths from the ideal code bin width. INL is the maximum deviation of the measured transition levels from the ideal transition levels. In this paper, the ideal transition levels are defined by an endpoint fit line passing through the first and last transition points in the transfer curve, i.e., T_1 and T_{N-1}, respectively, where N is the ADC's resolution. For the kth ADC transition level T_k, $k = 1, 2, \ldots, N-2$, the nonlinear errors can be calculated by

$$\mathrm{DNL}(k) = \frac{T_{k+1} - T_k}{\mathrm{LSB}} - 1 \tag{1}$$

$$\mathrm{INL}(k) = \frac{T_k - T_1}{\mathrm{LSB}} - (k-1) \tag{2}$$

where the least significant bit (LSB), which is the ideal code bin width, is defined as

$$\mathrm{LSB} = \frac{T_{N-1} - T_1}{N-2}. \tag{3}$$

Then, the INL and DNL of the ADC are the maximum values of the magnitudes of INL(k)'s and DNL(k)'s, respectively. From the equations, we can clearly see that ADCs' linearity characteristics are calculated from ADCs' transition levels. Thus, the major task of testing is to accurately estimate each transition level of ADCs under test.

There are several common methods of measuring the transition levels of ADCs. The most ubiquitous approach is the histogram test, which provides an effective way of full-code testing [4]–[6]. However, the accuracy of the test strongly depends on the distribution of the input stimuli, which is affected by both the linearity performance of the source signals and all the concerned random effects, such as the noise and the clock jitter. In addition, for an n-bit ADC under test, it needs $2^n - 1$ memory cells to save the histogram counts during the linearity characterization processes. Both of these two factors make the histogram test difficult to be directly used in BIST applications. Another commonly used method is the servo-loop feedback method, which is able to measure any specific ADC transition level using an additional precise digitizer [7]. However, this technique is quite slow and significantly limits the total number of ADC transition levels that can be tested. In some applications, particularly for high-resolution ADCs, reduced-code testing instead of full-code testing has to be applied to cut the testing time. In the case of built-in applications, the precise digitizer will dramatically increase the area overhead and the design efforts. Therefore, this technique is often not a feasible solution either.

Compared with the traditional methods, a successful BIST implementation for ADC linearity testing tends to satisfy the following conditions: First, it includes a very low-cost on-chip stimulus generator, which is more accurate than the ADCs under test and is able to provide stimulus signals for at-speed testing. Second, no complex digital signal processing and microprocessor are needed to obtain the measurements and the linearity performance of the ADC transition levels. Finally, the BIST strategy should be capable of characterizing the transition levels with small hardware overhead. Since the traditional high-accuracy source generators are either particularly area consuming or very slow, the first condition becomes the bottleneck of ADC linearity BIST. In fact, there is no widely accepted solution to building such source generators.

III. On-Chip Source Generator

As we have discussed, traditional high-accuracy circuits are too costly to be used in BIST applications. Some methods of using low-accuracy circuits with high test performance have been investigated [8], [9]. This section describes the structure of the proposed source generator, which only consists of small low-accuracy DACs, and evaluates its test performance.

A. Segmented DDEM DAC

The source generator is primarily a reconfigurable low-accuracy segmented current steering (SCS) DAC. The so-called deterministic dynamic element matching (DDEM) technique is used to control the reconfiguration and improve the accuracy [8], [10], [11].

The segmented structure achiev es a good combination of high resolution and small area since the decoders can be much simpler and smaller. As shown in Fig. 1, an n-bit SCS DAC usually consists of an n_M-bit thermometer-coded most significant bit (MSB) array and an n_L-bit binary-coded LSB array, where $n = n_M + n_L$. The MSB and LSB arrays generate currents according to their input digital codes, i.e., D_M and D_L, respectively. The total current generated is then forced to flow through a resistor to produce the output voltage. In the normal applications, the MSB array's linearity dominates the whole DAC's performance. As a result, it generally needs to meet the specification of the whole DAC and requires considerable consumption of area and power.

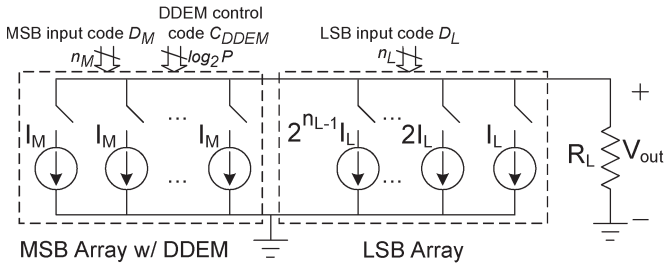

Fig. 1. n-bit SCS DAC.

This paper uses a low-accuracy thermometer-coded DAC as the MSB array to save cost. The DDEM method is applied to the MSB array to improve its accuracy. DDEM reconfigures the mappings between the current cells and the input digital codes. The basic idea of DDEM is that instead of generating the desired signal with a costly high-performance MSB array DAC, we create a set of cheap and "poor" DACs by reconfiguration. Each of these DACs generates a series of low-resolution and low-accuracy output samples. If all these samples, which are distributed in a common range, follow a nearly uniform distribution, the equivalent output linearity of the DAC will be improved. Assume that the MSB array has an n_M-bit resolution, and therefore, $N_M = 2^{n_M}$ current cells, $i_1, i_2, \ldots, i_{NM}$. DDEM creates P (a submultiple of N_M and an exponent of 2) different configurations, which is controlled by a $\log_2 P$-bit control code C_{DDEM}. For simplicity, we conceptually put all the current elements on a circle clockwise from i_1 to i_{NM} then back to i_1, as shown in Fig. 2. To generate an output voltage for input code d_M, we may start from i_1 and clockwise turn on d_M consecutive current cells. Then, P analog outputs can be generated for one digital input code by choosing P different current cells as the start point. In the DDEM algorithm, those P start points are evenly distributed on the circle. A simple 4-bit DDEM DAC example with $P = 4$ and $d_M = 5$ is illustrated in Fig. 2. The four start points selected are i_1, i_5, i_9, and i_{13}. Fig. 2(a)–(c) shows the cases that the selected five current cells start from i_1, i_5, and i_{13}, respectively.

B. Performance Analysis

In this part, we will analytically show the linearity improvement of the DAC and evaluate the overall testing performance.

First, assume that the outputs of the DDEM MSB array are used to measure a specific ADC transition level T_k. The procedure is that under each DDEM configuration (for example, the jth configuration, $j = 1, 2, \ldots, P$), we search for a digital input code d_j that satisfies $V_j(d_j) < T_k < V_j(d_j + 1)$, where $V_j(d_j)$ and $V_j(d_j + 1)$ are the MSB array outputs associated with input codes d_j and $d_j + 1$, respectively. Then, the measurement of T_k is represented by the average of $d_1, d_2, \ldots, d_P$ under different configurations, and the equivalent analog measurement of T_k is expressed by

$$\hat{T}_k = \frac{1}{P}\sum_{j=1}^{P} V_{id}(d_j) \tag{4}$$

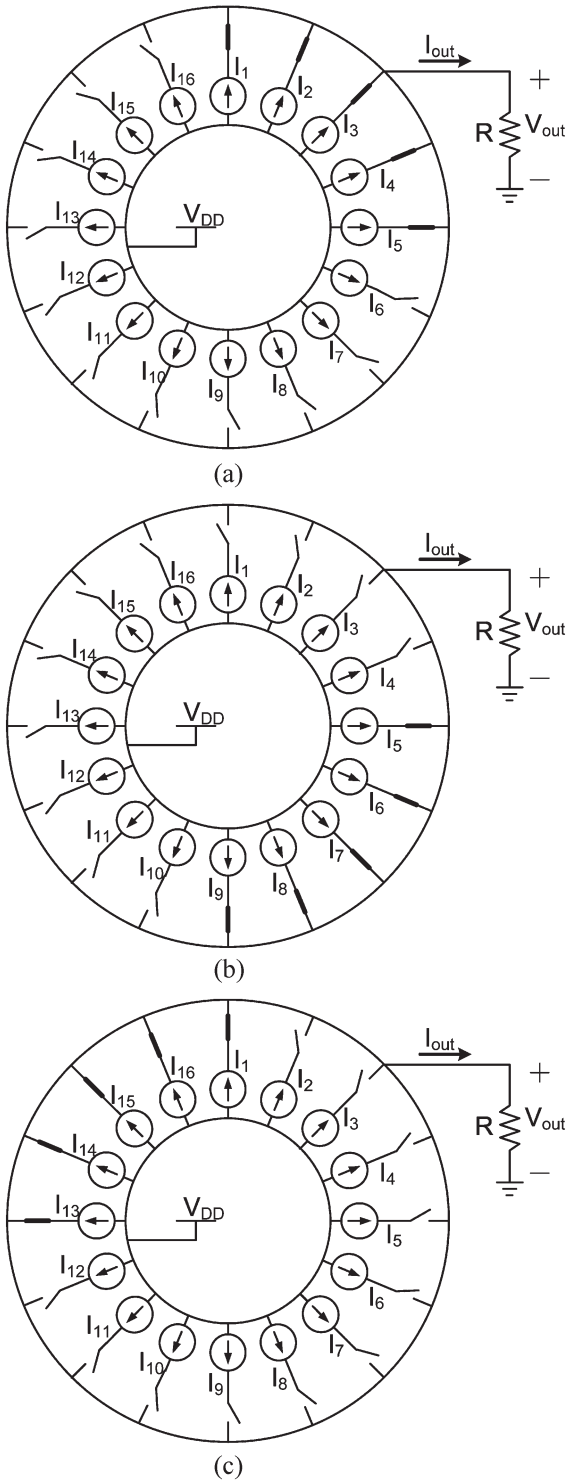

Fig. 2. Four-bit DDEM DAC with $P = 4$ and $d_M = 5$. (a) 1st output sample with $i_1 \sim i_5$ on. (b) 2nd output sample with $i_5 \sim i_9$ on. (c) 4th output sample with $i_{13} \sim i_{16}$ and i_1 on.

where $V_{id}(d_j)$ is the output voltage at code d_j if an ideal n_M-bit DAC is used as the MSB array. Thus, the measuring error is

$$e_k = \hat{T}_k - T_k = \frac{1}{P}\sum_{j=1}^{P} V_{id}(d_j) - T_k. \tag{5}$$

Under different configurations, T_k can be expressed in different ways as in

$$T_k = V_j(d_j) + r_j(k), \quad j = 1, 2, \ldots, P \tag{6}$$

where $r_j(k)$ is denoted as the residue voltage between the transition level and the MSB array output at code d_j. Substituting (6) into (5) leads to the further expression of the measuring error, i.e.,

$$e_k = \frac{1}{P}\sum_{j=1}^{P} r_j(k) - \frac{1}{P}\sum_{j=1}^{P}\left[V_j(d_j) - V_{id}(d_j)\right]. \tag{7}$$

It is noticed that $V_j(d_j) - V_{id}(d_j)$ is the INL of the jth-configuration MSB array at code d_j, which is designated as $\mathrm{INL}_j(d_j)$, and can be rewritten as the sum of $\mathrm{DNL}_j(m),\ m = 1, 2, \ldots, d_j$, which are the jth-configuration MSB array's DNL errors. In DDEM, the DNL errors of the MSB array are cyclically shifted with the current cells for different configurations. This fact, combined with the definition of the DAC's DNL, gives us

$$\sum_{j=1}^{P}\sum_{t=1}^{s*q} \mathrm{DNL}_j(t) = s \times \sum_{i=1}^{N_M} \mathrm{DNL}_1(i) = 0 \tag{8}$$

since the expression in (8) exactly covers the DNL errors of all the N_M current sources for s times, where $q = N_M/P$, and $s = 1, 2, \ldots, P$. Assume that s satisfies $d_j - sq \geqq 0$ for $j = 1, 2, \ldots, P$. We can rewrite the measuring error in (7) as

$$e_k = \frac{1}{P}\sum_{j=1}^{P} r_j(k) - \frac{\mathrm{LSB}_M}{P}\sum_{j=1}^{P}\sum_{t=1}^{d_j - sq} \mathrm{DNL}_j(t) \tag{9}$$

where LSB_M is the ideal MSB array LSB.

To evaluate the testing performance, we start with the first term in (9). The residue voltages $r_j(k)$'s are originally at the n_M-bit level because of the MSB array's resolution. With the help of the segmented structure, the resolution can be increased by adding the LSB array. Then, the transition level T_k can further be approached by the LSB array outputs. The new residue voltages will be at the $n_{\mathrm{DAC}} = n_M + n_L$ bits level because they are the difference between T_k and the segmented DAC's outputs that are the closest to but less than it. Furthermore, for any transition level T_k, the residue voltages are randomized by DDEM because of the mismatch errors. Thus, the variation of the first term in (9) is approximately at the $n_{\mathrm{DAC}} + 0.5\ \log_2 P$ bits level. The second term in (9) is induced by the nonlinearity of the original MSB array. If we assume that the linearity performance of the MSB array is not worse than its resolution, which is n_M bits, the second term can be simplified to the sum of a set of nonrepeating $\mathrm{DNL}_1(k)$'s divided by P. The maximum value of the sum is comparable to the INL of the original MSB array, i.e., INL_M. Then, the nonlinearity of the original MSB array is reduced by $\log_2 P$ bits. On the whole, the equivalent testing performance of the segmented DDEM DAC is expressed by

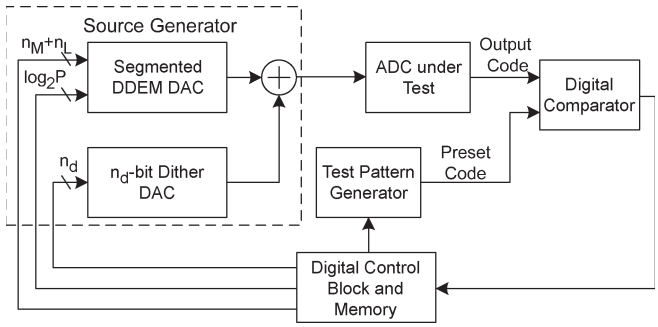

Fig. 3. Proposed ADC BIST structure.

$$n_{\mathrm{eq}} \approx \min\{n_{\mathrm{DAC}} + 0.5\ \log_2 P, \mathrm{ENOB}_M + \log_2 P\}\ \text{bits} \tag{10}$$

where $\mathrm{ENOB}_M = n_M - \log_2(\mathrm{INL}_M/0.5) = n_M - \log_2 \mathrm{INL}M - 1$ is the effective number of bits of the original MSB array. Therefore, if we assume that the segmented structure provides enough resolution so that the first term in (10) does not limit the testing performance, the linearity of the testing stimuli is improved by $\log_2 P$ bits.

C. Structure

The target of this paper is to test high-resolution ADCs, which requires highly linear source signals. The low-accuracy segmented DDEM DAC is built on-chip as the source generator. Considering the number of the current cells and the complexity of the digital control block, we still want the thermometer-coded MSB array as low resolution as possible. In this case, the second term in (10) will probably limit the test performance since when the MSB array is of low resolution, the number of DDEM configurations P has to be small. A solution to this problem is to incorporate another low-resolution DAC to generate extra linear dither steps at the output. As shown in Fig. 3, these small dithers are added to the outputs of the DDEM DAC. Each output of the DDEM DAC is spread by N_d dither levels, where N_d is the resolution of the dither DAC in decimal. Then, the measurement of the transition level T_k, i.e., m_k, is expressed as

$$m_k = \frac{1}{P}\sum_{j=1}^{P}\sum_{i=1}^{N_d} d_{j,i} \tag{11}$$

where $d_{j,i}$ is the obtained DDEM DAC input code when the jth DDEM configuration and the ith dither output are applied. $d_{j,i}$ and i satisfy $V_j(d_{j,i}) + V_d(i) < T_k < V_j(dj, i+1) + V_d(i)$, where $V_j(\bullet)$ and $V_d(\bullet)$ are the transfer functions of the jth-configuration DDEM DAC and the dither DAC, respectively. The output range of the dither DAC is set to be $q = N_M/P$ LSB_M's. It can be shown that the second term in (9) has a repeating form for different ADC transition levels with a period of q LSB_M's. Then, linearly spreading the error distribution over one period range and getting the average will effectively reduce the error variation and improve the testing

performance. Adding this dither DAC also increases the number of residue voltages averaged so that it will help reduce the error from the resolution limitation as well. It can be shown that the effect of the dither DAC on the testing performance is very similar to that of the DDEM. The equivalent test performance of the segmented DDEM DAC with dithering can be represented by

$$n_{\text{eq}} \approx \min\{n_{\text{DAC}} + 0.5(\log_2 P + n_d), \text{ENOB}_M + \log_2 P + n_d\} \text{ bits} \quad (12)$$

where n_d is the resolution of the dither DAC in bits. Here, we assume that the nonlinear errors of the LSB array and the dither DAC do not limit the testing performance. This assumption usually holds since the full ranges of the LSB array and the dither DACs are much smaller than the DAC's output range. For effective implementation, the parameters, such as n_M, n_L, P, and n_d, need to be optimized so that both terms in (12) are reduced to the same level. As shown in the analysis, the effects of the DDEM and dither DAC are similar. However, dithering cannot separately be used with a low-accuracy DAC since the test performance is dependent on the accuracy and the nonlinear error distribution of the DAC.

IV. ADC BIST Strategy

This part will discuss the structure of the testing system and the BIST procedure.

A. Testing Structure

The proposed testing structure is illustrated in Fig. 3. Stimulus signals to the ADC under test are generated by adding together the outputs of the dither DAC and the segmented DDEM DAC. Several digital codes, which include the input codes for the MSB and LSB arrays, the control code for the DDEM configuration, and the dither DAC input, are generated by a digital control block. This block simply consists of a state machine and a small number of memory cells. A preset code k is set by a test pattern generator for measuring the ADCs' kth transition level T_k. The digital comparator will compare the ADC output code with the preset code k and send the result back to the control block. In addition, the comparator and the control block form a digital feedback loop. During measurement, under each DDEM configuration and dither input, the feedback loop will help find the desired input codes d_M and d_L for the MSB and LSB arrays, respectively. These codes generate the stimulus sample that is the closest to but less than the transition level T_k. The codes will be recorded to get the measurement of T_k. Binary search is applied to find those codes with fewer iteration cycles. The detailed procedure for measuring the transition level T_k with the proposed structure is given in the list that follows.

1) Select a control code pair (j, i) for the DDEM configuration and the dither DAC input, where $j = 1, 2, \ldots, P$, and $i = 0, 1, \ldots, N_d - 1$.
2) Set k as the preset code for comparison. Do binary search for the input codes d_M and d_L with the following steps:

```
set d_M = 0, d_L = 0
for v = n_M : 1
  a_M = d_M + 2^(v - 1)
  a_L = d_L
  Set a_M and a_L as input codes for SCS DAC
  if ADC's output < k
    d_M = a_M
  end
  end
  for u = n_L : 1
    a_L = d_L + 2^(u - 1)
    a_M = d_M
    Set a_M and a_L as input codes for SCS DAC
    if ADC's output < k
      d_L = a_L
    end
    end
    d = d_M × 2^(n_L) + d_L
```

3) Add the obtained code d into a register. Go back to step 1 if there is an unused control code pair left.

After finishing the binary search for all the control code pairs, the algorithm uses the average (or the sum equivalently) of the obtained codes as the measurement of T_k and save it for later use. The processing needs only one memory cell and a digital adder. The total memory size is then mainly determined by how many transition levels we need to record for testing at one time. The testing time will be of great concern when high test performance is desired since the total times of binary search is $N_D P$.

In the implementation of the DDEM DAC, we introduce 1 bit overlapping between the MSB and LSB arrays to compensate for the considerable DNL errors in the MSB part and make sure that all the residue voltages in (9) are covered by the LSB array. In this case, we will have the DAC's resolution as $n_{\text{DAC}} = n_M + n_L - 1$ and the equivalent input code as $d = d_M * 2^{\wedge}(n_L - 1) + d_L$. A little change needs to be made in the second step of the procedure.

B. BIST Procedure

There are different approaches to verifying ADCs' linearity performance. Usually, full-code INL_k testing is preferable for complete performance identifications. However, for high-resolution ADCs, which are typically slow, the data acquisition time may be prohibitively long. To cut down the test time, sometimes, reduced-code testing is applied. In this case, only a small subset of the ADC output codes are guaranteed. On the other hand, for the production test, we may only need to know whether an ADC meets the specification or not. This is noted as pass/fail testing. It means that as long as we can find a transition level that is out of the error bound, the test is finished, and the characteristics of other transition levels are not anymore important. Based on the test procedure described in the previous section, we are able to develop different BIST strategies for different kinds of ADC testing.

The flowchart of a pass/fail BIST procedure for ADC linearity testing is shown in Fig. 4. The procedure starts after a

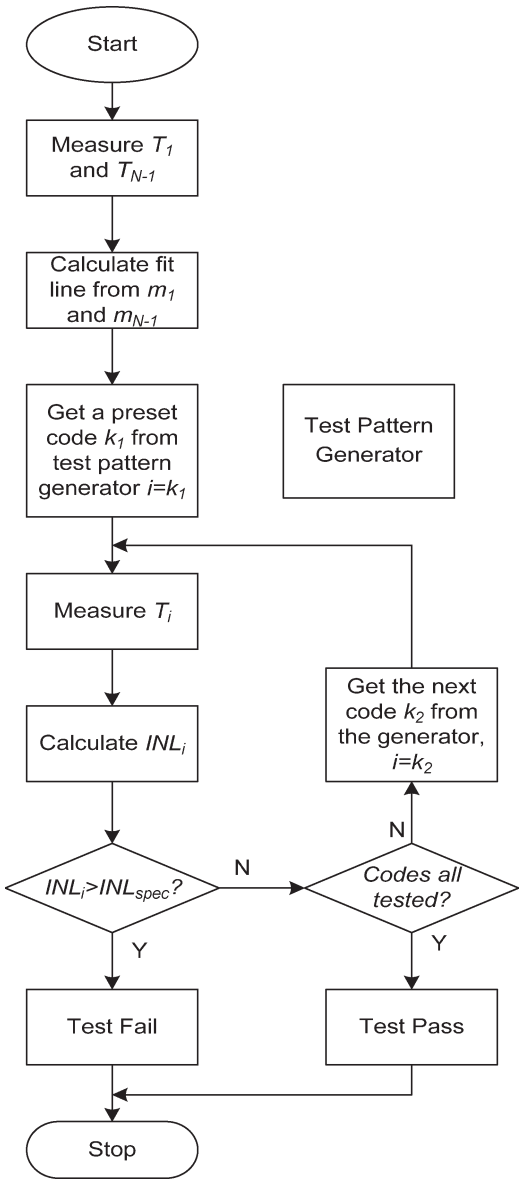

Fig. 4. Flowchart of a pass/fail BIST procedure.

testing enable signal is sent by the external digital tester. The digital control block in Fig. 3 controls testing using a state machine. The first step is to characterize the endpoint fit line of the ADC under test. The first and last transition levels, i.e., T_1 and T_{N-1}, respectively, will be measured by setting the preset code k equal to 1 and $N-1$, respectively. The measuring process for each transition level is described in the previous section. The measurements then are recorded in the memory cells as the references for the ideal transfer curve. For any preset code k between 1 and $N-1$, the measurement of T_k can be obtained and compared with the ideal transfer curve to get the information about INL_k. The procedure requires only simple linear calculations, which can be done by digital logic circuits. This INL_k then is compared with the specification. If it does not meet the specification, the ADC fails the test. Otherwise, the next transition level will be tested. If all the codes that need to be tested meet the specification, the ADC passes the test. After the test is finished, a notification signal and the testing results will be sent back to the digital tester.

The test pattern generator is built on-chip to create a list of codes for testing. A simple and general way of doing that is by using a counter. After measuring the fit line, the transition levels are sequentially tested from T_2 to T_{N-2}. However, that may not be an efficient way in terms of less test time if we can find some transition levels that are more possible to have large INL_k errors than others. In this case, it makes sense to put those transition levels in front of the list to reduce the average testing time for bad parts. Usually, that information can be achieved from the ADC structures. As an example, assume that n-bit pipeline ADCs using 1 bit/stage structure are under test. The gain error and the comparator offset error of each stage will cause nonlinearity. It can be shown that for a good design, the largest INL_k error happens the most probably around the position where the code k has its MSB changed from 0 to 1, which is 2^{n-1} in decimal form. Thus, in testing, several codes around 2^{n-1} can first be set by the test pattern generator to get a local maximal INL_k. If it is within the error bound, the next code for testing should be at the transition of the second MSB, which happens at two positions, i.e., 2^{n-2} and $2^{n-1}+2^{n-2}$, and so on. The code list can then be generated by a state machine based on this information. For other ADC structures such as successive approximation register ADCs, cyclic ADCs, and pipeline ADCs with different numbers of bits per stage, some modifications need to be made according to their own characteristics.

V. Simulation Results

Numerical simulations have been done to validate the testing performance of the stimulus generator and the proposed testing procedure. In the simulation, the segmented DDEM DAC has a 7-bit MSB array and a 6-bit LSB array. The full-scale range of the LSB array is equivalent to 2 LSB_M's for error compensation, where LSB_M is the ideal MSB array LSB. The number of configurations P is equal to 16. Thus, we have a 4-bit DDEM control code for configuration selection. The dither DAC has a 4-bit resolution and a full-scale range of 8 LSB_M's, which is equal to N_M/P, as explained in Section III-C. The current sources in the simulation are modeled by a nominal current with a random Gaussian-distributed mismatch error. Fig. 5 shows the linearity performance of the original MSB array. The INL is about 0.52 LSB, and then, the linearity of the MSB array is at only the 7-bit level. The LSB array and the dither DAC in the simulation are both about the 6-bit linear level.

From the analysis of the testing performance, we can calculate the equivalent test performance in bits as

$$\begin{aligned} n_{\mathrm{eq}} &\approx \min\{n_{\mathrm{DAC}} + 0.5(\log_2 P + n_d), \\ &\qquad \mathrm{ENOB}_{\mathrm{DAC}} + \log_2 P + n_d\} \\ &\approx \min\{12 + 0.5 \times (4+4), 7+4+4\} \\ &= \min\{16, 15\} = 15 \text{ bits}. \end{aligned} \tag{13}$$

The equivalent testing performance of the stimulus generator is at about the 15-bit level. In the simulation, a 12-bit ADC is

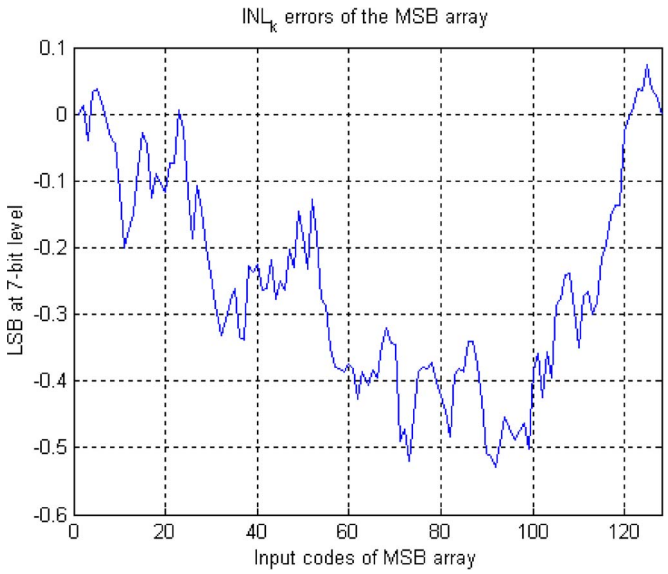

Fig. 5. INL$_k$ error of the MSB array.

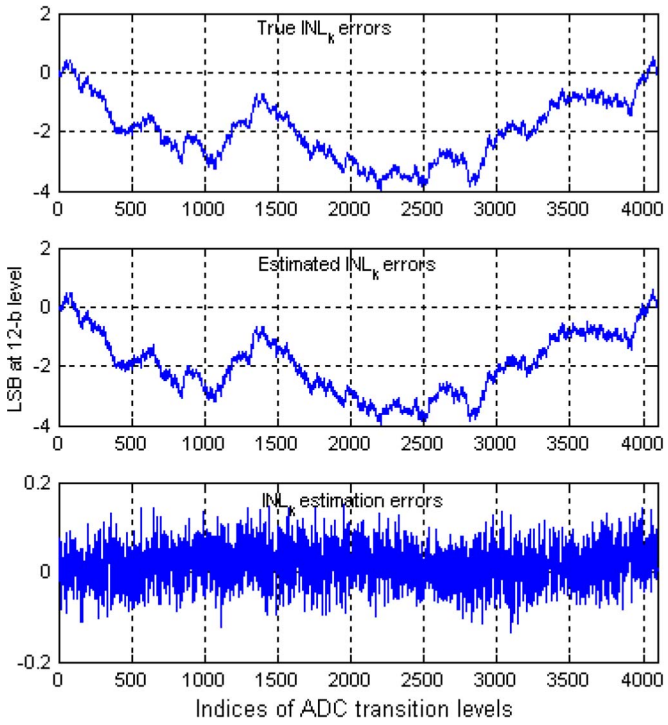

Fig. 6. INL$_k$ estimation errors of the ADC under test.

under test. The INL errors of the simulated ADC are shown at the top of Fig. 6. A white noise signal is added to the input samples of the ADC to create the noise effect of a practical ADC. The standard deviation of the additive noise is set to be 0.25 LSB at the 12-bit level. The measurement of the transition levels follows the test procedure described in Section IV-A. The INL$_k$ information of each transition level is then calculated from the measurements. Fig. 6 shows the true and estimated INL$_k$ errors of the ADC under test along with the estimation errors, which is the difference between the first two plots. From the simulation, the INL$_k$ estimation errors are bounded by about ± 0.15 LSB. Therefore, the testing performance of the stimulus

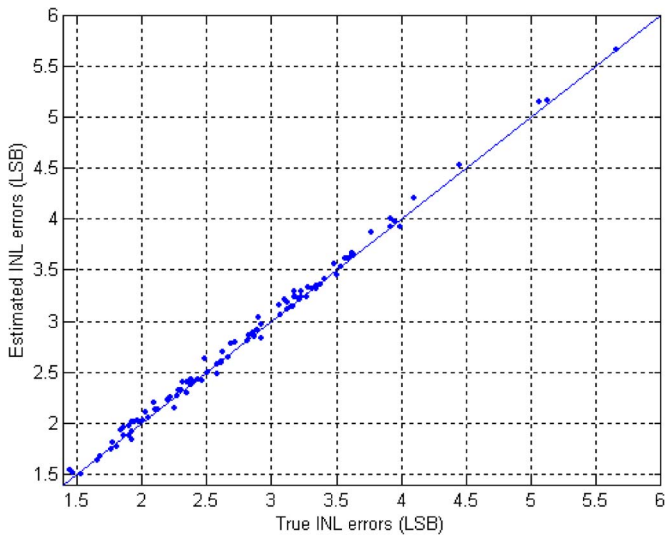

Fig. 7. Estimated and true INL errors of 100 twelve-bit ADCs.

source is evaluated to be at about the 15-bit level, which verifies the theoretical analysis in (13).

To validate the robustness of the method to the random mismatch errors, 100 different 12-bit ADCs are tested by 100 test systems with different mismatch errors in the simulation. The configurations and accuracy levels of the test systems are the same as those in the previous simulation. The results are shown in Fig. 7. Each dot in the figure represents one testing result. The true and estimated INLs of the ADCs are represented by the coordinates of the dot. The results show that the INL of the 100 ADCs varies from 1.5 LSB to 5.5 LSB, and the INL estimation errors are from -0.118 LSB to 0.139 LSB. The testing performance is very robust to the different implementations with different errors.

Analysis shows that the test performance can be improved by increasing several parameters, such as the number of configurations P and the resolution of the dither DAC n_d. In another simulation, P is increased while all the other system setups are the same as in the previous simulations. The same MSB array, as shown in Fig. 5, is used. Fig. 8 illustrates the reduction in the INL$_k$ estimation errors of a 14-bit ADC with increasing P. The standard deviation of the noise in this simulation is set to be 0.25 LSB at the 14-bit level. When P is increased, the test performance is improved along with the cost of test time.

VI. Experimental Results

The experimental results shown in this section are measured from the latest fabricated DDEM DAC in a 0.5-μm CMOS process [12]. The prototype chip was designed for investigating the output characteristics of the DACs with DDEM. It includes analog current sources designed with all minimal-size transistors and the DDEM logic control circuits. The DAC's resolution and the DDEM control parameter P are both programmable and can be up to 12 bits and 512, respectively. Although the Spectre simulation shows that the stimulus frequency can be as high as 100 MHz, the data are measured at 1 MHz because of the speed limitation of the high-precision digitizer used in the data acquisition. The differential outputs of the selected

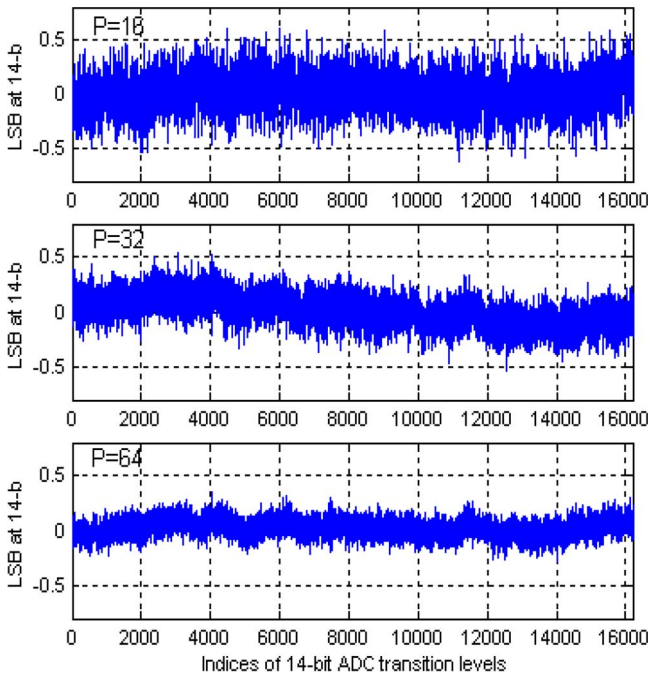

Fig. 8. INL_k estimation errors of a 14-bit ADC with $P = 16$, 32, and 64.

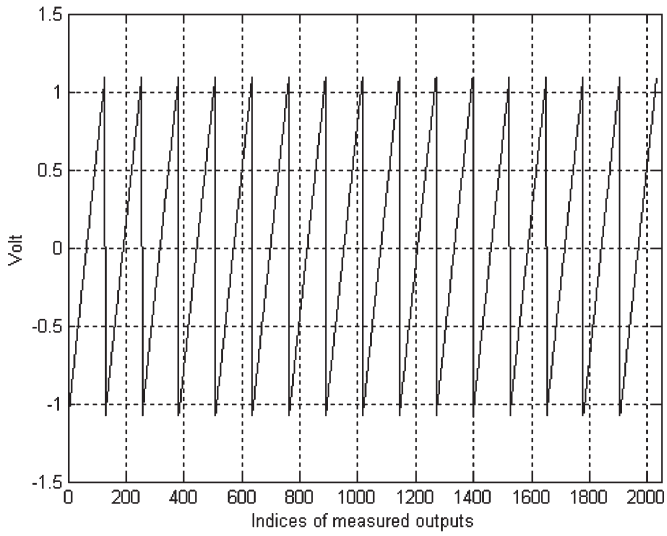

Fig. 9. Measured differential outputs of the DDEM MSB array.

7-bit DDEM MSB array with $P = 16$ are measured, as shown in Fig. 9. Each ramp in the figure shows the output characteristics of the MSB array under one specific DDEM control code. The linearity of the original MSB array is at about the 9-bit level, as shown in Fig. 10.

Similarly, output levels of the 6-bit LSB array and the 4-bit dither DAC are measured from the chip. Both of them are tested to be less than 8 bits linear. A simulated 12-bit ADC is tested using the measurements of the DAC outputs to verify the testing performance of the measured data. Fig. 11 shows the true and estimated INL_k errors along with the estimation errors. The results prove the testing performance of the proposed source generator and the testing procedure. It is noted that although the linearity of the MSB array is 2 bits better than in the simulation

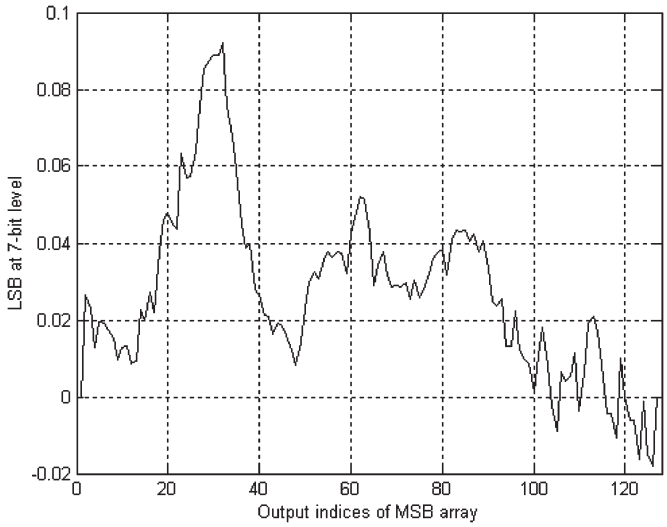

Fig. 10. Measured INL_k errors of the DDEM MSB array.

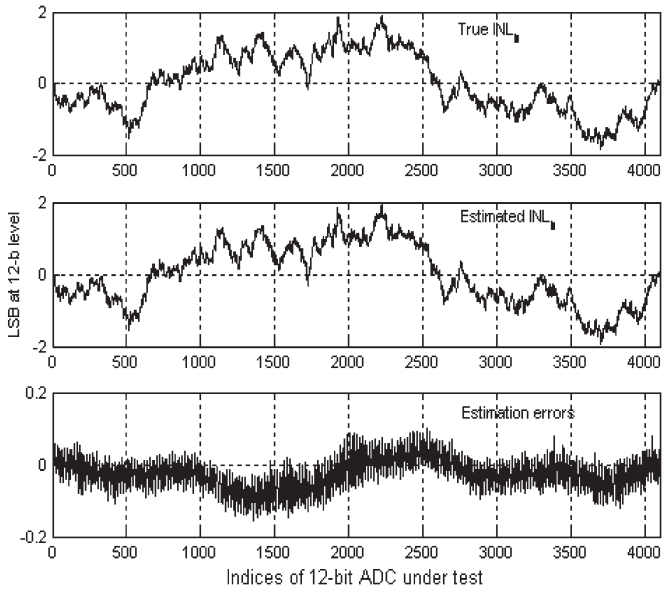

Fig. 11. Testing results of the simulated 12-bit ADC using measured data.

section, the testing performance is still at the 15- to 16-bit level because of the error from the resolution limitation, as in (12).

VII. Conclusion

Using a digital tester with BIST for AMS testing is an ideal way of reducing the test cost and improving the test quality. However, the traditional high-performance circuits and testing solutions are too costly and complicated to be built on-chip just for testing. In this paper, the authors have proposed a BIST strategy for ADC linearity testing, which is fully compatible with digital test environments using a low-cost digital tester and a simple digital DIB. Low-resolution and low-accuracy DACs (which are cost efficient) have been built on-chip as source generators. The testing performance has been guaranteed by the DDEM reconfiguration technique and the testing procedure. The design of the on-chip testing circuits could be as easy as the digital design because of the low accuracy requirements

on the analog blocks. Simulation and experimental results have demonstrated that the proposed strategy is able to test the INL_k error of 12-bit ADCs to the ± 0.15 LSB accuracy level using very low-accuracy DACs. In addition, the BIST strategy can easily be adopted for DAC testing if the digital comparator is replaced by an analog comparator, which compares the outputs of the DAC under test with the outputs of the source generator.

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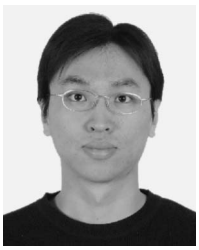

Hanqing Xing (S'06) received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2000 and 2003, respectively. He is currently working toward the Ph.D. degree in electrical engineering with Iowa State University, Ames, working in analog and mixed-signal design group.

His research interests include built-in self-test of embedded mixed-signal circuits, cost-effective testing methodologies, and design techniques.

Hanjun Jiang (S'01–M'07) received the B.E. degree in electronic engineering from Tsinghua University, Beijing, China, in 2001 and the Ph.D. degree in electrical engineering from Iowa State University, Ames, in 2005.

From July 2005 to December 2006, he was with Texas Instruments, Dallas. Afterward, he joined Tsinghua University, where he is currently an Assistant Researcher. He has been working on high-performance data converter design and built-in self-test, as well as integrated power management. His current research interest is in the area of low-power mixed-signal circuit design and system-level integration.

Degang Chen (S'90–M'92–SM'02) received the B.S. degree in instrumentation and automation from Tsinghua University, Beijing, China, in 1984 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 1988 and 1992, respectively.

From 1984 to 1986, he was with Beijing Institute of Control Engineering, Beijing, which is a space industry R&D institute. From March to August 1992, he was the John R. Pierce Instructor of electrical engineering with the California Institute of Technology, Pasadena. Afterward, he joined Iowa State University, Ames, where he is currently an Associate Professor with the Department of Electrical and Computer Engineering. He became an A. D. Welliver Faculty Fellow with the Boeing Company in the summer of 1999 and was with Dallas Semiconductor-Maxim in the summer of 2001. His research experience includes particulate contamination in microelectronic processing systems, vacuum robotics in microelectronics, adaptive and nonlinear control of electromechanical systems, and dynamics and control of atomic force microscopes. His current teaching and research interests are in the area of analog and mixed-signal VLSI integrated circuit design and testing. In particular, he is interested in low-cost high-accuracy test and built-in self-test of analog and mixed-signal and RF circuits, as well as in self-calibration and adaptive reconfiguration/repair strategies for enhancing the performance and yield of such circuits.

Dr. Chen was the recipient of the Best Paper Award at the 1990 IEEE Conference on Decision and Control and the Best Transaction Paper Award from the *ASME Journal of Dynamic Systems, Measurement, and Control* in 1995.

Randall L. Geiger (S'75–M'77–SM'82–F'90) received the B.S. degree in electrical engineering and the M.S. degree in mathematics from the University of Nebraska, Lincoln, in 1972 and 1973, respectively, and the Ph.D. degree in electrical engineering from Colorado State University, Fort Collins, in 1977.

He was a member of the faculty with the Department of Electrical Engineering, Texas A&M University, College Station, from 1977 to 1990. Since 1991, he has been a member of the faculty with the Department of Electrical and Computer Engineering, Iowa State University, Ames, where he is currently the Willard and Leitha Richardson Professor. His teaching and research interests are in the fields of analog and mixed-signal VLSI design, specifically in the areas of amplifier design, test, and built-in self-test of mixed signal circuits, data converter design, device modeling, and design for yield.

Dr. Geiger is a past member of the Board of Governors, a past Vice President of Publications, and a past President of the IEEE Circuits and Systems Society. He was an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II and the Circuits and Systems Society Editor for the *IEEE Circuits and Devices Magazine*. He was a member of the IEEE Publications Board and the IEEE Periodicals Council and is a past Chair of the Transactions Committee of the Periodicals Council. He has served in various capacities on the Technical Program Committees and the Organizing Committees for the IEEE International Symposium on Circuits and Systems and the IEEE Midwest Symposium on Circuits and Systems. He was the recipient of the Meritorious Service Award from the IEEE Circuits and Systems Society in 1996, the Golden Jubilee Medal from the IEEE Circuits and Systems Society in 2000, and the IEEE Millennium Medal in 2000.