High ResolutionCross Strip Anodes for Photon Counting detectors

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Cross Strip Anode Configuration

Cross strip readout is a multilayer anode with ~0.5mm period strip sets in orthogonal directions. This is comparable to cross delay line anodes, however without the delay line, Instead each strip is connected to an amplifier.

Cross strip is a multi-layer cross finger layout.

Fingers have ~0.5mm period on ceramic.

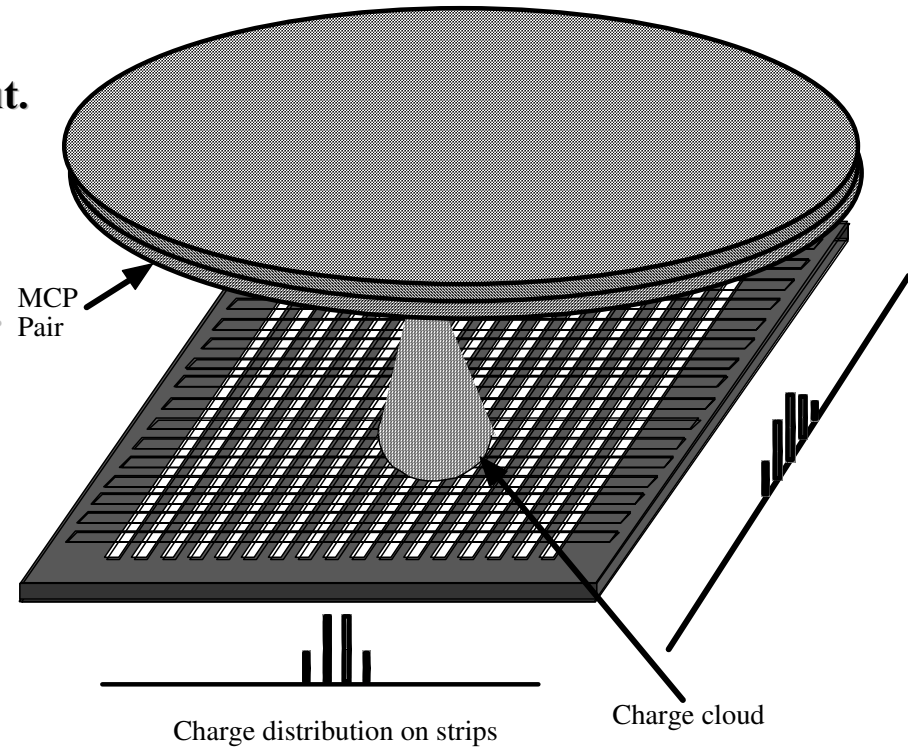
Charge spread over 5 strips per axis,

Event position derived from charge centroid.

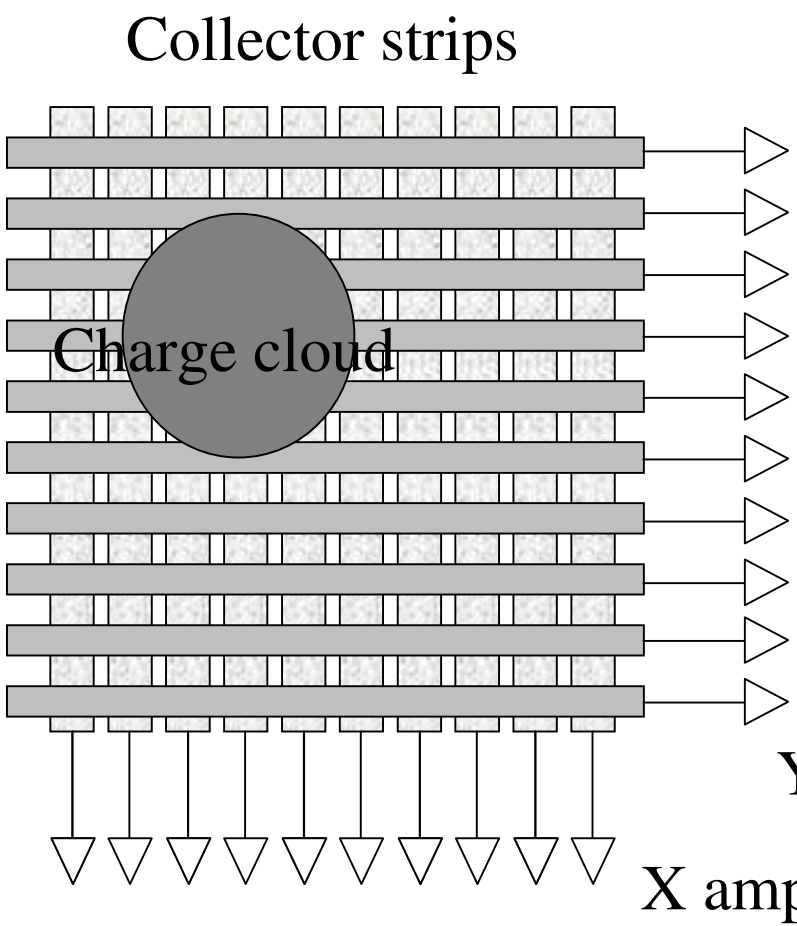
Can encode multiple simultaneous events.

Fast event propagation (few ns).

Compact and robust (900°C).



High ResolutionCross Strip Anodes



Fingers have ~0.5mm period on ceramic.

Charge spread over 5 strips per axis

Lower strips are exposed 50%

Upper strips cover other 50%

Connect amps to each strip

Use ASIC multi amplifier chips

Cross Strip Anode Configuration

Initial 8 x 8 mm test XS anode

0.5mm period, all metal/ceramic
Onboard wire-bonded preamplifier chips.
External amp, digitization and software centroid

Cross Strip Scheme Characteristics

- Low MCP gain (few x 10^6)
- Resolutions <10µm FWHM
- Linear images (few µm nonlinearity)
- Compact & robust (900°C capable)
- Very fast signal propagation (- 1ns)

Future potential advances

- Large formats >50mm possible
- Small, low power ASIC encoding
- High event rates (>1 MHz)
- Multiple simultaneous event capable

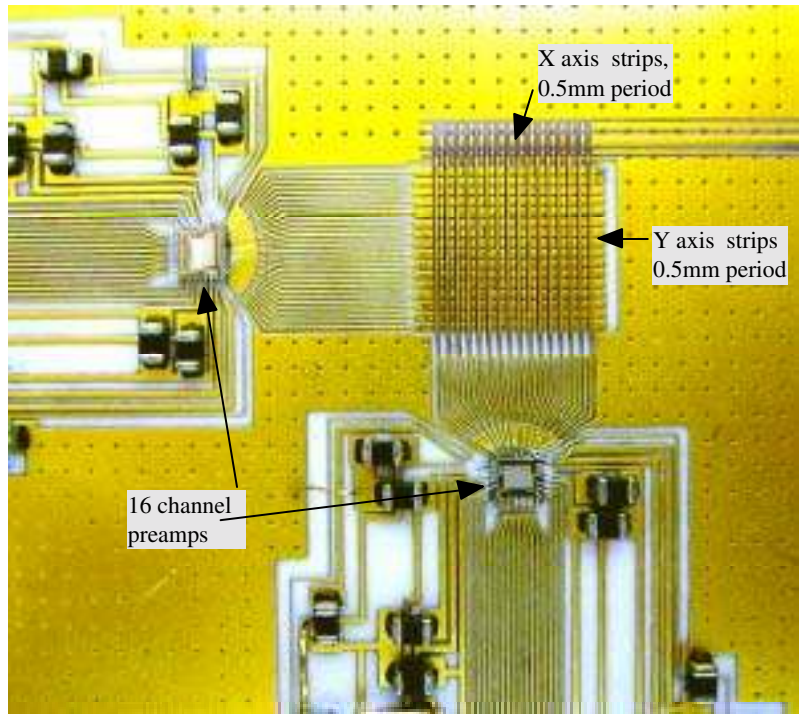
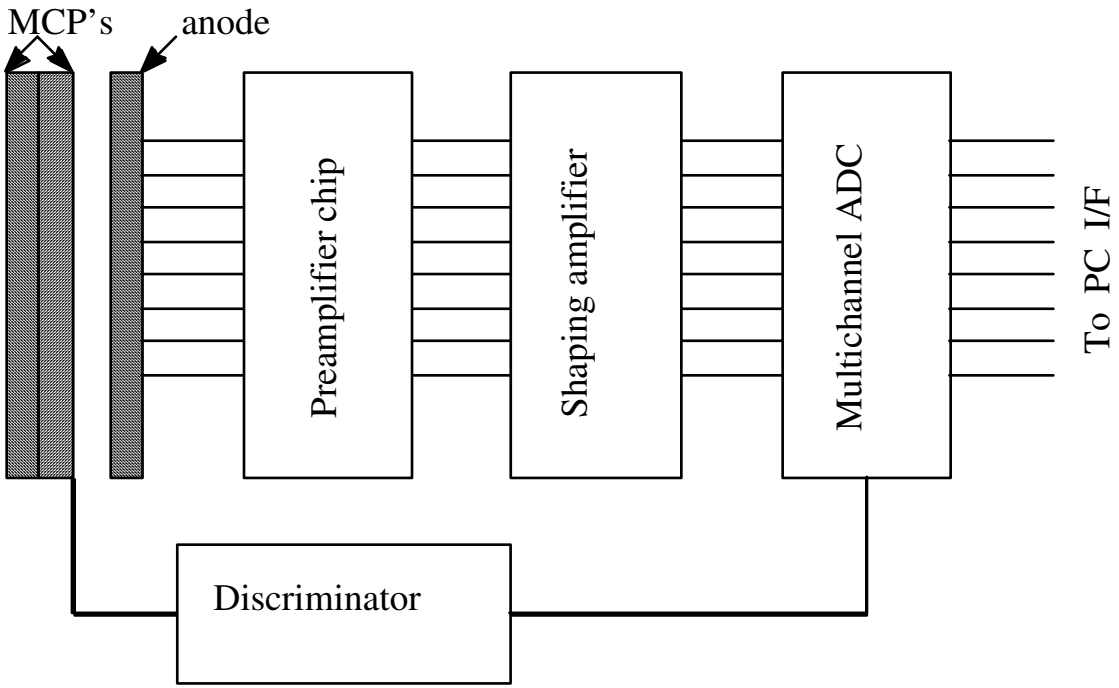
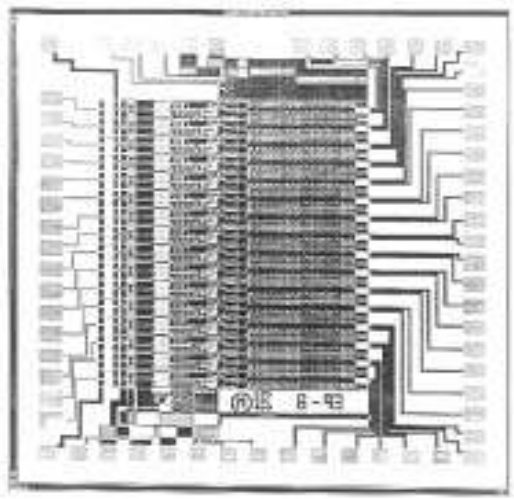


Photo of the 8 x 8mm test XS anode with its wire-bonded preamplifier chips.

Cross Strip Anode Electronics Chain

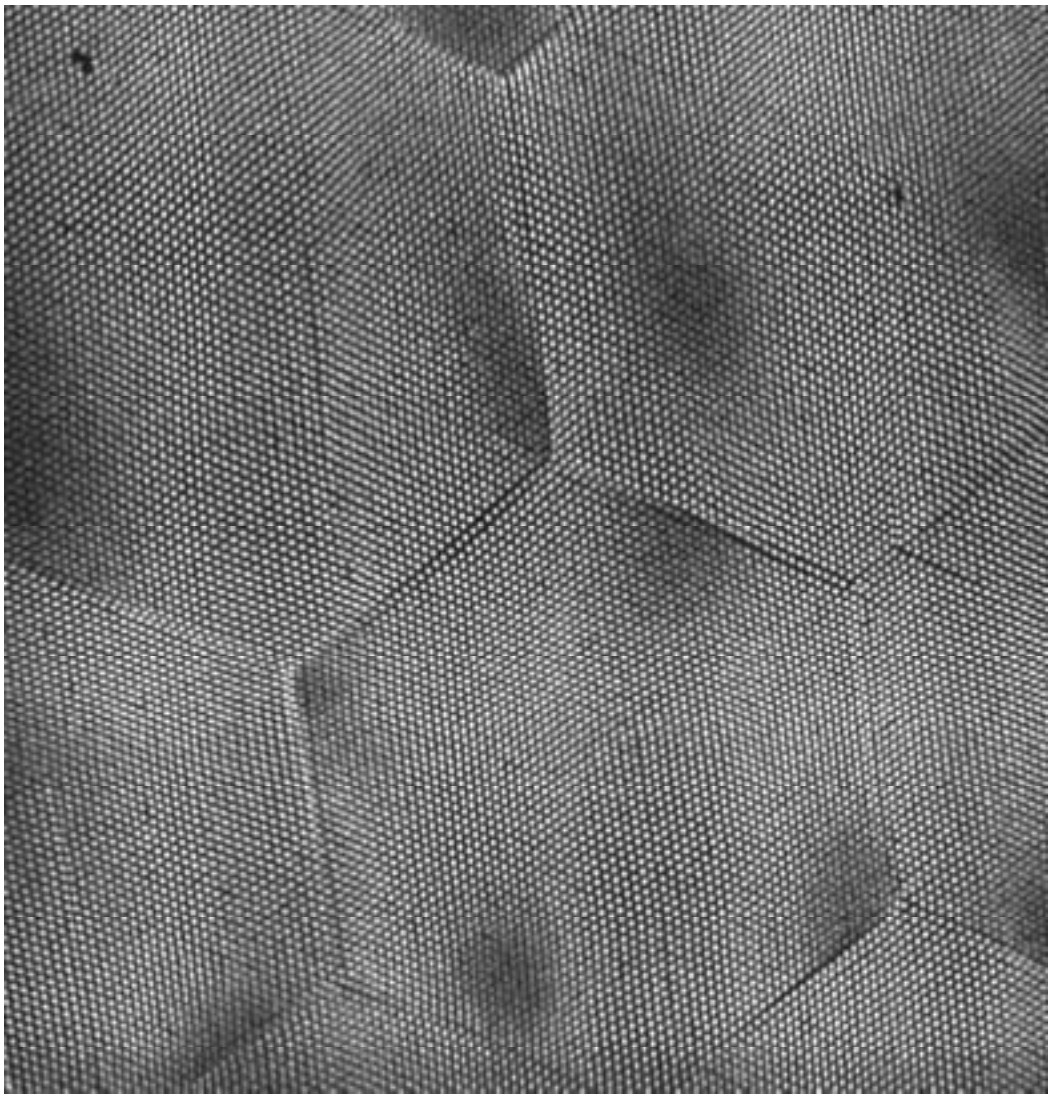


Schematic of the cross strip anode position encoding electronics test-bed system.
All signals amplified and digitized. Choose up to 12 bits per signal. Slow ADC's (10μs per digitization) using standard lab electronics, but sufficient for evaluation tests and flexible to select & diagnose parameter dependence.



ICD-2 preamplifier (16 ch) chip design that is being used for the current tests on the XS. ~1500e- rms noise, <20ns output, 10mW/ch.

Initial Images with 12µm MCP Pair and Cross Strip Anode



2 x 2 mm area imaged by cross strip anode. 12µm pore MCP's in a back to back pair with ~5 x 10^6 gain. Shows MCP multi-fiber modulation, dead pores, pore misalignments, and Moire beat modulation between the MCP's.

12µm MCP Detector Image Resolution

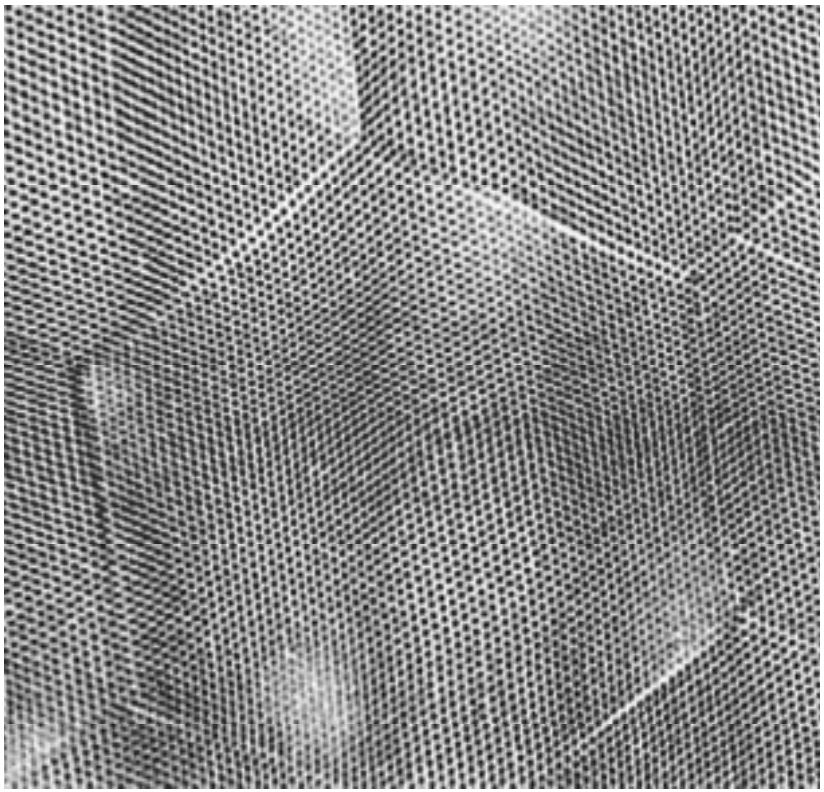
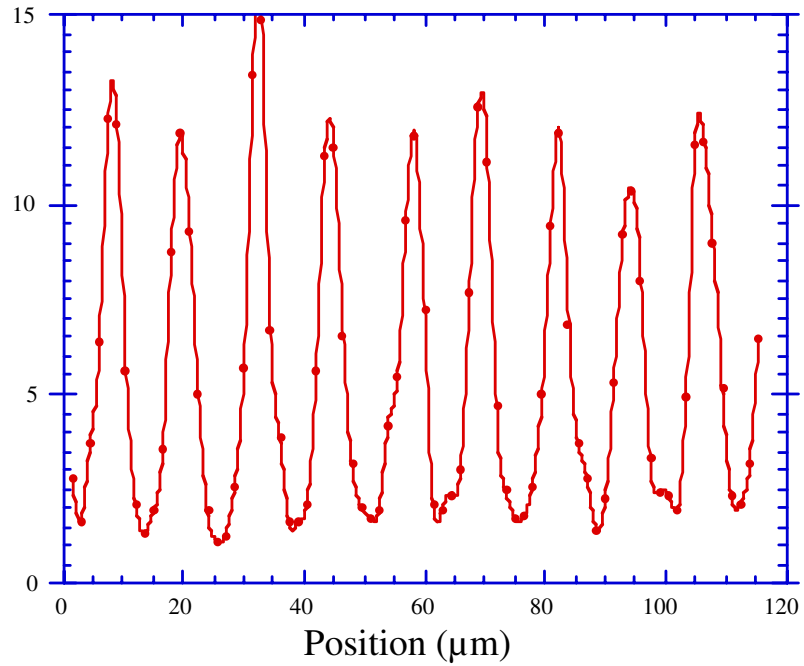


Image section of a 12µm pore MCP pair obtained at 5 x 10^6 gain with the XS anode.



An image histogram slice of the 12µm pore MCP image showing the significant level of modulation.

10µm MCP Detector Image Resolution

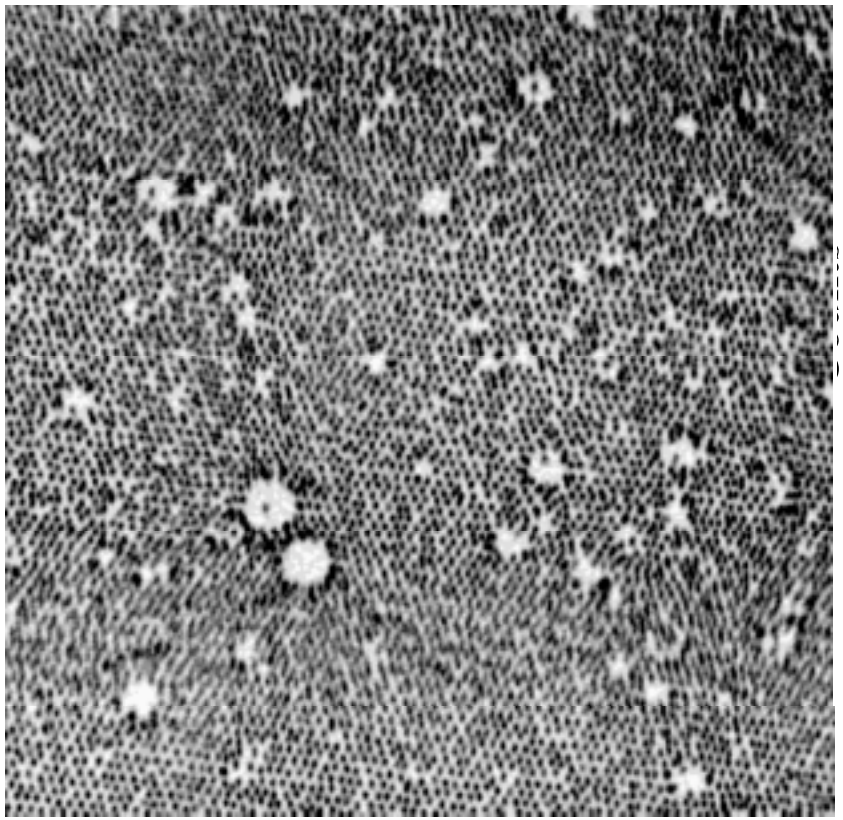


Image detail of a 10µm pore MCP pair obtained at 2 x 10^6 gain with the XS anode shows the defective MCP material.

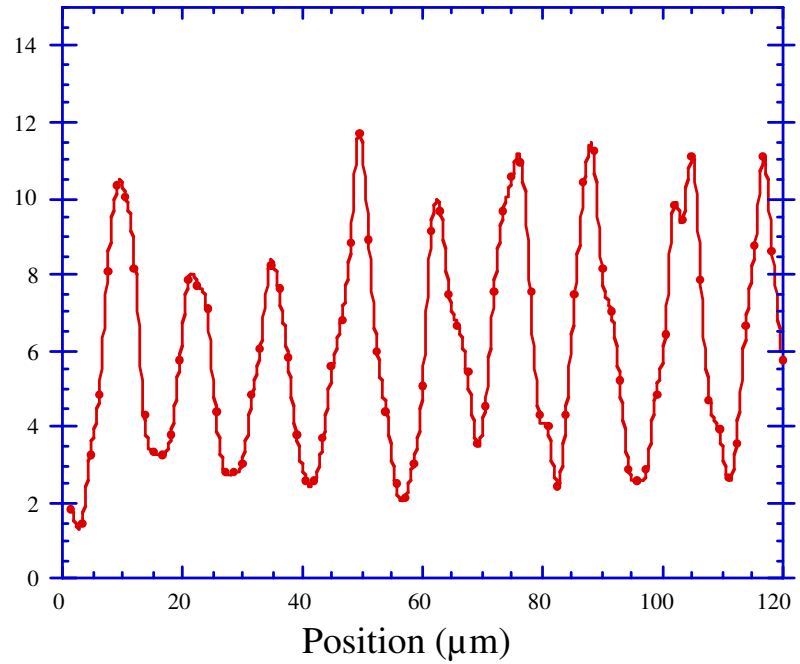
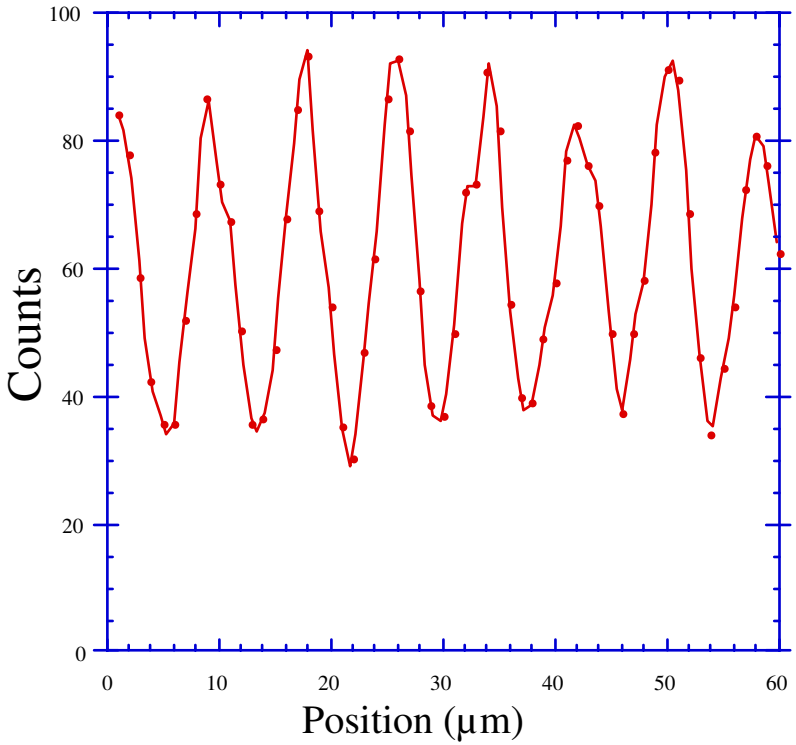
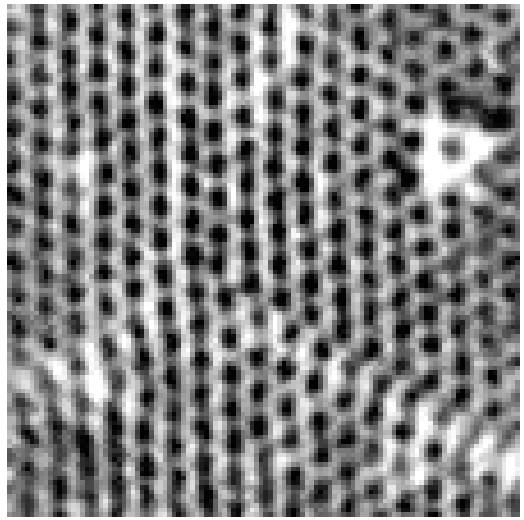


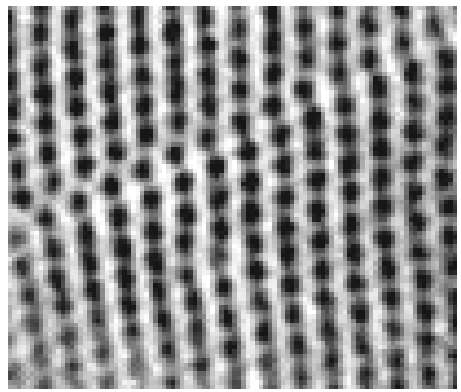
Image histogram slice of the 10µm pore MCP image showing the significant level of modulation.

7µm MCP Detector Image Resolution



Histogram in X of the 7µm pore MCP image at 2 x 10^6 gain showing a few µm resolution.

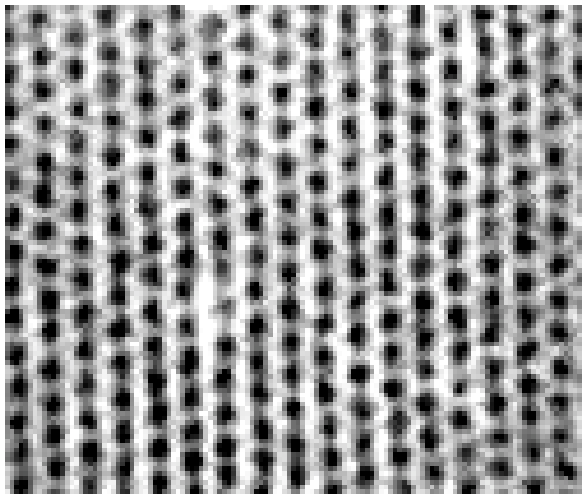


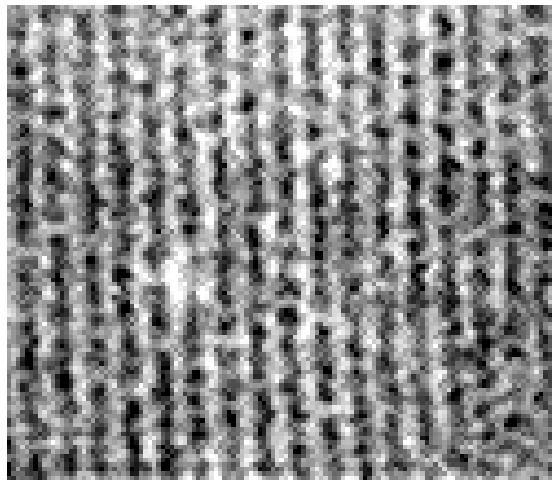


Images of the 7µm pore MCP pair at 2 x 10^6 gain showing multifiber boundaries and misaligned pores

7µm MCP Detector Image Resolution

12 bits





9 bits

10 bits

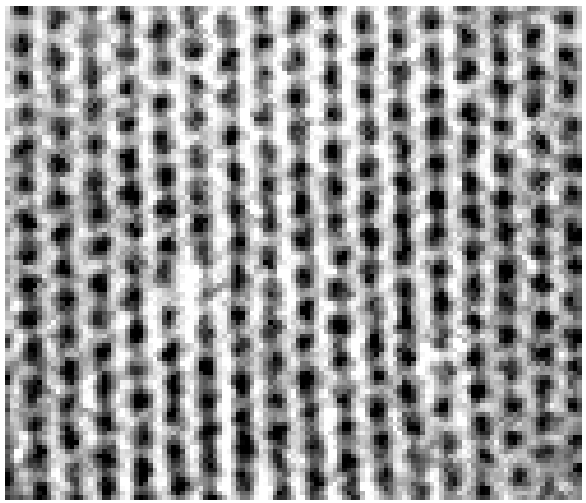
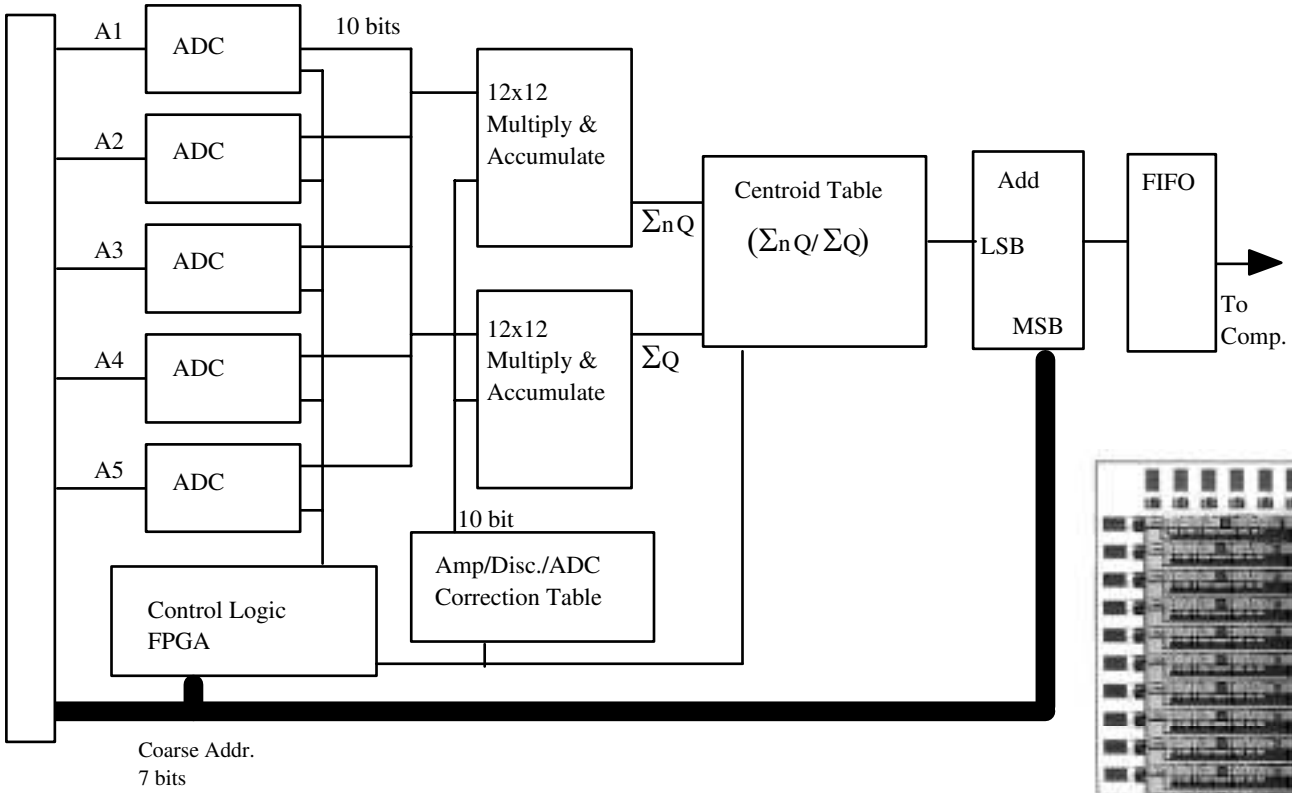
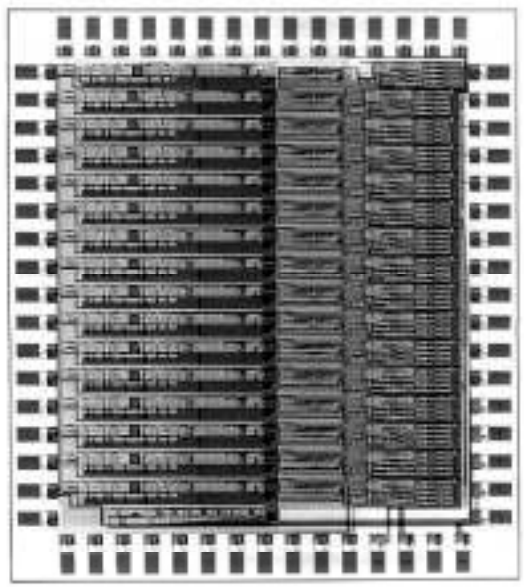


Image section of a 7µm MCP pair taken with the XS anode at different values of the signal digitization accuracy showing that the resolution does not degrade until 9 bits is reached.

Encoding Electronics Development Scheme





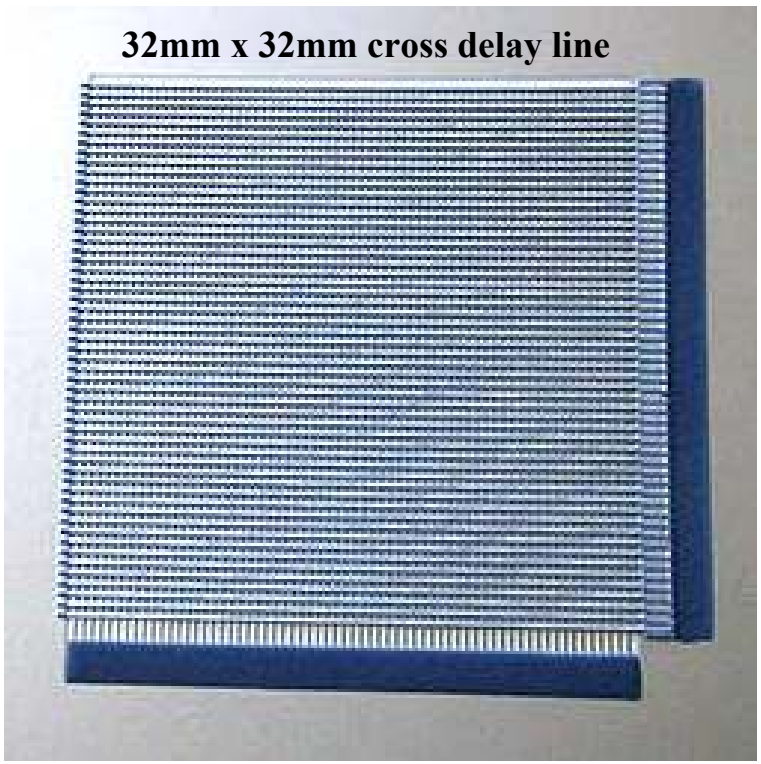
High speed hardware electronics chain downstream electronics can be implemented in standard modules
Overall processing speed should support >10MHz rates

15 in /5 out, second generation amplifier design

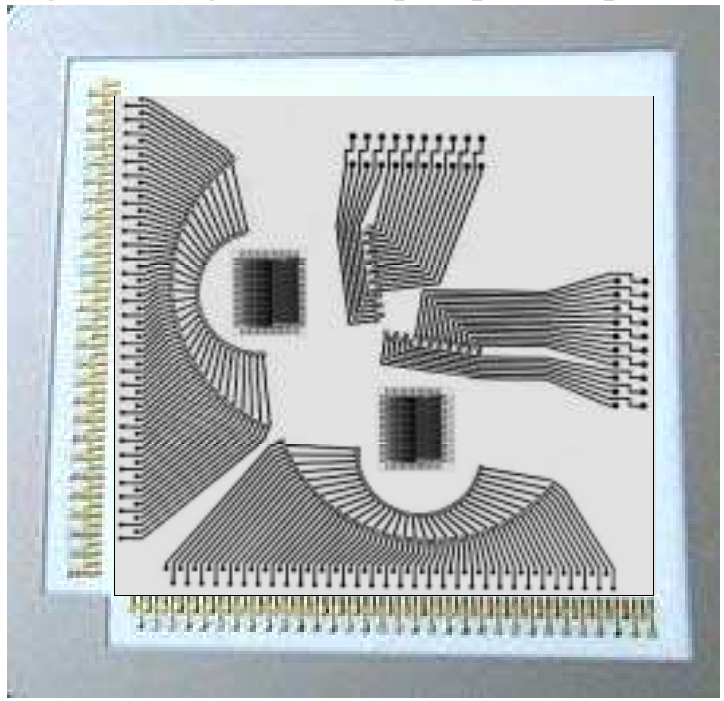
Integrated Cross Strip Anode Design

Anodes up to 32 x 32mm have been made
Signals are routed to anode backside by hermetic vias
Packaging can be compact with amp on anode backside
Anodes can be sealed to tube package with all electronics external

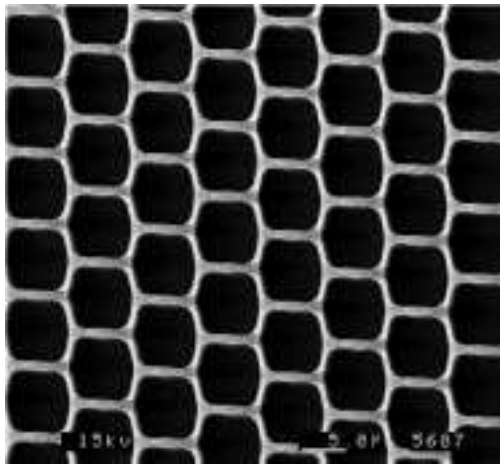
32mm x 32mm cross delay line



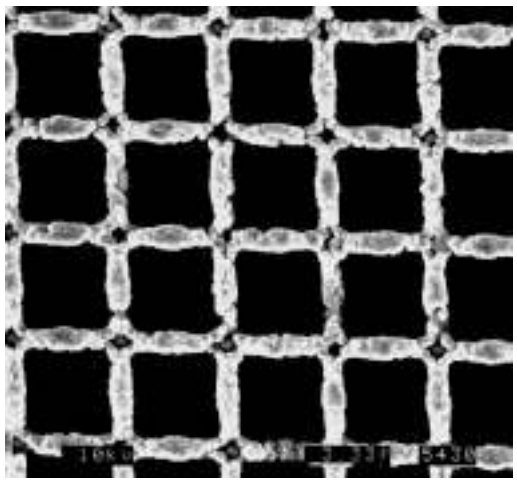
32mm x 32mm XS anode backside & proposed design showing fan-in, amp chip, & outputs



Small Pore and Silicon MCP Developments



Hexagonal pore Si MCP with ~7µm pores, >75% open area



Diamond coated Si MCP

Small pore MCP's are now available (5 -6 µm)

- Better spatial resolution - Faster response times
- Tight PHD at low gain - Lower background
- Now available in >100 x 50mm formats

Silicon MCP's

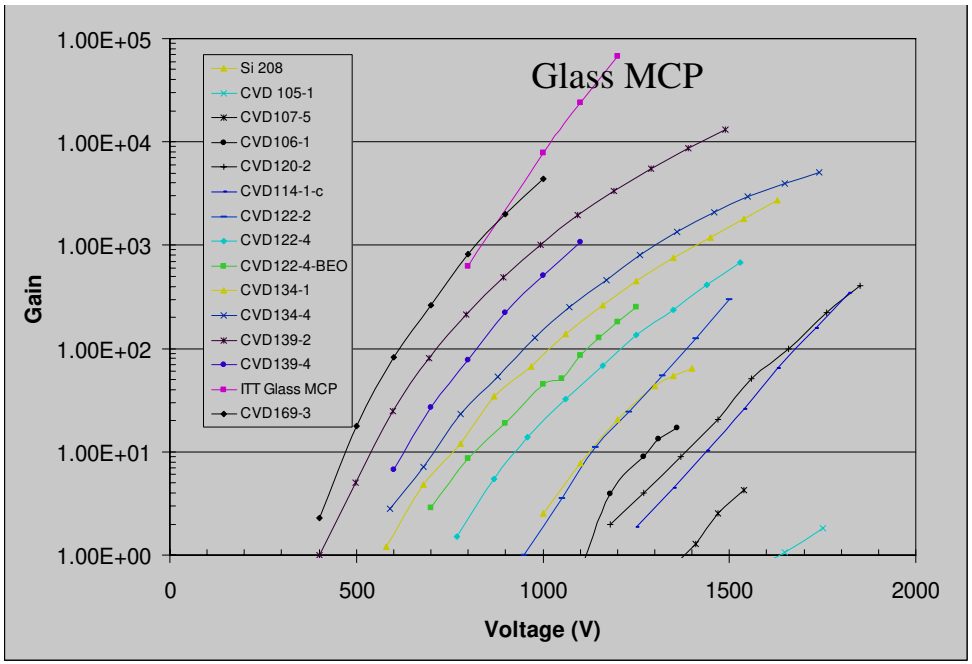
Silicon MCP's are made by photo-lithographic methods
Photolithographic etch process - very uniform pore pattern
No multifiber boundaries and array distortions of glass MCP's
Scalable to large substrate sizes (200mm) with small pores (5µm)
High temperature tolerance - CVD and "hot" processes OK
UHV compatible, low background (No radioactivity)
In collaboration with Nanosciences.

Silicon microchannel plates in test program

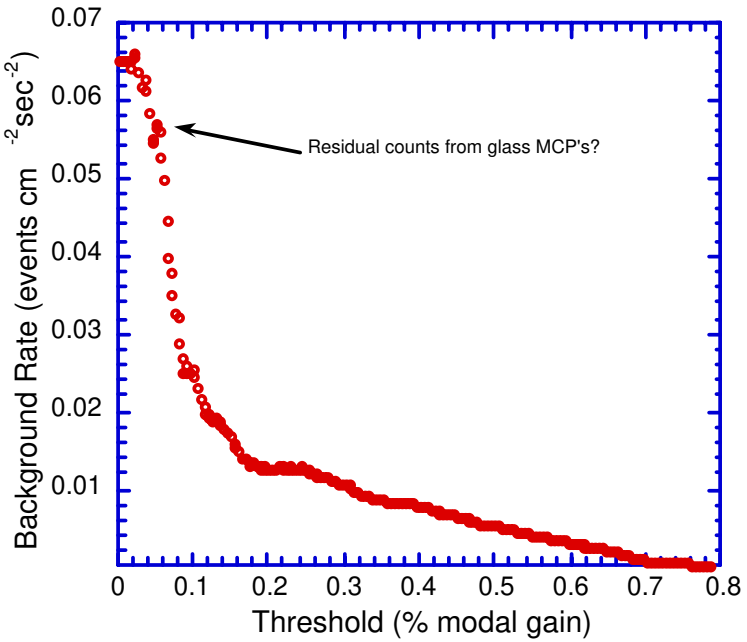
25mm diameter (75mm currently feasible)
40:1 L/D (>100:1 possible)
7µm pore size, hexagonal and square pore
~2° bias and 8°bias, resistances ~GΩ, to <100MΩ possible

Silicon MCP Performance Characteristics

- Many Si MCP's of 25mm diameter with ~7µm pores have been tested
- The performance is improving as production is being refined.
- Gain, quantum detection efficiency and pulse height are now very similar to glass MCP's
- Open area ratio is up to >75% for hexagonal pores
- The background rate is lower (0.02 events cm^{-2} sec^{-1}) than normal or low background glass
- CVD/MBE deposition of high temperature cathodes possible (Diamond made & measured)



Gain evolution of single Si MCP's

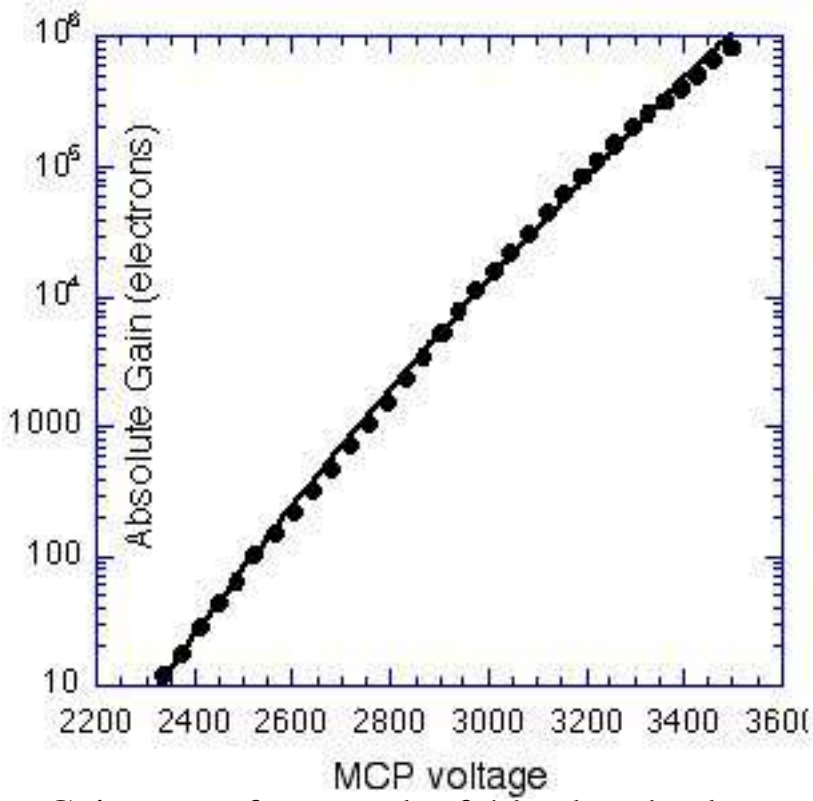


Si MCP background rate as a function of gain threshold.

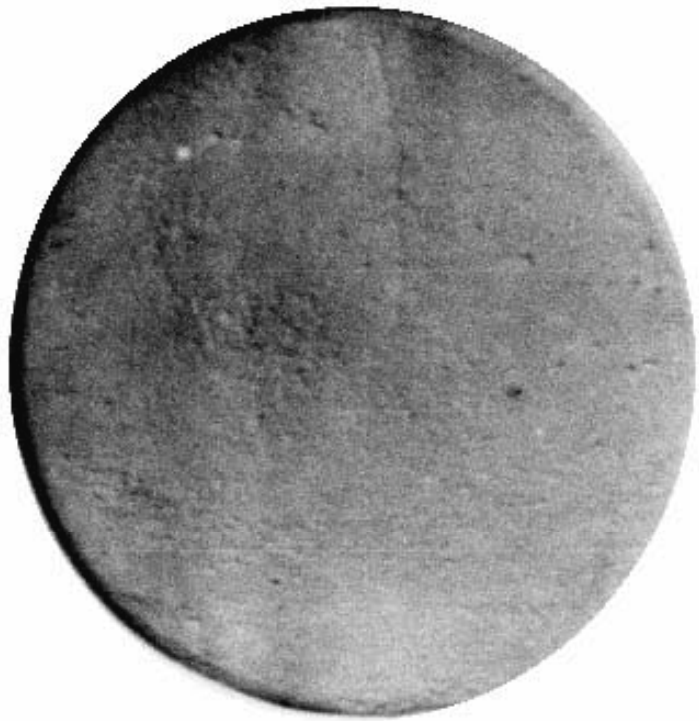
Silicon MCP Performance Characteristics

Gain and response uniformity are reasonably good.

- *We have tested the first stacks of Si MCP's (4) with gain up to 10^6*
- *Scrubbing of Si MCP's shows a tendency for the gain to increase!*
- *Si MCP's lack of any periodic modulation in the flat field images but do show evidence of defects*



Gain curve for a stack of 4 back to back Si MCP's with 6µm pores and 40:1 L/D.



An image of the fixed pattern response to a Hg vapor lamp with a stack of 4 Si MCP's. ~14mm area, 10^7 counts, ~50µm resolution XDL.

Cross Strip Readout Status Summary

- ~7µm pores are being resolved, <3µm electronic resolution
  3cm = 10k x 10k = 100 x 10^6 pixels!!!
  $1/pixel = $100 x 10^6 (ARISAKA!), will take $0.01/pixel, $$10^6$ bids!
- Image linearity is ~1µm level and shows pore misalignments
- Gain required is ~2 x 10^6, allows higher local event rates
- Lower gain means longer overall lifetime
- Packaging can be compact with amp on anode
- 32mm anode format implemented, test with Si MCP's soon

- **<u>Development Plan</u>**

- Fabrication of amp/disc/sparse chips
- Integrate downstream electronics into small package
- Power requirement of ~2W for 30mm readout
- High counting rates of 5MHz feasible
- Develop 40mm+ anode formats