Analog Integr Circ Sig Process (2012) 72:531–539
DOI 10.1007/s10470-011-9752-0

High-resolution multi-bit second-order incremental converter with 1.5-μV residual offset and 94-dB SFDR

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Received: 16 December 2010 / Revised: 21 July 2011 / Accepted: 10 August 2011 / Published online: 21 August 2011

Abstract This paper describes an incremental converter based on a second order ΣΔ modulator. The scheme uses a 3-bit DAC with inherent linearity, an optimal reset of integrators, and gives rise to an effective offset cancellation with a novel technique based on single or double chopping. The circuit, fabricated in a mixed 0.18-0.6 μm CMOS technology, obtains 1.5-μV residual offset with $2V_{PP}$ fully differential range. The measured resolution is 19 bit obtained with 512 clock periods.

Keywords CMOS analog integrated circuits · Sigma–delta modulation · Analog-to-digital conversion

1 Introduction

Incremental converters are used for low conversion rate and high resolution. The typical application is for sensors and instrumentations that require low offset and high dynamic range, [1]. Having a large number of bit in the incremental converter relaxes the gain requirement of the operational amplifier (op-amp), but makes more important the request of having very low offset in the data converter. Obviously, more bits in the quantizer require more power. However, the benefit of a lower swing and relaxed requirements of the op-amp performances, as shown in the following, well compensates for the power cost. An incremental converter has the same scheme of a ΣΔ modulator, but it uses a sampled and held input for the entire conversion cycle. The equivalent number of bit of an incremental converter depends on the order of the modulator, the number of bits used in the quantizer, the digital post processing and the number of clock cycles. High resolution demands for high order modulator. However, when the order of the modulator is higher than two, the stability requirement limits the effectiveness of the architecture. Supposing to use a single-bit quantizer and, as post processing, the cascade of a number of accumulators equal to the order of the scheme, with N clock cycles, the converter achieves $\log_2 N$ bit for a first order, $\log_2(N(N-1))$ for a second order, and $\log_2(\alpha N(N-1)(N-2))$ for a third order, where α can be as low as 1/32, [2]. Therefore, the benefit of a third order scheme is significantly reduced. Common incremental converter implementations use single-bit quantizer, which ensures intrinsic linearity, because mismatch between unity elements in multi-bit solutions would cause non-linearity that can not be adequately fixed by dynamic elements matching (DEM) techniques, normally used in ΣΔ modulators, [3]. Nevertheless, multi-bit solutions would be very attractive because they grant a substantial reduction of the conversion time. For instance, a 3-bit second-order modulator achieves 18 (20) bit of resolution with 256 (512) clock periods instead of 724 (1448) required by the single-bit counterpart.

This paper obtains 19 bit and virtually zero offset using a second order incremental scheme with $N = 512$. Three main innovations favour the result. They are: the use of a 3-bit quantizer with inherent linearity, an optimal reset of the integrators to avoid a major error at the first clock period, a single or double chopping that cancels the offset.

The paper is organized as follows. Sect. 2 describes conventional solutions and their features while Sect. 3

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presents and discusses the techniques used in this design. Sect. 4 and 5 give circuital details and measurement results, respectively. Finally, Sect. 4 draws some conclusion.

2 Conventional architectures and features

An incremental converter is a ΣΔ modulator with initial reset of integrators. For high order architectures, it is necessary to use single stage schemes because MASH solutions, studied in [4] for single-bit stages, are not able to generate the analog quantization error with enough precision and require calibration for inter-stage gain mismatch correction. Moreover, the mismatch between unity elements prevents the use of multi-bit quantizers. The use of single-bit quantizer in ΣΔ modulators grants an intrinsic linearity, but brings a number of drawbacks. Firstly, the input of the first integrator is wide as well as the output swing of integrators. This is because the quantization error is half of the converter reference voltage, V_{Ref}. The latter problem is fixed by a suitable choice of the supply voltage, V_{DD}, and V_{Ref}. In order to avoid op-amps saturation, V_{Ref} is a small fraction of V_{DD}. More important is the large signal at the input differential stages that causes slewing. The issue is analysed referring to the scheme of Fig. 1, a single-bit second order incremental converter with input feed-forward. The injecting network is made by an input switched capacitor that injects its signal on the first integrator. Immediately after the switching of Φ_1, capacitors C_1, C_2, and C_3 (the equivalent amplifier output capacitance) determine the input differential voltage, V_{d}. It is $V_{\mathrm{d}} = V_{\mathrm{in}} \times C_1/(C_1 + C_{\mathrm{eq}})$, where C_{eq} is the series connection of C_2 and C_3 in parallel with C_8. For large values of V_{in}, V_{d} can become larger than $\sqrt{2}V_{\mathrm{ov}}$, the overdrive voltage of the input pair. Therefore, the input stage of the op-amp fully unbalances. This leads the op-amp in the slew-rate mode. However, increasing the bias current does not help because even if the slew-rate improves, the full unbalance is difficult to avoid because it depends on the overdrive voltage of the input pair. This is critical for the linearity and requires a large number of time constants to ensure that the non linear error does not affect the output voltage. On the contrary, when the differential input is small, the feedback always controls the output waveform that becomes exponential or a combination of exponentials thus determining an error at the end of the injection period that is proportional to the input and that can be seen as a gain error.

3 Employed circuit techniques

This design uses a 3-bit quantizer to benefit the multiple advantages granted by the multi-bit solution. Among them, the significant reduction of the input of the first integrator reduces the jumps of V_{d} and keeps the op-amp out of the slewing conditions. The output range of the op-amp of the first stage is minimal. The overall resolution increases or, alternatively, the number of needed clock periods diminishes. As known, the critical block is the DAC feeding back the modulator output signal to the first integrator input. Since conventional DEM techniques are not effective in compensating for mismatch between unity elements in multi-bit DAC of an incremental converter, this design uses, as discussed shortly, an intrinsically linear solution.

3.1 Intrinsically linear DAC

A 3-bit switched capacitor (SC) DAC uses eight nominally equal unity capacitances, $C_{\mathrm{u}} = C_1 = 8$, pre-charged to the positive or negative reference under the control of a

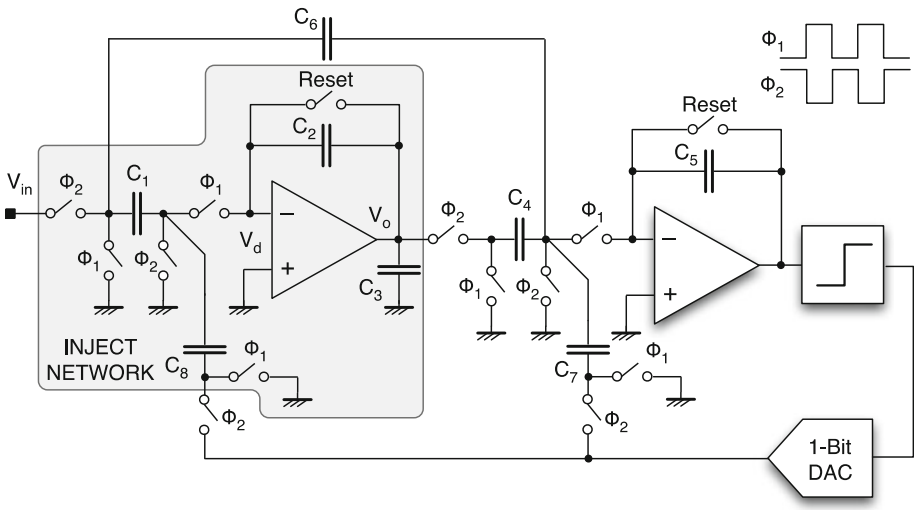

Fig. 1 Single-bit second order incremental converter scheme

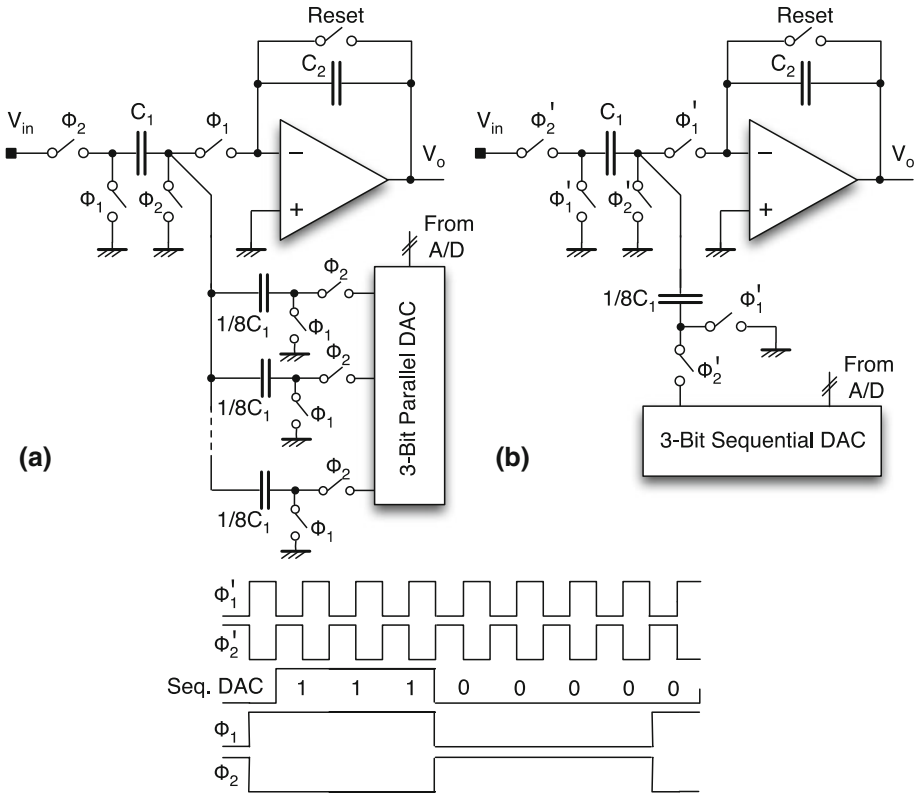

Fig. 2 (**a**) Parallel DAC; (**b**) sequential 3-bit DAC and its phases

thermometric digital code (Fig. 2(a)). This design uses only one switched capacitor unity capacitance that runs at eight times the switching frequency. The control of the DAC is also eight times faster and produces, sequentially, the output voltage according to the input code. This operation is shown in Fig. 2 for converting 3/8. Since each injection is the same because the converter uses the same capacitor, the DAC is intrinsically linear. The same fast SC scheme is used for the input signal, as shown in the block diagram of Fig. 3(a). Notice that a conventional 3-bit DAC made by 8 unity elements, that would give rise to lower power consumption, can not be used because of the elements mismatch.

The use of a faster clock seems, at a first glance, a penalty. However, this method, together with the use of a 3-bit quantizer, avoids slewing error in the op-amp, thus improving linearity performance. The problem can be studied considering only the differential input pair, made of two n-channel MOS transistors, M_1 and M_2, fed by a current source, I_{SS}. It is the main source of non-linearity for large differential input signals. With balanced input and transistors in saturation region, the currents flowing through M_1 and M_2 are given by $I_1 = I_2 = K(V_{ov0})^2$, being $K = \mu_n C_{ox}(W/L)/2$ and $V_{ov0} = V_{GS0} - V_{th}$. When a differential input is applied, currents I_1 and I_2 become

$$I_1 = K\left(V_{OV} - \frac{V_{in}}{2}\right)^2 \tag{1}$$

$$I_2 = K\left(V_{OV} + \frac{V_{in}}{2}\right)^2 \tag{2}$$

and holds

$$I_1 - I_2 = I_{SS} = 2KV_{OV0}^2 \tag{3}$$

Combining the above expressions, the overdrive voltage results

$$V_{OV} = \sqrt{V_{OV0}^2 - \left(\frac{V_{in}}{2}\right)^2} \tag{4}$$

Equations 1, 2, and 4 give rise to the circuit differential output current. Figure 4 shows a typical result for $I_{SS} = 1$ mA and different values of V_{ov0}, namely 0.15, 0.25, and 0.35 V.

The non-linear response denotes non-linearity in the operation of the amplifier in Fig. 5, a conventional switched-capacitor integrator. As already mentioned, when using the conventional single-bit approach and ±1 V references, the large value of the input signal can make the amplifier input differential voltage close or higher than $\sqrt{2}V_{ov}$. This brings the amplifier in the non-linear region or even in slew-rate mode. The use of the non-linear transconductance gain in a behavioural model of the circuit of Fig. 5 determines a non-linear transient after the beginning of phase 1 in response to a constant input V_{in}. At the end of phase 1, the voltage does not reach the final value giving rise to an error like the one of Fig. 6. The simulation uses

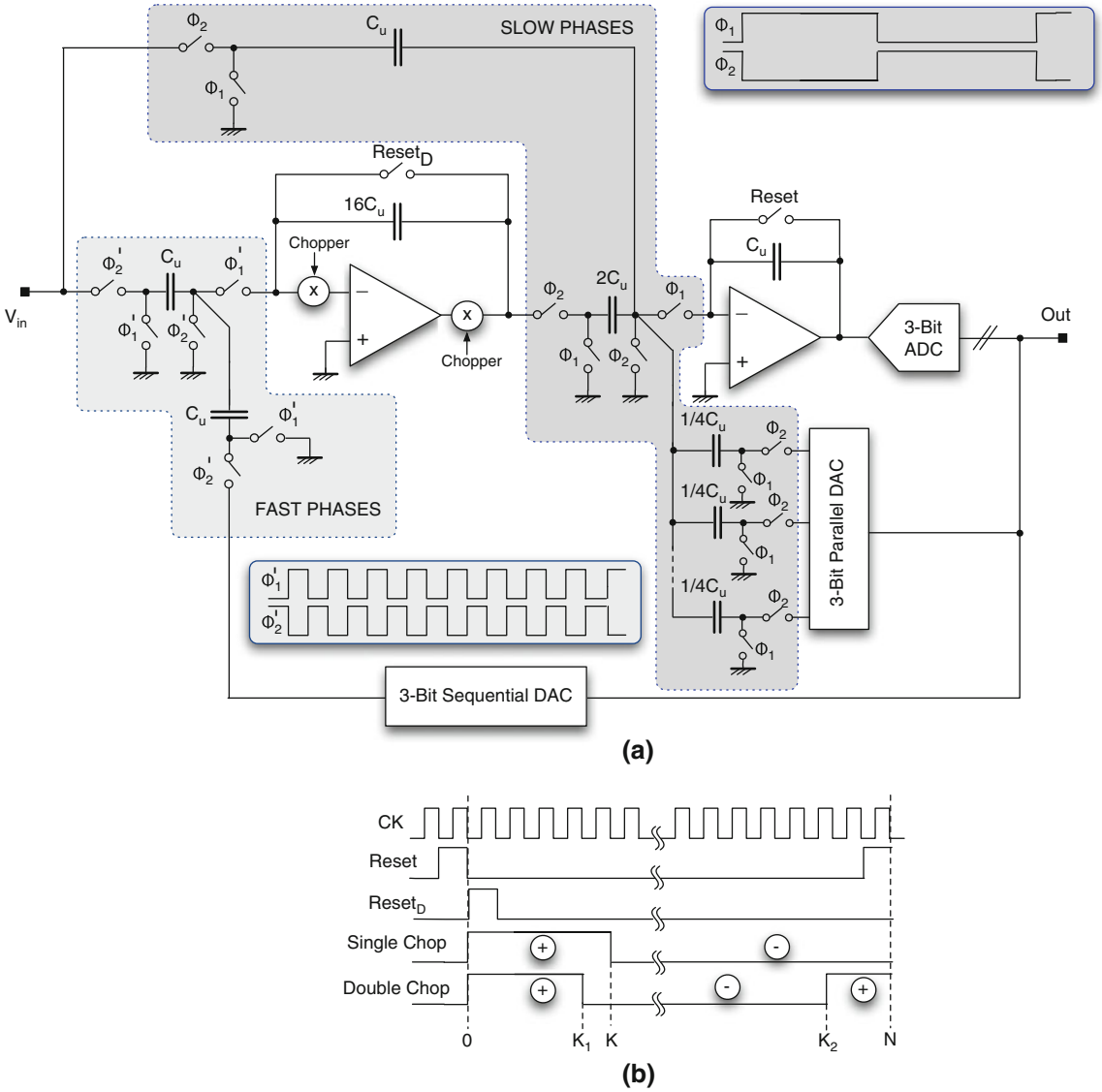

Fig. 3 Detailed block diagram of the proposed scheme (**a**) and control phases (**b**)

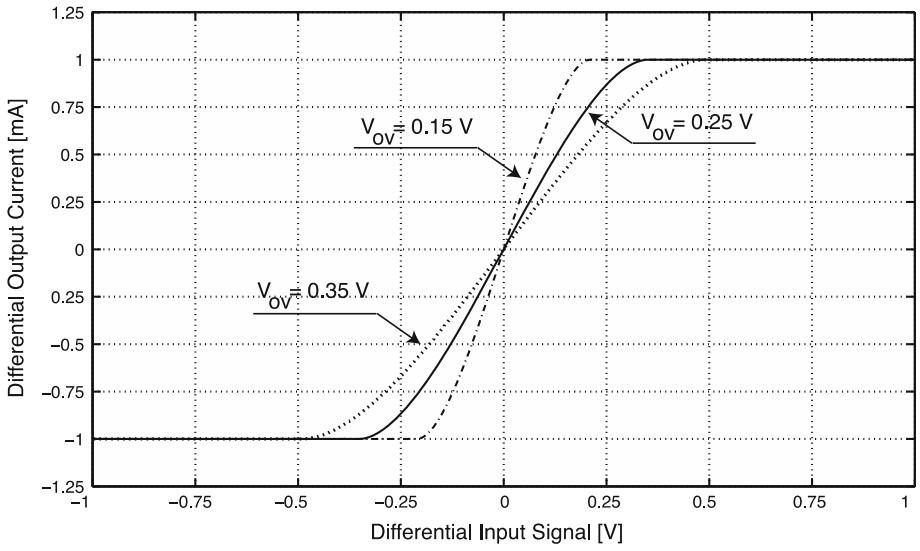

Fig. 4 Differential output current as a function of the differential input signal

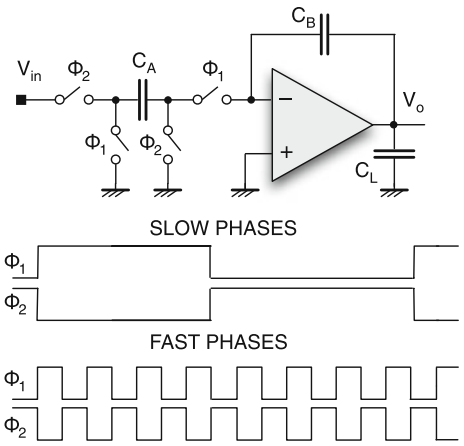

Fig. 5 Switched-capacitor integrator

$I_{SS} = 1$ mA, $V_{ov0} = 0.35$ V, $C_A = C_B = C$, and $C_L = C/2$. Moreover, $5T_{CK}/2 = g_m/C$. Figure 6 shows that the non-linearity of the response significantly increases at low overdrive. The very large error even with $V_{ov0} = 0.35$ V recommends using much higher currents to enable ± 1 V of input range.

Figure 7 shows the error with 3-bit quantizer that reduces by eight the input swing and a consequent faster control phases that decrease the integration time to $T_{CK}/8$. Moreover, the injecting capacitance becomes smaller by a factor of eight. The smaller input signal keeps the amplifier out of the slewing condition and the operation in a mild non-linear region results in an error at the end of every fast injection strongly reduced. Figure 7 shows an error lower by about three orders of magnitude. Therefore, since multi-

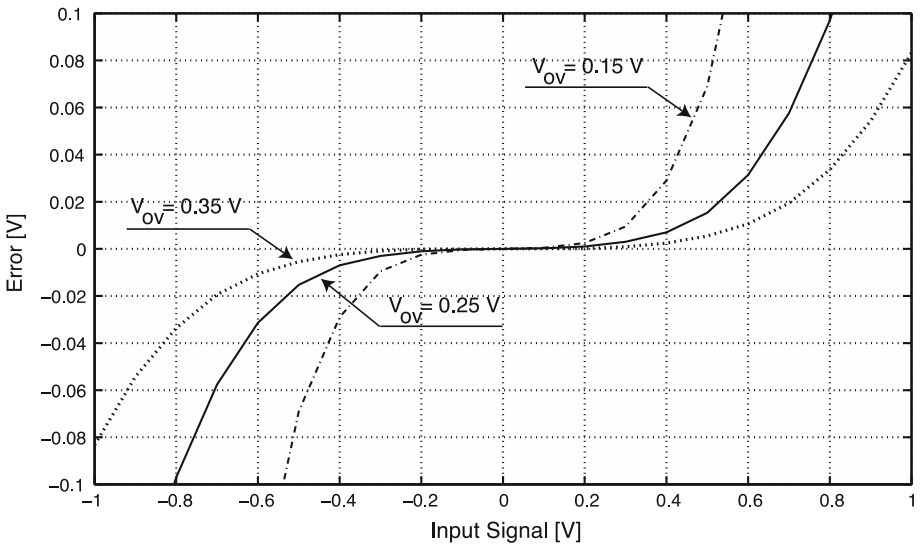

Fig. 6 Simulated error as a function of the input signal (single-bit case)

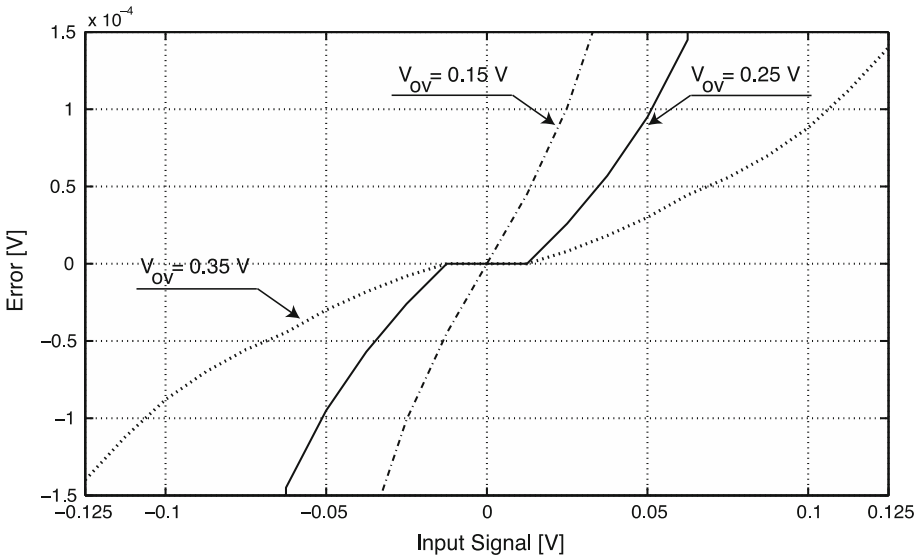

Fig. 7 Simulated error as a function of the input signal (3-bit case)

bit conversion requires 8 consecutive injections, the final error is expected lower by more than one order of magnitude.

3.2 Optimal reset

In incremental converters, any error assumes different weight depending at which time it has been injected along the conversion. In particular, in a second-order modulator, if an error is injected at the first clock period, the first integrator stores it for the entire conversion cycle. Therefore, the second integrator amplifies it by $(N-1)$ times. An eventual other error injected at the second clock cycle is accumulated $(N-2)$ times and so forth. A multi-bit quantizer generates a replica close to the input by half LSB. Since the input signal and its quantization are subtracted at the input of the first integrator, the result is a small fraction of the full scale. This is true when the feedback is established; i.e., after the second clock period, because in the first clock period the control of the DAC is zero. Unfortunately, as mentioned above, the weight of errors at the beginning of the conversion is maximum. Therefore, the slewing error at the first clock period must be avoided. This design achieves the result by keeping the reset of the first integrator during the first clock period. The capacitor used for the input feed-forward injects the input signal in the second integrator, allowing the first 3-bit quantization. Therefore, in the next clock period, the feedback on the first integrator is established and the reset can be removed, as detailed in the phases scheme of Fig. 3(b), [5].

3.3 Offset nulling

A relevant feature of this design is its capability to null the offset. The method is applied to the first integrator, but can be used in the second integrator as well, if needed. The cancellation accounts for the post processing used. This design cancels the offset supposing that the post processing is the cascade of two delayed accumulators. However, the extension of the technique to a cascade of three integrators is straightforward. A possible offset nulling technique uses a chopper [6] on the first op-amp controlled by a fractal sequence, as described in [7]. That method obtains the result under some constrains on the number of clock periods.

In this design, the offset cancellation is achieved with a single step chopping or, to obtain a better accuracy, with two chopping steps. Offset, V_{os}, is equivalent to a DC input signal. Its effect at the output of the two post processing accumulators is $V_{os}N(N-1)/2$ that, divided by the full scale amplitude $N(N-1)/2$, obtains the input offset. A single chopping after K clock cycles, as shown in Fig. 3(b), reverses the offset for the remaining $R=(N-K)$ clock periods. Therefore, the output contributions of the offset before chopping and its one reverse after chopping sum into

$$\frac{V_{OS}}{2}[K(K-1)+2K(R-1)-(R-1)(R-2)]; \qquad (5)$$

therefore, suitable values of N and K obtain a minimum of the multiplying coefficient in 5. It may happen that, for a given number of clock periods, N, the corresponding K can obtain an unsatisfactory residual offset. A better figure is obtained by a second chopping (see Fig. 3(b)) that generates a further positive term in 5 suitable to trim the zeroing operation. In real circuits, in addition to the input referred offset that is reversed by chopping, there are small terms that give rise to an offset in front of the chopper. They can be cancelled out by a foreground calibration that sets the value of K (or K_1 and K_2).

4 Circuit design

The design of the fully differential version of the scheme in Fig. 3(a) has been realized by a mixed 0.18–0.6 μm double-poly six metal layers CMOS technology. An SC structure running at $8f_{CK}$ ($f_{CK}=1$ MHz) has the purpose to sample the input voltage and injects its charge synchronously with the high speed sequential DAC (Fig. 2(b)). The DAC of the second stage is a normal parallel architecture with thermometric control (Fig. 2(a)). The effects of the mismatch between unity elements of the second DAC, referred to the input divided by $(N-1)$, is negligible. The second integrator and the relative DAC, with eight capacitances, use the slow clock.

The 3-bit flash uses eight simple latched comparators. The operational amplifiers are conventional telescopic cascode capable to reach a 120-dB gain and 24-MHz and 18-MHz GBW for the first and the second integrator, respectively. The low ratio of GBW and clock frequency just causes an incomplete injection $(1-e^{-t_S/\tau})$. This, since $t_s=6\tau$, is a linear error affecting the integrator gain much lower than the one caused by the capacitor mismatch. The $1/f$ op-amp noise is assumed to fade below the sampling frequency, and then its contribution is cancelled together with the offset by chopper technique.

The chosen value of the sampling capacitances is $C_u=C_{in}=C_{DAC}=1.6$ pF. In each fast clock period, the injected square noise charge is 4 kTC_{in}. After a complete slow clock period, the noise charge, injected eight times on the 16 C_u of the first integrator, gives rise to an input referred noise voltage $v^2_{n,in}=kT/(2C_u)$, sharing a benefit

of the average over eight fast clock periods. If the noise enters at clock period K, its square contribution is amplified at the output by $(N-K-1)^2$. Therefore, the quadratic superposition of all the noise injections becomes $V^2_{\mathrm{n,out}} = MkT/(2C_{\mathrm{u}})$, where

$$M = \sum_{i=1}^{N-1} i^2 = \frac{(N-1)^3}{3} + \frac{(N-1)^2}{2} + \frac{(N-1)}{6} \qquad (6)$$

that is input referred by dividing it by the square of the processor gain $G = N(N-1)/2$

$$V^2_{\mathrm{n,in}} = \frac{kT}{2C_{\mathrm{in}}} \times \frac{M}{G^2}. \qquad (7)$$

Expression 7, with $N = 512$, gives $V_{\mathrm{n,in}} = 2.3$ μV. Therefore, the use of a ±2 V peak-to-peak differential full scale voltage would enable about 124-dB SNR.

5 Measurement results

Figure 8 depicts the chip microphotograph. It shows, in transparency, the layout and the two integrators, the 3-bit quantizer, and the phase generators outlined. To avoid interferences, a shield of metal six almost covers the active area. The chip area, including pads, is 1,550 × 1,550 μm^2. Input and output chopping of the first op-amp can be controlled either internally, after a pre-defined number of clock periods, or externally to emulate a possible foreground calibration and to enable double chopping. The output is the 3-bit signal generated by the flash. The digital data processing is done externally to the chip. The nominal supply voltage is 3.3 V. With $N = 512$, the 3-bit granted by the quantizer leads to 1,046,528 quantization steps equivalent to about 20 bit.

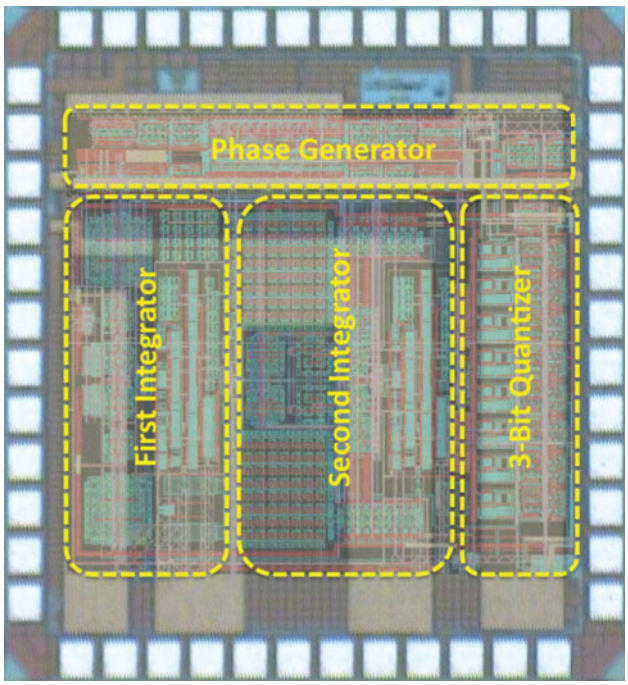

Fig. 8 Chip microphotograph with key blocks outlined

Figure 9 shows the output counts of the first and second accumulator of the post processing without chopping. The final count value of the second integrator denotes −4042 LSB offset, corresponding to the −3.9 mV offset of one of the 40 samples available. The use of a single chopping at the clock period # 150 reduces that offset to 18.4 μV. A double chopping solution allows further reducing the residual offset below 2 μV, with first and second chop at the clock periods # 128 and # 384, respectively.

As shortly mentioned in the Sect. 3, a possible foreground calibration can optimize the chopping timing in order to account for possible offset contribution in front of the chopper itself.

Figure 10 shows the output counts of the first and second accumulator of the post processing when a not chopped offset of 1.95 mV is intentionally added at the converter input. Notice that, chopping at the clock periods # 65 and # 455 removes the offset.

Figure 11 gives the histogram of 255 repeated measures with shorted inputs. It measures the input referred noise whose variance is 4.13 μV, resulting in 19.9 bit of resolution. Thanks to a double chopping, the residual offset is −1.5 μV.

Figure 12 shows the measured output spectrum of a 283-Hz sine wave and virtually zero DC component obtained with 1,024 points. Second, third, fourth, and fifth harmonics are at −94, −99, −117, and −120 dB$_c$, respectively. The SNDR is 116 dB and the SFDR is 94 dB. The non-optimized power consumption is 6 mW.

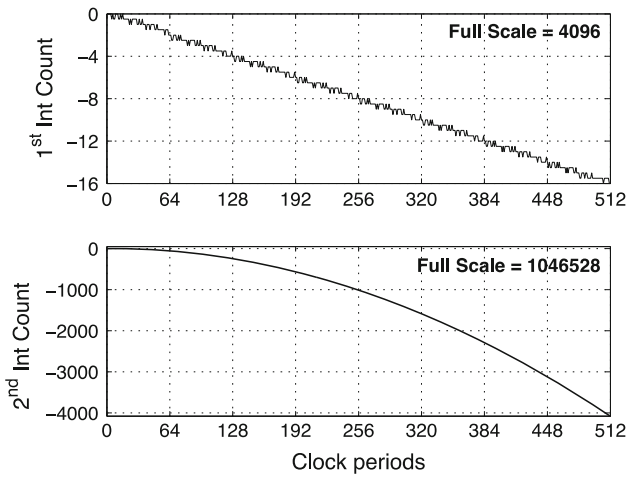

Fig. 9 First (*top*) and second (*bottom*) integrator count with no chopping

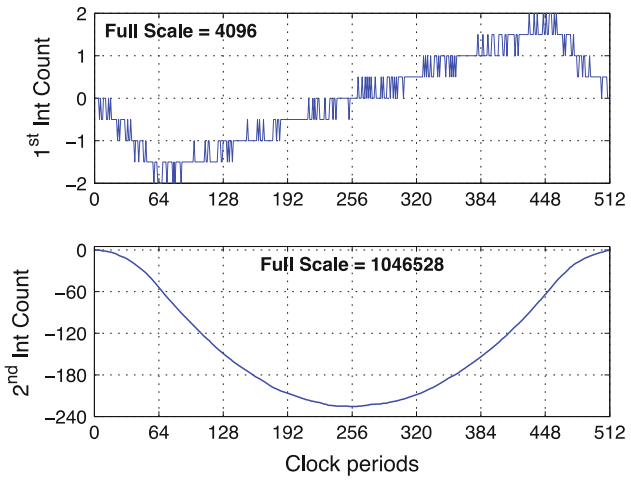

Fig. 10 First (*top*) and second (*bottom*) integrator count with double chopping

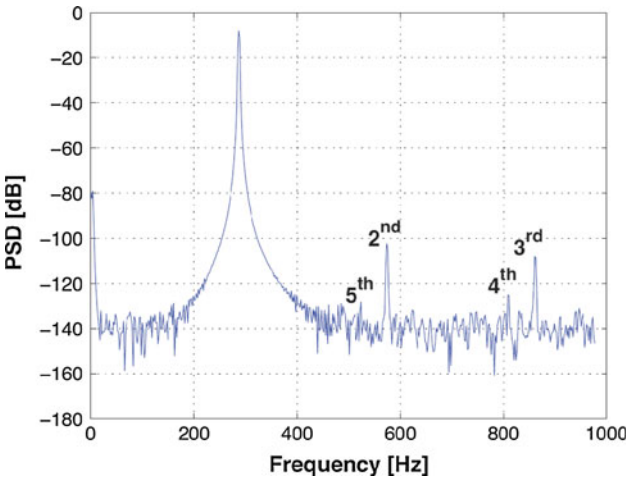

Fig. 12 Measured output spectrum. FFT obtained with 1,024 points. Conversion periods = 512, f_N = 976.5 Hz

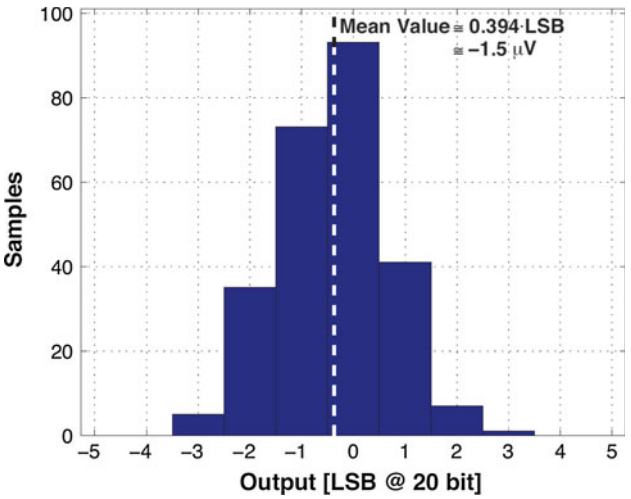

Fig. 11 Obtained distribution with converter short circuited inputs

6 Conclusion

In this paper a multi-bit incremental converter, fabricated in a mixed 0.18–0.6 μm CMOS technology, featuring 19 bit of resolution with 512 clock periods and achieving 1.5-μV residual offset is presented. The purpose of this work was to reduce the number of clock periods necessary to achieve a defined resolution without increasing the order of the modulator and to cancel the offset in an effective way. For the first goal we proposed and implemented the use of 3-bit quantizer together with an intrinsically linear feedback DAC. The cancellation of the offset benefits a single step or double step chopping method. The technique overcomes the limits of a conventional chopping strategy that is not suitable for Nyquist rate oversampled algorithm and avoids complex switching sequences. Experimental results fully demonstrate the effectiveness of all the proposed techniques.

Acknowledgments The authors wish to thank Aldo Peña Perez of the Integrated Microsystems Laboratory, University of Pavia, for his help and National Semiconductors for chip fabrication. This study is partially funded by FIRB, Italian National Program, Project RBAP06L4S5.

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