High-Resolution Stamp Fabrication by Edge Lithography

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HIGH-RESOLUTION STAMP FABRICATION BY EDGE LITHOGRAPHY

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Chapter 1

Introduction

Nanoimprint lithography is a lithographic technology that promises high throughput patterning of nanostructures. Replicas of the pattern with high resolution is achieved by mechanical deformation of imprint polymers independent of light diffractions or beam scattering of other lithographic tools. The research described in this thesis focuses on the fabrication of high resolution stamp for thermal nanoimprint lithography (T-NIL) applications.

Nanoridges are fabricated by edge lithography and micromachining techniques. Conventional UV lithography is employed for pattern definition instead of high resolution lithography methods. The creation of nano-sized patterns is accomplished by edge lithography, which by definition means converting the edges of the original pattern into the feature of the final pattern. In this chapter, an introduction will be given concerning the development of nanoimprint lithography with the emphasis of stamp fabrication. The origination and development of edge lithography for creating nanostructures in Si are demonstrated. We will give an overview of the widely used micromachining technologies that have been applied in fabricating NIL stamps. The chapter ends with the objectives and outline of the thesis.

1.1 Nanoimprint lithography

Nanofabrication is the process aiming at fabricating arbitrary shaped patterns with a dimension $\leq$100 nm. The primary drive for the development of nanofabrication is the requirement of ever-shrinking IC devices dimensions, which relies primarily on the improvement of lithographic techniques. In addition to conventional UV photolithography,

which has a highest resolution of 2 μm, high resolution lithographic techniques have been developed to meet the requirement. These techniques include, for example, deep ultraviolet lithography (DUV), X-ray lithography, electron beam lithography (EBL), focused ion beam (FIB), etc. At present, the high resolution lithography techniques are generally suffering from problems such as high cost, low throughput and limited access. To circumvent the dependence on high resolution lithographic technologies, researches have been investigating alternative routes for fabricating nanostructures. These techniques, to name a few, include nanoimprint lithography, soft lithography, scanning-probe-based techniques, and dip-pen lithography.

Nanoimprint lithography (NIL) is a lithographic technology that promises high throughput. Thermal NIL (T-NIL) was first developed by Chou's group in the 1990s [1]. As a variant, step-and-flash imprint lithography (S-FIL), which was developed by Wilson's group, uses a transparent stamp and UV curable monomer to complete the imprint [2]. The schematics of T-NIL and S-FIL are shown in Figure 1.1. In T-NIL, a substrate made of hard material with nanostructures is used as the stamp. Before imprint, the stamp is treated with an anti-adhesion layer to assist demolding. A substrate is cleaned and coated with imprint polymer. Then the stamp is brought into contact with the substrate. The imprint process is performed at a elevated temperature and pressure for a certain amount of time. Then the stamp is separated from the substrate after lowering the temperature and releasing the pressure. A reversed pattern from that in the stamp is replicated in the imprint polymer. In the last step, the residual layer in the imprint polymer can be directionally removed by reactive ion etching (RIE). From here on, the imprinted substrate is ready for further process. In S-FIL, the substrate is first coated with an organic pattern transfer layer, then a surface treated, transparent stamp is brought close and aligned to the coated substrate. Once in proximity, a drop of UV curable monomer is introduced into the gap between the stamp and substrate. The gap is closed when the stamp contacts the coated organic transfer layer. Then the assembly is irradiated by UV light to cure the monomer, which leaves the substrate with a solidified reverse replica of the stamp on the substrate. The pattern can be successively transferred from the monomer to the organic transfer layer with the help of RIE. The difference between T-NIL and S-FIL is that T-NIL normally asks for high temperature and pressure while S-FIL is performed at room temperature and low pressure up to 1 bar.

Figure 1.2 is the earliest example made by Chou *et al.* showing NIL being able to faithfully transfer features from the stamp into imprint polymer [1]. It shows that T-NIL is a high throughput and low cost process, easy to handle and requires simple process equipment. Although there is still challenges existing for the perfection of the technology

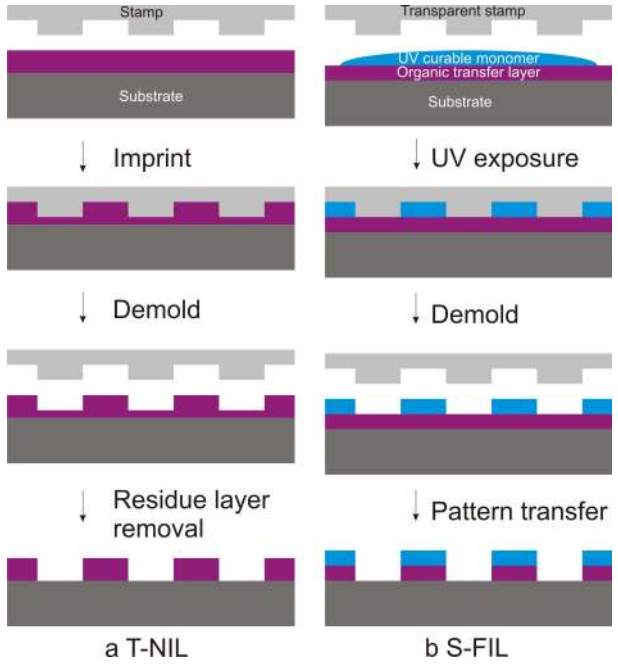

Figure 1.1: Schematics: (a) T-NIL; (b) S-FIL

itself, it is potentially interesting and found to be useful in various applications, such as electronics, optical, photonic, and biological fields.

The best performance of NIL is normally co-determined by many factors such as stamp quality, physical and chemical properties of imprint polymers, imprint conditions (pressure, temperature, and duration), etc [3, 4, 5]. Amongst them, stamp fabrication and polymer issues are the main factors influencing the performance of T-NIL. The stamp used for T-NIL is normally made of hard materials, such as Si, SiO_2, metals (e.g. nickel). The hard materials promise retaining the nanostructure properties, such as shape and aspect ratio, during T-NIL under high temperature and pressure conditions. The imprint polymers used in T-NIL should be able to deform easily during the imprint process; and they should be able to retain the imprinted replica during the demolding process. Therefore, thermoplastic materials are explored as suitable imprint polymers for T-NIL applications. These thermoplastic materials have a glass transition temperature (T_g), above which the Young's modulus and the viscosity drop several orders of magnitude compared to those at room temperature. During T-NIL, the imprint temperature is chosen ca. 70-90°C above T_g such that the polymer reaches a viscous flow state. A pressure is applied when the

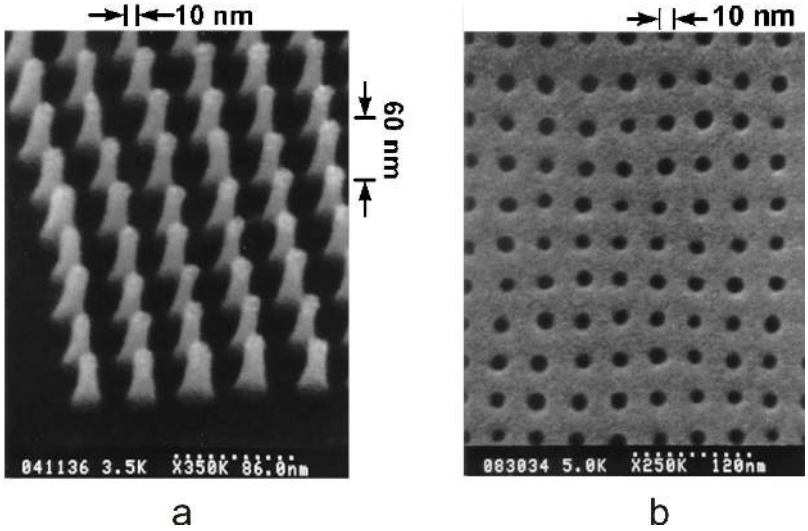

Figure 1.2: SEM images:(a) SiO_2 mold of pillars of minimum 10 nm diameter, 60 nm height and 40 nm period; (b) Imprint results in PMMA. Images are taken from [1].

required temperature is reached to assist polymer deformation. The demolding process is performed when the temperature is decreased lower than T_g to preserve the imprinted pattern.

As the focus of this thesis, in the following sections, a general review regarding the approaches and technologies for stamp fabrication for T-NIL applications is introduced followed by an overview of micromachining technologies employed for stamp fabrication in our research.

1.2 Stamp fabrication for thermal nanoimprint lithography applications

The fabrication of hard stamp with nanostructures for T-NIL applications requires the compatibility with conventional micromachining technologies. Lithographic techniques, therefore, constitutes the primary determination of feature resolution. Conventional UV photolithography has been widely and successfully applied in micromachining for pattern definition with minimum feature sizes of 2 μm. High resolution lithographic tools have been implemented and have been demonstrated being able to fabricate nanostructures with sub-200 nm dimensions successfully. For example, electron beam lithography is able

to fabricate nanostructures with sub-10 nm resolutions and laser interference lithography can create large-area periodic structures with feature size ca. 100-200 nm. Industry implemented the current state-of-art deep UV lithography tools which can achieve minimum feature size down to 50 nm. Extreme UV lithography is considered as the next generation lithography tools for mass production. The fabrication of nanostructures by means of high resolution lithographic tools is also referred to as conventional nanofabrication approaches. In addition to conventional nanofabrication approaches, researchers have been investigating stamp fabrication by means of unconventional nanofabrication approaches, in which nanofabrication proceeds via conventional UV photolithography with the integration of micromachining techniques. Many review papers have discussed examples of nanofabrication [6, 7]. In this section, an introduction to conventional nanofabrication approaches and unconventional nanofabrication approaches by edge lithography will be given.

1.2.1 Stamp fabrication by high resolution lithography techniques

Beam writing technologies

Beam writing technologies have the general operational principle in employing a focused beam scanning over a susceptible material surface. Electrons and ions are the energetic particles used in electron beam lithography (EBL) and focused ion beam (FIB) respectively. EBL has become a standard tool in generating nano-sized patterns with arbitrary shapes. In this technology, a focused electron beam is used to write directly onto a photoresist. PMMA is the most commonly used resist material in EBL, which is exposed by energetic electrons. The electrons include incident electrons, forward and backscattered electrons, and secondary electrons. The resolution obtained by EBL is primarily determined by the size of the beam. Other factors, such as scattering of electrons in the resist layer and generation of secondary electrons from the underlying substrate, also influence the resolution of this technology [8]. EBL writing has the advantage of creating arbitrary fine patterns but has the disadvantage of low throughput, which limits its application in the IC industry. To improve the throughput by EBL, it has also been implemented as projection printing systems, such as projection electron beam lithography (SCALPEL) and PREVAIL approaches [9]. Since the projection approaches generally suffer from difficulties such as mask fabrication and scan range enlargement, EBL writing systems have become the commonly used approach for pattern definition in the research field of nanofabrication. The highest resolution of EBL can be achieved by tuning the thickness of PMMA, electron beam energy and substrate materials. The results show that the

satisfactory line width resolution made in PMMA is 10 nm [8, 10, 11]. Microfabrication techniques, such as plasma etching and lift-off techniques, have been implemented with EBL to produce nanostructures [11, 12]. Furthermore, EBL has been used for create masks for electronics applications.

Focused ion beam takes advantage of an ion beam which has a higher energy than other particle beams. It is explored in a projection process known as focused ion beam lithography (FIBL) and a direct write process known as FIB milling (FIBM) [13].

Deep UV and extreme UV lithography

Although beam writing technologies have the advantage of generating arbitrarily shaped patterns with sub-10 nm resolutions, the slow processing speed limits its application in large volume production. Photolithography fulfills the purpose of mass production, however, optical diffraction prevents it from being useful in nano-sized pattern definition. Therefore, deep UV (DUV) lithography was developed by employing wavelength of 248 nm KrF and 193 nm ArF excimer lasers. Currently, feature size down to 50 nm is achieved by DUV lithography.

Extreme UV lithography (EUVL) was first proposed in 1988 [14] as one of the routes of next-generation lithography (NGL). A detailed review regarding origination and latest technological development of EUVL is given by the Wu *et al.* [15]. EUVL is regarded as a natural extension to optical lithography in the sense that EUVL uses masks with 4-5 fold reduction which is achievable by current micromachining technologies. Although a broad wavelength ranging from 5 nm to 50 nm is applicable to EUVL, 13.5 nm EUV is the current candidate corresponding to a Mo/Si multilayer reflective mirror. Although the wavelength in EUV is significantly shorter than that in conventional UV and DUV lithography, the resolution is co-determined by EUV source, resist matters and mask defects. As discussed in the review by Wu *et al.*, many challenges need to be overcome before EUVL cab be implemented for mass production [15].

1.2.2 Unconventional methods for stamp fabrication

The high resolution lithography techniques are commercially available and have been implemented in industry. However, their application in the research field is limited due to the high expenses and limited access. Therefore, researchers have been investigating alternatives, i.e. unconventional nanofabrication approaches. Gates *et al.* published a comprehensive review concerning the unconventional approaches to nanofabrication [6]. In general, unconventional nanofabrication can be achieved by either top-down or bottom-

up approaches. Bottom-up approaches use interactions between molecules or colloidal particles to assemble nanostructure in two or three dimensions. Top-down approaches employ conventional photolithography in combination with micromachining technologies to fabricate nanostructures. Edge lithography is one of the unconventional nanofabrication methods successfully utilized to create nanostructures in the top-down route. A general review regarding the development and application of edge lithography will be introduced in the following sections.

Edge lithography

Edge lithography can be defined as that the edge of the original pattern becomes the feature of the final pattern. In the 1970s, researchers had explored the use of edges for shadow deposition. Dean *et al.* fabricated a sub-micrometer self-aligned dual-gate GaAs FET using conventional photolithography and shadow deposition technique [16]. Later Jelk *et al.* fabricated 0.15 μm lines on glass substrates using shadow deposition and lift-off technology [17]. Flanders *et.al.* fabricated ca. 10 nm linewidth mask using isotropic Si etching in combination with shadow deposition technique [18].

The shadow deposition technique was further developed taking advantage of the edges of steps to fabricate 10 nm metal lines [19]. In this method, as shown in Figure 1.3, a metal layer was evaporated (or sputtered) under an angle over a topography with vertical sidewalls fabricated by X-ray lithography and RIE. Metal lines of 10 nm were created after removing the material on the top and the bottom of the topography by ion beam etching. Following a similar approach, Prober *et.al.* opted for fabricating 30 nm metal lines using shadow deposition and ion beam etching [20].

Flanders *et al.* further advanced the edge defined technique to double grating patterns [21]. The fabrication scheme is illustrated in Figure 1.4. The fabrication started from creating a SiO_2 parent grating pattern with vertical sidewalls by X-ray lithography, metal lift-off and RIE technologies. A layer of Si_3N_4 was deposited over the grating pattern. Then the Si_3N_4 at the top and the bottom of the grating pattern was removed by CHF_3 plasma while leaving the material at the edge taking advantage of the directionality of RIE. A grating pattern made of Si_3N_4 with doubled number of the parent pattern was formed after removing the parent SiO_2 grating by buffered HF (BHF) solution. The fabrication scheme was continued, as illustrated in Figure 1.4 (B), by LPCVD Si over the created Si_3N_4 grating pattern, directional selective removal of LPCVD Si at the top and the bottom of the grating pattern and final removal of Si_3N_4 taking advantage of the selectivity between Si_3N_4 and Si in concentrated HF solution.

Generally speaking, good selectivity between materials is crucial for the successful

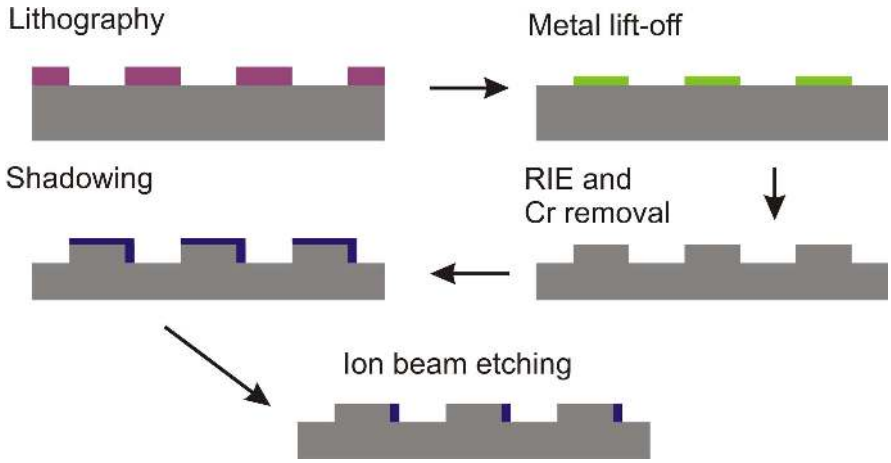

Figure 1.3: 10 nm linewidth metal structure fabrication by Flanders *et al.* [19].

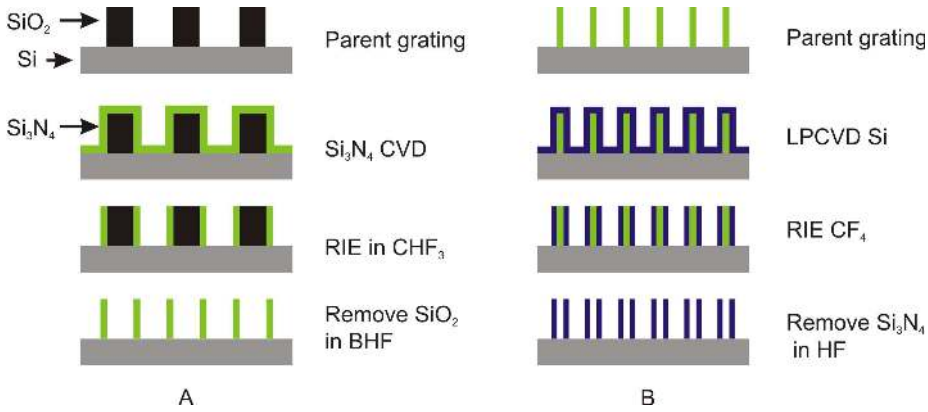

Figure 1.4: Edge defined techniques to double grating pattern by Flanders *et al.* [21]: (A) Pattern doubled after first X-ray lithography; (B) Continued fabrication of (A).

implementation of edge lithography. In Flander's case, for example, the selectivities between Si, SiO_2 and Si_3N_4 in both plasma etching and wet etching technologies should be well considered [21]. The advantage of using edge lithography is that the resolution is no longer determined by lithographic tools but by the material thickness deposited at parent structure edges. Therefore, it provides the possibility of fabricating nanostructures without relying on wavelength depending lithographic tools. By using the same concept, Choi *et al.* fabricated sub-10 nm Si nanowire arrays using conventional UV lithography, which was named size reduction lithography [22]. Size reduction lithography was integra-

ted with DUV lithography to create Si wires of sub-20 nm wide and 110 nm high with ca. 250 nm pitch [23]. The fabrication process flow and results are shown in Figure 1.5. Moreover, it was demonstrated that the Si mold was successfully utilized as stamp in T-NIL together with metal lift-off to fabricate Pt nanowires [23].

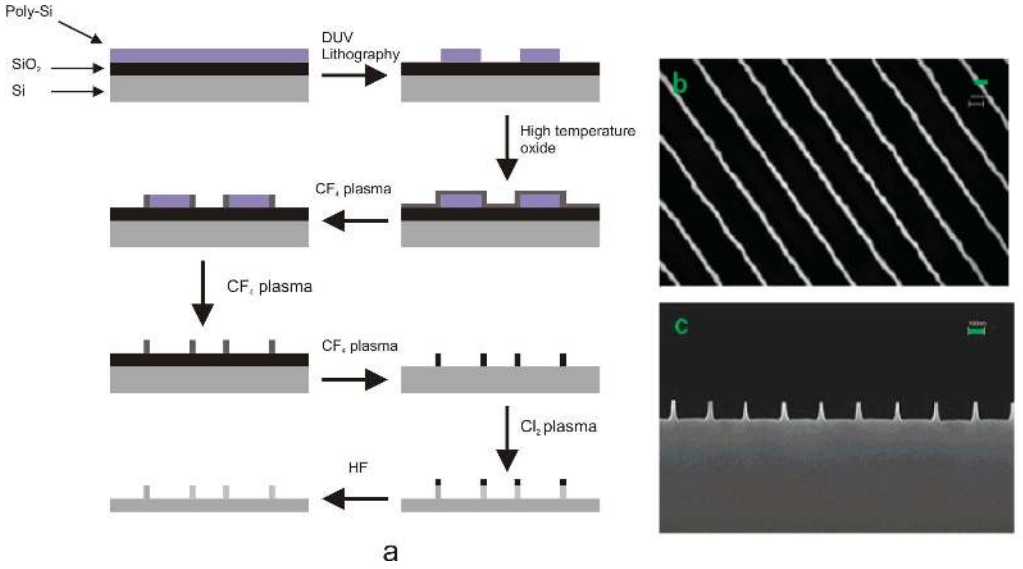

Figure 1.5: Si mold fabrication by Yan *et al.* [23]: (a) Schematic drawing of the size reduction lithography process flow; (b),(c) SEM images of the final fabricated Si nanostructures of 16 nm wide and 110 nm high with 250 nm pitch.

In addition to making grating patterns, Kwon *et al.* utilized the mold with Si nanowires fabricated by the size reduction lithography to create Si nanopillars by mold-to-mold cross imprint (MTMCI) techniques [24]. Figure 1.6 shows the schematic of MTMCI. Different from conventional NIL procedures, the fabricated Si mold was used both as the imprint substrate and stamp. The grating pattern was imprinted into the polymer in a perpendicular direction to the gratings on the substrate. After residual layer removal to expose the grating pattern on the substrate, Cr was evaporated followed by a lift-off step to create Cr gratings standing on top of Si gratings on the substrate. Si nanopillars were created through directional plasma etching using Cr as the mask. Since both the Si and Cr gratings function as the etching mask, the Si nanopillars were formed standing on the intersection of the square fields on the substrate wafer. The fabrication results of Si nanopillars are shown in Figure 1.7.

The examples shown above share the basic idea of using the thin film deposited at

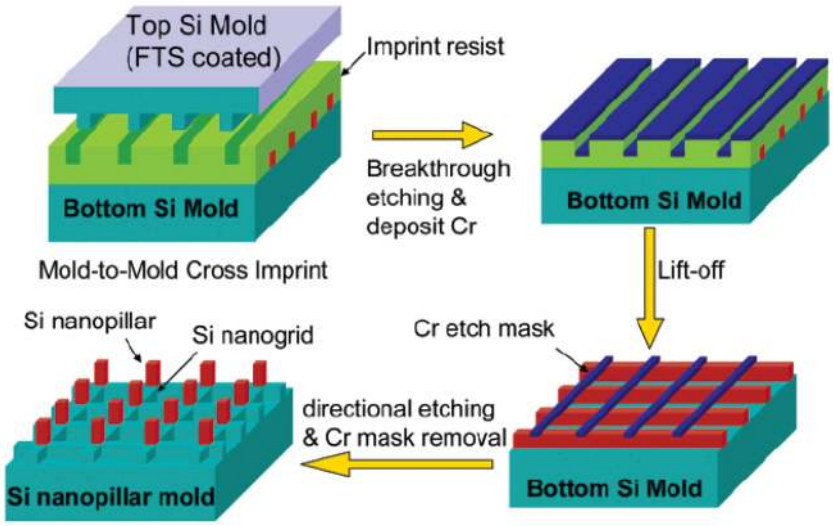

Figure 1.6: Schematic of MTMCI taken from Kwon *et al.* [24].

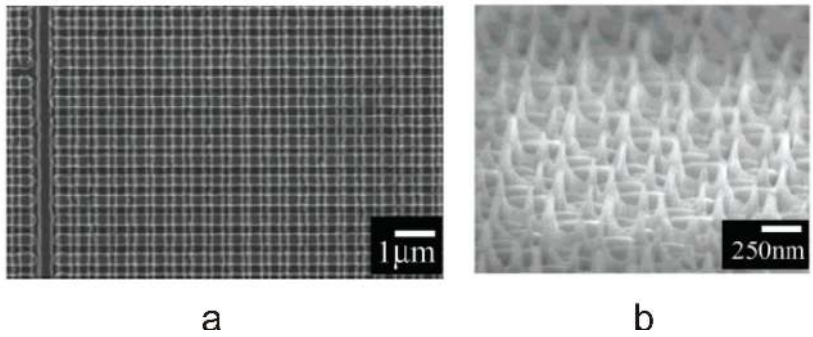

Figure 1.7: SEM images of nanopillars made by MTMCI taken from Kwon *et al.* [24]:(a) Top view; (b) angled view.

the vertical step edges as the etching mask for the followed pattern transfer steps. The fabrication of smooth vertical step edges then becomes the primary requisite for the success of these fabrication schemes. Since the thin film deposited at step edges is within few hundreds of nanometers, plasma etching is chosen over wet etching considering its directionality and selectivity. As in the SEM images shown above, the fabricated nanostructures do not have perfect vertical sidewall profiles, which can be a result of plasma etching chemistry, mask layer quality, etc. Processed in a different approach, Gabriec *et*

al. fabricated SiO_2 nano-lines created by oxidizing poly-Si step edges using Si_3N_4 as the mask [25]. The fabrication scheme is shown in Figure 1.8.

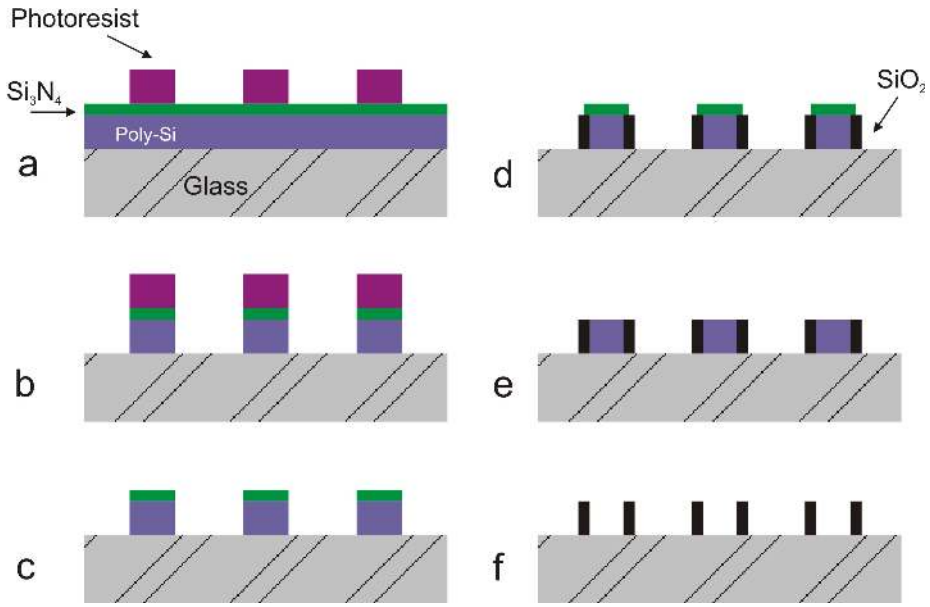

Figure 1.8: SiO_2 nano-lines fabrication by Gabriec *et al.* [25].

In nanofabrication, a smooth surface is always preferred and has always been addressed, especially for fluidic and nanoimprint applications. Therefore, researchers have explored the use of wet chemical etching taking advantage of Si crystalline orientations to create smooth vertical sidewalls to function as edges. Gabriec and co-workers elicited the idea of using mono-crystalline Si to fabricate step edges with vertical sidewalls using wet etching methods [25, 26]. In an attempt to improve accuracy and to show its use in T-NIL, Haneveld *et al.* created SiO_2 nanoridges by local oxidation of sharp edges in <110> Si wafers using a full-wet procedure and silicon rich nitride (SiN_x) as the mask [27]. Figure 1.9 is the schematic of the SiO_2 nanoridge fabrication process. The smooth vertical sidewalls were created by using <110> Si wafer and normal photoresist developer OPD 4262, which contains 2.5% of TMAH and other organic solvents. OPD 4262 has a low etch rate of 3.7 nm/min on <110> Si planes and provides smooth surface finish to both <110> and <111> planes. SiO_2 nanoridges were created by oxidizing the smooth vertical Si sidewalls using SiN_x as the mask. Liang *et al.* also demonstrated the fabrication of Si nano-lines utilizing Si <110> SOI substrates and wet anisotropic Si etching for S-FIL [28].

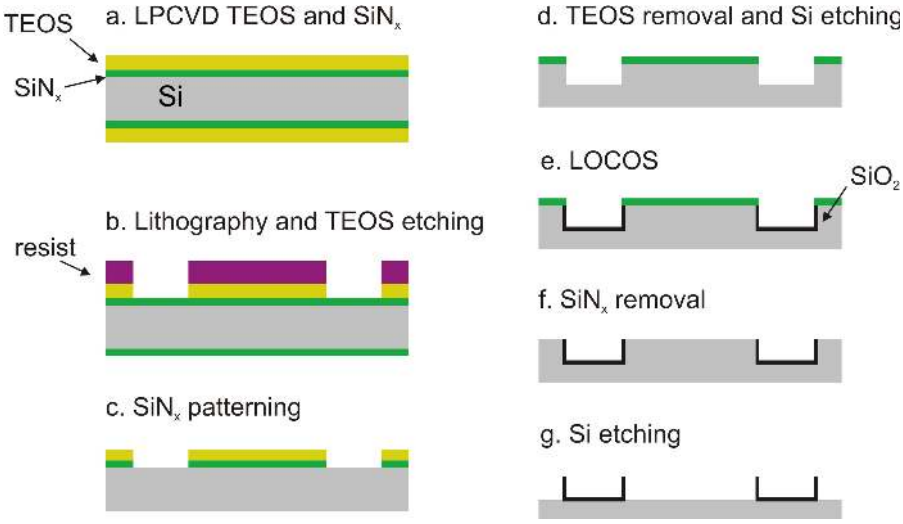

Figure 1.9: SiO_2 Nanoridge fabrication by Haneveld *et al.* [27].

Repeated edge lithography

Multi-nanostructures can be generated by sequential conformal material deposition and selective etching steps. Cerofolini *et al.* demonstrated the multi-spacer patterning technique (M-SPT) which was shown to have potential in nanoelectronics applications [29, 30]. The M-SPT fabrication scheme generally comprises the following steps, as shown in Figure 1.10: (a) sacrificial structures with vertical sidewalls patterned by photolithography and directional etching; (b) conformal deposition of one layer; (c) maskless directional etching of this layer to fabricated the first spacer; (d)-(e) the formation of the second spacer by conformal deposition of another layer and maskless directional etching; (f) multi-spacer formation by repeating step (b) to (e). Poly-Si deposition and thermal oxidation of the poly-Si layer were alternated to create multi-spacer made of poly-Si and SiO_2. The fabrication results are shown in Figure 1.11.

Other researchers have also demonstrated the fabrication of spacer-like structures employing similar working principles to SPT. Choi *et al.* demonstrated the fabrication of nanoscale phosphosilicate glass (PSG) complementary metal oxide semiconductor (CMOS) by conformal deposition of PSG over a SiGe block pattern [31]. Degroote *et al.* used SPT in combination with resist-based patterning to define a Si-Fin with a critical dimension below 20 nm [32].

As an alternative to M-SPT, Sonkusale *et al.* developed the so-called planar edge

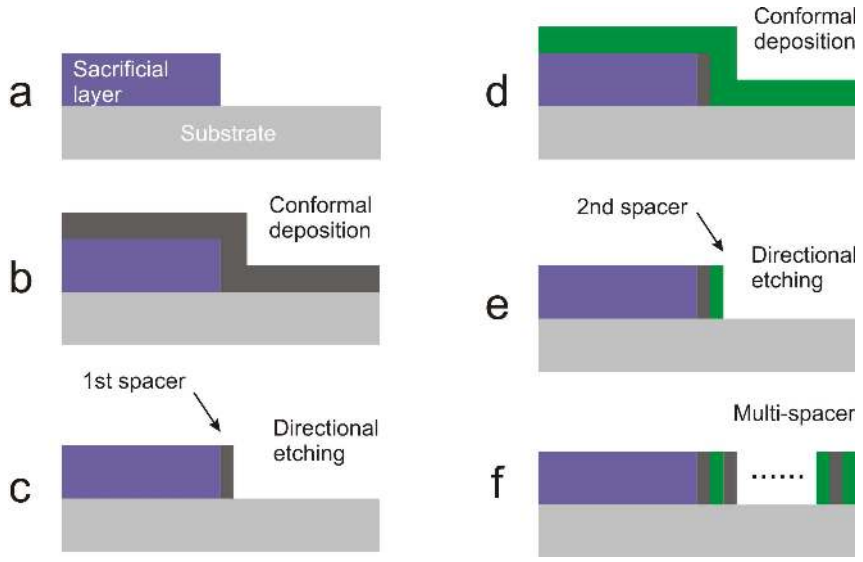

Figure 1.10: Multi-spacer patterning technique by Cerofolini *et al.* [29].

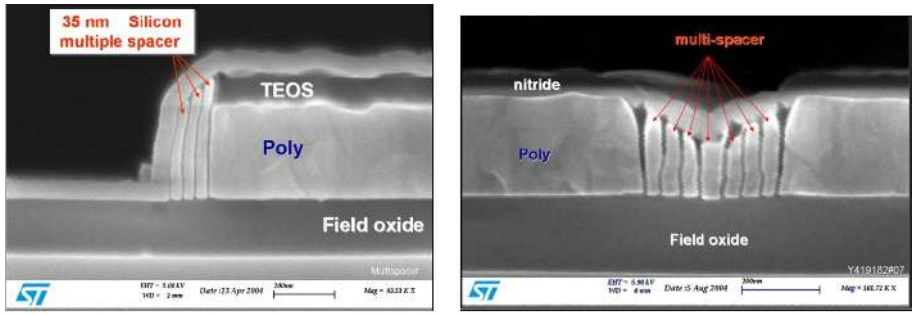

Figure 1.11: SEM images of cross-section of multi-spacer structures fabricated by Cerofolini *et al.*: (a) Three spacers; (b) seven spacers. Images are taken from [29].

defined alternate layer (PEDAL) process to fabricate nanowires for NIL application [33, 34]. Figure 1.12 shows the schematic drawing of PEDAL process flow. The fabrication started with the creation of poly-Si sacrificial structure with vertical sidewalls on top of Si substrates by RIE. Then silicon nitride of 25 nm and amorphous-Si (a-Si) of 50 nm were alternately deposited over the created trench structures. After deposition, the trench was planarized by spinning organic polymer followed by etching the polymer,

silicon nitride and a-Si by RIE. The planaization was finished until the poly-Si sacrificial layer was reached. Either silicon nitride or a-Si nanowires can be fabricated by selective etching either of these materials. SEM images shown in Figure 1.13 confirm the successful fabrication of a-Si nanowires of 25 nm wide with 50 nm spacings. Moreover, Hussain *et al.* also employed a similar process flow to fabricate Si nanowires as template for NIL applications [35].

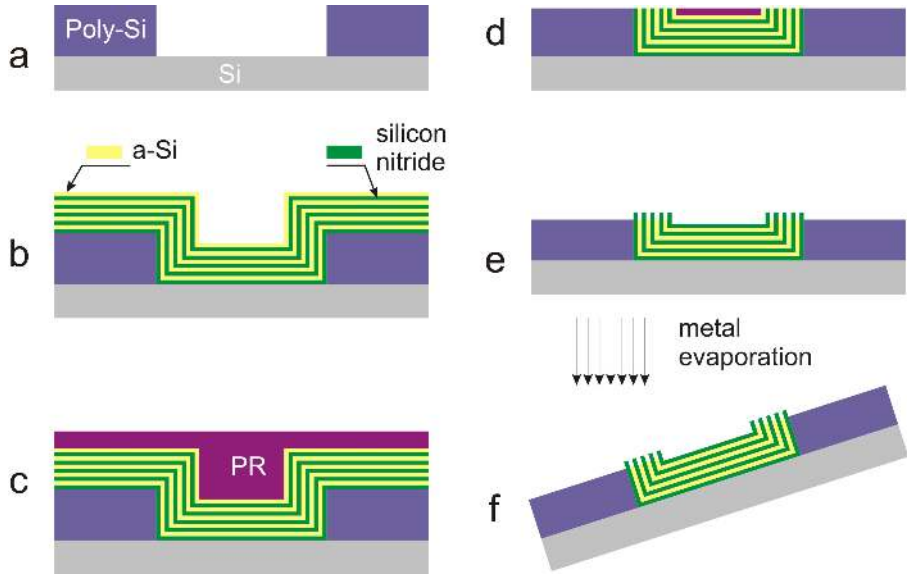

Figure 1.12: Process scheme of nanowire fabrication by PEDAL process by Sonkusale *et al.* [33, 34]

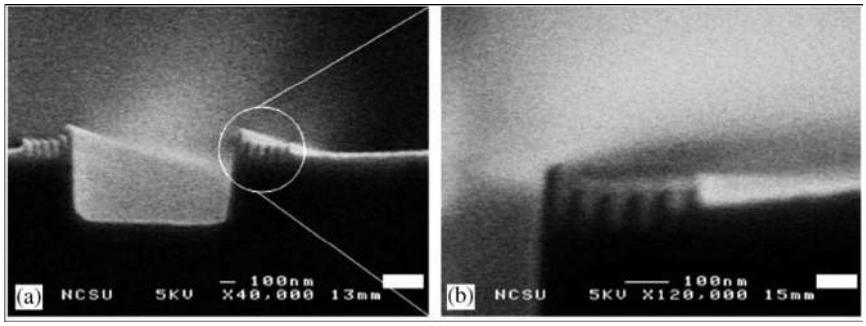

Figure 1.13: SEM images of nanowires fabricated by PEDAL process by Sonkusale *et al.* [33]

1.3 Micromachining technology as a tool for stamp fabrication

Micromachining is the term used to describe fabricating micron-sized features. Generally, this technology is referred as micro-electro-mechanical system (MEMS), micromachines (in Japan) or micro systems technology (MST in Europe). Micromachining process is initially borrowed from IC industry with additional adaptations specifically to silicon micromachining. The micromachining process generally consists of material deposition, lithographic patterning and etching techniques. Many studies provide general introduction to micromachining techniques [36, 37].

1.3.1 Deposition methods

Epitaxy, sputtering, evaporation, chemical-vapor deposition (CVD), and spin-on methods are common deposition methods to obtain uniform layers of semiconductor materials, metals, insulators, and polymers.

Epitaxy is a deposition method to grow crystalline silicon with different dopant and concentration over crystalline substrates such as silicon and sapphire (Al_2O_3). It is a widely used step in CMOS fabrication and is efficient in forming wafer-scale p-n junctions for controlled electrochemical etching.

Amorphous silicon dioxide is obtained by oxidizing silicon in either dry oxygen or water vapor environment, which are generally referred as dry and wet oxidation. The oxidation process is performed at a elevated temperature between 800°C and 1200 °C. Oxidation mechanisms have been extensively studied [38, 39, 40]. Oxide quality and thickness with respect to temperature, oxidation environment and time are also well documented [41].

Sputtering and evaporation are the common methods for metal as well as insulating materials deposition. In sputtering deposition, a target made of a material to be deposited is physically bombarded by a flux of inert gas (usually argon) in a vacuum chamber at a pressure of 0.1-10 Pa. Target atoms or molecules are ejected and deposited onto the wafer. When the target size is larger than the wafer size, the directional randomness of the sputtering process results in good step coverage. In an evaporation process, a source material is heated up to a high temperature to generate a vapor which condenses on a substrate to form a film. It is performed in a vacuum chamber with a background pressure typically below 10^{-4} Pa to avoid film contamination. The source material can be heated either by electrical current running through a resistor or by scanning a high voltage (e.g. 10 kV) electron beam over. The evaporation process is a directional deposition process

from a relatively small source, which results in material deposition under an angle to the wafers and hence causes poor step coverage.

Chemical vapor deposition (CVD) initiates chemical reactions of reactive species in a controlled atmosphere on heated substrates. In contrast to sputtering, CVD is a high temperature process which is usually performed above 300°C. Common thin films deposited by CVD include amorphous/poly-silicon, silicon oxide, silicon nitride, tungsten, titanium and tantalum as well as their nitrides, and most recently, copper and low-permittivity dielectric insulators. CVD processes are further categorized into atmospheric-pressure (APCVD), low-pressure (LPCVD) and plasma-enhanced (PECVD). APCVD and LPCVD work at high temperatures, e.g. 400°C to 800°C. In PECVD, the substrate is normally heated up to ca. 300°C. Substrate temperature, gas flow, presence of dopants, and pressure are important process variables for all types of CVD.

Poly/amorphous silicon, LPCVD silicon oxide and silicon nitride are the most common materials that can be obtained by CVD methods. Polysilicon is deposited by pyrolysis of silane (SiH_4) to silicon and hydrogen at a temperature typically between 550°C and 700°C. It is also possible to do the deposition in a low pressure PECVD reactor which will result in amorphous silicon.

Silicon oxide deposited at a temperature below 500°C by silane and oxygen reaction in an APCVD, LPCVD or PECVD reactor is called low-temperature oxide (LTO) due to the low temperature deposition process. LTO is often used for passivation coating on aluminum, in which case the deposition temperature should be kept below 400°C to avoid Al layer degradation. The silicon dioxide deposited in a LPCVD reactor at a temperature between 650°C and 750°C by pyrolysis of tetraethoxysilane ($Si(OC_2H_4)_4$) is referred as TEOS. Another method used for silicon dioxide deposition utilizes dichlorosilane ($SiCl_2H_2$) reacting with nitrous oxide (N_2O) in a LPCVD reactor at a temperature near 900°C.

Stoichiometric silicon nitride (Si_3N_4) is deposited at atmospheric pressure by reacting silane (SiH_4) and ammonia (NH_3) or at low pressure by reacting dichlorosilane ($SiCl_2H_2$) and ammonia. The deposition temperature for either method is between 700°C and 900°C. Both CVD and LPCVD deposit silicon nitride with a high tensile stress approaching 1000 MPa. For some micromachining applications, to reduce the tensile stress, silicon rich nitride is deposited in a LPCVD reactor at a temperature between 800°C to 850°C, which results in a tensile stress around 100 MPa.

Unlike the deposition described above, the spin-on method is a simple process in which dielectric insulators and organic materials can be coated. The equipment is simple and a variable tunable spin-coater normally meets the requirement. Organic materials can be

either dispensed on a wafer surface by a nozzle or manually. Spinning can be carried out at a speed between 500 to 5000 rpm for 30 to 60 s to obtain a uniform layer thickness. The spinning rate is tuned according to the specific layer thickness requirement and polymer properties.

1.3.2 Wet etching

Wet chemical etching is one of the key technologies in micromachining. The methods are generally categorized into isotropic and anisotropic mechanisms. In isotropic etching, materials are removed at the same speed in all directions. Amorphous materials are generally etched isotropically by wet chemical solutions, such as hydrofluoric acid (HF) solutions used for SiO_2 etching, and 50% HF and phosphoric acid (H_3PO_4) for silicon nitride etching. In contrast, in anisotropic etching, the etching is preferable to some directions over others, which results in cavities with vertical or slanted sidewalls. Si anisotropic etching by strongly basic solutions (e.g. KOH) is the most commonly used type of anisotropic etching. Figure 1.14 shows the SEM images of anisotropically and isotropically etched Si cavities.

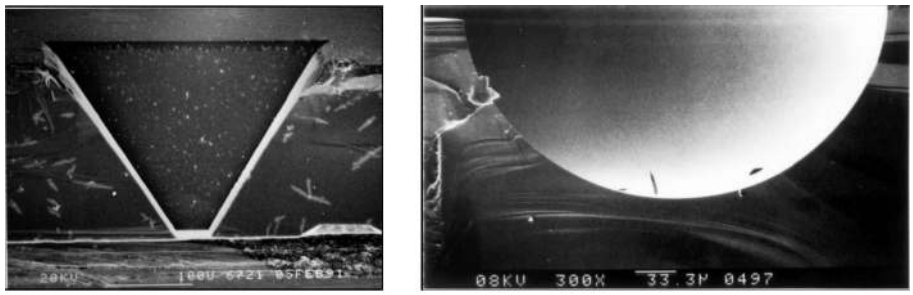

Figure 1.14: SEM images (a) Anisotropically etched Si cavity by EDP solutions; (b) Isotropically etched Si cavity by a solution made of HNO_3:HF:CH_3OOH. Images are taken from [42].

Anisotropic Si etching

Anisotropic silicon etching stems from etch rate differeces depending on silicon crystal orientation and wet chemicals. The crystal structure of silicon is of diamond type and has a lattice constant $a = 5.43\mathring{A}$. The lattice structure, as illustrated in Figure 1.15, is face centered cubic (FCC) with two atoms in the unit cell, which are $1/4a$ along the main

diagonal of the cube. Crystal planes are characterized by sets of three indices, the so

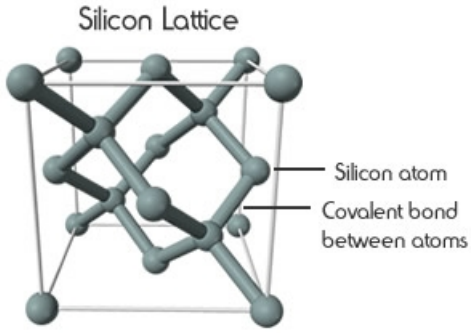

Figure 1.15: Illustration of silicon lattice

called Miller indices. Generally <111> Si planes show the slowest etch rate. Therefore, different shapes of structures can be realized by utilizing <100> and <110> oriented Si wafers to stop etching automatically at <111> Si planes. The Si anisotropic etch rate depends on etchant, temperature, concentration of the etchant, doping of the substrate and stirring [43]. Seidel *et al.* reported reviews over Si etching depending on its crystal orientation as well as the influence of doping [44, 45].

Anisotropic Si wet etching can be performed using aqueous alkali-hydroxide solutions, EDP solutions (ethylendiamine, pyrocatechol, and water), NH_4OH, and tetramethyl ammonium hydroxide ($((CH_3)_4NOH$,TMAH). EDP solution is the earliest wet chemical explored for Si etching. It is toxic and degrades with ease when it is in contact with oxygen. Moreover, precipitation of silicates occurs after Si etching. At present, therefore, KOH and TMAH are the most commonly used less dangerous Si etchants. KOH is less dangerous, easy to handle and has fast etch rates. The etch rate is proportional to $[H_2O]^4[KOH]^{1/2}$ and therefore shows its maximum at a KOH concentration of 20 wt% [44]. Futhermore, temperature exerts a much larger influence on the etch rate than the silicon crystal orientation [44]. Since KOH generally shows poor selectivity to oxide, silicon nitride is suggested as the appropriate masking material in Si etching using KOH. A disadvantage of Si etching by KOH is that potassium ions remain on the Si surface after etching, which makes it not compatible with IC fabrication. For MEMS purposes, for example, before oxidation, a RCA2 cleaning step ($HCl:H_2O:H_2O_2$=1:5:1, heated up to 80°C, the wafers are immersed in the solution for 10 to 15 min) should be performed to remove all the metal ions to avoid furnace contamination.

TMAH is also a nontoxic and easy to handle Si etchant. It is an organic solution

therefore it is compatible with IC fabrication. Researchers have investigated the etch rate of Si in TMAH solutions as a function of the temperature and concentration [46, 47, 48]. Tabata *et al.* reported that the etch rate of <100> and <110> Si planes decreases with increase of the concentration from 5 to 40 wt% [46]. The smoothness of both types of Si planes improves with the increase of the TMAH concentration and the most smooth bottom surface for <100> and <110> Si planes appears at concentrations of 22 wt% and 30 wt% respectively. The ratio of the etch rates between <111> and <100> planes varies between 0.02 to 0.05 with the maximum at a concentration of 22 wt%. The etch rate of thermal SiO_2 is almost 4 orders of magnitude lower than that for the <100> and <110> planes.

Isotropic etching thin films

Silicon dioxide and silicon nitride are the most commonly used mask materials for MEMS applications. Silicon oxide can be obtained by either wet or dry oxidation or by means of LPCVD, e.g. of LTO and TEOS. It is easily etched in HF solutions, e.g. 1%HF, BHF and 50%HF. In wet anisotropic Si etching, SiO_2 is a good mask when EDP and TMAH are used as the etchants. However, the fast etch rate of SiO_2 in KOH solutions makes it a less favorable masking material in this case. Silicon nitride can be etched in both phosphoric acid (H_3PO_4) at 160°C-180°C and 50%HF. The high selectvitivity between silicon oxide and silicon nitride in hot H_3PO_4 acid and 50%HF, which is about 10:1 and 1:100, is utilized for selectively etching each other. Silicon nitride exhibits an extremely low etch rate in KOH solutions and hence is a good mask for Si anisotropic etching by KOH.

1.3.3 Plasma etching

Wet chemical etching is easy to handle and allows batch processing. However, the design flexibility is compromised by wet Si etching due to the Si crystal orientation dependence. Therefore, dry plasma assisted etching is introduced and is increasingly used due to its ability of faithfully transferring patterns from the mask layers into Si without relying on Si crystal orientation and its cleanliness and compatibility with vacuum processing technologies.

Plasma is generated when a voltage is applied in a reactor. Plasma etching can be categorized into physical plasma etching and chemical reaction etching. In physical plasma etching, as shown in Figure 1.16 (a), ion bombardment dominates the etching process while the influence of radicals is neglected. Chemical reactive etching involves the

generation of chemically reactive neutrals (radicals) and ions that are accelerated under the effect of an electric field toward a target substrate. When the etching process is purely chemical, which is dominated by radicals reacting with substrate materials, as in a barrel system, it is referred to as *plasma etching*. Isotropic profiles are achieved by pure chemical radical etching, which is shown in Figure 1.16 (b). When ion bombardment is involved in the process and plays a synergistic role, the process is called *reactive ion etching* (RIE). Figure 1.16 (c) shows a structures with vertical sidewalls obtained by RIE.

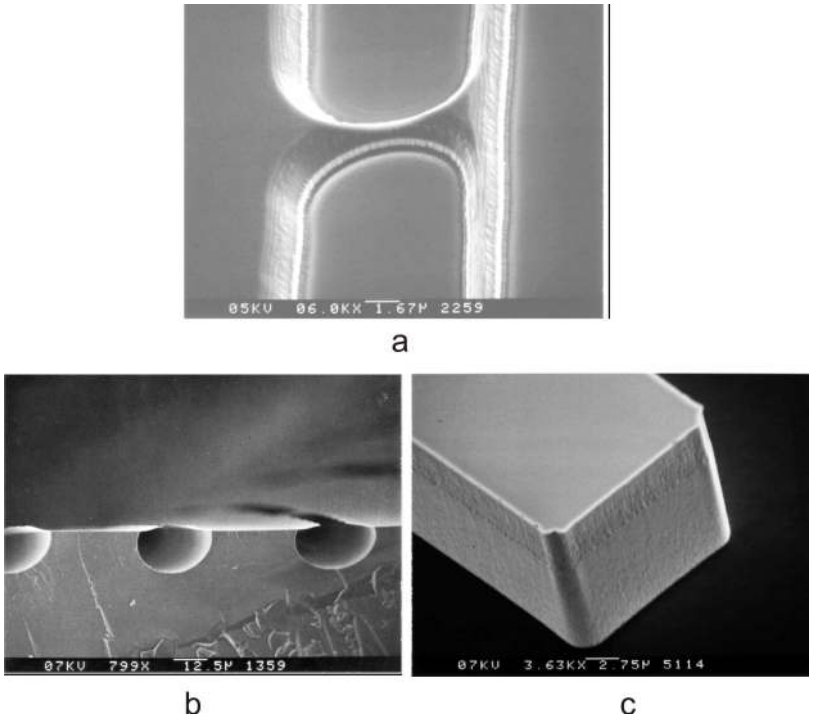

Figure 1.16: SEM images showing the basic mechanisms of dry plasma etching: (a) physical plasma etching; (b) Pure chemical radical etching; (b) RIE: ion bombardment plays the synergistic role. Images are taken from [42].

Reactive ion etching

The chemically reactive species generated in plasma include neutrals (N), radicals (R), electrons (E), ions (I), photons (P), and phonons (T). The photons are responsible for the characteristic glow of the plasma. The *glow region* is full of electrons and only a small electrical field exists. The energetic particles in the glow region are transported to

a sample surface through the plasma boundary layer. The charged species recombine at the walls of plasma boundaries. In the adjacent region, electrons and ions diffuse to the sample, better known as *sheath region*. A strong electrical field exists in the *sheath region* which brings ions and reactive species to the sample surface while drives electrons and negative ions away from the surface. Radicals have only thermal energy and will leave the boundary layer for the sample surface in all directions while the ions will leave the boundary layer under an angle of 90°. Since electrons are much more mobile than ions, the sheath region can be modeled as a rectifier. The thickness of the sheath is related to the electron mean free path, and increases with decreasing gas pressure.

Etching mechanism

In the basic RIE system, an rf glow discharge is used to generate from a suitable feed gas (e.g. SF_6, CF_4, Cl_2, CHF_3, NF_3) by electron-impact dissociation/ionization. The etching plasma gas consists of neutrals, electrons, photons, radicals and positive and negative ions. The substrate or wafer is placed on an rf driven capacitively coupled electrode. During etching, electrons are attracted to the substrate since they are more mobile than the ions are. Therefore, negative charge is formed on the electrode after the ignition of plasma, which is also referred to as *dc self-bias* voltage. The reactive species travel from the bulk of the plasma to the wafer by diffusion. Positive ions are forced to the electrode as a result of the dc-bias voltage formation, which will also assist etching. Reactive species first adsorb on the substrate, which can be assisted by ion bombardment by creating active sites for adsorption. Then the reaction between the reactive species and the wafer surface takes place. When this process is enhanced by ion bombardment, it is called ion-induced RIE. The desorption of the reaction products into the gas phase requires the reaction products to be volatile. Moreover, when blocking film is formed, it should be removed by ion bombardment via sputtering. This mechanism is also called ion-inhibitor RIE. The desorbed species into the bulk of plasma should be pumped out to avoid redeposition. Detailed discussion about plasma, such as etching mechanism, chemistry, surface finish, etc., can be found else where [49, 50, 51].

Chlorine and bromine containing plasmas have in the beginning been widely used for Si etching due to their fast etch rates and high anisotropy. However, such gases are corrosive and toxic to reactor materials and more importantly hazardous to environment [52]. Fluorine containing gases such as CF_4 and SF_6 are less corrosive and toxic and show higher selectivity to masking materials. Therefore, F-based plasma etching is now playing a dominant role in Si etching in MEMS applications.

The basic mixed plasma etching is reactive ion etching with two or more gas mixtures

performed at room temperature, such as SF_6/O_2 and $SF_6/O_2/CHF_3$ gas mixtures [53, 54]. To achieve anisotropic etching profile, plasma etching are generally performed by mixed or pulsed processes. The two most distinguished approaches are the so-called Bosch process developed by Laermer and Schilp [55] and the cryogenic RIE developed by Tachi *et al.* [56]. The Bosch process is a room temperature process with continuously alternating etching and passivating steps. It is able to provide a fast Si etch rate with scallop sidewall finish. Typically, a Si etch rate of 2 μm/min and selectivity to resist of 75:1 can be achieved. Cryogenic etching uses low bias F-based high density plasma with lowered Si substrate temperature. The sidewall passivation is enhanced by lowering the substrate temperature such that the reactivity of F-radicals is decreased and ion bombardment dominates the bottom passivation cleaning and etching.

Flurocarbon based etching

Mogab *et al.* studied the etching of Si using CF_4 etching Si and indicated that the etch rate is directly related to the F atom density [57]. A CF_4 plasma produces CF_3^+, CF_3, F, CF_3^- and F^-, in which negative ions (CF_3^- and F^-) do not usually contribute to the etching while both CF_3 radicals and CF_3^+ react readily with clean Si surface [58, 59, 60].

The use of CF_4 plasma with the addition of hydrogen and oxygen to control the etch rate of Si and SiO_2 was first reported by Heinecke in 1975 [61]. The addition of hydrogen to CF_4 plasma has two effects: (1) H_2 reduces the F-atom density by forming HF and hence decreases the etch rate of Si; and (2) H_2 reacts with CF_3 radicals forming a C_xF_y film on the Si surface which stops Si etching. Therefore hydrogen addition into CF_4 plasma increases the etching of SiO_2 by suppressing the attack of Si [61, 62, 52].

The etch rate of Si is increased with the addition of O_2 into CF_4 glow discharge [63, 64, 65, 66]. There are several speculations concerning the reaction between CF_4 and O_2, such as the oxidation of CF_4 in the gas phase to form CF_3O_2, oxidation of carbon on the etched surface in the vacuum system, or oxidation of the fluorocarbon polymer deposited on surfaces [49]. The overall consequence, however, is generally the same, that is a carbon-oxygen bond is formed (e.g., CO, CO_2 or COF_2), which suppresses recombination reactions [58]. The maximum Si etch rate is obtained when the O_2 content produces the maximum F atom concentration and the oxidation of Si surface limits the etching reaction [63, 66]. At low O_2 percentage, the increase of Si etch rate is due to the decrease of the $Si_xO_yF_z$ layer thickness as a result of rise of the F concentration. The $Si_xO_yF_z$ layer grows thicker as a result of increased oxidation and decreased fluorination of the Si surface with the increase of O_2 content in CF_4/O_2 mixture [66]. In contrast, the etching of SiO_2 with CF_4/O_2 plasma is different from that of Si since there is no significant retarding

effect of oxygen [57, 67]. Oehrlein*et al.* accomplished the removal of fluorocarbon residue after CF_4/40% H_2 RIE by annealing samples in O_2 ambient at 400°C followed by BHF etching [68].

The CHF_3/CF_4 based plasma was also implemented to tune the desired selectivity between Si and SiO_2. Oehrlein *et al.* investigated the Si and SiO_2 using CF_4 and CHF_3 in an electron cyclotron resonance (ECR) discharge system [69]. It is suggested that oxide-to-silicon etch selectivity is a result of selective fluorocarbon film deposition onto the silicon surface which prevented Si etching, which is ca. 5.5 nm and 2.5 nm in CHF_3 and CF_4 plasma respectively. Standaert *et al.* proposed the mechanism that silicon etching in a fluorocarbon plasma involves the diffusion of reactive and volatile species through a fluorocarbon steady state layer [62]. This mechanism has been proven to be applicable when ICP is used to generate CHF_3 plasma to etch Si and SiO_2 [70]. The experimental results obtained by Rolland *et al.* also suggested that the selectivity between Si/SiO_2 was considerably improved by adding CH_4 to CHF_3 by means of the formation of 6 nm thick fluorocarbon residue [71].

SF_6 based etching

To circumvent carbon deposition on Si surface, SF_6 was investigated as a proper etchant for Si etching [72]. Eisele first reported that SF_6 is able to achieve a high Si etch rate without the addition of O_2 [73]. SF_6 dissociates into F and SF_x radicals that react readily with Si and the end product is SiF_4, which is a volatile gas and can be pumped out. No sulfuric residue is found on the Si surface after etching. Flamm studied the reaction of fluorine with silicon and concluded that F radicals dominate the etching, which results in isotropic characteristics [74]. SF_6/O_2 is an alternative to CF_4/O_2 for plasma etching of Si and SiO_2. A general review of the etching mechanism of Si in SF_6/O_2 plasma has been given by Ryan *et al.* [75]. The addition of O_2 into SF_6 increases the etch rate of Si, which has a similar effect as the adition of O_2 to CF_4 plasma. d'Agostino investigated the etching mechanism of Si and SiO_2 in SF_6-O_2 mixture [76]. Different from O atoms competing with F atoms for chemisorption on a Si surface in CF_4/O_4 plasma, the increase of O_2 content in a SF_6/O_2 mixture leads to a greater oxygen coverage and a lower etch rate. It was also suggested that the etch rates in SF_6/O_2 plasma are 5 to 10 times faster than those in CF_4/O_4 plasma under the same conditions.

When SF_6 is used in mixed RIE at room temperature, it is common to have both O_2 and CHF_3 as the inhibitors for sidewall passivation. When a SF_6/CHF_3 combination is used, CHF_3 forms CF_2 by dissociation which works as a sidewall inhibitor [77, 78, 79]. It has also been demonstrated that the etch rate and etching anisotropy are influenced

by SF_6/CHF_3 percentage, power supply and pressure. As discussed above, the addition of O_2 will increase the F-atom density preventing it from recombination into SF_6. A competition exists between O_2 and CHF_3, in which the former one forms the passivating SiO_xF_y layer while the latter one removes it. The addition of O_2 helps subtly control profile [54, 80].

In the late 1980s, Tachi *et al.* introduced the idea of low-temperature RIE [56]. The results showed that Si trenches with vertical sidewalls were achieved and high selectivity between Si, SiO_2 and photoresist are obtained at a temperature from -110°C to -130°C. The cryogenic Si etching is made possible since sidewall etching by radicals is suppressed by lowering the substrate temperature while the etching at the Si bottom surface is not largely influenced because ion bombardment dominates reactive ion etching [81, 82, 83, 84]. It was observed that the cooling temperature should go below -140°C to avoid SF_6 freezing on the Si surface, which is in correspondence with the results obtained earlier by Oostra and co-workers, who first investigated the reaction of Si with SF_6 with Ar^+ ions bombardment at low temperatures and concluded that new molecular products can be formed at a temperature down to 100 K [85]. Moreover, Tsujimoto *et al.* demonstrated that cryogenic Si etching shows a Si crystal orientation dependence down to -150°C [86]. The performance of SF_6/O_2 mixture etching Si at cryogenic temperature depends on many factors, e.g. gas flow, oxygen concentration, ion impact, temperature, etc [87].

Parameters influencing etching

The performance of plasma is influenced by factors such as system configuration, pressure, temperature, gas flow, loading, etc. Jansen *et al.* analyzed the RIE process in the aspects of system settings, equipment parameters, plasma characteristics and trench forming mechanisms [88]. Chapman *et al.* first investigated the dependence of plasma etching rates on the flow rate of the etching gas [89]. It was observed that the decrease of etch rate with the decrease of gas flow is due to insufficient gas supply and the etch rate can also be reduced because of the pumping of active species with very high flow rates [89]. The flow rate dependence of etching has further implications to other etching parameters such as preferred flow rate, pressure and flow changes, etching selectivity, etch uniformity, etc. [90]. Pressure has a major influence on plasma etching by the sheath potentials and ion bombardment energy, the electron energy, the ratio of ions to neutrals, the rate of chemical kinetics, etc. Temperature has a profound influence on discharge chemistry in plasma etching, as discussed in cryogenic etching, which is differed from gas temperature and substrate temperature.

The etch directionality is mainly determined by the directed energy into an etching

reaction, which can be accomplished by neutral, ion, electron, or photon bombardment of a surface exposed to a chemical etchant. Gerlach-Meyer *et al.* performed the famous experiment of Si etching using XeF_2 molecules with and without 1 keV Ne^+ bombardment to prove the dependence of directional etching on ion bombardment [91]. Jansen *et al.* have done an extensive study regarding various aspects influencing the performance of deep reactive ion etching (DRIE) with respect to Si etch rate, etch profile and selectivity to mask materials [92].

1.4 Aim of the research and thesis outline

The thesis describes the research results obtained for high resolution stamp fabrication for thermal nanoimprint lithography applications. As described in the preceding sections, many researchers have explored the possibilities of fabricating nanostructures by edge lithography in combination with Si micromachining technologies utilizing either conventional UV lithography or high resolution lithography for pattern definition. In this project, we have investigated the fabrication of nanoridges originating from SiO_2 nanoridge fabrication by oxidizing vertical Si sidewalls using SiN_x as the mask [27]. The fabricated SiO_2 shows sub-20 nm resolution, however, the fragile nanoridge properties prevent the stamp from re-use in T-NIL. Consequently, we have developed the concept of advanced edge lithography to produce Si nanoridges made of crystalline Si and repeated advanced edge lithography to create multi-Si nanoridges taking advantage of Si anisotropic etching. The mechanical strength has been greatly improved and the stamps have been successfully applied in T-NIL. Furthermore, Si plasma etching is integrated into the advanced edge lithography scheme to produce Si nanoridges with arbitrary contours independent of Si crystal orientation. Finally, we show the application of Si nanoridges in alternative nanofabrication approaches. The thesis is organized as the follows:

Chapter 2 describes the fabrication of a SiO_2 nanoridge stamp reinforced with silicon nitride for its use in nanoimprint lithography. The fabrication process is based on edge lithography using conventional optical lithography and wet anisotropic etching of <110> silicon wafers. SiO_2 nano-ridges of 20 nm in width were fabricated. A silicon-rich nitride layer is deposited over the original SiO_2 nano-ridges to improve the ridge strength and to achieve a positively tapered shape which is beneficial for T-NIL. A replica of the nanoridges with silicon-rich nitride shield is obtained by imprinting the stamp into thermoplastic nanoimprint polymer mr-I 7010E.

In Chapter 3, nanoridges are created in <110> single crystal silicon using a full-wet etching procedure including local oxidation of silicon (LOCOS) and employing an adapted

edge lithography technique on top of conventional photolithography. Ridges down to 10 nm in width have been produced. The silicon ridges have no inbuilt stress and are therefore less fragile than previously fabricated oxide ridges. The ridge sample is used as a template in T-NIL and a full 100 mm wafer size imprint has been successfully carried out in both polymethylmethacrylate (PMMA) and mr-I 7020E polymer. Moreover, the imprinted pattern in PMMA is subsequently transferred into a device wafer.

A multi-Si nanoridge fabrication scheme and its application in nanoimprint lithography (NIL) are presented in Chapter 4. Triple Si nanoridges approximately 120 nm high and 40 nm wide separated by 40 nm spacing are fabricated and successfully applied as a stamp in nanoimprint lithography. The fabrication scheme, using a full-wet etching procedure in combination with repeated edge lithography, consists of hot H_3PO_4 acid SiN_x retraction etching, 20% KOH Si etching, 50% HF SiN_x retraction etching and LOCal Oxidation of Silicon (LOCOS). Si nanoridges with smooth vertical sidewalls are fabricated by using Si <110> substrates and KOH etching. The presented technology utilizes a conventional photolithography technique, and the fabrication of multi-Si nanoridges on a full wafer scale has been demonstrated.

In Chapter 5, Si dry plasma etching technique is employed to integrate with advanced edge lithography method for nanoridge fabrication to avoid the dependence on Si crystalline orientation as to create Si nanoridges with arbitrary contours. We demonstrate the possibility of creating arbitrary contours by using a mask containing circular contour structures. Si etching using SF_6/O_2 gas mixtures performed at cryogenic temperature using Alcatel/Adixen AMS 100 SE deep reactive ion etching (DRIE) system is explored and proven capable of providing a Si etch rate of ca. 70 nm/min with a smooth surface finish. The explored etching recipe is first used in combination with Cr functioning as the masking material. Although nanoridges with perfectly vertical sidewalls can be achieved, the introduction of Cr causes severe sidewall roughness due to Cr layer line edge roughness. Therefore, SU-8 2000.5 is later introduced as a proper material for pattern definition as well as a mask during Si cryogenic etching. Although the initial SU-8 pattern definition needs further improvement, we successfully demonstrate the fabrication of Si nanoridges having arbitrary contours with a smooth surface finish.

Chapter 6 presents the creation of nanostructures by means of self-assembly, microcontact printing (μCP) and capillary force lithography (CFL). The fabricated Si nanoridges with sub-100 nm width described in Chapter 3 are employed for high resolution pattern definition in thermal nanoimprint lithography (T-NIL) and CFL. T-NIL is successfully implemented with self-assembly and μCP respectively to function as alternative nanofabrication approaches. The thesis ends up with conclusions and outlook to the project.

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Chapter 2

Fabrication of a silicon oxide stamp by edge lithography reinforced with silicon nitride for nanoimprint lithography[1]

In this chapter, the fabrication of a stamp reinforced with silicon nitride is presented for its use in nanoimprint lithography. The fabrication process is based on edge lithography using conventional optical lithography and wet anisotropic etching of <110> silicon wafers. SiO_2 nanoridges of 20 nm in width were fabricated. A silicon rich nitride layer is deposited over the original SiO_2 nanoridges to improve the ridge strength and to achieve a positive tapered shape which is beneficial for nanoimprinting. A replica of the nanoridges with silicon rich nitride shield is obtained by imprinting the stamp into thermoplastic nanoimprint polymer mr-I 7010E.

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2.1 Introduction

Nanoimprint lithography (NIL) is an emerging lithographic technology that promises high-throughput patterning of nanostructures. NIL has its merits in directly fabricating patterns of nano-scale from a single hard stamp regardless of optical lithography limitations. The stamp used in NIL has the same functionality and importance as the mask used in conventional photolithography. There are two major NIL methods available: step and flash imprint lithography (S-FIL) [1] and thermal NIL [2]. In S-FIL, a low-viscosity photocurable monomer is dispensed onto a substrate. A transparent stamp, which can be made from fused silica for example, is brought into contact with monomer. After UV exposure the patterned and hardened polymer is ready for the next steps. Thermal NIL was first introduced by the Chou's group in the mid-1990s [2]. Although the stamps prepared for thermal NIL should be strong enough to stand the high pressure during imprint, transparency is not an issue and basically any hard material can be used. The critical points need to be considered when choosing a proper material for thermal NIL stamp fabrication including material hardness, material thermal expansion coefficient and compatibility with conventional micro-fabrication principles [3]. In thermal NIL a widespread choice of stamp material is silicon with an oxide layer on top. To obtain nanostructures in imprint with high resolution, the primary concern is to fabricate a stamp with high resolution. At present, electron beam lithography (EBL) is the most standard means of fabricating stamps with high resolution [4, 5, 6].

Except for EBL, edge lithography has also been explored as a method for thermal NIL stamp fabrication. Edge lithography can be referred to as selectively depositing or removing materials on the edges which are defined by photolithography. As an example, Choi *et al.* introduced a silicon nanowire fabrication scheme by edge lithography, in which material deposited at the edges of a pattern defined by conventional photolithography was used as the etching mask to achieve the final nano-sized features using dry etchingmethods [7]. This fabrication scheme was further integrated with deep UV lithography to increase pattern density for nanoimprint utilization [8] and mold-to-mold cross imprint (MTMCI) [9]. As another example, Grabiec *et al.* demonstrated a NIL stamp fabrication scheme using local oxidation of silicon [10]. In this fabrication process, the pattern was defined by conventional UV lithography and dry etching was employed to transfer the pattern into silicon nitride and then poly-silicon, which were deposited on the transparent quartz substrate. Vertical silicon sidewalls were achieved and then dry oxidized using the silicon nitride layer as the mask. Nano-width SiO_2 lines on quartz substrate were achieved after removal of the protective silicon nitride and then silicon. To obtain the vertical

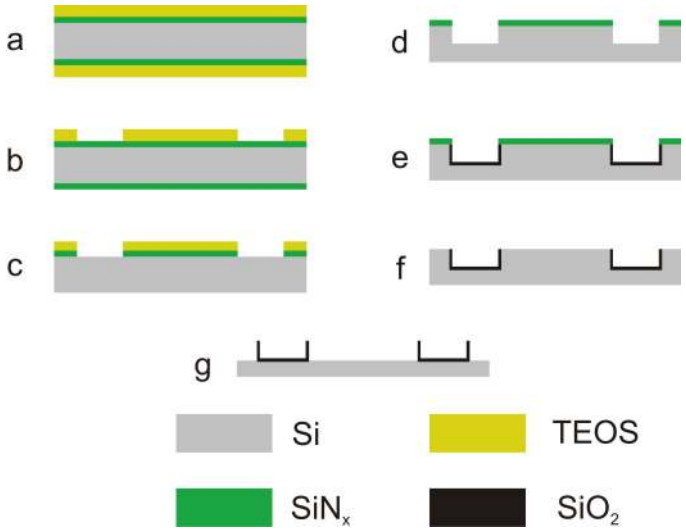

Figure 2.1: Illustration of SiO_2 nanoridge fabrication process

sidewalls, the dry silicon etching step in [10] was substituted by KOH anisotropic silicon etching when a mono-crystal <110> silicon substrate was used [11]. This anisotropic wet <110> silicon etching method results in vertical and smooth silicon sidewalls due to the automatic etching stop on silicon <111> planes.

Previously we reported the fabrication of a nanoimprint stamp having SiO_2 nanoridges [12] using a somewhat similar approach to that described in [11]. Our SiO_2 nanoridge fabrication scheme uses a whole wet etching scheme. To further develop the SiO_2 nanoridge fabrication technology, this chapter concentrates on the extension and analysis of the fabrication method. The mechanical strength and shape of nanoridges are improved by depositing a layer of silicon rich nitride over the original SiO_2 nanoridges. Examples of using this reinforced stamp for nanoimprint are demonstrated in thermoplastic nanoimprint polymer mr-I 7010E.

2.2 Experimental details

2.2.1 NIL stamp fabrication

Figure 2.1 illustrates the SiO_2 nanoridge stamp fabrication process. For detailed experimental descriptions, readers could refer to [12]. Here we concisely present the experimental data for ease of understanding.

(a) Starting with a 100 mm <110> silicon wafer, a 15 nm thick silicon rich nitride (SiN_x) layer is deposited (LPCVD) followed by a 40 nm conventional LPCVD TEOS (silicon oxide formed by decomposing TetraEthylOrthoSilicate [13]).

(b) A photolithography technique is employed to pattern the prepared substrate using resist with a mask containing a 4 μm line grating pattern. The grating pattern covers the whole 100 mm silicon wafer surface. This pattern is transferred into a TEOS layer using 1% HF.

(c) After removing the photoresist, 85% H_3PO_4 acid heated up to 180°C is used to pattern the SiN_x by using TEOS as the mask.

(d) The TEOS is removed in 1%HF. Then the patterned SiN_x is transferred into the silicon substrate using OPD4262 as the etchant, which has a TMAH concentration of 2.5%.

(e) The area on the silicon substrate which is not protected by SiN_x is dry oxidized at a temperature of 950°C. This is also called LOCOS (local oxidation of silicon) [14, 15].

(f) Then 180°C 85% H_3PO_4 acid is used again to remove the SiN_x mask layer.

(g) The fabrication of SiO_2 nanoridges is completed by etching back into silicon using OPD4262.

2.2.2 Nanoimprint lithography

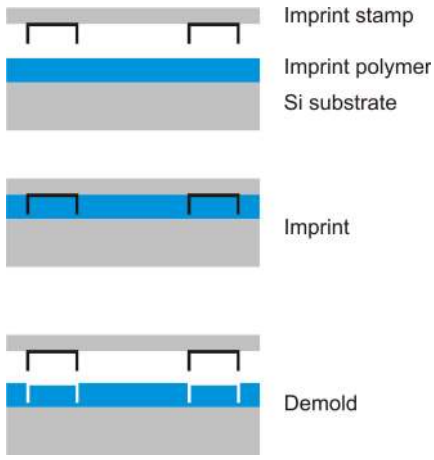

Figure 2.2: Illustration of nanoimprint lithography using nanoridge stamps

Figure 2.2 is a simple illustration of thermal NIL. First a substrate, silicon for example, with a spin-coated thermal plastic polymer is prepared. Then the imprint stamp is

brought into contact with the imprint resist. In the imprint step, a temperature about 70°C to 80°C higher than the imprint polymer glass transition temperature T_g is added [3]. A high pressure according to a different imprint polymer requirement is applied after the specific temperature is reached and kept for a few minutes. In the demold step, the pressure is released after the temperature is decreased a few celsius lower than T_g and then the stamp is separated from the imprint polymer. Reactive ion etching (RIE) can be employed to remove the residue layer for further pattern transfer to the substrate. Thermoplastic imprint polymer mr-I 7010E (Microresist Technology GmbH) is used as the imprint polymer in our experiment. It has a glass transition temperature of 60°C. The imprinting using this polymer can be performed at an imprint temperature from 125°C to 150°C, pressure from 20 to 50 bar, imprint time from 1 to 4 min and demold temperature from 40°C to 60°C [16].

2.3 Results and discussion

2.3.1 TEOS patterning

In Figure 2.1(b), 1% HF is used as the etchant to pattern TEOS. The etch rate of TEOS in 1% HF is about 30 nm/min [17]. Visual inspection of the etching stop is not possible in this step since the underlying SiN_x shows also hydrophilic surface characteristics like the TEOS layer. Therefore, 3 min etch, almost 100% over-etch, is carried out to ensure complete pattern transfer.

2.3.2 SiN_x patterning

Phosphoric acid heated up to 180°C is used twice to etch SiN_x: step (c) and step (f) in the fabrication scheme. It is known that the etch rate of SiN_x in 85% H_3PO_4 at 180°C is about 4 nm/min [17]. According to this etch rate, in step (c), the 15 nm thick SiN_x should be finished patterning in 4 min. Completion of the etch can be indicated by observing water running along the 4 μm grating pattern since a silicon substrate has hydrophobic surface characteristics. However, at least 6 min is needed to receive this visual information. We can explain this discrepancy by noting that there is neither a loadlock nor nitrogen blow during wafer loading in the silicon rich nitride low pressure chemical vapor deposition tube in our cleanroom. Therefore air can flow into the tube where the standby temperature is kept at 700°C during wafer loading. It is expected that a thin native oxide layer is formed on the wafer surface during the loading process in spite of the native oxide removal (by using 1% HF) before deposition. As the etch rate of

thermal SiO_2 in 180°C 85% H_3PO_4 acid is 0.3 nm/min [17], the formation of this oxide layer can be the reason causing the prolonged SiN_x etching. The 40 nm TEOS layer is thick enough to serve as SiN_x patterning mask since the etch rate of TEOS in 85% H_3PO_4 is 2.1 nm/min [17].

Concerning SiN_x removal in step (f), 9 min etching time of SiN_x is needed if the previous LOCOS step is set around 30 min. This prolonged etching time can be explained by the fact that SiN_x is oxidized during LOCOS [18]. For example, it is found that when the oxidation time is increased from 30 min to 3 h, the etching time is increased from 9 min to 15min accordingly. It can be concluded that the etching time of SiN_x after LOCOS depends on the oxidation time. Finally, a few nanometers of SiO_2 will be consumed in this SiN_x removal step.

2.3.3 Silicon dioxide nanoridges

As mentioned in the experimental section, the SiO_2 nanoridges are made by dry oxidation at 950°C. Dry oxidation is selected considering wafer uniformity. Oxidation temperature cannot go beyond 1100°C, otherwise the protective SiN_x can go through compositional change, which consequently influences the subsequent etching process [17]. The height of the SiO_2 nanoridges is mainly determined by wet silicon etching using OPD4262 (about 3.7 nm/min at 20°C [12]), Figure 2.1(d), and the thickness can be tuned by oxidation time, Figure 2.1(e). Figure 2.3 is an electron scanning microscopy (SEM) picture showing a SiO_2 nanoridge having a maximum width of 20 nm after 25 min LOCOS. Figure 2.4 illustrates a SiO_2 nanoridge having a maximum width of 80 nm after 3 h LOCOS.

The grating pattern defined on the photoresist generally has rough edges due to the limitation of the optical lithography technique, which is limiting the nanoridge dimension accuracy. To avoid this unwanted roughness, the pattern is transferred into <110> silicon wafer using anisotropic wet etching (OPD4262) which stops smoothly at silicon <111> planes. OPD4262 has a TMAH content of 2.5% and it gives the bottom <110> surface a smooth finish after etching. Therefore we can end up with straight and smooth vertical silicon <111> sidewalls which are in contrast to the much rougher sidewalls found in [19, 10] as well as a smooth bottom surface, as shown in Figure 2.5. The height and width of the SiO_2 nanoridges can be deliberately tuned by silicon etching time and oxidation time, respectively. In other words, the aspect ratio of the SiO_2 nanoridges can be as high as needed. However, the mechanical strength of the SiO_2 nano-ridges is limited due to compressive stress and the fragile corner, as will be explained further on. Nevertheless, in our experiments, SiO_2 nanoridges having a high aspect ratio with a height of 150 nm

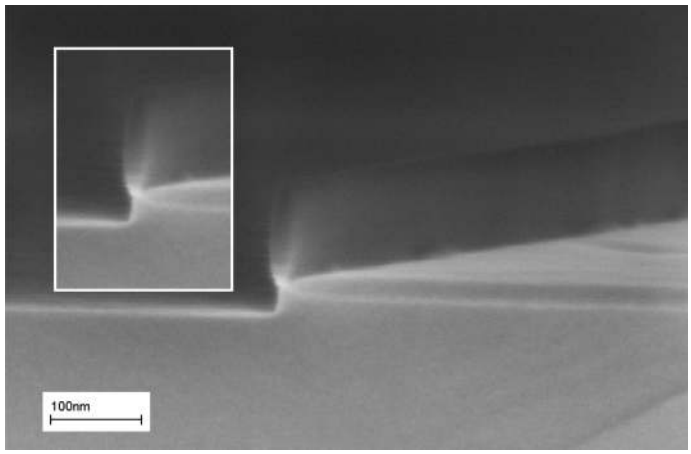

Figure 2.3: SEM picture of a SiO_2 nano-ridge having a maximum width of 20 nm with individual nanoridge zoom-in.

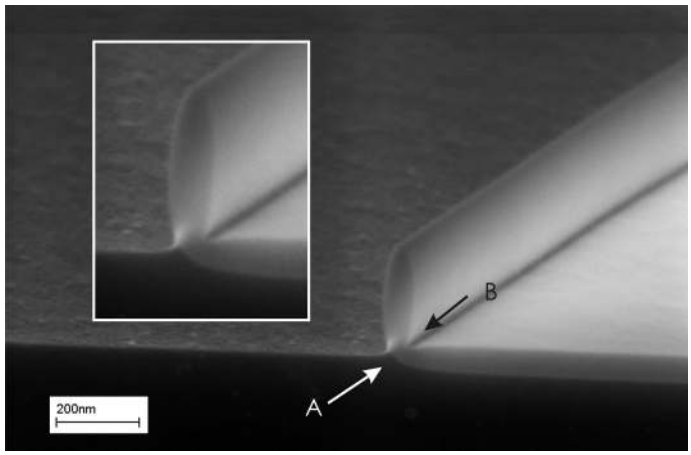

Figure 2.4: SEM picture of a SiO_2 nanoridge having a maximum width of 80 nm with individual nanoridge zoom-in.

and a maximum width of 20 nm are fabricated successfully. In another experiment it was possible to fabricate SiO_2 nanoridges of 15 nm in width and 100 nm in height. However, the nanoridges were not strong enough to withstand the handling before taking the SEM picture and broke as shown in Figure 2.6. It is expected that this fragile profile is also limiting in a thermal NIL process.

The fragile shape of the SiO_2 nanoridges is inherent to the oxidation process. Marcus

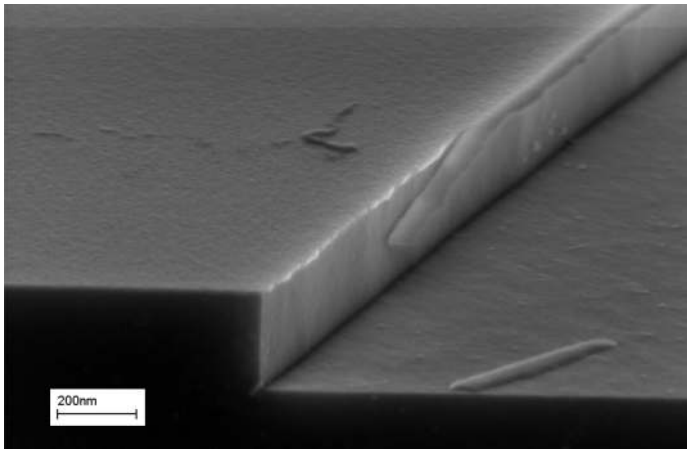

Figure 2.5: Silicon etching with SiN_x mask using OPD4262 finished with smooth <110> and <111> silicon planes.

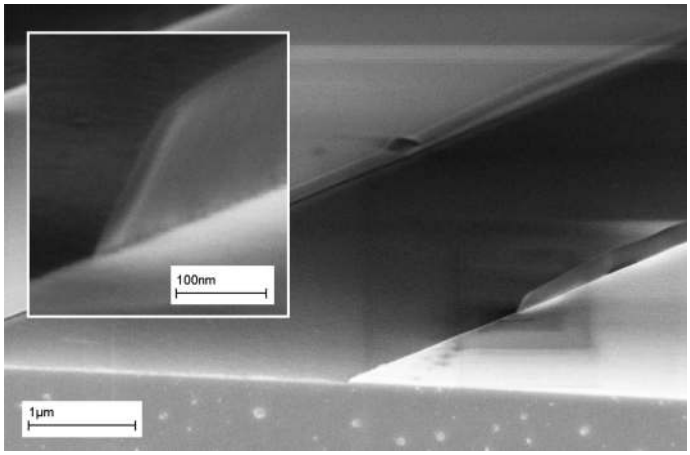

Figure 2.6: SEM picture of a SiO_2 nanoridge having a maximum width of 15 nm with individual nanoridge zoom-in.

and Sheng studied the oxidation on shaped silicon surfaces [20]. A schematic drawing of the oxidation of silicon at shaped surfaces is shown in Figure 2.7. The convex corner is rounded, while the concave corner is sharpened after oxidation. The rounding and sharpening effects at the corner lead to the non-uniform silicon oxide layer thickness: d is thinner than both w and h. In Figure 2.3 and Figure 2.4, we can clearly observe the rounding and sharpening effects and the non-uniform thermal oxide thickness. In

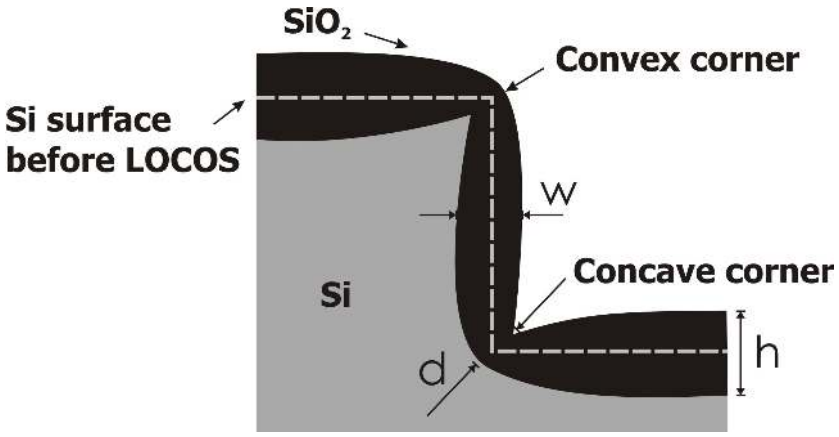

Figure 2.7: Schematic drawing of oxidation of silicon at shaped surfaces.

addition, Marcus *et al.* also pointed out that the formation of non-uniform thick thermal oxide is due to the stress configuration when the nonplanar silicon surface is oxidized at a temperature lower than 1050°C to 1100°C. If oxidized at a temperature higher than 1050°C to 1100°C, oxide can flow as a consequence of decreased viscosity and hence the stress is released [21]. In our case, we cannot increase the temperature higher than 1100°C, otherwise the SiN_x mask layerwill experience a compositional change, as discussed in section 3.3. Therefore we cannot avoid the fragile silicon oxide corner in this fabrication process.

As the main object of making the nanoridges is for thermal NIL, the ridges should be strong enough to withstand imprint conditions, say, high temperature and high pressure. The SiO_2 nano-ridges can survive the high temperature and high pressure. The thinning effect at the corner of a SiO_2 nanoridge brought by LOCOS, as shown in Figure 2.7, also referring to points A and B in Figure 2.4, however, can be a critical point since it may lead to the nanoridge broken during demolding in thermal NIL, especially when it is completely or partly exposed, referring to Figure 2.3 and Figure 2.4, respectively. Moreover, thermal oxidation of silicon creates high compressive stress in the grown oxide layer. We believe that this stress might cause buckling effects which would result in fracture. The silicon etching depth in Figure 2.1(g) can be tuned less deep than that in Figure 2.1(d), as the example in Figure 2.8 shows. But it cannot help avoid the fracture of the nanoridges due to the highly compressive stress of silicon oxide.

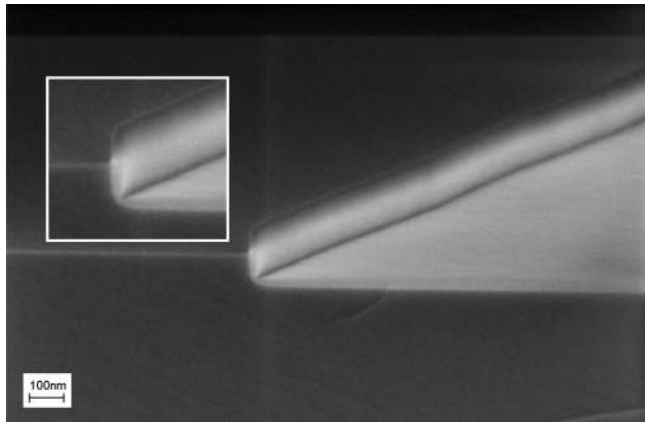

Figure 2.8: SEM picture of a SiO_2 nanoridge strengthened by tuning the second silicon etching step less deep (referring to Figure 2.1 step (g)) with individual nanoridge zoom-in.

2.3.4 Nanoridges with a SiN_x shield

To overcome the problem brought by the fragile corner and compressive stress of SiO_2 nanoridges, we chose to deposit another layer of SiN_x after step (g) in the fabrication scheme. SiN_x is chosen because it is a harder material compared with SiO_2 and it adds tensile stress which compensates the compressive stress brought by SiO_2. Figure 2.9 illustrates a SiN_x nanoridge of 120 nm in width. The SiN_x is deposited over a sample

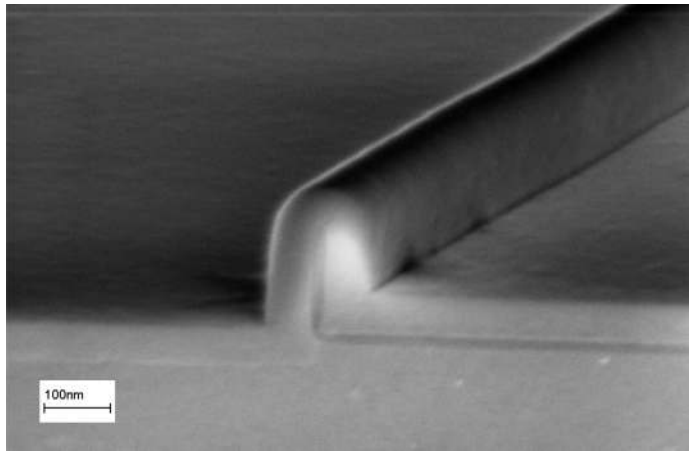

Figure 2.9: SEM picture of a SiN_x nano-ridge of 120 nm in width.

of SiO_2 nanoridges having a maximum width of 20 nm. LPCVD SiN_x gives a conformal coverage over the original SiO_2 nanoridges. In Figure 2.9, it is not difficult to see the over-etch in silicon in accordance with step (g) of the fabrication scheme. The over-etch, which went beneath the bottom of SiO_2 layer, together with the thinning corner of the SiO_2 nanoridges, was covered by SiN_x. The additional SiN_x deposition results in nanoridges with a sidewall angle slightly larger than 90° on both sides. Moreover, deposition also leads to a rounded top surface [13].

The nanoridges with a SiN_x shield have their merits in stronger ridge strength and slightly positive tapered shape compared with the original SiO_2 nanoridges. The conformal coverage provided by SiN_x deposition removes the fragile corner brought by the oxidation process, as indicated by points A and B in Figure 2.4. Together with stress compensation of SiN_x to SiO_2, this additional SiN_x deposition makes the nanoridges stronger. The improved stiffness enables the stamp to be reusable in NIL; and the positive tapered shape is advantageous for easy demolding. We can observe from Figure 2.9 that by additional SiN_x deposition the height of the nanoridges remains the same as before while the width of the nanoridges is enlarged on both sides of the SiO_2 nanoridge. The SiN_x shield will widen the width of the SiO_2 nanoridge and decrease the aspect ratio. To minimize the loss of aspect ratio, a thinner layer of stoichiometric silicon nitride (Si_3N_4) may be used in stead since stoichiometric silicon nitride has a higher tensile stress than low-stress silicon rich nitride.

2.3.5 Nanoimprint lithography by using a SiN_x reinforced nanoridge stamp

The samples with nanoridges fabricated are used as stamps for thermal NIL. After cleaning the imprint stamp in Piranha solution (H_2SO_4:H_2O_2=3:1), a monolayer of 1H,1H,2H,2H-perfluorodecyltrichlorosilane (PFDTS), which acts as the antiadhesion layer, is coated in the gas phase under vacuum conditions in a desiccator. Since PFDTS works with the hydroxylic group on the silicon dioxide surface or silicon surface with a native oxide layer, the imprint stamp with silicon nitride nanoridges is first dry oxidized at 950°C for 1 h to convert the top SiN_x layer into silicon oxide [18]. Actually it has been reported that a native oxide layer exists on the silicon nitride surface and hence further silanization is possible [22]. We find that PFDTS can indeed be coated on the SiN_x stamp since the surface turns from hydrophilic into hydrophobic. However, experimental evidence showed that the SiN_x stamp can be demolded much easier when PFDTS is coated on the stamp which goes through dry oxidation treatment. Full 100 mm wafer size imprint

is done using the Obducat thermal-imprint machine (Obducat, Sweden). The imprint process using mr-I 7010E is carried out at a temperature of 140°C and pressure of 40 bar for 3 min. The demold temperature is 55°C. Figure 2.11 shows the imprint replica

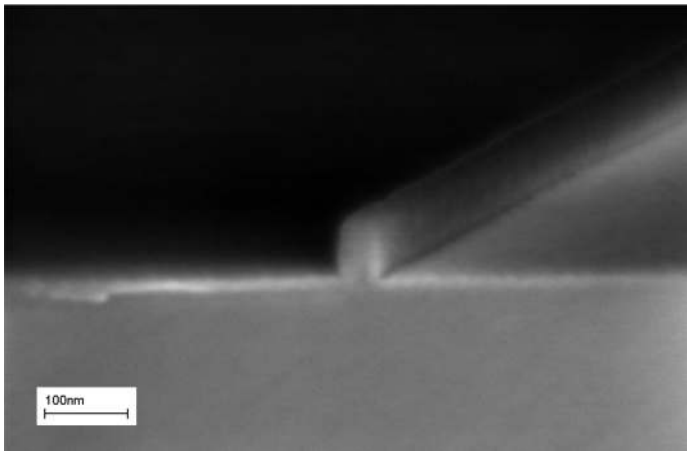

Figure 2.10: SEM picture of the imprint stamp: SiN_x nanoridge with a height of 80 nm and width of 40 nm.

with cross-section view of the SiN_x nanoridge of 80 nm height and 40 nm width shown in Figure 2.10. Since the imprint polymer mr-I 7010E gave a thickness of 100 nm, we tuned the imprint with the stamp having a feature height below 100 nm.

2.4 Conclusions

We presented the nanoimprint stamp fabrication of SiO_2 and SiN_x nanoridges using edge lithography and wet anisotropic etching <110> silicon wafer. The nanoridges were fabricated out of micron-sized structures defined by conventional optical lithography. The maximum width of the SiO_2 nanoridges can be tuned from 20 nm to around 100 nm depending on the oxidation time. The shape of the SiO_2 nano-ridge is an intrinsic characteristic in oxidation. The strength of the SiO_2 nanoridges can be improved by tuning the silicon etching time in step (g) to be less than that in step (d) in the fabrication scheme, comparing Figure 2.3 with Figure 2.8. Another option for strengthening is to deposit a layer of SiN_x over the original SiO_2 nanoridges. Experiments showed that the extra SiN_x deposition over the SiO_2 nano-ridges strengthened the nanostructures and consequently made the imprint stamp reusable. The stamp replication in mr-I 7010E

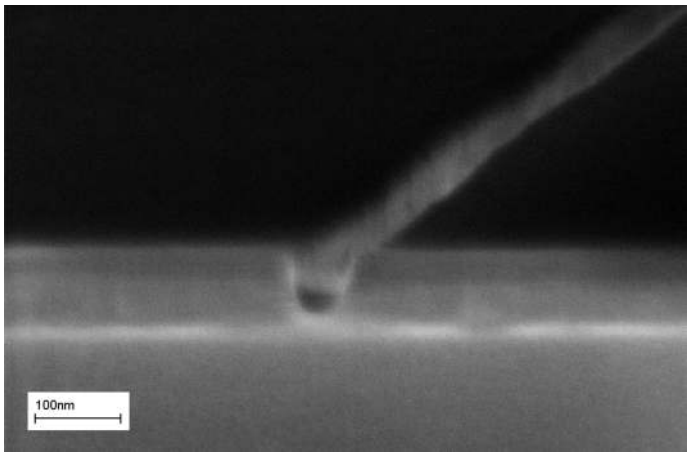

Figure 2.11: SEM picture of the imprint replica in mr-I 7010E using the stamp shown in Figure 2.10.

using SiN_x nanoridges is obtained by using NIL. Although the strength and shape of the nanoridges are improved by this additional SiN_x deposition, it may lead to the loss of the original SiO_2 nanoridge aspect ratio. It is expected that stoichiometric silicon nitride (Si_3N_4) deposition may minimize this loss since it has a higher tensile stress and hence a thinner layer is effective to perform the stress compensation.

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Chapter 3

Sub-10 nm silicon ridge nanofabrication by advanced edge lithography for NIL applications[1]

A new nanofabrication scheme is presented to form stamps useful in thermal nanoimprint lithography (T-NIL). The stamp is created in a <110> single crystalline silicon wafer using a full-wet etching procedure including local oxidation of silicon (LOCOS) and employing an adapted edge lithography technique on top of conventional photolithography. Ridges down to 10 nm in width have been produced. The silicon ridges have no inbuilt stress and are therefore less fragile than previously fabricated oxide ridges. The ridge sample is used as a template in T-NIL and a full 100 mm wafer size imprint has been successfully carried out in both polymethylmethacrylate (PMMA) and mr-I 7020E polymer. Moreover, the imprinted pattern in PMMA is subsequently transferred into a device wafer.

[1]This chapter has been published in: Y. Zhao, E. Berenschot, H. Jansen, N. Tas, J. Huskens and M. Elwenspoek, Sub-10 nm silicon ridge nanofabrication by advanced edge lithography for NIL applications, *Microelectronic Engineering*, 86(4-6):832-835, 2009

3.1 Introduction

In 2005 Gates *et al.* published an overview on new approaches to nanofabrication [1]. In their work they also considered (old) conventional processes like photolithography (mainstream production using the parallel printing technique) and scanning beam lithography such as electron beam lithography (EBL, mainly a high-fidelity production and repair serial writing technique). Printing technology evidently has the major advantage over beam writing, which enables patterning of large areas in a single shot.

Nevertheless, intense commercial pressure to ever downscale the feature's dimensions (for better performance with respect to information storage and signal processing, new functionalities such as quantum effects, and/or reduced costs) has let to a variation of novel techniques which could become the standard in the near future [1, 2]. These techniques can be arranged in a few major categories. The first group consists of mechanical printing techniques such as thermal nanoimprint lithography (T-NIL, [3]), and step and flash imprint lithography (S-FIL, [4]). In both T-NIL and S-FIL the shape of the mould is transferred into mostly a polymer on top of a substrate. A second group is mechanical beam writing or scanning probe lithography (SPL) in which a mechanical stylus produces the pattern down to the atomic level. Finally, a large group of edge lithography (EL) is under development. In this technique the edges of the original pattern become the features of the final pattern (and, so, it has the ability to double a pattern). It is the latter technique which is the main topic of this study.

Although a multitude of possible schemes exists in EL, one attractive technique uses controlled deposition and/or undercutting of lithographically defined edges. In one of the oldest examples, Dean *et al.* fabricated a sub micrometer self-aligned dual gate GaAs FET using conventional photolithography and shadow deposition [5]. Later, Jelks *et al.* fabricated thin metallic lines on top of a glass substrate using shadow deposition and lift-off lithography [6]. Around the same time, Flanders *et al.* fabricated thin ridges by exploring shadow deposition in combination with wet anisotropic etching of <100> silicon [7] and Prober *et al.* opted for shadowing an ion beam etch to produce thin metallic lines [8]. In a similar approach, Flanders *et al.* showed a sequence of EL together with directional reactive ion etching (RIE), which allowed him in the successive multiplication of the number of lines in a grating pattern [9, 10]. Much later, Love *et al.* made a smart variation on the shadowing technique by performing a controlled undercut prior to the shadow deposition and was able to create ultra small trenches [11] and Tas *et al.* employed sacrificial layer etching from edges and subsequent surface tension drive assembly to construct 2D-confined nanochannels [12]. Finally, using the same concept

as proposed by Flanders, Choi *et al.* fabricated nanometer sized lines into single crystal silicon [13], which later evolved into a technique to produce dots instead of the usual contour lines, which is characteristic for EL [14].

All the above EL techniques have in common that they are the final product of nanoengineering. It is the quest of the current study to explore the usefulness of EL as an intermediate product in constructing stamps for T-NIL and thus reducing production costs drastically. Therefore, resolution, accuracy and strength are critical issues in order to compete with other stamp fabrication techniques (mostly EBL). In 2004, Gabriec *et al.* showed the fabricated of nano-lines for S-FIL purposes by lateral oxidation at the step edges of a pattern formed previously in a polysilicon layer by RIE [15]. Although this resulted in high resolution, accuracy is weak due to the use of RIE and polysilicon in conjunction with conventional print lithography. Moreover, no experiments were given to show its ability to transfer the pattern using neither T-NIL nor SFIL (the focus of their work). In an attempt to improve both accuracy and show its usage in T-NIL, Haneveld *et al.* created nanoridges by local oxidation of sharp edges in <110> silicon using a full-wet procedure with silicon nitride as an etch mask [16]. Smoothness and verticality of the structures are guaranteed by using wet anisotropic etching of the crystalline silicon [17]. Although structures were realized easily adjustable and very accurate between 7 and 20 nm wide, 40 to 150 nm high, and centimeters long they suffered from mechanical strength during T-NIL. This issue has been addressed in a follow-up paper by us and it was found that the compressive stress in the oxide ridge was the main cause of failure after successive T-NIL use [18]. The strength was improved by reinforcing the oxide ridge with tensile stressed nitride to compensate for the oxide stress. As an additional feature, easier demoulding characteristics was found during T-NIL due to improvements in the shape of the ridge. However, due to the extra layer of nitride, the original sub-30 nm resolution was lost.

Therefore, it is the purpose of the current paper to improve the weakness of the oxide ridges (fragile) or reinforced ridges (resolution) while keeping its strong points (accuracy). This is done by altering the process flow in such a way that silicon ridges are formed. Silicon is a widespread and accepted choice in T-NIL. It is our quest to find the (nano) limitations, usefulness and benefits of silicon templates using EL.

3.2 Fabrication

Figure 3.1 shows the single silicon ridge fabrication scheme using edge lithography. (a) A <110> silicon wafer is prepared with 15 nm low pressure chemical vapour deposition

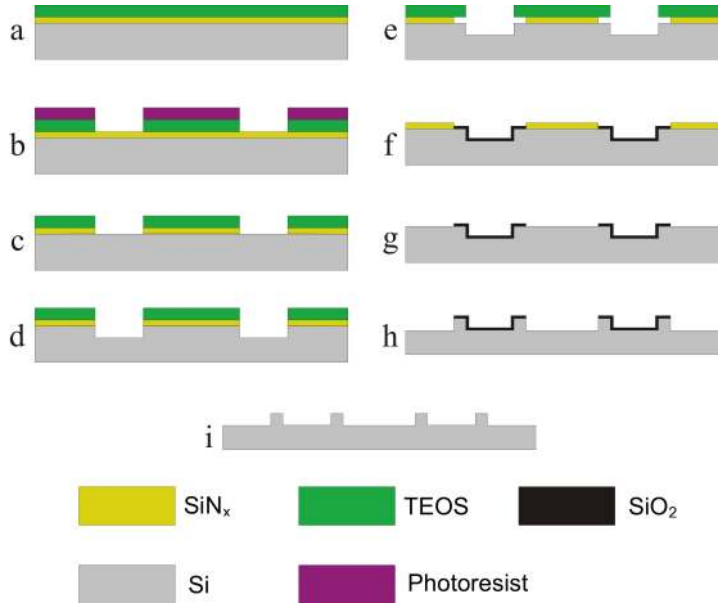

Figure 3.1: Fabrication scheme of silicon ridges by edge lithography.

(LPCVD) silicon rich nitride (SiN_x) and 80 nm LPCVD TetraEthylOrthoSilicate (TEOS) followed by annealing at 900°C for 1 h in nitrogen. (b) The prepared substrate is patterned by conventional UV photolithography using a mask containing a 4 μm grating pattern and resist (Olin 907-12). The grating is transferred from the resist into the TEOS using BHF (buffered HF, NH_4F/HF (7:1)) for 30 s. (c) After stripping the resist (fuming 100%HNO_3 acid), the nitride layer is etched in hot phosphoric acid (85%H_3PO_4 acid heated up to 180°C). (d) Subsequently, the silicon is anisotropically etched in OPD4262 (2.5%TMAH). (e) Undercuts are formed by etching nitride in hot phosphoric acid. (f) After TEOS removal in 1%HF, the wafer is dry oxidized at a temperature of 950°C for 5 min using nitride as a mask, which is also referred as LOCal Oxidation of Silicon (LOCOS) procedure. (g) The nitride layer is stripped in hot phosphoric acid. (h) Anisotropic silicon etching is performed in OPD4262. (i) Finally, the silicon ridge is obtained after removing the oxide in 1%HF. A scanning electron microscope (SEM) picture of a silicon ridge is shown in Figure 3.2. It shows a ridge 100 nm in height and only 10 nm in width having almost perfectly straight and smooth sidewalls. This is the consequence of the ability of the OPD solution to remove surface irregularities at <111> planes and these planes are exactly the planes of the sidewalls of the silicon ridges we observe in the picture.

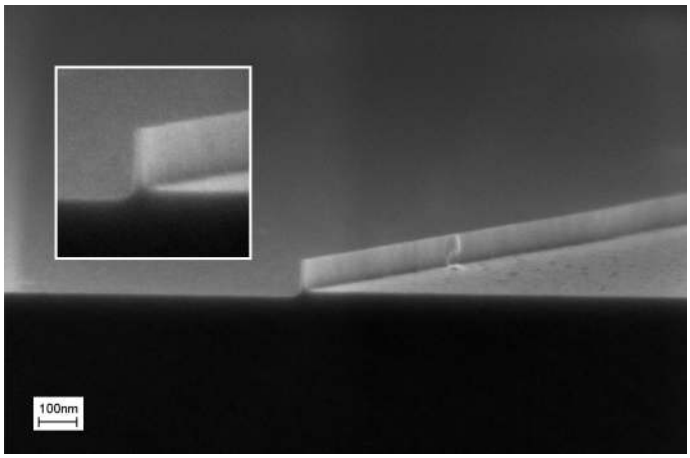

Figure 3.2: SEM image of a 10 nm wide and 100 nm high silicon ridge.

3.3 Discussion

The annealing step increases the selectivity between the nitride and TEOS in hot phosphoric acid, which is 1.4 (4.2 nm/min to 2.9 nm/min) without annealing and 7.6 (4.2 nm/min to 0.55 nm/min) after 900°C annealing [19]. The 80 nm thick TEOS together with the increased selectivity allows controllable undercuts from the nitride layer. The vertical sidewall in step (d) is achieved by wet anisotropic etching of <110> silicon in OPD 4262, which is discussed extensively in our previous publications [17, 16, 18].

The height of the ridge is determined by the etch times in steps (d) and (h), while the width is in the first place determined by the nitride undercut in step (e). However, the etch selectivity between a <110> and <111> silicon plane is about 5:1 in OPD4262. This means that about 20 nm of the <111> surface is etched during the etching of 100 nm <110> silicon. Using this selectivity and the etch rates of both Si and SiN_x, the dimension of the silicon ridge can be well estimated and controlled. For example, to fabricate Si nanoridge with a certain height, the width can be calculated by subtracting two times the undercut in Si from the undercut in SiN_x.

It is observed in Figure 3.3 that the top surface of the ridge is not perfectly flat. The height of side B is lower and more rounded than side A. This is because the exposed silicon (side B) is also etched in hot phosphoric acid while performing the undercut in fabrication step (e) while side A is still protected. Therefore, the tilted silicon shape depends on the nitride-to-silicon selectivity in hot phosphoric acid and this issue should be improved or at least considered in future template fabrication.

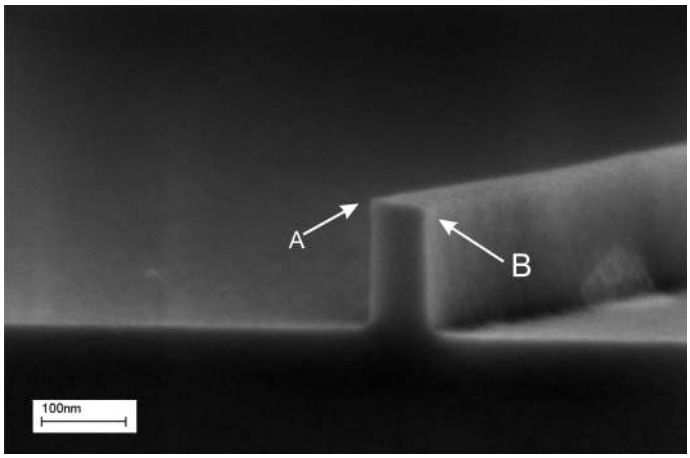

Figure 3.3: SEM image of a 40 nm wide and 100 nm high silicon ridge.

3.4 Imprint and pattern transfer

The fabricated EL stamp with ridges is used in T-NIL. Before imprint, the wafer template is cleaned in Piranha (H_2SO_4:H_2O_2 = 3:1) for 30 min, rinsed with DI water and spin dried. Then, a monolayer of 1H,1H,2H,2H-perfluorodecyltrichlorosilane is coated from a gas phase under vacuum condition in a desiccator [20]. This layer acts as the anti-adhesion layer on the mold to facilitate demolding. The imprint process using a full 100 mm wafer stamp is performed onto a device wafer coated with an imprint polymer using Obducat T-NIL machine (Obducat, Sweden). The imprint process has been repeated for many times using both PMMA (Acros) and mr-I 7020E (Microresist, GmbH). Figure 3.4 shows an imprint image in mr-I 7020E using a stamp with 40 nm wide and 100 nm high Si ridges. T-NIL using mr-I 7020E is carried out at 140°C and 40 bar for 3 min and the demold temperature is 55°C [21]. Imprint using PMMA (molecular weight of 35 kD obtained from Acros, Tg = 108°C, 160 nm film thickness can be obtained after spin coating 3 wt.% PMMA at 3000 rpm) is carried out at 180°C and 40 bar for 5 min and the demold temperature is 90°C. Experiments showed that wafer templates with ridges having a dimension of 150 nm in height and 30 nm in width could be used at least 20 times without any detectable failure.

To test how accurate the imprinted pattern is duplicated, the device wafer is etched with a state-of-the-art etch tool (Adixen AMS100SE DRIE) using the imprint polymer as a mask. Figure 3.5 and Figure 3.6 show the imprinted pattern in PMMA transferred into the silicon device wafer. The residual layer is first removed by O_2 RIE (Elektrotech

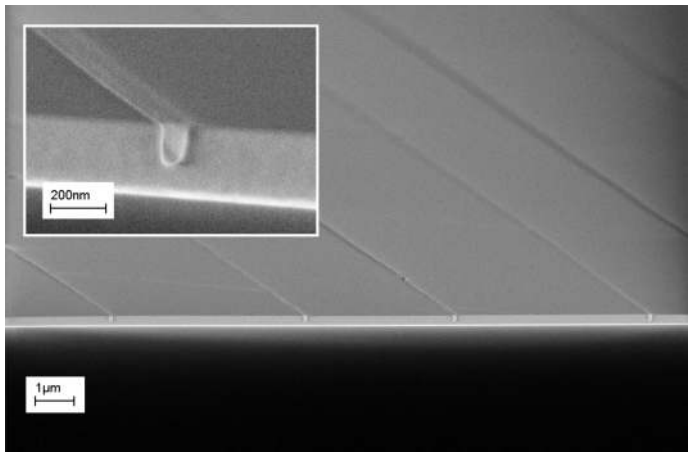

Figure 3.4: Imprinted ridges in mr-I 7020E using a stamp with 40 nm wide and 100 nm high Si ridges.

Twin system PF 340, pressure, 20 mTorr; O_2 flow, 20 sccm; power, 20 W) for 30 s. The imprinted trench with a width of 30 nm is enlarged to 50 nm after O_2 plasma bombardment. The thickness of PMMA layer decreases from 150 nm to approximate 100 nm after O_2 RIE. In the subsequent Si deep reactive-ion etching (DRIE), trenches with both an aspect ratio of 1:1 (Figure 3.5) and with a high aspect ratio of approximately 30:1 (Figure 3.6) can be achieved. Detailed explanations concerning DRIE can be referred

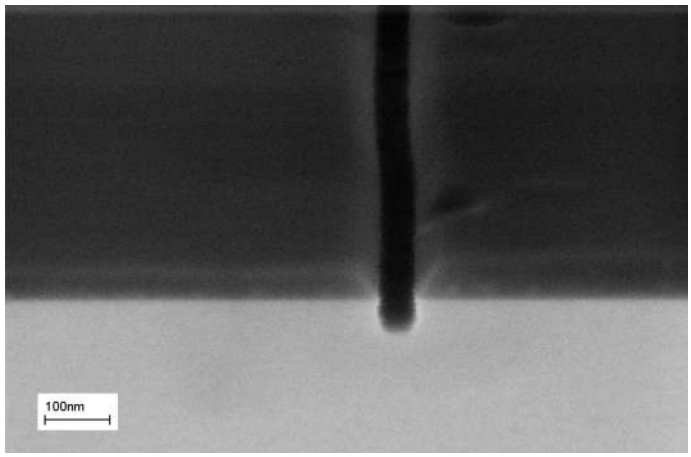

Figure 3.5: Pattern transfer from PMMA into a silicon device wafer: trench with an aspect ratio about 1:1.

to [22]. The undercuts and scallops observed at the sidewalls of the trenches in Figure 3.6 are caused by the pulsed mode DRIE procedure (SF_6/C_4F_8) and can be reduced by proper tuning of the etch tool but has not been the subject of the current study.

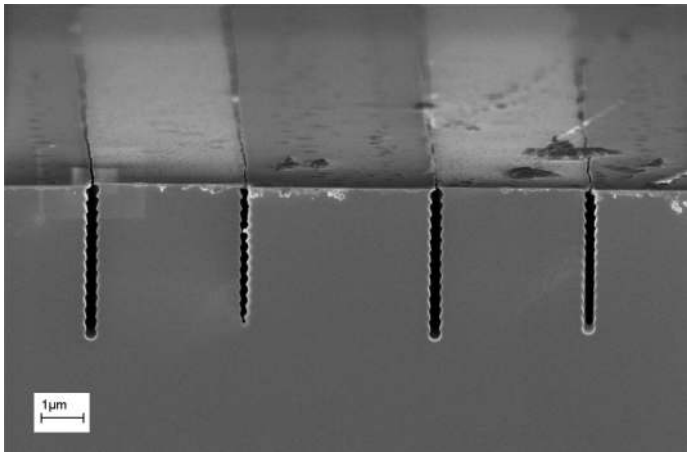

Figure 3.6: Pattern transfer from PMMA into a silicon device wafer: trenches with a high aspect ratio about 30:1.

3.5 Conclusions

We have demonstrated a novel edge lithography (EL) scheme. The approach is a completely wet and wafer-scale fabrication scheme of single crystalline silicon ridges for its application as master in thermal nanoimprint lithography (T-NIL). Its main distinguishing feature with respect to other competitive EL techniques is its ability to control both the width and height of the fabricated structure down to the 10 nm scale. The master is applied as template in T-NIL and successfully transferred into a Si device wafer.

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Chapter 4

Multi-silicon ridge nanofabrication by repeated edge lithography[1]

We present a multi-Si nanoridge fabrication scheme and its application in nanoimprint lithography (NIL). Triple Si nanoridges approximately 120 nm high and 40 nm wide separated by 40 nm spacing are fabricated and successfully applied as a stamp in nanoimprint lithography. The fabrication scheme, using a full-wet etching procedure in combination with repeated edge lithography, consists of hot H_3PO_4 acid SiN_x retraction etching, 20% KOH Si etching, 50% HF SiN_x retraction etching and LOCal Oxidation of Silicon (LOCOS). Si nanoridges with smooth vertical sidewalls are fabricated by using Si <110> substrates and KOH etching. The presented technology utilizes a conventional photolithography technique, and the fabrication of multi-Si nanoridges on a full wafer scale has been demonstrated.

4.1 Introduction

Beam writing techniques, such as electron beam lithography (EBL) and focused ion beam lithography (FIB), have become the conventional and standard means of nanofabrication.

[1]This chapter has been published in: Y. Zhao, E. Berenschot, H. Jansen, N. Tas, J. Huskens and M. Elwenspoek, Multi-silicon ridge nanofabrication by repeated edge lithography, *Nanotechnology*, 20:315305(7pp), 2009

To reduce the high cost and low throughput of nanofabrication using beam writing techniques, the fabrication of nano-structures employing unconventional methods has been an attractive research topic in nanotechnology [1]. Researchers have explored the possibilities of integration of micro-machining technologies, for example conventional photolithography, chemical vapor deposition of materials and micro-machining etching methods, into nanofabrication. Amongst all the unconventional methods, edge lithography is widely used and has proven to be a competent means of nanofabrication in combination with micro-machining technologies [2]. In edge lithography, the edges of the original pattern become the features of the final pattern.

Developed in a similar way to edge lithography, the spacer patterning technique (SPT) generally comprises: (1) sacrificial structures with vertical sidewalls patterned by photolithography and directional etching; (2) conformal deposition of another layer; (3) maskless directional etching of this layer; and (4) final selective etching of the sacrificial layer [3]. Several publications have demonstrated the fabrication of spacer-like structures employing similar working principles to SPT. Choi *et al.* demonstrated the fabrication of nanoscale phosphosilicate glass (PSG) complementary metal oxide semiconductor (CMOS) by conformal deposition of PSG over an SiGe block pattern defined by photolithography, reactive ion etching of this PSG and removal of the SiGe sacrificial pattern [4]. Degroote used a SPT in combination with resist based patterning to define a Si-Fin with a critical dimension below 20 nm [5]. Based on SPT, multi-SPT was developed by repeating a series of conformal deposition and anisotropic etching steps; it was shown to have potential in nanoelectronics applications [6, 7].

The multi-spacer patterns can also be created by a so-called planar edge defined alternate layer (PEDAL) process [8, 9]. The PEDAL process consists of: (1) fabrication of trench-like structures with vertical sidewalls; (2) alternating deposition of materials upon the trench-like structure, e.g. silicon nitride and polysilicon; (3) substrate planarization by a spin-coated polymer; (4) etch-back of the polymer, silicon nitride and polysilicon by RIE etching; and finally (5) selective polysilicon etching to obtain spacers made of silicon nitride. Hussain *et al.* employed a similar process flow to fabricate a template with Si nanowires for nanoimprint applications [10].

Generally, the critical dimensions of the spacers fabricated by either SPT or PEDAL are defined by the conformal layer deposition. The initial pattern with vertical sidewalls determines the verticality of the spacers. Both smoothness of the initial pattern sidewalls and selective dry etching influence the smoothness and the shape of the spacer sidewalls. In the previous chapter, we introduced a related but different technique - the fabrication of monocrystalline Si nanoridge by using a full-wet etch procedure including local oxidation

of silicon (LOCOS) and an adapted edge lithography technique on top of conventional photolithography [2]. Here, we present the fabrication of multi-monocrystalline Si nanoridges using repeated edge lithography, which consists of sequentially performed SiN_x retraction etching in hot H_3PO_4 acid, Si etching in KOH, SiN_x retraction etching in 50% HF and LOCOS.

4.2 Fabrication

The fabrication scheme for multi-Si nanoridges is shown in Figure 4.1: (A) 100 mm, double side polished, p-type Si <110> substrates are used. The substrate is prepared with 200 nm low pressure vapor deposition (LPCVD) silicon-rich nitride (SiN_x) and 50 nm LPCVD tetraethylorthosilicate (TEOS) annealed in a furnace with a N_2 atmosphere at 1050°C for 1 h. (B) The substrate is patterned by conventional photolithography using a resist mask (Olin 907-12) containing 4 μm gratings covering the whole wafer surface. The substrate is treated in UV/ozone for 300 s to increase the hydrophilicity of the photoresist to improve TEOS wet etching. Then the TEOS is patterned by buffered HF (NH_4F:HF = 7:1) for 45 s. Since the SiN_x surface shows hydrophilic behavior, like TEOS, about 10% over-etch is performed here to ensure complete pattern transfer. A dummy wafer with only a TEOS layer is used to test the etch rate. The completion of etching can be observed when the wafer surface turns from hydrophilic to hydrophobic. The etch rate of TEOS annealed at 1050°C in buffered HF is approximately 80 nm/min. (C) After stripping the photoresist in 100% HNO_3 for 20 min, the SiN_x is patterned in 85% H_3PO_4 heated up to 180°C (referred to as hot H_3PO_4 acid in the remainder of the paper) using TEOS as the mask for 55 min. The completion of etching can be observed when water runs along the patterned surface, since the Si surface shows hydrophobic characteristics. The etch rate of 1050°C annealed SiN_x and TEOS in hot H_3PO_4 acid is 3.9 nm/min and 0.29 nm/min, respectively [11]. The SiN_x etching is carried out with about 10% over-etch to ensure complete pattern transfer. (D) Before Si etching, TEOS is stripped in 1% HF for 20 min. Anisotropic Si etching is performed in 20% KOH used at room temperature (referred to as 20% KOH in the remainder of the paper) for 5 min and followed by RCA-2 cleaning (a mixture of $HCl:H_2O_2:H_2O$ of 5:1:1 at 80°C) for 10 to 15 min to remove contaminants harmful to the oxidation furnace in step F. The etch rate of Si <110> in 20% KOH solution is 25 nm/min. (E) Then SiN_x retraction etching is carried out in 50% HF for 25 min to obtain an opening on the Si surface. The etch rate of SiN_x in 50% HF dropped from 2.7 nm/min before annealing to 1.7 nm/min after annealing at 1050°C. (F) Subsequently the exposed Si part is dry oxidized at 950 °C

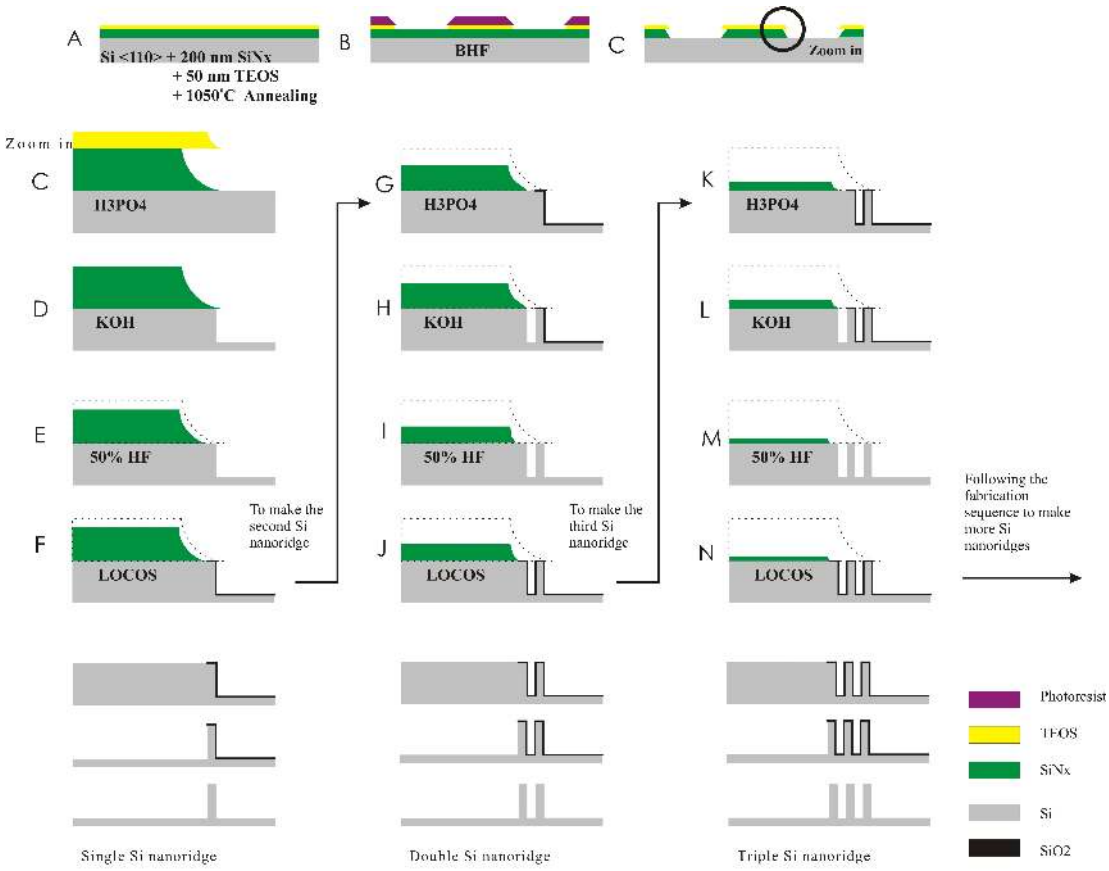

Figure 4.1: Multi-Si nanoridge fabrication scheme: (A)-(C) substrate preparation, grating pattern definition by photolithography and transfer into the top layers; (D) Si etching using 20% KOH; (E) SiN_x retraction etching using 50% HF; (F) LOCOS; (G)-(J) and (K)-(M) repeated edge lithography consisting of SiN_x retraction etching by hot H_3PO_4 acid, Si etching using 20% KOH, SiN_x retraction etching by 50% HF and LOCOS. The fabrication sequence can be stopped by SiN_x total removal using hot H_3PO_4 acid, Si etching in 20% KOH and final removal of SiO_2 in 50% HF.

for 15 min using SiN_x as the mask (the so-called LOCOS process). (G) SiN_x retraction etching is performed in hot H_3PO_4 acid for 8 min to make an opening in the Si surface. (H) Si etching in 20% KOH for 10 min. Figure 4.2 to Figure 4.6 show the fabrication results in accordance with steps (D) to (H).

This edge lithography scheme, which consists of hot H_3PO_4 acid SiN_x retraction etching (G, K), 20% KOH Si etching (D, H, L), 50% HF SiN_x retraction etching (E, I, M)

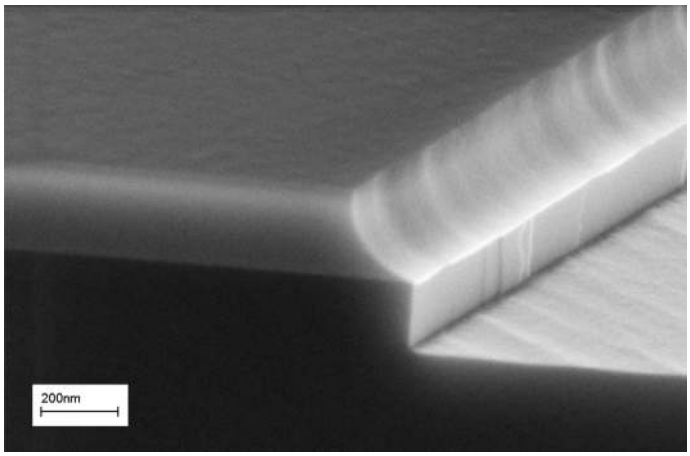

Figure 4.2: SEM image showing the etch result after step (D) of Figure 4.1: Si etching in 20% KOH for 5 min.

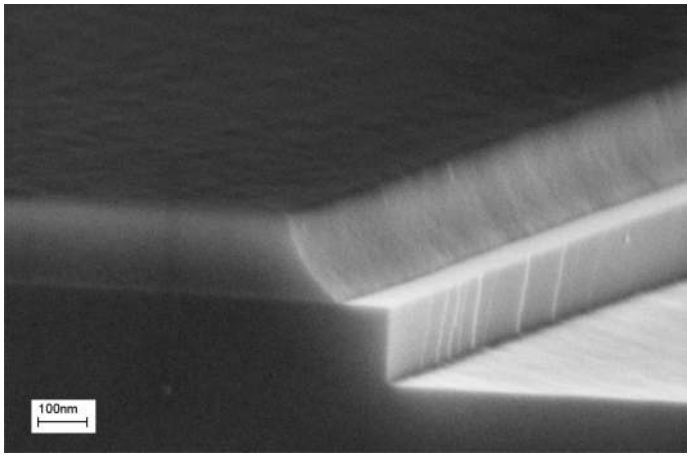

Figure 4.3: SEM image showing the result after step (E) of Figure 4.1: SiN_x etching in 50%HF for 25 min.

and LOCOS (F, J, N), is repeated to fabricate multi- Si nanoridges. By iterating the repeated edge lithography steps results in the second fabricated Si nanoridge illustrated in Figure 4.7 and Figure 4.8. By terminating the fabrication scheme, for example after step (F), (J) or (N), single, double or triple Si nanoridges can be obtained by complete removal of SiN_x in hot H_3PO_4 acid, Si etching in 20% KOH and then complete removal of SiO_2 in 50% HF. Stopped at step (N), Figure 4.9 and Figure 4.10 show examples of

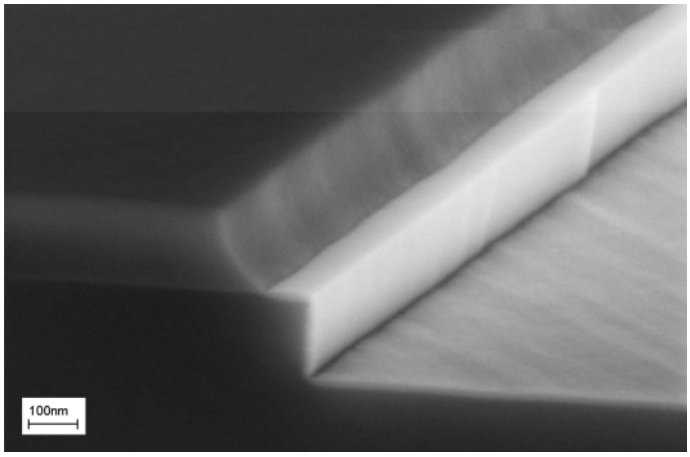

Figure 4.4: SEM image showing the result after step (F) of Figure 4.1: LOCOS at 950°C for 15 min.

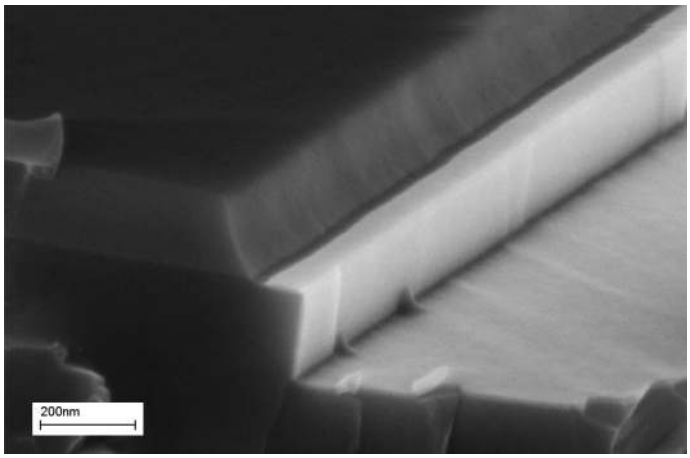

Figure 4.5: SEM image showing the result after step (G) of Figure 4.1: SiN_x etching in hot H_3PO_4 acid for 8 min.

triple Si nanoridges by complete removal of SiN_x in hot H_3PO_4 acid, Si etching in 20% KOH for 5 min and complete SiO_2 removal in 50%HF.

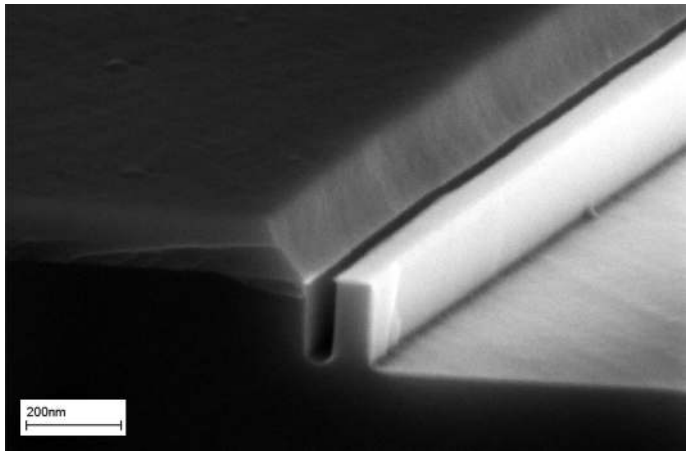

Figure 4.6: SEM image showing the result after step (H) of Figure 4.1: the first Si ridge is finished by anisotropic etching of Si in 20% KOH for 10 min.

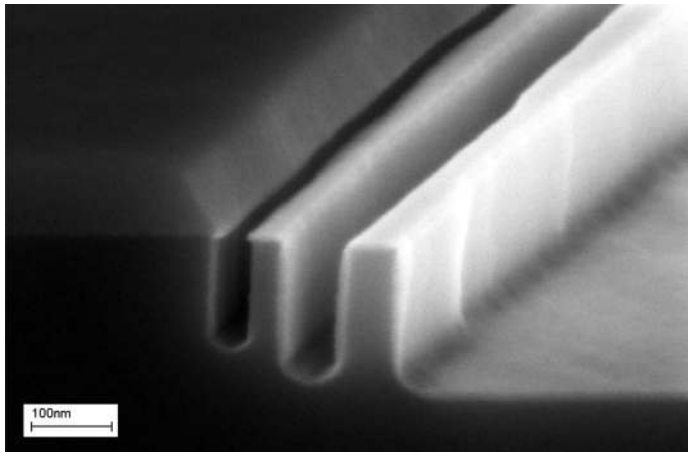

Figure 4.7: Continuation of Si nanoridge fabrication after Figure 4.6 by repeating 50% HF SiN_x retraction etching for 25 min, LOCOS at 950°C for 15 min, hot H_3PO_4 acid SiN_x retraction etching for 8 min and 20% KOH Si etching for 10 min.

4.3 Discussion

4.3.1 Substrate preparation and layer patterning

To illustrate the feasibility of the multi-Si nanoridge fabrication scheme, we chose to deposit 200 nm SiN_x and then 50 nm TEOS. The 1050°C annealing step is introduced

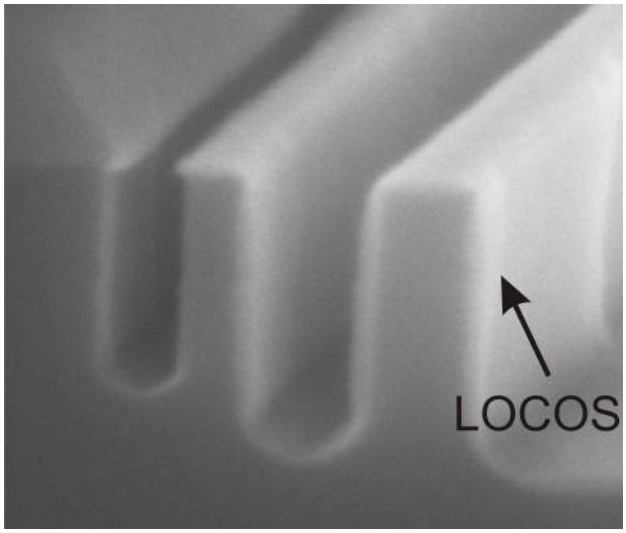

Figure 4.8: Magnification of Figure 4.7 showing the non-uniform LOCOS inside the narrow trench.

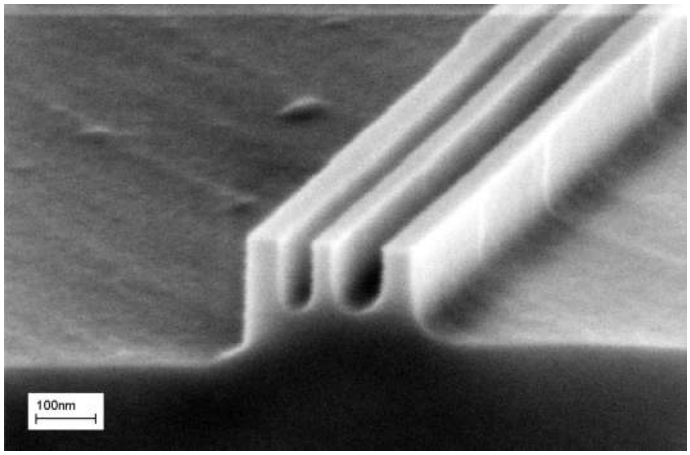

Figure 4.9: SEM image of triple Si nanoridges after complete removal of SiN_x, 20% KOH etching and final removal of SiO2 in 50% HF.

to increase the etch selectivity of SiN_x to TEOS in hot H_3PO_4 acid from 1.4 (4.2 to 2.9 nm/min) to 15 (3.9 to 0.29 nm/min) [11]. Therefore, 50 nm TEOS is sufficient for pattern transfer into 200 nm SiN_x in 52 min. Normally 10% over-etch is performed to ensure complete etching. As shown in Fig4.2, SiN_x displays an isotropically etched profile

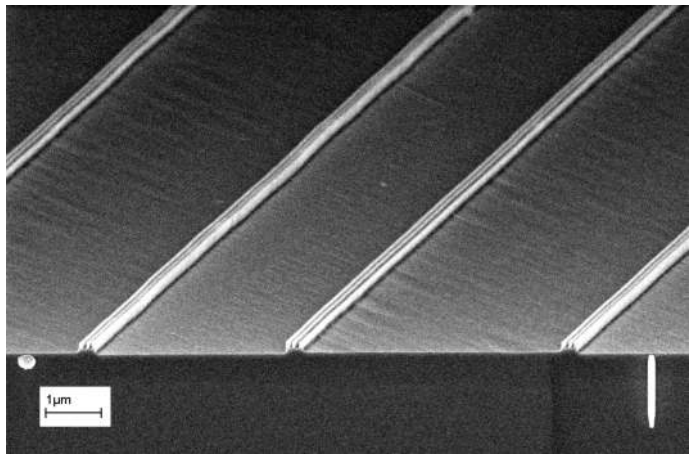

Figure 4.10: SEM image of an overview of groups of triple Si nanoridges.

	25%KOH, 75°C, [nm/min]	20%KOH, 20°C, [nm/min]	5%TMAH, 75°C, [nm/min]	OPD4262, 20°C, [nm/min]
<110>	1800	25	75	3.7
selectivity <111>:<110>	1:400	1:400	1:100	1:5

Table 4.1: Etch rates of Si <110> planes and selectivity between Si <111>:<110> planes in different etch solutions

after etching in hot H_3PO_4 acid using TEOS as the mask.

4.3.2 Si etching in 20% KOH at room temperature (step D, H, L)

In Figure 4.2, the vertical smooth Si sidewalls are achieved by 20% KOH etching of Si <110> substrate, which automatically stops etching at Si <111> planes. For the purpose of this fabrication scheme, 20% KOH is used instead of other standard wet chemicals for Si etching, which include OPD 4262, 5% tetramethylammonium hydroxide (TMAH) used at 70°C and 25% KOH used at 75°C. Table 4.1 lists the etch rates of <110> Si and selectivities between Si <111> and Si <110> planes in these wet chemicals. The etch rates of Si <110> in 5% TMAH used at 70°C and 25% KOH used at 75°C are too fast to be useful. Although the slow etch rate of OPD 4262 is favorable, the etch

selectivity between the Si <111> and <110> planes makes the etching of Si <111> planes non-negligible while making Si nanoridges 100 nm to 200 nm deep and a few tens of nanometers wide. Therefore the use of OPD 4262 in this scheme can lead to reduced control of the lateral dimensions of multi-Si nanoridges, and consequently making the control of spacing dimension more difficult. Therefore, 20% KOH is selected, considering the relatively low etch rate on Si <110> planes and high selectivity between Si <111> and <110> planes [12]. Moreover, the effect of line edge roughness brought by the use of conventional photolithography is avoided by self-alignment to Si <111> planes in KOH etching [13].

To obtain a relatively even level of the Si surface surrounding the Si nanoridges, the first KOH etching shown in Figure 4.2 is executed for 5 min while the following 20% KOH Si etching shown in Figure 4.6 and Figure 4.7 is performed for 10 min. It is estimated that the large difference in the trench aspect ratio is the reason for the difference in etching time. In Figure 4.6 and Figure 4.7, the trench aspect ratio (depth to width) is approximately 3:1 (120 nm:40 nm), while the trench aspect ratio is about 0.03:1 (120 nm:4000 nm) in Figure 4.2. In this specific case, to obtain an even trench depth, etching the nano-sized opening takes roughly twice as long as the time needed for the 4 μm opening. This effect can be called KOH lag and closely resembles RIE lag [14]. At present, we assume the reason behind the KOH lag is the depletion of active species into deep and narrow trenches.

4.3.3 SiN_x retraction etching using a 50% HF (step E, I, M)

After Si patterning in 20% KOH and RCA-2 cleaning, SiN_x is etched in both lateral and vertical directions using 50% HF for 25 min to receive an approximately 40 nm opening on the Si surface, as shown in Figure 4.3. As the Si edge is exposed to the etchant, 50% HF is used instead of hot H_3PO_4 to avoid Si surface attack [2].

4.3.4 LOCOS (step F, J, N)

The LOCOS step is executed to form a thermal SiO_2 layer on the fabricated Si edges to protect them from being deteriorated in the following hot H_3PO_4 acid SiN_x retraction etching and 20% KOH Si etching steps. Except for the purpose of serving as the protective layer, this SiO_2 layer influences the dimensions of the fabricated Si ridges and spacing between them. Since Si is consumed during oxidation, the LOCOS step leads to shrinkage in Si nanoridge height and width and widening of the spacing. Therefore we tried decreasing the oxidation time to minimize the influence of LOCOS. A thickness of

2 nm SiO_2 proved to be sufficient to withstand 20% KOH etching Si <110> for 400 nm at room temperature [12]. Figure 4.11 shows a Si ridge with a cleavage at the side. In

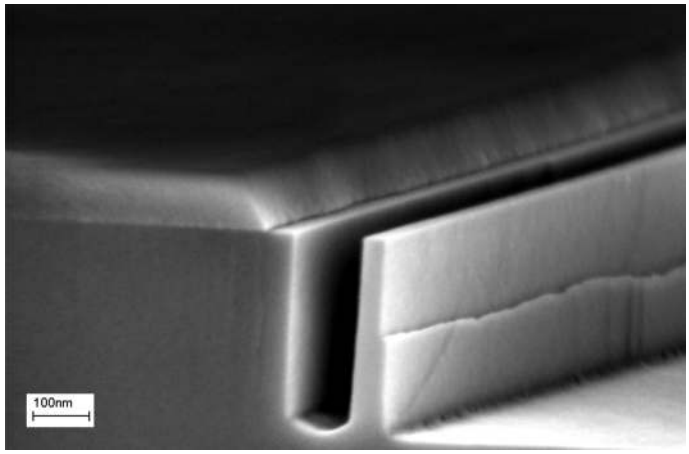

Figure 4.11: SEM image of a Si nanoridge with a cleavage at its side.

this case, the protective SiO_2 was obtained by 5 min LOCOS (about 10 nm SiO_2 obtained), which proved to be insufficient due to the non-uniform SiO_2 thickness at shaped Si surfaces as discussed by Marcus *et al.* [15]. The drawings shown in Figure 4.12 illustrate the shaped Si surface after LOCOS for 5 min followed by etching in hot H_3PO_4 acid for 15 min [16]. Since the SiO_2 at the top corner is thinner, it can first be etched away during SiN_x retraction etching in hot H_3PO_4 acid. The cleavage is then made during the next 20% KOH Si etching step as a result of opening at the protective SiO_2 layer. It is reported that the non-uniform SiO_2 thickness can be suppressed by: (1) increasing the oxidation temperature, (2) adding NH_3 gas during dry oxidation; or (3) decreasing the oxidation rate by inert gas addition [15, 17, 18]. All of these solutions are based on the fact that the oxide stress is reduced by viscous relaxation. Concerning this multi-Si nanoridge fabrication scheme, the LOCOS temperature cannot go beyond 1100°C so as to keep the intrinsic characteristics of SiN_x [19]. Besides improving the uniformity of oxide growth, the selectivity between the SiN_x and SiO_2 layers might be increased as found by Vos *et al.* [20]. The improvement of the SiO_2 growth or SiN_x selectivity needs further investigation but this is beyond the scope of this paper.

The result of LOCOS inside a narrow trench after dry oxidation can be observed in Figure 4.8 with the help of the illustration in Figure 4.12. Clearly, the thickness of the grown oxide layer depends on the position along the wall. At the convex and concave

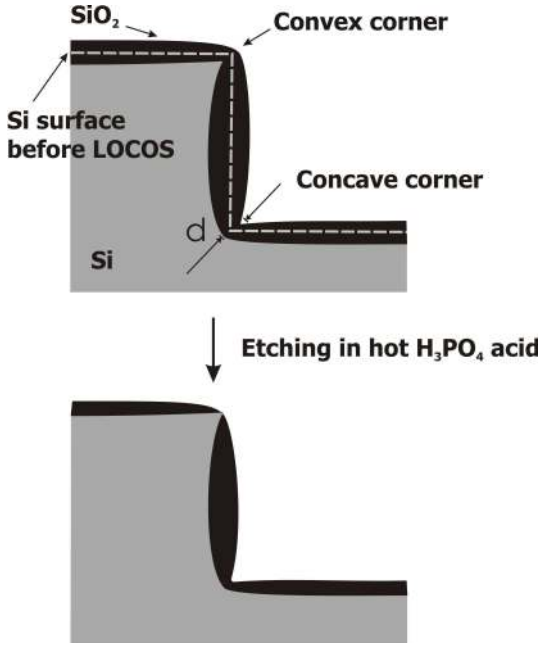

Figure 4.12: Illustrations of oxidation of a shaped Si surface. Top: oxidation of shaped Si surface [16]. Bottom: SiO_2 etched in hot H_3PO_4 acid.

corners it is less than on the other positions as observed by Marcus *et al.* [15]. Moreover, the thickness depends on the orientation of the underlying silicon surface [21]. Depletion of the oxidizing agent seems to be unlikely because both the narrow (40 nm) as well as the wide open trenches (4 μm) have an almost identical oxide layer at their surface Further research is needed to fully understand the oxidation behavior in narrow high aspect ratio trenches.

4.3.5 SiN_x retraction etching using hot H_3PO_4 acid (steps G, K)

After LOCOS, hot H_3PO_4 acid is used for SiN_x retraction etching taking advantage of the selectivity between SiN_x and SiO_2 (3.9 to 0.25 nm/min). An opening of 20 nm on the Si surface is obtained by etching SiN_x in hot H_3PO_4 acid for 8 min, as shown in Figure 4.5. Because the SiN_x etch rate is 3.9 nm/min, we should have observed 31 nm of retraction. However, SiN_x is partly oxidized during the LOCOS [22]. Due to this oxide, we have a delay of approximately 2 min before SiN_x starts etching. Finally, we find that the etching of SiN_x in hot H_3PO_4 acid plays an important role in influencing

the uniformity of etching over the whole wafer. Therefore, a stirrer is used to maintain a uniform temperature within the heated acid.

4.3.6 The determination of multi-Si nanoridge dimensions

As can be concluded from the previous discussions, the height of the Si nanoridges is predominantly determined by 20% KOH Si etching while the width of each Si nanoridge and the opening between the Si nanoridges are largely determined by 50% HF SiN_x retraction etching and hot H_3PO_4 acid SiN_x retraction etching, respectively. Moreover, the LOCOS step influences the dimensions of the multi-Si nanoridges by reducing the width and height of the Si nanoridges and consequently widening the spacing between them. In other words, the width and height of the fabricated Si nanoridges are decreased in the subsequent fabrication steps due to the consumption of Si in LOCOS. Also the proposed multi-Si ridge nanofabrication scheme is performed with uniform results on a full 100 mm wafer scale. By knowing these factors, each Si nanoridge and spacing can be tuned according to specific requirements after calculation and careful experimental handling. Furthermore, the Si substrate is prepared with 200 nm SiN_x substrate can be prepared with different SiN_x layer thicknesses considering the dimensions and number of Si nanoridges required. Accordingly, the TEOS layer thickness can also be tuned as needed. Since the multi-Si nanoridge process steps can be well controlled, we assume that the fabrication of Si nanoridges down to 10 nm is attainable, as we have already demonstrated the successful wafer-scale fabrication of single Si nanoridges down to 10 nm by edge lithography in our previous publication [2].

4.4 Application in nanoimprint lithography

The fabricated triple Si nanoridge sample, as shown in Figure 4.9 and Figure 4.10, is used in thermal nanoimprinting [23]. Before imprinting, the wafer template is cleaned in Piranha (H_2SO_4:H_2O_2 = 3:1, around 100°C) for 30 min, rinsed with deionized (DI) water and blown dry with N_2. Then, a monolayer of 1H,1H,2H,2H-perfluorodecyltrichlorosilane is deposited from the gas phase under vacuum condition in a desiccator. This layer acts as the anti-adhesion layer on the mold to facilitate demolding. The imprint process is performed on a wafer coated with PMMA (MW 38 kDa, 4 wt.% as to receive 200 nm layer thickness at 3000 rpm spin rate) using an Obducat thermal nanoimprint machine. The imprint is carried out at 180°C and 40 bar for 10 min and the demold temperature is 90°C. The imprint result is shown in Figure 4.13. We observed polymer filling problems

inside Si narrow trenches of the imprint sample, as can be seen in the image. We did not try to solve the problem since polymer filling is a typical issue in thermal nanoimprinting and goes beyond the focus of this paper.

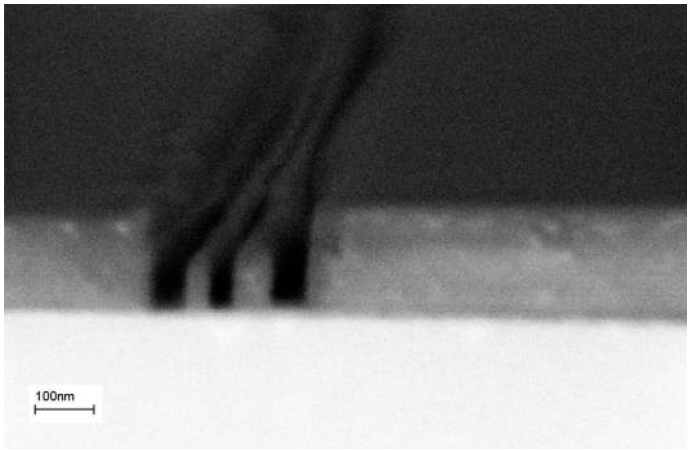

Figure 4.13: SEM image of thermal nanoimprint in PMMA (38 kDa) using the triple Si ridge template as shown in Figure 4.9.

4.5 Conclusions

A multi-Si ridge nanofabrication scheme has been successfully used in producing multi-Si nanoridges. The use of 20% KOH and a Si <110> substrate promises to obtain smooth and vertical Si sidewalls, which automatically stops at the Si <111> planes. Different from spacer patterning technology, the incorporation of LOCOS improves the dimension and shape of the silicon ridges. Without relying on the resolution of beam writing technologies, the width of an individual Si nanoridge and spacing can be well controlled by SiN_x retraction etching in 50% HF and hot H_3PO_4 acid, respectively. We have demonstrated ridges 120 nm high, 40 nm wide and 40 nm apart but are confident of reaching sub-10 nm resolution without complicating the process scheme. We can fabricate these multi-Si nanoridges with uniform dimensions within the 100 mmwafer scale by using photolithography and the full-wet etching scheme. Multi-Si nanoridges with specific dimensions can be produced by modifying the fabrication parameters as required, such as the layer thickness of SiN_x and TEOS, etching time of SiN_x and Si and oxidation time.

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Chapter 5

Combining retraction edge lithography and plasma etching for arbitrary contour nanoridge fabrication

Edge lithography in combination with fluorine-based plasma etching is employed to avoid the dependence on crystal orientation in single crystal silicon to create monolithic nanoridges with arbitrary contours. This is demonstrated by using a mask with circular structures and Si etching at cryogenic temperature with SF_6+O_2 plasma mixtures. Initially, the explored etch recipe was used with Cr as the masking material. Although nanoridges with perfect vertical sidewalls have been achieved, the Cr causes severe sidewall roughness due to line edge roughness. Therefore, SU-8 polymer is used instead. Although the SU-8 pattern definition needs further improvement, we demonstrate the possibility of fabricating Si nanoridges of arbitrary contours providing a width below 50 nm and a height between 25 and 500 nm with smooth surface finish. Artifacts in the ridge profile are observed and are mainly caused by the bird's beak phenomenon which is characteristic for the used LOCOS process.

5.1 Introduction

Nanofabrication is one of the essential ingredients in the development of new nanodevices. High resolution lithography tools have been developed to meet the ever-increasing demands of fabricating such structures. At present, deep ultraviolet lithography (DUVL) using 193 nm immersion scanners has been implemented almost exclusively in industry to achieve sub-50 nm pattern definition, even though the investments for such systems are incredible. But, due to wavelength limitations of the photons, some so-called ″Next Generation Lithography (NGL)″ tools are foreseen to replace DUVL. However, most of the candidates are still on the crossroads of hope and hype. For example, electron beam lithography (EBL) and focused ion beam lithography (FIB) have proven to be able to create arbitrary nanostructures with a resolution down to 10 nm. But, they suffer from low throughput due to the series operation. A more serious candidate for NGL is extreme UV lithography (EUVL) operating at 13.5 nm and being useful for nanoelectronics production due to its parallel processing feature and excellent multi-level registration ability. However, it suffers from high cost of operation and implementation (A preproduction EUV tool from ASML costs a staggering 90 million Euros). Therefore, the attractiveness of Nanoimprint Lithography (NIL), due to its simplicity and low cost of operation, is by some people recognized to succeed EUVL as the most probable NGL runner. Nevertheless, NIL is only a perfect candidate for rapid prototyping or showing proof-of-principle single-mask devices in research laboratories, as it still faces serious problems with respect to overlay and throughput. Ironically enough, ongoing improvements, such as double patterning, will further stretch the capabilities of DUVL and the 11 nm node is already scheduled by some valiant speakers for 2015.

So, researchers have been investigating new methods of nanofabrication to circumvent the limited accessibility or throughput of high resolution tools. For example, in 2005 Gate published a comprehensive review on the subject of unconventional ways of nanofabrication [1]. Amongst all the presented methods, edge lithography (EL) in combination with micromachining has proven to be a competent means of nanofabrication [2, 3, 4, 5]. EL-based nanofabrication can be performed via wet and plasma etch methodologies. In wet etch dominated EL, advantage is taken of crystal orientation and edges in substrates are created by anisotropic Si etching using solutions like potassium hydroxide (KOH) and tetra-methyl-ammonium hydroxide (TMAH) [6, 7, 8]. Smooth sidewalls are obtained since the etching slows down at <111> planes. Wet etching has the advantage that the process is relatively easy to handle, but only limited shapes of patterns can be created. Therefore, plasma etching has been increasingly used due to its ability of faithfully transferring pat-

terns from mask layers into Si without relying on crystal orientation. Researchers showed fabrication of nanostructures by means of plasma etching in combination with EL for NIL applications [9, 10]. These fabricated nanostructures, however, showed inclined sidewalls as well as inferior surface finish compared with that obtained by wet etching.

In this paper, we focus on the fabrication of Si nanoridges with arbitrary contours by the integration of advanced EL [4] and plasma etching. The basic idea of EL combined with wet anisotropic etching has been extensively discussed in our previous publications [2, 3, 4, 5]. Therefore, the primary concern of this paper is to develop a plasma recipe having an etch rate about 50 nm/min with high selectivity to SiO_2 and being able to provide a smooth surface finish as well as vertical sidewalls. The outcome of this study is not only useful in creating stamps for NIL purposes, but is also valuable to construct Si nanowires and devices alike.

For many decades, Cl and Br-based Si plasma etching has been widely used in industry providing ease of profile control. For example, Sato investigated in 1987 the trench formation process of Cl-based Si reactive ion etching (RIE) [11] and Krings considered deep Si trenches using $CBrF_3$ and SF_6 plasma [12]. In the more recent work, Choi and Kwon used HBr and Cl_2 plasmas for directional Si profiles [9, 10], Gomez investigated the etching of high aspect ratio structures using SF_6/O_2/HBr and $SF_6/O_2/Cl_2$ gas mixtures [13] and Choi demonstrated Si trench profile evolution by using gas mixtures containing SF_6, O_2, CF_4, HBr, and Cl_2 [14]. However, Cl and Br-containing gases are corrosive to reactor materials and, more importantly, hazardous to the environment [15]. F-containing gases such as CF_4 and SF_6 are less corrosive and toxic and show higher selectivity to masking materials. Therefore, F-based plasma etching is now playing a dominant role in Si MEMS applications. Currently, mixed (e.g. cryogenic) and pulsed (e.g. Bosch) processes are the most commonly used F-plasma approaches to achieve anisotropic etch profiles. Lately, Jansen gave a detailed review concerning the mechanism and influence of parameters in Bosch and cryostat DRIE processes [16]. Cryogenic Si DRIE with its smooth surface finish is chosen over Bosch processing as the latter typically shows pronounced scalloping of the sidewalls which is disastrous for NIL demolding and nano-structuring in general [17, 18]. Therefore, we investigated to find a suitable DRIE recipe to meet our requirements by using SF_6/O_2 based plasma etching at cryogenic temperature.

Next, the development of proper Si DRIE recipes is discussed. By using the selected recipe, two schemes capable of fabricating nanoridges with arbitrary contours are demonstrated. In the first scheme, positive photosensitive resist and Cr are used as masking layers. In the other scheme, negative resist SU-8 is used. By fabricating Si nanoridges with circular contours, we demonstrate the possibility of fabricating nanoridges with ar-

bitrary contours. The procedure is based on retraction EL; retraction because it utilizes an additional procedure on top of the simple EL scheme [2, 3] to enable the tuning of the width of monolithic structures [4, 5].

5.2 Silicon cryogenic deep reactive ion etching (DRIE)

5.2.1 Experimental

The aim of this section is to develop a fluorine-based plasma etching recipe slow enough to enable the precise fabrication of shallow nanoridges in the order of 100 nm or less. In the SF_6-based cryogenic Si etch experiment, an Alcatel AMS100SE Deep RIE system is used. A detailed description and explanation of how to achieve structures with perfectly straight sidewalls can be found in the review paper of Jansen [16]. In a nutshell, SF_6 decomposes inside the plasma glow and forms F radicals. F etches Si spontaneously and forms the volatile end-product SiF_4. Therefore, to promote vertical walls, the etch needs an inhibitor to prevent lateral etching. Typical inhibitors are oxygen or fluorocarbon-based gases. O_2, as first investigated by d'Agostino [19], is preferred as it has the advantage over CHF_3 to avoid fluorocarbon contamination of the Si surface [20, 21]. O_2 helps to form the inhibiting SiO_xF_y layer both at the bottom and sidewalls of trenches. By decreasing the temperature, spontaneous etching of Si is greatly reduced and ion bombardment plays the main role in cleaning the bottom surface while leaving the sidewall protected [22, 23, 24, 25]. The black silicon method (BSM) is employed as a convenient method to optimize the etch recipe and will be treated next [26, 27, 28].

Figure 5.1 is the process flow used to find the proper plasma etch recipe. <100> Si substrates are prepared with 20 and 50 nm thermally grown SiO_2 by dry oxidation at 950°C for 30 min and 2 h respectively. The substrates are patterned by UVL using a mask containing a grating pattern; 4 μm lines and 4 μm spacing (i.e. 50% Si load). After 1 min ozone treatment, the pattern is transferred into SiO_2 using Buffered HF (NH_4F:HF=7:1) for 50 sec. As shown in Figure 5.2, the resist pattern is eroded during BHF and a small enhanced undercut at the resist-oxide interface is visible. Nevertheless, the shape in the oxide mask is well-defined and useful in the current study. Then fuming HNO_3 acid is used to remove the resist. Before dry etching, the prepared substrates are etched in 1%HF for 30 sec to remove native oxide on the patterned Si surface. Although the SiO_2 layer ends up with a non-directional profile, its influence on Si etching can be neglected if the selectivity between SiO_2 and Si is sufficiently high.

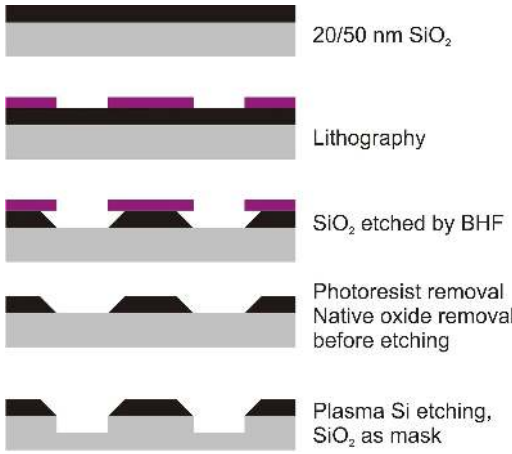

Figure 5.1: Fabrication scheme to find a directional DRIE recipe

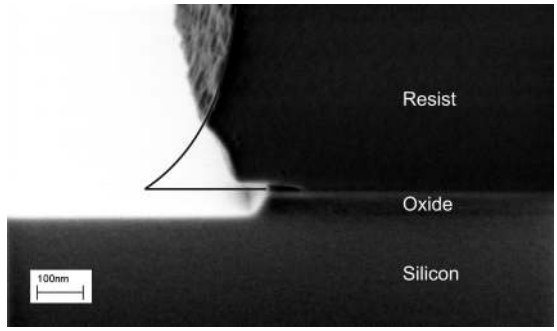

Figure 5.2: Resist and oxide profile after BHF etching

5.2.2 Results and discussion

In order to have a controllable DRIE nanorecipe, we start with a setting having an isotropic etch rate of around 200 nm/min using 15 sccm pure SF_6 gas and 200 W ICP power (see Figure 6 of ref. [16], Table 5.1-Rec.A). The substrate holder temperature is at 0°C and is located at 200 mm from the high density plasma source, and the etch time is initially fixed at 10 min. The etching is performed with the throttle valve 100% open to have low chamber pressure. This is to ensure a highly directional ion beam. As expected, after etching with pure SF_6 an isotropic profile is observed. Then 30 sccm O_2 is added, but the Si profile remains mostly isotropic as shown in Figure 5.3.a. Only after adding 50 sccm of oxygen inhibitor, the undercut vanishes and black silicon appears (Figure 5.3.b). To

Parameters	Recipe A	Recipe B	Recipe C	Recipe D	Recipe E	Recipe F
SF_6 (sccm)	15	15	15	15	15	15
O_2 (sccm)	0	30	50	50	30	30
ICP (W)	200	200	200	200	200	200
CCP (W), on/off (msec)	0	0	0	20 20/80	20 20/80	20 20/80
Wafer Temp. (°C)	0	0	0	0	-50	-100
He backside cooling (mbar)	10	10	10	10	10	10
Throttle valve position	100%	100%	100%	100%	100%	100%
Substrate holder distance (mm)	200	200	200	200	200	200
Etch rate (50% Si load, nm/min)	240	60	20	70	100	50
Profile	isotropic	Fig. 5.3.a	5.3.b	Fig. 5.3.c	Fig. 5.4	Fig. 5.4

Table 5.1: DRIE recipe investigation following BSM

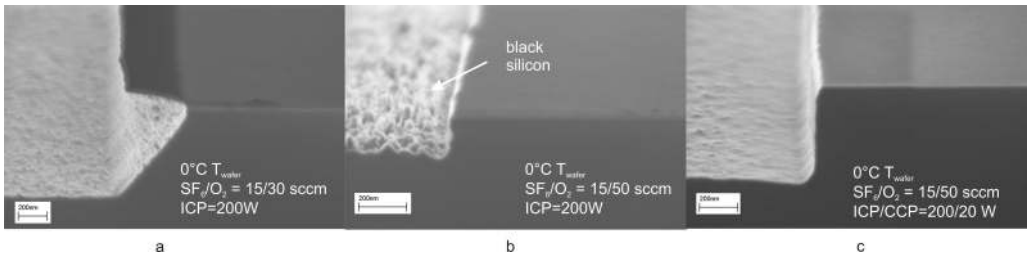

Figure 5.3: Black Silicon Method (BSM) to find the directional etching condition in SF_6 plasma. (a) Insufficient oxygen addition, (b) BS appears at 50 sccm O_2 and (c) disappears by adding 20 W CCP.

selectively remove the bottom protection, 20 W CCP power is applied. In Figure 5.3.c, Si trenches are fabricated at 0°C and 70 nm/min with vertical sidewalls (Table 5.1-Rec.D). However, the bottom is still relatively rough. This might be due to the huge amount of oxygen radicals together with the SiF_4 reaction products producing silica particles and dusty plasma [29]. For this reason, another approach is used to lower the oxygen concentration; the temperature of the wafer is lowered according to BSM [24, 25]. After 1 min etching at -50°C using recipe E, an undercut of 35 nm is visible directly underneath the 20 nm oxide mask (Figure 5.4). This phenomenon is related to the bottling effect, which can be minimized at lower pressure or bias [24, 28]. As both variables are already at the lower limit, we further lower the substrate temperature from -50 to -130°C to improve sidewall protection [25] as demonstrated in Figure 5.4. It is observed that the

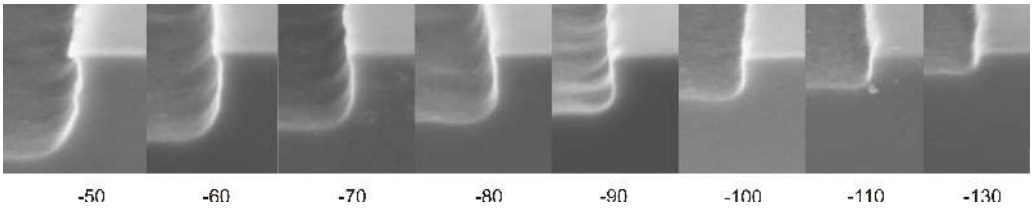

Figure 5.4: Si trench profile for various temperatures after 1 min etching (20 nm oxide mask in all cases).

trench profile becomes more vertical and the undercut reduces when the temperature is lowered and, at the same time, the etch rate decreases. At -130°C the sidewall profile shows even positive taper. Considering verticality, etch rate of Si (50 nm/min), and etch selectivity between Si to SiO_2 (20:1), etching at -100°C provides the most satisfactory result (Table 5.1-Rec.F).

5.3 Si nanoridge fabrication using Cr as the mask

5.3.1 Experimental

Figure 5.5 is the schematic of nanoridge fabrication using positive resist for pattern definition and both the resist and Cr as the mask during etching. The flow includes the previous DRIE result but uses a nitride layer instead of the oxide. The reason is that a LOCOS step will be included to create ridges, which is based on a nitride mask to enable local oxidation of silicon surfaces. The fabrication process comprises of:

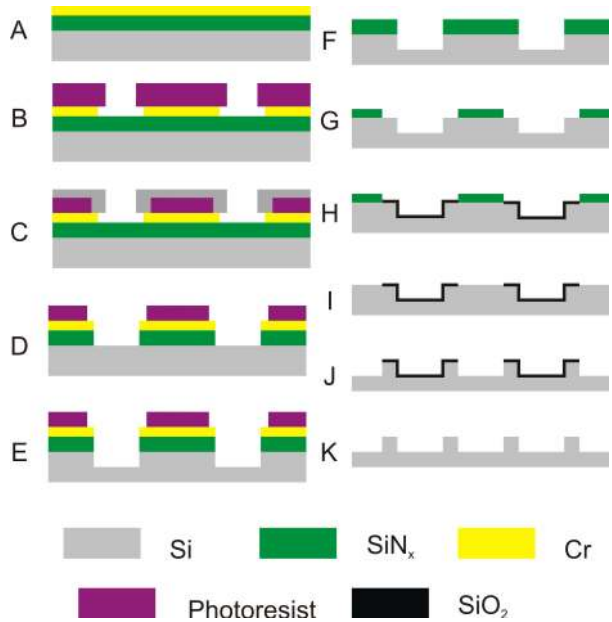

Figure 5.5: Fabrication of Si nanoridges using Cr as etch mask

(A) 100 mm single side polished p-type <100> Si wafers are used. After cleaning with HNO_3 solutions and native oxide removal in 1%HF for 1 min, the substrates are prepared with 100 nm silicon rich nitride (SiN_x) by low pressure vapor deposition (LPCVD) and 30 nm Cr by evaporation.

(B) The wafers are patterned by UVL using 1700 nm thick positive resist Olin 907-17. Two masks are used: mask 1 contains a 4 μm grating pattern and mask 2 contains hexagonally packed dots of 5 μm diameter with 12.5 μm center-center distance. The transparent area of the two masks is 50% and 15% respectively. After lithography, the substrates are treated in a UV-ozone reactor (UV PRS-100) for 300 sec to improve the

surface wetting of resist. Then, the Cr layer is etched for 35 sec at about 60 nm/min in Cr etch (ceric ammonium nitrate : acetic acid : water = 22:9:69 wt.%). A 5 sec over-etch is performed to ensure complete pattern transfer.

(C) The resist is partly etched (to prevent metal resputtering: see discussion) by RIE for 90 sec at 10°C, using 20 sccm oxygen flow, 70 mTorr pressure, and 50 W CCP power. Shower head is implemented in this step to lower the self-bias.

(D) SiN_x RIE (Elektrotech PF340) at 10°C is followed using a CHF_3/O_2 gas mixture of 25 sccm/5 sccm, 10 mTorr pressure, and 75 W CCP. The etch rate is about 50 nm/min and 15 sec over-etch time is applied. The total etch time is therefore 2 min 15 sec.

(E) The wafer is baked on a hot plate for 30 min at 120°C to avoid resist cracking during the following cryogenic DRIE process with parameter setting as listed in Table 5.1-Rec.F. The etch time depends on the requested height and is typically between 1 and 3 minutes.

(F) The resist is stripped for 20 min in 100% HNO_3 followed by Cr etch. A RCA-2 cleaning ($HCl:H_2O:H_2O_2$ = 1:5:1, heated up to 80°C) is performed for 15 min to remove any possible metal residue.

(G) SiN_x is isotropically etched for 26 min in 50% HF at 3.3 nm/min to allow mask retraction, after which a SiN_x layer of appr. 15 nm remains to function as a mask for the following LOCOS step.

(H) After standard cleaning and native oxide removal, the wafer is dry oxidized for 30 min at 950°C (i.e. 20nm oxide at the <100> plane) using SiN_x as the mask (LOCOS).

(I) SiN_x is stripped in 85% H_3PO_4 heated up to 180°C (referred as hot H_3PO_4 in the rest of the chapter) in 6 min .

(J) Si cryogenic DRIE (Table 5.1-Rec.F) is performed again, using thermal SiO_2 as the mask (1-3 minutes).

(K) The final Si nanoridges are obtained after complete removal of the thermal SiO_2 layer in 50% HF solution for 5 sec.

5.3.2 Results and discussion

SiN_x reactive ion etching (RIE)

The SiN_x layer is indispensible since it is needed to function as the protective layer during LOCOS (Figure 5.5.H). The SiN_x RIE (Figure 5.5.D) is performed using an Elektrotech Twin PF340 parallel-plate system [21]. To receive a vertical Si sidewall, a masking layer having vertical profile and selective resistivity to plasma are requested. Olin 907-17 resist is used for pattern definition having a slightly positive tapered profile, which is intensified

after hard bake at 120°C as a result of polymer re-flow. Since the SiN_x RIE recipe has a SiN_x to resist selectivity of 1:1, the sidewall profile and surface finish of the resist are exactly copied into the SiN_x layer, as shown in Figure 5.6.a. Wet chemical Cr etching

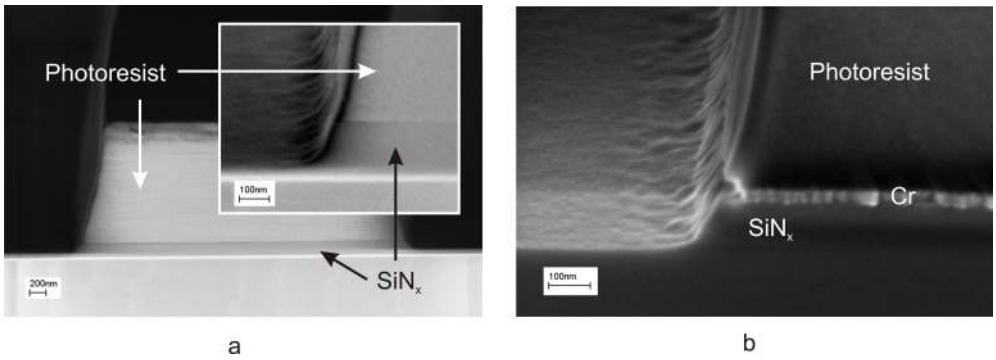

Figure 5.6: Masking material selections for SiN_x RIE (a) resist and (b) Cr and resist after wet Cr etching.

leads to an undercut in between the resist and SiN_x layers. When SiN_x RIE is continued with the existence of this gap, the Cr layer does not function as the mask and hence the SiN_x profile copies that of the resist, which is demonstrated in Figure 5.6.b. But, it is known that Cr is a selective mask for plasma etching [15, 22]. Therefore Cr is tried to be exposed during SiN_x RIE. In Figure 5.7.a, we show this after stripping resist. Due to the

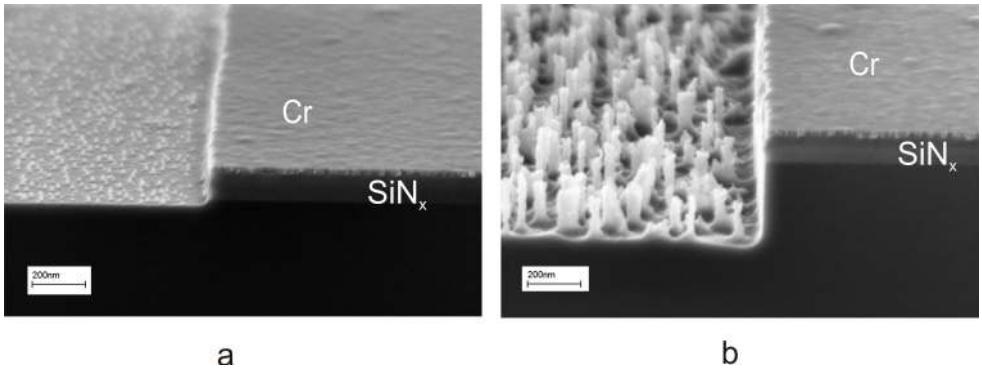

Figure 5.7: Cr mask for (a) SiN_x RIE and (b) subsequent Si DRIE

high bias in SiN_x RIE, about 400 V, the Cr material is re-deposited on the adjacent SiN_x surface [27]. The re-deposition forms a micro-mask followed by micro-pillar formation at the bottom of the trenches during Si DRIE, as shown in Figure 5.7.b. We conclude that

Cr can work as a mask in RIE to achieve vertical profiles. However, the high dc bias during SiN_x RIE induces Cr re-deposition, which negatively affects further processing.

As a solution to prevent black silicon formation, lateral retraction etching of the resist by O_2 RIE is carried out before SiN_x RIE to minimize the amount of Cr exposed to the plasma. The showerhead is installed to lower the self-bias [15]. Figure 5.8.a-c are showing resist retraction etching for 3 min, SiN_x RIE using resist and Cr as the mask, and the following Si DRIE respectively. As a comparison, Figure 5.8.d is showing Si DRIE performed using Cr as the mask after resist removal by fuming HNO_3. In this case, Cr is not re-deposited since the bias during Si DRIE is sufficiently low. We conclude

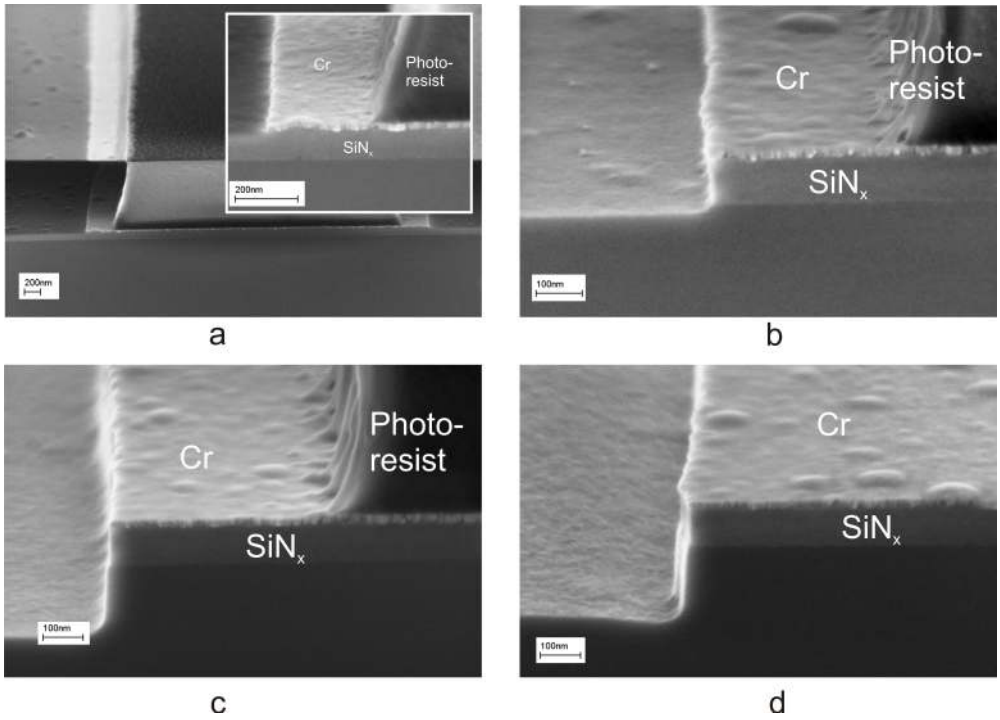

Figure 5.8: The etch results using Cr as the mask after (a) resist O_2 RIE lateral retraction etching (b) SiN_x RIE (c) Si DRIE for 2 min and (d) Si DRIE without resist showing identical performance

that surface roughening originates in the SiN_x RIE step. Currently, we use a capacitive coupled plasma for this task. This has the disadvantage that a high bias develops during RIE at power high enough for a reasonable etch rate. For this reason, the showerhead is installed as it lowers the anode/cathode area ratio and thus the self-bias. State-of-the-art

RIE systems/recipes might prevent surface roughening, but this is beyond the scope of this paper.

SiN_x retraction etching using 50% HF

In Figure 5.5.F, the Cr layer is removed before SiN_x retraction etching in 50%HF. This retraction mechanism is described and analyzed in detail in our previous paper [5]. We were trying to keep the Cr as the masking layer for SiN_x retraction etching. This approach has the advantage that a thin layer thickness of SiN_x, such as 15 nm, can be fixed to fabricate nanoridges with different width. However, it is observed that pin-holes in the Cr layer as a result of the evaporation quality lead to the penetration of 50%HF into the SiN_x layer underneath. Consequently, the opening in the SiN_x layer is oxidized in the following LOCOS step and it will function as a mask for the Si DRIE and finally produces nano-pillar structures together with the nanoridges, as shown in Figure 5.9. But, although the

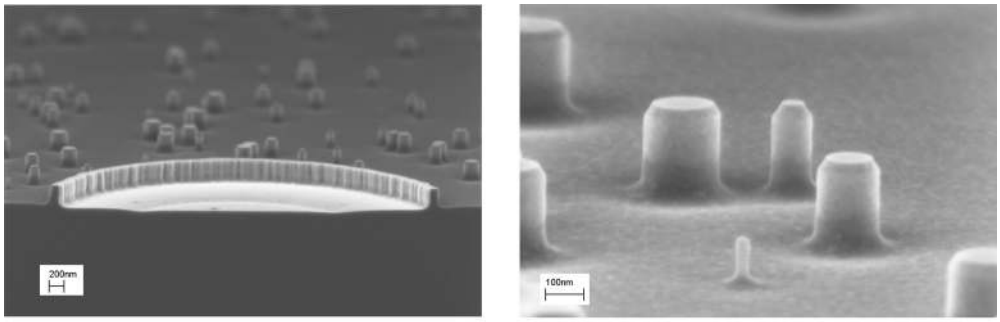

Figure 5.9: (a) nano-pillars are fabricated together with nanoridges due to the use of Cr as the mask (b) zoom-in.

fabrication of nano-pillar is not desired, it shines light on the fabrication of nano-pillars with perfect cylindrical shape via a maskless scheme. We can image that randomly distributed nano-pillars with a diameter down to 100 nm, as shown in Figure 5.9.b, can be fabricated by evaporating a thin Cr layer on top of a thin SiN_x surface and treating it maskless with 50%HF. The diameter of the nano-pillars might be easily controlled by SiN_x layer thickness and etching in 50%HF.

LOCal Oxidation of Silicon (LOCOS) at different temperature and its influence on Si DRIE

The oxidation of Si edge steps using SiN_x as the mask (Figure 5.5.H) is performed at 950°C for 30 min. This choice needs some explanation. The Si convex corner at the top of a steep sidewall is sharpened while the concave corner at the bottom is rounded, which has been demonstrated by Marcus [30]. We performed a series of experiments to examine at what extent the sharpening can be suppressed by increasing oxidation temperature. Trenches of 120 nm deep with vertical sidewalls are prepared taking advantage of Si <110> wafers and anisotropic etching by OPD 4262 as shown in Figure 5.10 [7]. Figure 5.11 shows the results of oxidation of these step edges without (left column) and

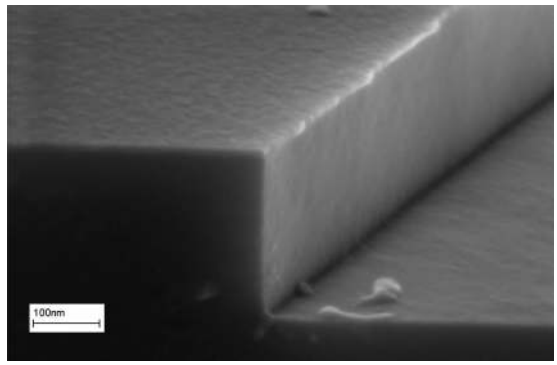

Figure 5.10: Profile after OPD4262 etch.

with (right column) 15 nm SiN_x mask. The preparation of the latter is based on Figure 1 in Ref. [5], that is, a Si<110> wafer is coated with 100 nm LPCVD SiN_x and 80 nm TEOS annealed at 900°C in a N_2 atmosphere for 1 h. After lithography, the TEOS is patterned in BHF and the nitride is etched in hot H_3PO_4. Subsequently, the Si is patterned in OPD 4262 to obtain a step of around 150 nm in height as shown schematically in Figure 5.12.a. Then, SiN_x retraction etching is performed in 50%HF leaving ca. 50 nm nitride and 50 nm unprotected silicon at the topside (Figure 5.12.b.top) or 15 nm nitride and 85 nm unprotected silicon (Figure 5.12.b.bottom). The oxidation is performed for 60 min at 950°C, 40 min at 1000°C, 24 min at 1050°C and 12 min at 1100°C to receive a similar SiO_2 layer thickness of 50 nm at the <110> surface (Figure 5.11 and Figure 5.12.c/d). For better observation of the LOCOS profile, a 100 nm poly-Si is deposited over the total structure and the wafer is cleaved followed by a 1%HF dip for 5 min. The results confirm the data published earlier that the Si sharpening at the convex

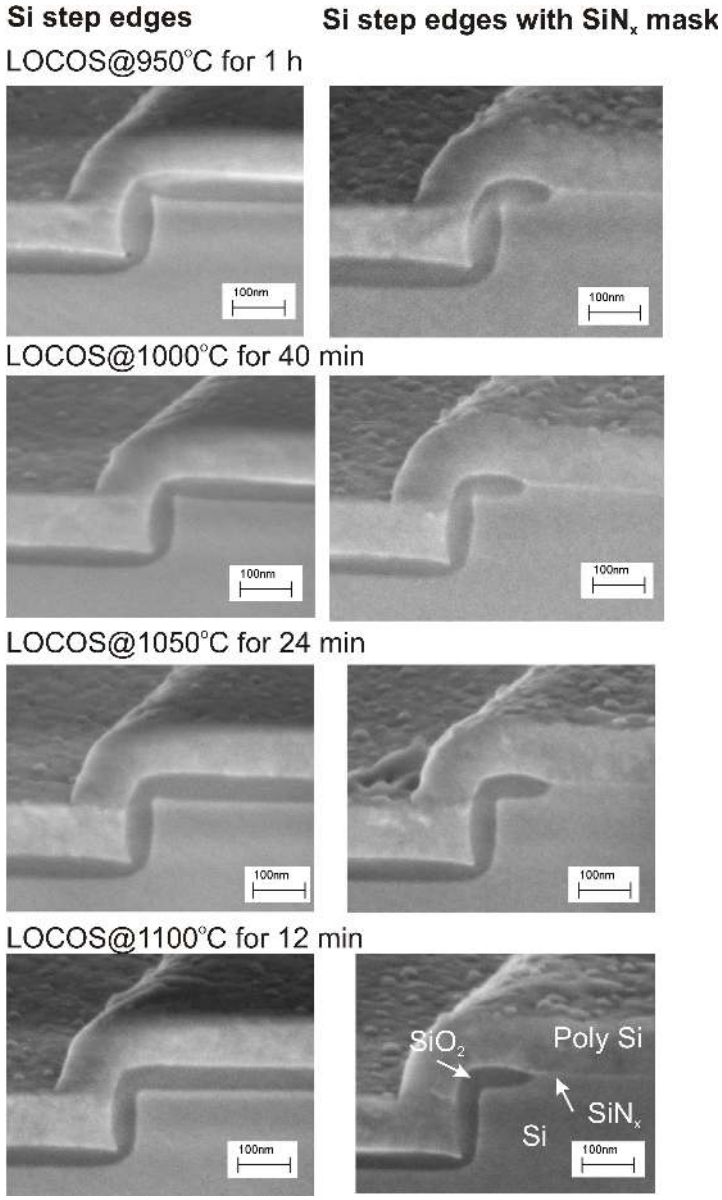

Figure 5.11: LOCOS step edges (left) without and (right) with 15 nm SiN_x mask

corners is suppressed at higher oxidation temperature. However, with SiN_x mask present, an in-plane tapered phenomenon (so-called bird's beak [30]) appears at the interface between Si, SiO_2 and SiN_x (Figure 5.11.right). This beak leads to a step edge abnormity in

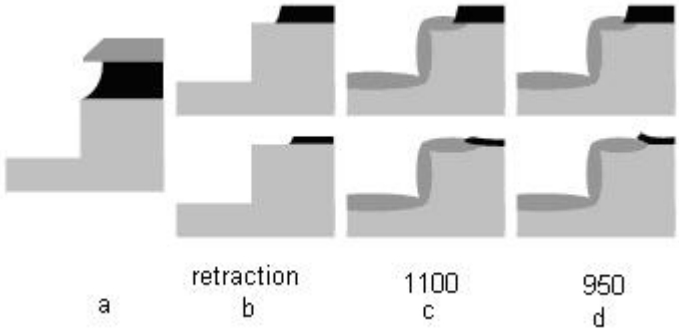

Figure 5.12: Bird's beak phenomenon

the Si nanoridge sidewall during the second Si DRIE due to the non-uniform SiO_2 layer thickness as explained next: At sufficiently high temperatures and/or relatively thick nitride layers, the oxide will reflow laterally and the nitride layer will not bend upwards that much (Figure 5.12.c.top and Figure 5.11.d.top). Consequently, it will form a ″sharp oxide beak″, which is bad for the following Si DRIE step as it causes mask retraction and an edge artifact as observed in Figure 5.13. In contrast, at sufficiently low temperatures

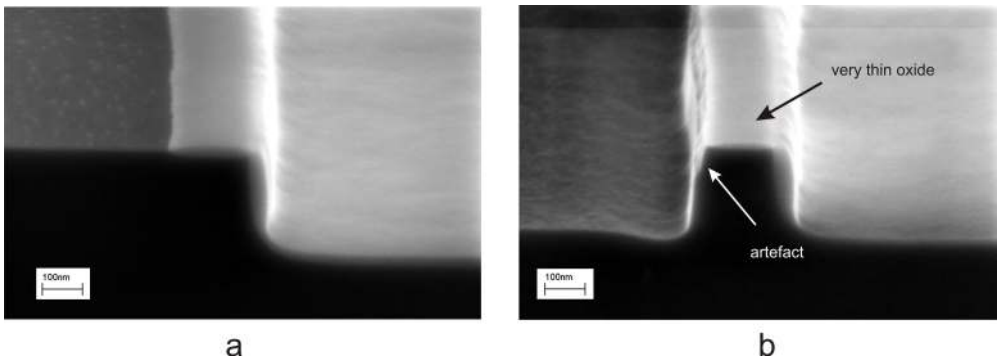

Figure 5.13: (a) LOCOS performed for 20 min at 1000°C; (b) second Si DRIE forming an irregular step edge.

and thin enough nitride, the LOCOS will push the nitride layer upwards and the bird's beak is more rounded (Figure 5.11 top right and Figure 5.12.d.bottom). Furthermore, as discussed in our previous paper, the increase of oxidation temperature will change the SiN_x structure and slow down the etch rate in hot H_3PO_4 [3] as listed in Table 5.2. As the etch rate of thermally grown oxide is independent of oxidation temperature, this means

	As grown	Oxidation @ 950°C for 60 min	Oxidation @ 1000°C for 40 min	Oxidation @ 1050°C for 24 min	Oxidation @ 1100°C for 12 min	Oxidation @ 1150°C for 6 min
50%HF (nm/min)	3.3	2.8	2.5	2.4	2.1	1.8
hot H_3PO_4	4.8	4.2	3.8	3.0	2.7	2.2

Table 5.2: Etch rate of SiN_x in 50%HF and hot H_3PO_4 acid after oxidation at different temperatures.

that the selectivity drops. The effect of a bad selectivity is that the very thin oxide at the convex corner might be fully eroded and leaving exposed silicon at this corner during the next silicon plasma etch step. Both mentioned problems become pronounced for 1000°C and higher, so we have restricted the oxidation temperature to 950°C even though the convex sharpening is more pronounced.

Final chromium fabrication results

The final results using Cr as mask are shown in Figure 5.14. During fabricating the

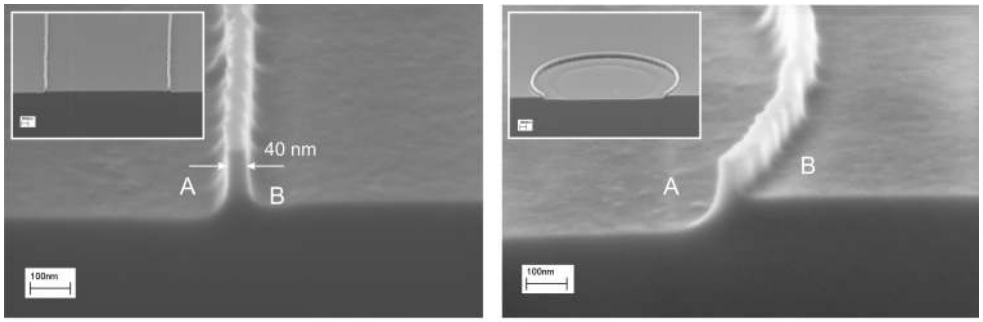

Figure 5.14: Fabrication results of nanoridges (a) nanoridge line and (b) nanoridge circle.

nanoridges with the two different contours, both the Si DRIE (Figure 5.5.E and J) are performed for 2 min. In Figure 5.14.a, side A and side B have comparable heights, since the loading in both cases is 50%. In Figure 5.14.b, the height of the nanoridge in the inner circle (A) is deeper than that of the outer circle (B) due to the change in loading, which is increased from 15% (step E) to 85% (step J) [16]. Of course, it is possible to tune the etch

time in order to receive identical heights. Moreover, it is observed in Figure 5.14.b that an extra circle appears inside the circular nanoridge. This is believed to be a result of resist charging during the first silicon plasma etch step. So, Cr can be used as a mask to fabricate vertical Si sidewalls in cryogenic plasma etching with smooth Si surface finish, but the rough Cr edge (probably caused by wet anisotropic etching of the poly-crystalline material) is copied into SiN_x and Si. Therefore, in the following section the use of negative resist SU-8 is introduced.

5.4 Si nanoridge with arbitrary contour fabrication using SU-8 as the mask

5.4.1 Experimental

Figure 5.15 shows the schematic of nanoridge fabrication using SU-8 for pattern definition and as an etch mask. The fabrication scheme consists of the following steps:

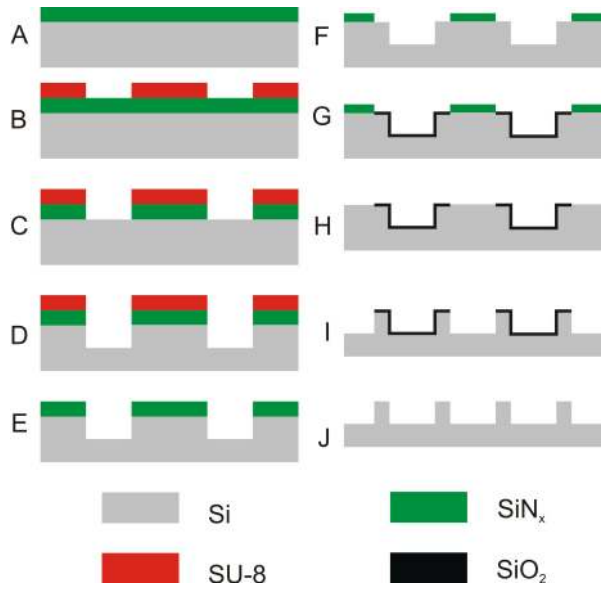

Figure 5.15: Fabrication of Si nanoridge using SU-8.

(A) <100> Si wafers are prepared with 60 nm SiN_x.

(B) The wafers are patterned by conventional UVL using negative resist SU-8 2000.5. The mask containing hexagonally packed dots of 5 μm in diameter is used. After piranha

cleaning (H_2SO_4:H_2O_2 = 3:1 heated up to 100°C), SU-8 is spin-coated for 30 sec at 3000 rpm resulting in a layer of 450 nm. The SU-8 procedure is carried out according to the manual provided by MicroChem. The soft bake is performed on a leveled hot plate: (1) starting from 25°C, the temperature ramps up by 2°C/min, stops at 65°C for 1 min; (2) the temperature continues ramping and stops at 95°C for 2 min; and finally (3) the temperature ramps down to 25°C. After soft bake, the wafers are exposed under UV light for 20 s using the EVG mask aligner having exposure intensity of 12 mW/cm^2 and with ASC-filter installed. The post exposure bake follows the same procedure as that of soft bake. The wafers are developed by immersing them in PGMEA (RER 600, ARCH Chemicals) for 1 min, and followed by 1 min in isopropanol. After development, the wafers are hard baked on a hot plate for 2 h at 120°C.

(C) SU-8 residue at the foot of the SU-8 structure is removed by O_2 plasma for 5 min (Tepla300). SiN_x RIE at 10°C is followed using a CHF_3/O_2 gas mixture of 25 sccm/5 sccm, pressure of 10 mTorr, CCP of 75 W.

(D) The Si DRIE is performed using SU-8 as the mask with the recipe as shown in Table 5.1-Rec.F.

(E) SU-8 is stripped in piranha solution for 30 min.

F) to J) follow the same procedure as steps G) to K) of Figure 5.5.

5.4.2 Results and discussion

SU-8 thickness

SU-8 is a negative epoxy resist which was initially developed as thick-film resist for electroplating in the LIGA process. In recent years, it has been widely used in fabricating micromechanical devices, such as for microfluidic and optic applications. Various types of SU-8 are available providing layers from 0.5-100 μm thick and requiring different preparation procedures to receive the best results. SU-8 5 and SU-8 2 capable of producing 5 μm and 2 μm layer thickness respectively were first tested. Although these two types of SU-8 can provide nearly vertical sidewall definition after lithography, they suffer from top and bottom defects which are found to be detrimental for fine patterning the thin sub-100 nm SiN_x layer underneath. More important, as shown in Figure 5.16, additional circular pattern appears at the bottom of the Si surface during Si DRIE. This effect is similar to what we have observed in Figure 5.14.b and is also believed to be a result of SU-8 2 charging during SF_6/O_2 etching. Therefore, SU-8 2000.5 which is able to provide a layer thickness ca. 450 nm is used in lithography process.

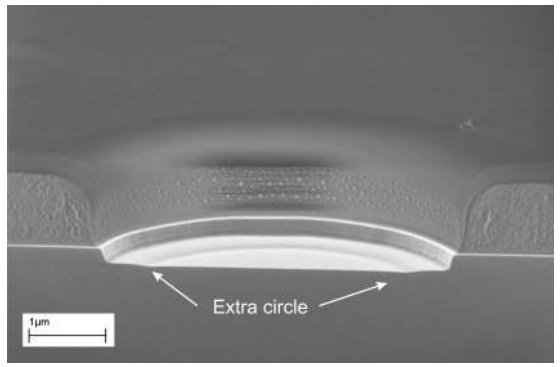

Figure 5.16: In Si DRIE using SU-8 2 an additional circular pattern is created.

Final SU-8 fabrication results

Figure 5.17.a-d are the fabrication results in accordance to step B to D of Figure 5.15. After lithography, the SU-8 residue at the foot of the pattern (Figure 5.17.a) is removed by O_2 plasma (Figure 5.17.b) using the barrel plasma system (Tepla300) to avoid plasma ion bombardment of the SU-8 surface. The operating power is 300 W and the pressure is 1 mbar. Chamber temperature can not be controlled but is measured to be ca. 140°C. In Figure 5.17.c, the SiN_x profile copies that of SU-8 resist due to the poor selectivity of SiN_x to resist in RIE. The profile is more positive tapered than that in Figure 5.17.a and b mainly due to SU-8 processing instabilities. In the Si DRIE, as shown in Figure 5.17.d, the SiN_x works as the etch mask. Since the selectivity between Si and SiN_x is reasonable (4:1) during Si DRIE, nearly vertical sidewalls have been achieved.

During experimentation we experienced strong non-uniformities in SU-8 patterning over the 100 mm wafer. More specific, the SU-8 sidewall profile in the 450 nm thin film is not as vertical as that has been achieved in thicker SU-8 films. It can be caused by many factors during experimental handling and parameter adjustment. For example, it is observed that the use of an ASC i-line filter (2 nm bandwidth centered at 365 nm) improves the sidewall verticality although the exposure time increases threefold up to 20 sec. Furthermore, a satisfactory pattern definition can only be achieved for 70% of the patterned area. At present, we are not sure about the cause of this non-uniformity, but these results have not been further explored as it is beyond the scope of the present study. Nevertheless, some first trials have been performed to improve sidewall verticality using the i-line filter as shown in Figure 5.18.

The final fabricated Si nanoridges with circular contour are shown in Figure 5.19. In

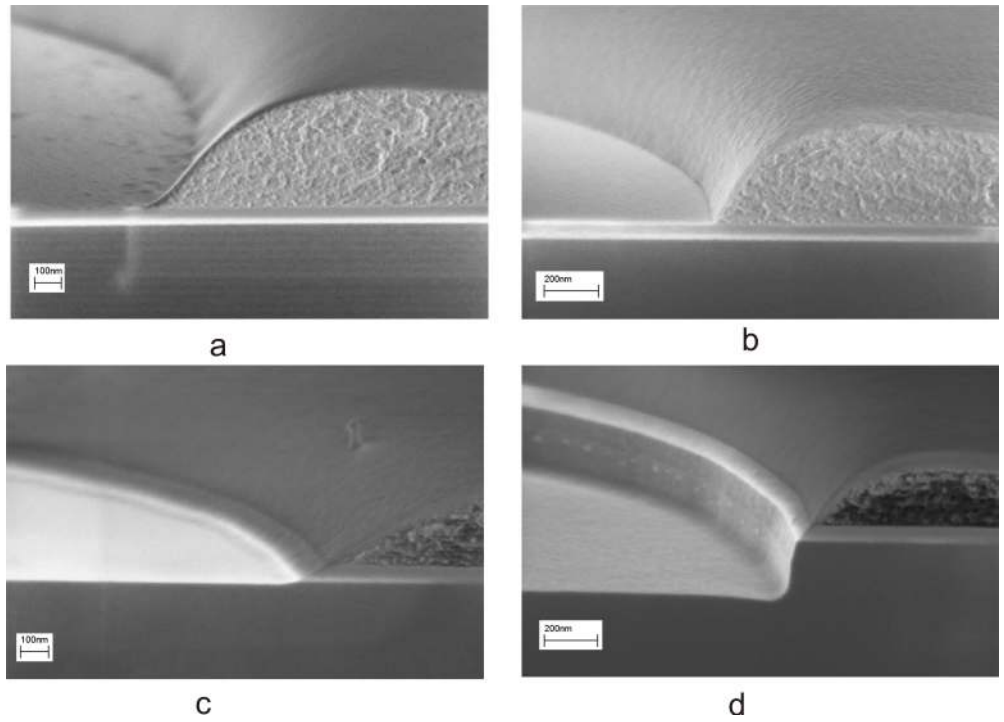

Figure 5.17: (a) Pattern definition by conventional UV lithography using SU-8; (b) O_2 plasma treatment to remove SU-8 residue at the foot (c) SiN_x RIE and (d) Si DRIE

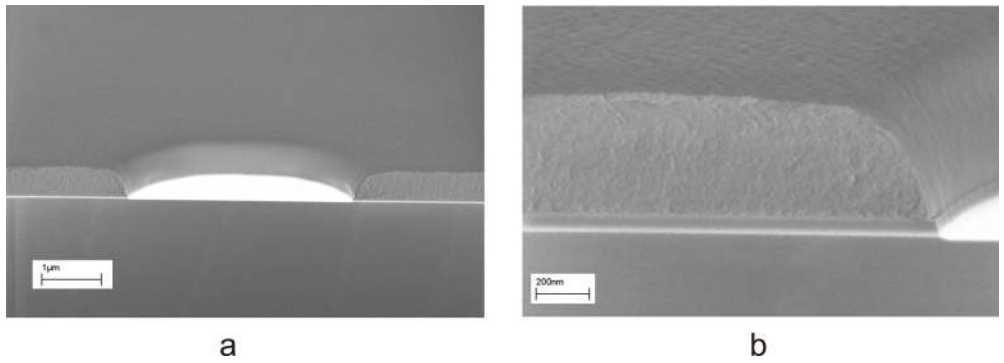

Figure 5.18: Well shaped SU-8 2000.5 and SiN_x etching profiles: (a) an overview (b) a zoom-in view

comparison with Figure 5.14, the use of SU-8 greatly improves the sidewall roughness caused by Cr, although the sidewall verticality is less. As we mentioned before, further

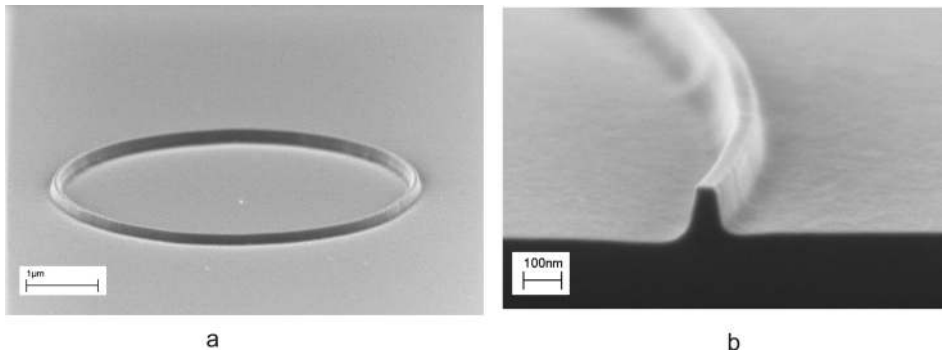

Figure 5.19: Fabricated circular Si nanoridges by SU-8 pattern definition (a) A full nanoridge pattern with circular contour (b) a cross-section view

research especially regarding the experimental patterning procedure of SU-8 needs to be done to tackle the problem.

5.5 Determination step dimension

In the previous sections, the fabrication of monolithic silicon ridges has been demonstrated. When a ridge with a specific width and height is requested the following design rules are useful. The width of the ridges is determined by the nitride thickness and the amount of retraction etching. As the nitride should be sufficiently thin to bend during the LOCOS step while still acting as a protective mask, 15 nm is chosen. Thus, the thickness of the deposited nitride is the aimed width of the ridge plus 15 nm. The possible height of the ridge is depending on the nominal etch rate and the selectivity during the silicon DRIE step. Due to start up instabilities, the minimum etch depth is around 25 nm (30sec at 50nm/min) and the maximum artifact-free height is around 500 nm.

5.6 Conclusions

We demonstrate the fabrication of Si nanoridges with arbitrary contours by plasma etching and advanced edge lithography. The investigation of the Si etch recipe is based on the Black Silicon Method using the Alcatel DRIE system. Si etching, using SF_6/O_2 gas mixture performed at cryogenic temperature, provides an etch rate of about 50 nm/min with a smooth surface finish as well as a reasonable selectivity to SiO_2 and SiN_x. By using the recipe, positive resist is used for pattern definition and both resist and Cr layers

are employed as masking material to fabricate Si nanoridges with vertical sidewall profile. However, sidewall roughness is introduced as a result of Cr layer line edge roughness probably due to its poly-crystalline morphology. Therefore, 450 nm thin negative resist SU-8 is explored for pattern definition and used as masking material during plasma etching. It functions as a good mask to produce smooth sidewalls. The high selectivity of the Si DRIE recipe ensures the achievement of nanoridges with nearly vertical sidewalls profile although the initial SU-8 definition shows positive tapered profiles. Based on the successful fabrication of nanoridges having a width below 50 nm and a tunable height between 25 and 500 nm with circular contours, we conclude that nanoridges with arbitrary contours can be produced by the proposed technique. However, the main restriction of this procedure is the LOCOS process, which introduces the bird's beak effect and also convex corner sharpening and limits the aspect ratio (height over width) of sub-25nm structures drastically to less than 10.

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Chapter 6

Application of stamps fabricated by edge lithography in alternative nanofabrication[1]

This chapter presents the creation of nanostructures by means of self-assembly, microcontact printing (μCP) and capillary force lithography (CFL). The fabricated Si nanoridges with sub-100 nm width described in Chapter 3 are employed for high resolution pattern definition in thermal nanoimprint lithography (T-NIL) and CFL. T-NIL is successfully implemented with self-assembly and μCP respectively to function as alternative nanofabrication approaches.

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6.1 Introduction

Nature uses nanoscale architectures to convert light into chemical energy, e.g. by photosynthesis. Take the photosynthetic system of purple bacteria for example. It is organized by several peripheral antenna complexes (LH2) surrounding the core antennae (LH1), each of which encloses a reaction center. The antenna complexes (LH2, LH1) and the reaction center together form a photosynthetic unit (PSU). PSUs are interconnected in larger domains, in which energy transfer takes place. To investigate the properties of the energy transfer, the integration of T-NIL and self-assembly is here demonstrated capable of building artificial nanoassemblies of these light harvesting LH2 antenna. The creation of the bionanoassemblies aims at exploring the energy transfer properties of the light harvesting complexes, which is accomplished by producing biomolecular photonic wires.

A self-assembled monolayer (SAM) is an ordered molecular assembly by a spontaneous chemical synthesis at the interface [1]. The molecules used to form SAMs have the property to assemble with high order. SAMs can be formed from either gas phase or liquid phase. The assembly of biomolecules has been explored by using electrostatic interactions, covalent bonds, biospecific interactions and supramolecular interactions while retaining their biological activity. To build the light harvesting LH2 antenna assembly, multivalent interactions were used to selectively position the proteins onto the β-cyclodextin (β-CD) monolayers [2] patterned by T-NIL. β-CD is a water soluble cyclic oligosaccharide made of seven glucose units. The so-called molecular printboard consisting of self-assembled cyclodextrin monolayers on different surfaces such as SiO_2 and gold enables the assembly of building blocks by multivalent interactions [2].

Microcontact printing (μCP) [3] is a soft lithographic technique that can generate patterned SAMs on both planar and nonplanar surfaces [4]. The concept of μCP is straightforward. An elastomeric stamp, mostly made of poly(dimethyl siloxane) (PDMS), is fabricated by casting a prepolymer of PDMS over a patterned substrate with a pretreated anti-adhesion layer. After curing PDMS, it is carefully peeled off from the substrate. Contact printing is not diffraction limited, in contrast to photolithography, and is in principle able to generate patterns with sub-100 nm resolution. However, the limited mechanical stability of the soft stamp prohibits the creation of high resolution nanostructures. Therefore, the idea of chemically patterned flat stamps was introduced to solve these problems. Initially, chemically patterned flat stamps were produced by oxidizing flat PDMS through a shadow mask followed by silane reaction [5]. The commercially available shadow masks have the highest resolution of 350 nm. Therefore, we introduced new methods to prepare chemically patterned flat PDMS stamps with higher resolution.

With the help of T-NIL, a chemically patterned composite PDMS-glass stamp is here fabricated for high resolution μCP applications. The idea of creating stamps for high resoltuion μCP is further explored by CFL. CFL was developed by combining the essence of nanoimprint lithography, in which imprinting is performed in a molten polymer, and contact printing, in which an elastomeric stamp is used to achieve better contact [6, 7]. In CFL, a stamp made of PDMS is placed on the imprint polymer spin-coated on a substrate. When the stamp and substrate are heated above the the glass transition temperature (T_g) of the polymer, capillary forces drive the polymer flow into the cavities of the imprint stamp and thus the negative replica of the stamp is formed. The chemically patterned composite PDMS-glass stamps fabricated by T-NIL and CFL respectively are here successfully employed in μCP to create sub-100 nm nanostructures in Au substrates.

6.2 Experimental

In this section, Si nanoridge substrates fabricated as described in Chapter 3 are used as stamps in T-NIL and CFL. Before usage, stamps were cleaned in piranha solution (H_2SO_4:H_2O_2 = 3:1) for 30 min, rinsed with DI water and dried in a stream of nitrogen. Then, a monolayer of 1H,1H,2H,2H-perfluorodecyltrichlorosilane (PFDTS) was assembled from gas phase under vacuum in a desiccator [8]. This layer acts as the anti-adhesion layer on the mold to facilitate demolding.

6.2.1 Fabrication of bionanoassemblies by NIL and self-assembly

In the T-NIL step, imprint substrates (microscope coverslips, Menzel-glaser # 1,5) were cleaned using piranha solution and blown dry in a stream of N_2. Then a 90 nm thick layer of PMMA (20 g/L) was spin-coated. The stamp and substrate were put in contact and the imprint was carried out at 180°C and 40 bar using a Specac hydraulic press system. The stamp and substrate were separated at a temperature of 110°C. After imprint, the residual layer was removed and the substrate was activated by O_2 RIE for 20 s by an Elektrotech Twin system PF 340 at 20W, 10 mTorr and 10 sccm O_2 flow. The activated substrate surface was functionalized using an aminoalkyl SAM from the gas phase [9]. Afterwards the remaining PMMA was removed in actone and the complementary areas were passivated with 2-[methoxy(polyethyleneoxy)propyl]trimethoxysilane (PEG silane) in distilled toluene for 2 h. Then the substrates were rinsed with toluene followed by ethanol and dried in a stream of N_2.

Before β-CD assembly onto the aminoalkyl SAM surface, the amino-terminated SAM

was first transformed into an isothiocyanate-terminated surface by exposure to a 0.1 M solution of 1,4-phenylenediisothiocyanate in toluene at 50 °C for 2 h under N_2. After rinsing with toluene and drying with N_2, β-CD heptamine was attached by reacting it with the isothiocyanate-terminated SAM in a 1 mM solution in Millipore water (pH 8.5) at 50 °C for 2 h followed by sonication in water, rinsing with water and gently drying in a stream of N_2.

The prepared substrate was treated with 25 μl of 1 mM AdHEG for 10 min. The adamantyl modified light harvesting protein was deposited onto the substrate from a drop (25 μl, 0.4 μM) in an aqueous buffered solution (20mM HEPES, pH 8.0, 0.03 wt% β-DDM (n-dodecyl-β-D-maltoside), 1 mM AdHEG) onto the substrate. The protein immobilization was accomplished by incubating the protein in a humid environment for 20 min.

6.2.2 High resolution μCP stamp fabrication by T-NIL and CFL

To fabricate the PDMS-glass substrate, the liquid prepolymer of PDMS was first cast onto the polished side of a Si wafer, on which an antiadhesion layer of PFDTS has been deposited. After degassing, a glass substrate was placed in the liquid PDMS which sank to the bottom of the solution leaving a thin PDMS layer between the glass substrate and the Si wafer. The PDMS-glass substrate was peeled off from the Si substrate after curing the PDMS at 60°C for 8 h.

The fabrication of the PDMS-glass stamp was accomplished by thermal nanoimprint lithography (T-NIL). During fabrication, thermal imprint resist mr-I 85 (T_g of 85°C) obtained from Microresist was used. Before spin coating, the PDMS was treated shortly with O_2 plasma for 15 s using an Elektrotech Twin system PF 340 at 10 mTorr, 10W, 20 sccm O_2 flow for better film quality. Mr-I 85 resist was spin-coated onto the substrate followed by a soft baking at 140°C for 2 min. The Si imprint stamp was brought into contact with the spin-coated PDMS-glass substrate. The T-NIL process was performed at a temperature of 140°C, a pressure of 2 bar for 5 min using a Specac hydraulic press system. The imprint stamp and substrate were separated at 50°C. After imprint, the residual layer was removed by RIE O_2 plasma using an Elektrotech Twin system PF 340 at 10 mTorr, 10W and 10 sccm O_2 flow. The etch rate of mr-I 85 was about 1 to 5 nm/s. An extra 15 s etching was applied as to fully activate the PDMS surface. Immediately after the surface activation, PFDTS was deposited from the gas phase. Finally the substrate was dipped into 80°C cyclohexane for 1 min to remove the mr-I 85 resist layer.

In another set of experiments, CFL was employed to fabricate the PDMS-glass stamp.

After PDMS surface activation by O_2 plasma, 20 nm mr-I 85 resist was spin-coated onto the substrate followed by a soft baking at 140°C for 2 min. Before imprinting, the Si stamp and the PDMS-glass substrate coated with the imprint resist mr-I 85 were equilibrated at the annealing temperature of 150°C for 30 min. Then the stamp and substrate were brought into contact and a weight about 0.1 bar was applied on top of the Si stamp. The system was left at 150°C for 30 min. The stamp and substrate were separated after the system was cooled down to 50°C for 10 min. After CFL, O_2 plasma was applied for 30 s to activate the exposed PDMS areas. PFDTS was deposited from the gas phase onto the oxidized PDMS surface immediately after PDMS surface activation. Finally the substrate is dipped into 80°C cyclohexane for 1 min to remove the mr-I 85 resist layer.

6.2.3 Nanofabrication by high resolution μCP

The PFDTS-modified PDMS-glass stamps either fabricated by T-NIL or CFL were used for μCP on a Au substrate (obtained from Ssens BV, Hengelo, the Netherlands) to produce metal nanopatterns by μCP and wet etching. In the (-)μCP approach, which is the regular μCP method, the PDMS-glass stamp was inked with a few drops of octadecanethiol (ODT) solution in ethanol (1 mM) and dried in a stream of N_2. Then the stamp was pressed against the Au surface at the initial stage of the printing to induce conformal contact. After contact printing for 1 min, the stamp and substrate were separated. Au nanogrooves were fabricated by Au etching in a $S_2O_3^{2-}$/ferri/ferrocyanide-based solution using ODT as the mask. In the (+)μCP case, the PDMS-glass stamp was inked with a poly(propyleneimine) dendrimer with dialkyl sulfide end groups (G3-M). The contact printing was performed for 2 min followed by dipping the substrate in 0.1 mM ODT solution for 5 s. A freshly prepared solution consisting of 10 mM $Fe(NO_3)_3$, 15 mM thiourea, and 1.2% HCl was used as etchant to remove the gold in the G3-M covered area to create nanolines.

6.3 Results and discussion

6.3.1 Light harvesting complexes construction and energy transfer

Multivalent host-guest interactions were utilized to selectively assemble functional light harvesting LH2 antenna complexes onto nanometer structured β-cyclodextrin monolayers patterned by NIL [10]. The fabrication process is shown in Figure 6.1. T-NIL was used as a top-down approach to control the lateral dimensions on the nanometer scale. Si

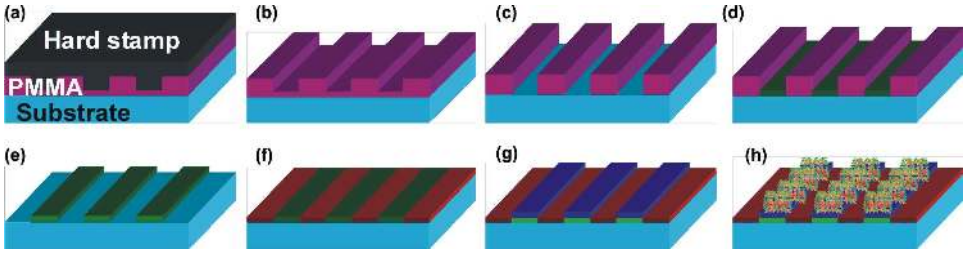

Figure 6.1: Process flow of the attachment of light harvesting antenna complexes: (a) T-NIL in PMMA; (b) demolding of the Si stamp; (c) residual layer removal; (d) aminoalkyl SAM formation on the polymer-free areas; (e) imprint polymer removal; (f) chemical passivation of complementary areas by PEG silane; (g) self-assembly of β-CD monolayer on to the aminoalkyl SAM monolayer; (h) assembly of the LH2$_n$Ad protein complexes on the β-CD monolayer. Images are taken from [11].

nanoridges of 40 nm wide with 4 μm spacing were used since the dimensions are favorable for the fluorescence microscopy characterization. After imprint and residual layer removal, aminoalkyl and PEG silane were patterned onto the glass substrate. β-Cyclodextrin was selectively anchored to the aminoalkyl SAM areas. Multivalent host-guest interactions are employed to position adamantyl-substituted biomolecules onto the β-CD areas with proper orientation, pooling density, and specificity. The LH2 complex was bioengineered with cysteine residues, which were modified with iodoacetyltri(ethylene glycol)mono(adamantyl ether), AdI, block 3 in Figure 6.2. The modified protein complex is referred to as Ad$_n$LH2. During the absorption of Ad$_n$LH2 onto the β-CD patterned surface, hexa(ethyleneglycol)mono(adamantylether) AdHEG, block 2 in Figure 6.2, is added as a temporary blocking agent for β-CD cavities [12]. AdHEG is being displaced by competition since Ad$_n$LH2 shows higher affinity because of the formation of multivalent interactions to the surface.

Fluorescence imaging enabled the real-time characterization of the optical properties of the LH2 complex after modification and the specific adsorption of proteins to the β-CD monolayers, as shown in Figure 6.3 (a). When the non-modified LH2 was incubated onto the β-CD monolayer and rinsed with buffer, the average spectra indicate that non-specific binding dominates (blue box trace ■). In another case, when the substrate was pre-treated with the temporary blocking agent AdHEG, the non-specific binding is reduced by 94% (open box trace □). The increase of signal intensity (green star trace ★) reveals the specific binding of the multivalent Ad$_n$LH2 proteins to the β-CD areas by replacing the monovalent AdHEG. Moreover, the spectral response from the immobilized Ad$_n$LH2 complexes shows no difference from that of non-modified LH2 complexes (red

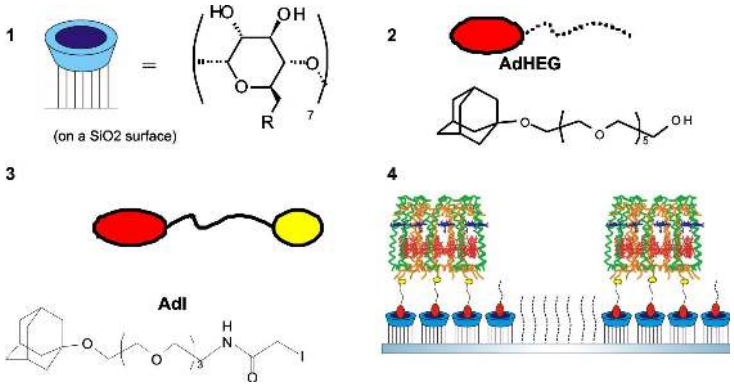

Figure 6.2: Representation of host, guest and target molecules: 1.β-CD, host molecule; 2.hexa(ethylene glycol)mono(adamantyl ether) (AdHEG); 3.iodoacetyl-tri(ethylene glycol)mono(adamantyl ether) (ADI); 4.Ad$_n$LH2 on the β-CD monolayer. Images are taken from [11].

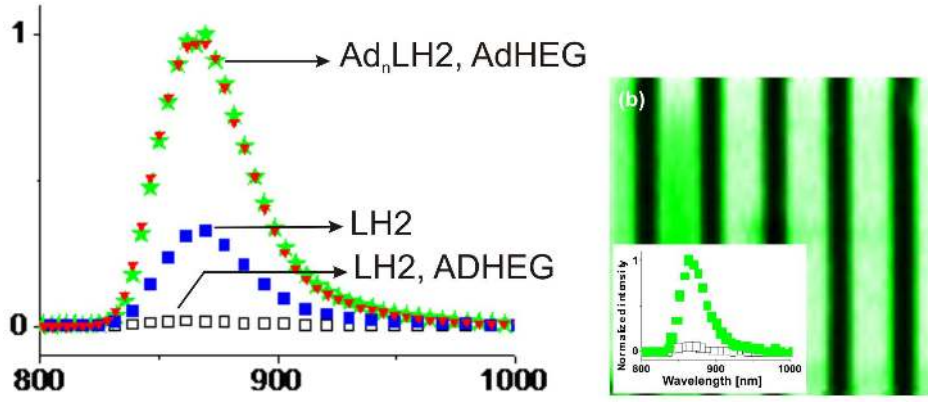

Figure 6.3: (a) Fluorescence spectra: Non-labeled LH2 (blue, ■), non-labeled LH2, 1 mM AdHEG (open, □), Ad$_n$LH2 1 mM AdHEG (green, ★), reference spectrum of non-labeled LH2 in solution (red, ▼); (b) Fluorescent spectral image of Ad$_n$LH2 patterns (β-CD/PEG); inset emission spectra active β-CD areas (green,■), passivated PEG areas (open,□). Images are taken from [11].

triangle trace ▼), which proves that the integrity of LH2 proteins is maintained during the labeling and surface adsorption procedures. The emission spectra shown in Figure 6.3 (b) indicate the selective assembly of the proteins to the β-CD (green box trace ■) area while the PEG SAM functions as a protein-resistant layer (open box trace □).

The solution AFM image of the assembly of Ad_nLH2 complexes on the β-CD surface is shown in Figure 6.4 (a). Although the sample with nanoridges of 40 nm wide was used in T-NIL, it is observed that the width of bionanoassemblies increases to 80±5 nm as a result of residual layer removal by O_2 RIE (Figure 6.1(c)). The fluorescence image as shown in Figure 6.4(b) also indicates that the LH2 complexes remain fluorescent upon chemical modification and patterning on the surface, i.e. the biological activity of the complexes is preserved during the process. Further experimental data support excitonic transport along the nanometer wide LH2 lines [11].

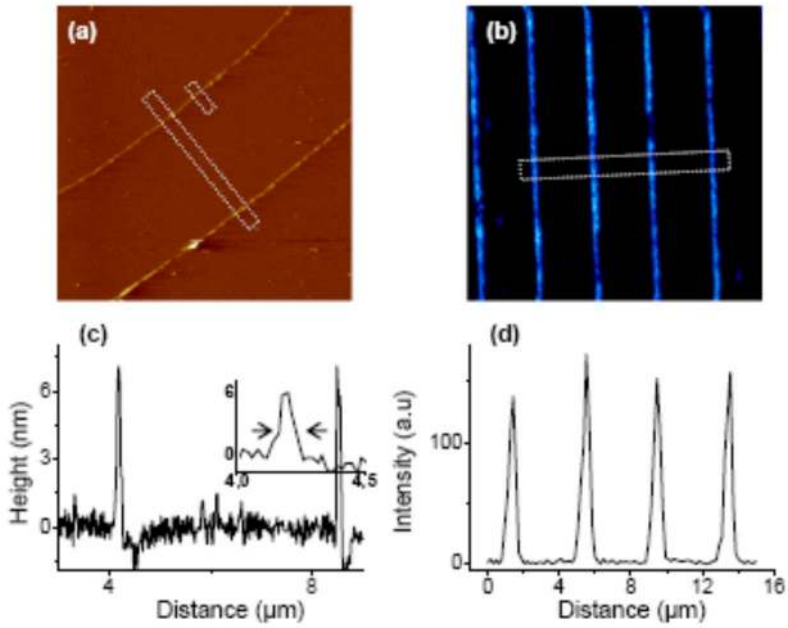

Figure 6.4: (a) AFM height image in liquid of $Ad_nLH2\beta$-CD/PEG SAM; (b) False color fluorescence image; (c) FWHM of 80 nm; (d)cross section of (b). Images are taken from [11].

6.3.2 High resolution PDMS-glass soft stamp fabrication by T-NIL and its application in μCP

Composite stamps take advantage of the stiffness brought by the glass substrate as well as the flexibility of PDMS to obtain conformal contact. The schematic of the PDMS-glass stamp fabrication by T-NIL is shown in Figure 6.5. Here, the glass is used to provide

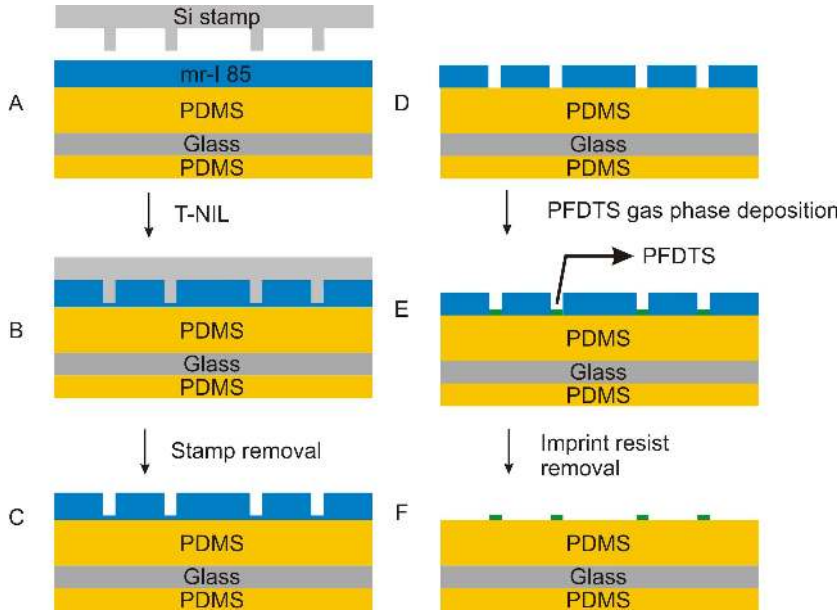

Figure 6.5: Schematic of glass-PDMS stamp fabrication [13]

support for the application of pressure during T-NIL. During T-NIL on the PDMS surface, mr-I 85 was explored as the proper T-NIL resist instead of the commonly used PMMA (T_g=98°C) because of its lower T_g of 85°C and lower imprint pressure to avoid damaging PDMS and was to obtain a better adhesion to the PDMS surface. The imprint resist thickness was tuned to have a maximum residual layer thickness of 10 nm after T-NIL to avoid loss of resolution and damage to the PDMS surface during O_2 RIE. A low pressure (2 bar) was applied taking advantage of the conformal contact brought by the flexible PDMS substrate. After the formation of the PFDTS chemical patterns, the imprint resist was removed by cyclohexane. Although the solvent also causes some swelling of the PDMS, it is reversible upon applying vacuum. Therefore, the resolution of the PFDTS patterns is not compromised, which is proven by the followed μCP results.

The chemically patterned PDMS-glass stamps fabricated by T-NIL were employed in μCP. Figure 6.6 shows the schematics of (-)μCP and (+)μCP. By following these procedures [13], the results of applying the stamp containing Si nanoridges for T-NIL application and the subsequent (-)/(+)μCP are shown in Figure 6.7. Si nanoridges of 50 nm wide and 100 nm high were used for T-NIL to fabricate the composite PDMS-glass stamps. Nanogrooves of about 50±5 nm wide were achieved in mr-I 85 on the PDMS

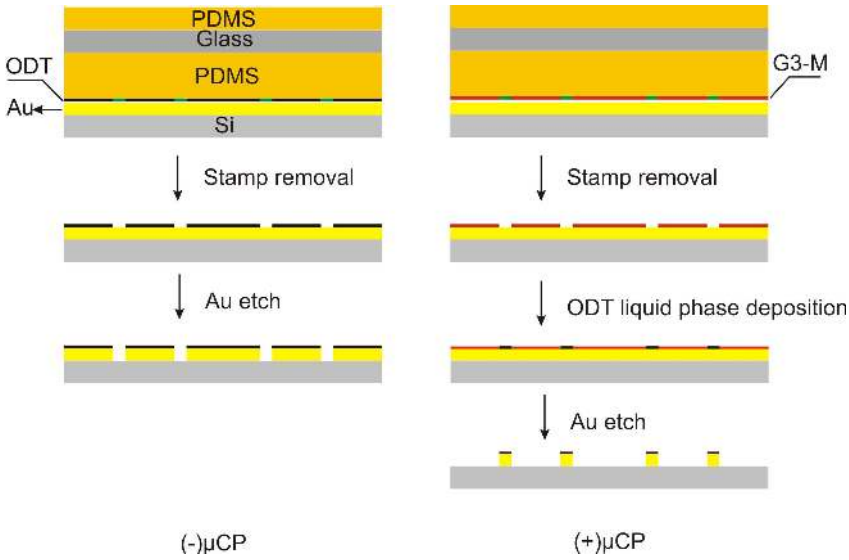

Figure 6.6: Schematic nanofabrication by (-)μCP and (+)μCP [13]

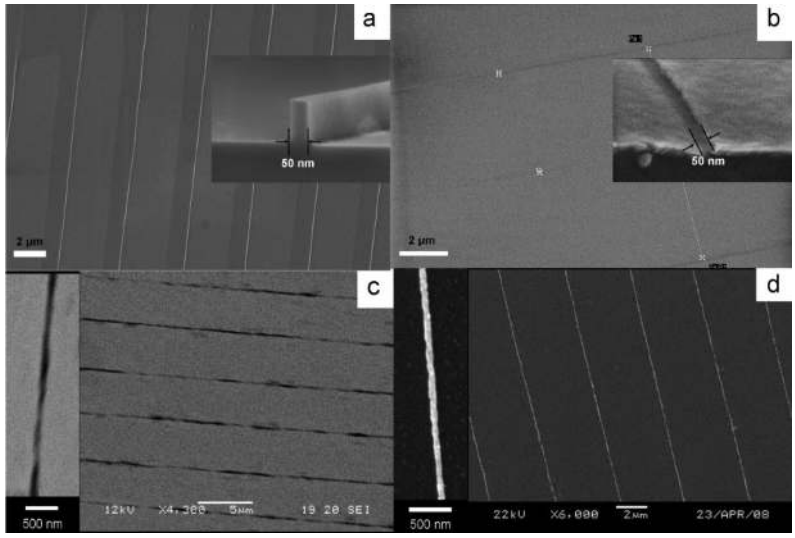

Figure 6.7: (a)SEM image of the top view of the imprint stamp; (b)imprint result in mr-I 85 on the glass-PDMS substrate; (c)Au nanogrooves made by (-)μCP; (d)Au nanolines made by (-)μCP, taken from [13].

substrate. The distortion of pattern definition was controlled by minimizing the residual layer thickness by spin coating. The PFDTS modified PDMS stamps were used for μCP on a Au surface and consequently for creating Au nanogrooves of 95±25 nm wide by (-)μCP and nanolines of 85±10 nm wide by (+)μCP. The increase of the widths of the nanogrooves and nanolines is fully attributed to isotropic wet-etching of the gold, which indicates that ink diffusion is not an issue here.

6.3.3 High resolution PDMS-glass μCP stamp fabrication by CFL and nanofabrication by μCP

CFL was used as another method to create chemically patterned flat stamps. In CFL, as shown in Figure 6.8, pressure may build up within the voids between imprint stamp and

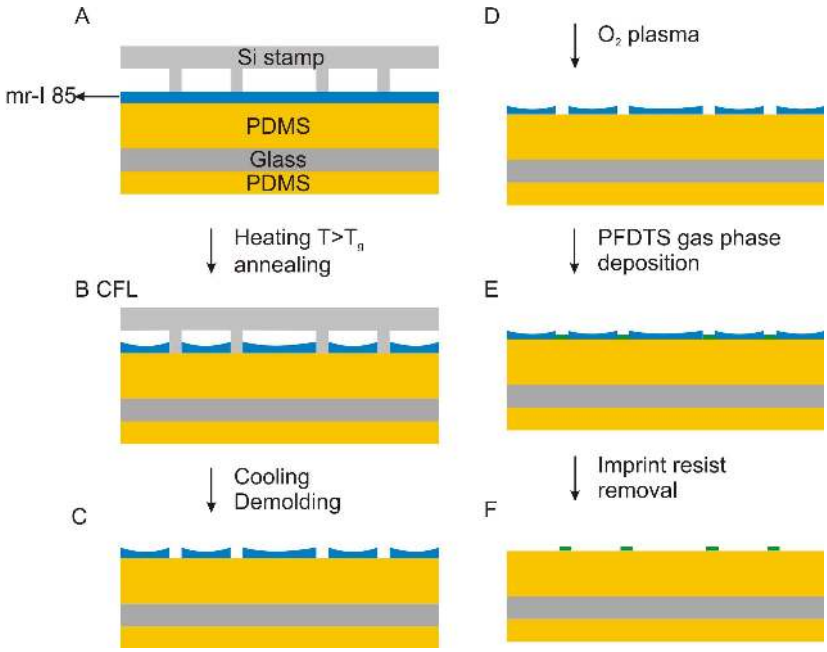

Figure 6.8: Schematic of glass-PDMS stamp fabrication by CFL [14]

substrate. Therefore, the thickness of the spin-coated imprint resist (mr-I 85) was put to half of the step height of the imprint stamp to avoid problems of the pressure build-up. In this experiment, a resist layer of 20 nm was used when the sub-100 nm wide Si nanoridge stamp was utilized for CFL. Before CFL, the Si stamp and PDMS substrate with the spin-coated imprint polymer were placed in a 150°C preheated vacuum oven for 30 min

for equilibration. The temperature was set higher than the T_g of the imprint resist (mr-I 85) to ensure polymer mobility for CFL. During CFL, a small weight of about 0.1 bar was applied on top of the Si stamp to prevent the separation substrate and stamp. CFL offers the advantage of patterning the flat PDMS surface without the formation of a residual layer, and hence the O_2 plasma etching time is shortened, and only serves the purpose of PDMS surface activation. Moreover, the low pressure applied during CFL avoids damage to the PDMS surface.

By using CFL, nanogrooves of about 50 nm separated by 4 μm were fabricated in the imprint resist on top of the PDMS surface as shown in Figure 6.9. Since the space between Si nanoridges (4 μm) is much larger than the width of Si nanoridges (50 nm), the polymer can easily move into the cavities and form a U-shape along the sides of the Si nanoridges. Therefore, the polymer thickness does not experience a great change before and after CFL. Figure 6.10 shows the SEM image of 80±15 wide Au nanolines fabricated by (+)μCP (see Figure 6.7) using a CFL-fabricated PDMS-glass stamp. The observed feature widening is attributed to the wet etching step.

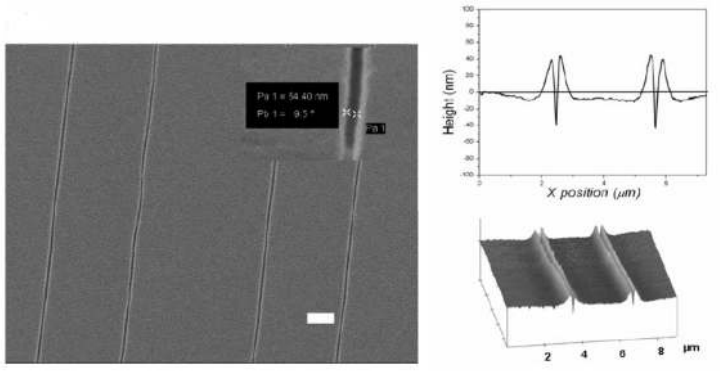

Figure 6.9: SEM and AFM images of nanogrooves fabricated by CFL, taken from [14].

6.4 Conclusions

Stamps composed of Si nanoridges as described in Chapter 3 have been successfully demonstrated for application in alternative nanofabrication schemes. The assembly of Ad_nLH2 complexes on β-CD surfaces was accomplished by the combination of T-NIL and self-assembly by multivalent host-guest interactions. The LH2 nanolines are achieved on a 80 nm wide scale. The fluorescence spectral indicate that the integrity of LH2

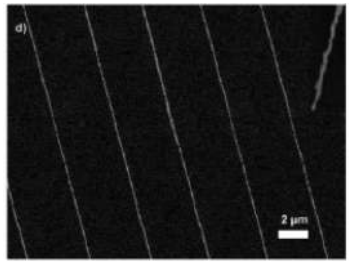

Figure 6.10: SEM image of 80±15 nm wide Au nano lines fabricated by (+)μCP using a CFL fabricated PDMS-glass stamp. Image is taken from [14].

complexes remained unaltered upon chemical modification and patterning on the surface. The use of T-NIL provides high-throughput fabrication of bionanoassenblies on surfaces for the investigation of protein properties.

Chemically patterned PDMS-glass stamps were fabricated by T-NIL and CFL. T-NIL enables the achievement of sub-100 nm pattern definition on the PDMS-glass substrate. CFL was further utilized for PDMS-glass substrate patterning to avoid PDMS distortion. The flexible nature of PDMS facilitates conformal contact in both T-NIL and CFL. Nanogrooves of ca. 90 nm width as well as nanolines of ca. 80 nm width in Au substrate were fabricated by μCP and wet etching techniques. The use of high resolution PDMS-glass stamps for μCP eliminates the ink diffusion and stamp deformation problems which are encountered when using conventional PDMS stamps and therefore enables the achievement of high resolution nano-sized pattern definition by μCP.

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Chapter 7

Conclusions and outlook

7.1 Conclusions

The fabrication of high resolution stamps for thermal nanoimprint applications has been presented. Instead of creating nanostructures by means of high resolution lithographic techniques, we demonstrated the fabrication of nanoridges with conventional UV lithography and edge lithography. In Chapter 2, SiO_2 nanoridges reinforced with an additional SiN_x shield have been fabricated by oxidizing vertical Si trench sidewalls. From Chapter 3 to Chapter 5, advanced edge lithography schemes have been presented creating monolithic Si nanoridges. Nanoridges in line-shaped contours have been fabricated through Chapter 2 to Chapter 4. The fabrication schemes employ wet Si anisotropic etching techniques by taking advantage of Si <110> wafers. OPD 4262 was used as the proper Si etchant in the SiO_2 and monocrystalline Si nanoridge fabrication schemes while 20% KOH was employed for creating multi-Si nanoridges. In Chapter 5, a cryogenic Si plasma etching recipe has been developed for fabricating Si nanoridges with arbitrary contours by advanced edge lithography. In the wet anisotropic etching dominated scheme, a smooth Si sidewall finish has been achieved taking advantage of Si wet anisotropic etching which automatically stops at Si <111> planes. In the Si dry plasma etching scheme, Si nanoridges with circular contours have been fabricated using a 500 nm SU-8 layer for pattern definition and as the plasma etching masking material. SU-8 is preferred to the combination of positive photoresist and Cr in achieving a smooth Si sidewall finish.

Si edges have been created by SiN_x lateral retraction etching in the advanced edge lithography schemes. 50%HF was used when the retraction etching is performed with a single SiN_x layer. H_3PO_4 heated up to 180°C was used when TEOS was used as the mask

for retraction etching. H_3PO_4 has the disadvantage over 50%HF that erosion occurs at sharp Si step edges during retraction etching.

The edge lithography schemes were performed by local oxidation of Si using SiN_x as the mask and selective etching of SiN_x and SiO_2 in H_3PO_4. The oxidation of Si edges with a vertical sidewall introduces the sharpening of the Si convex corner while the concave corner at the bottom of the edge is rounded. Sidewall cleavage was observed as a result of this non-uniform SiO_2 layer thickness in the multi-Si nanoridge fabrication scheme. We proved that the convex corner sharpening can be released by increasing the oxidation temperature as has been suggested previously by other researchers. However, the increase of oxidation temperature leads to the change of SiN_x properties, which consequently showed as the decreasing of SiN_x etch rates both in 50%HF and H_3PO_4. A infinite etch selectivity between SiN_x and SiO_2 is highly appriciated in the Si plasma etching scheme.

Si nanoridges presented in Chapter 3 have been repeatedly used in nanoimprint processes. The Si material satisfies the general requirements of thermal NIL, i.e. the shape of nanostructures is retained during the high temperature and pressure imprint process. Moreover, monolithic Si nanoridges with a sub-20 nm width have been proven to be much stronger in enduring the mechanical demolding step than SiO_2 nanoridges with the same dimensions, which are broken as a result of the fragile SiO_2 corner. Moreover, it was observed that the shape of the high resolution Si nanoridges can be faithfully replicated in the thermoplastic imprint polymer. The high fidelity pattern transfer ensures T-NIL to be used as a relatively easy and high-throughput nanofabrication method. In Chapter 6, the nanoassembly of light harvesting antenna complexes with a resolution of about 80 nm has been achieved with the combination of T-NIL and self-assembly. The Si nanoridges have also been employed to fabricate high resolution chemically patterned PMDS-glass stamps for μCP either by T-NIL or CFL. Since conventional UV lithography was employed for initial pattern definition, the presented fabrication schemes allow for batch processing and the nanoridge structures are separated by micrometer spacings. These less densely distributed nanostructures are beneficial for the ease of protein observation by fluorescence microscopy and prohibit ink diffusion during μCP.

7.2 Outlook

In this thesis, nanoridges have been created by edge lithography in combination with the conventional UV lithography technique. The pattern resolution is defined by the material deposited at step edges instead of being determined by the lithographic tools. Therefore, this method provides an alternate way of fabricating high resolution nano-

structures without the implementation of high resolution lithographic tools. Moreover, the edge lithography is an add-on technology which in principle can be integrated with any lithography technique to further improve the lithographic resolution.

The concept of edge lithography was explored in this thesis by means of SiN_x retraction etching and oxidation of Si using SiN_x as the mask. As discussed in the previous section, we encountered problems such as non-uniform SiO_2 layer thickness during oxidizing structured Si surfaces and etching selectivities of SiN_x to SiO_2 and Si in H_3PO_4. These problems are inherent from the micromachining technology and therefore can not be solved easily at present. To avoid these problems, the presented edge lithography concept can be approached using new schemes by means of alternative passivation and selective etching methods.

The fabricated Si nanoridges have been successfully applied for fabricating bionanoassemblies and for creating high resolution chemically patterned PDMS-glass stamps. Owing to the high fidelity of pattern replication by NIL, we believe that edge lithography can be further investigated to create structures applicable to other nanofabrication methodologies, e.g. in nano-fluidic and nanoelectronics.

Appendix A

Experimental data

A.1 Deposition methods and conditions

1. Spin coating

   Uniform layers of positive photoresist (Olin 907-12 and Olin 907-17), negative photoresist SU-8 and T-NIL resist PMMA are all obtained by spin coating. For the ease of maintenance, these three types of organic polymer are coated on dedicated spin-coaters. Positive and negative resist coating were performed by Delta 20 spin-coater which has a spin speed up to 6000 rpm. PMMA film is obtained by Delta 10 spin-coater. Positive photoresist and SU-8 were spin-coated at 3000 rpm in the experiments, after which 1.7 μm thick Olin 907-17, 1.2 μm thick Olin 907-12 and 450 nm thick SU-8 2000.5 can be obtained. Approximately 80 nm and 100 nm PMMA layers can be obtained by spin-coating 2 wt.% and 3 wt.% PMMA solution in toluene at a speed of 3000 rpm.

2. Dry oxidation of Si

   Dry oxidation of Si and nitride/oxide annealing processes were performed in the Amtech Tempress Omega Junior system, which is referred as A2 in the MESA+ nanolab. O_2 and N_2 are available in the system. The standby temperature of the system is 700°C and the maximum temperature can reach up to 1150°C. During system temperature ramping up/down, the temperature is incresed/decreased by 2°C/min with N_2 continuously flushing the system. O_2 is released into the system when the tube temperature reached the desired value. The oxidation was performed at 950°C through the thesis and Table A.1 can be used as a reference for oxidation.

Oxidation (min)	Si <100> oxide (nm)	Si <110> oxide (nm)
0	2.27	2.38
6	8.29	12.33
12	12.2	17.51
24	17.78	25.67
48	28.06	38.58
96	45.68	59.1
192	75.88	91.43

Table A.1: Oxide thickness vs. oxidation time at 950°C

3. LPCVD silicon rich nitride (SiN_x)

   SiN_x was deposited by Amtech Tempress Diffusion system. Two types of SiN_x can be deposited by two Amtech Tempress Diffusion systems, which are referred as G3 and G4 in the MESA+ nanolab. In the G3 tube, the deposition temperature is 850°C and pressure is 150 mTorr with a gas flow of SiH_2Cl_2 and NH_3 of 100 and 25 sccm respectively. The deposition rate is ca. 3.9 to 6 nm/min. In the G4 tube, the deposition temperature is 850°C and pressure is 200 mTorr with a a gas flow of SiH_2Cl_2 and NH_3 of 150 and 50 sccm respectively. The deposition rate is 10 nm/min. The standby temperature is 750°C for G3 and 700°C for G4.

4. LPCVD TEOS

   TEOS was deposited using the Amtech Tempress Omega Junior system. The system has a standby temperature of 600°C. The deposition is performed at 700°C and a pressure of 200 mTorr by pyrolysis of $Si(OC_2H_2)_4$, which has a flow rate of 50 sccm during deposition. The deposition rate in this case is ca. 10 nm/min.

5. LPCVD Poly-Si

   The deposition of ploy-Si was performed by Amtech Tempress Omega Junior system. The poly-Si film is deposited by pyrolysis of SiH_4 at a temperature of 590°C or at 610°C and a pressure of 200 mTorr. The deposition rate in this case is ca. 3.3 nm/min. Amorphous Si is obtained by the same system by lowering the temperature to either 500°C or 550°C. The deposition rate is ca. 1.7 nm/min. The stand by temperature of the system is 610°C.

6. Cr evaporation

Cr was deposited by evaporation by e-gun evaporation machine Balzers BAK 600. The base pressure of system is 2e-6 mbar. Before deposition, the base pressure should be pumped lower than 2e-6 mbar. During evaporation, the metal source is heated up by current, e.g. the evaporation rate is ca. 1.1Å /s at 36 mA current.

A.2 Etch rates

The etch rates of materials used in this thesis in different etchants and temperatures are listed in Table A.2. Detailed information concerning KOH and TMAH etching is documented in [1, 2, 3]. The etch rates of SiN_x as listed in Table A.2 are obtained by testing the SiN_x from G3 tube. The composition of SiN_x obtained from G3 and G4 is different since the gas composition is different during deposition. The etch rate of SiN_x from G4 in 50% HF is 4.8 nm/min while the etch rate in H_3PO_4 remains the same as that from G3.

A.3 Dry plasma etching equipments and settings

In this thesis, dry plasma etching was performed in the form of pure chemical etching, reactive ion etching and cryogenic etching. Tepla 300 O_2 plasma etching system is a barrel system and is used for organic materials stripping, which can accommodate 25 wafers maximum for one run. The operating power is up to 1000 W and the pressure is 1 mbar. Chamber temperature can not be controlled but is measured to be ca. 140°C.

Reactive ion etching was performed using Elektrotech Twin system PF 340 which consists of a parallel-plate system with an RF generator operating at 13.56 MHz. The temperature of the substrate holder is water cooled at 10°C. O_2, CHF_3, SF_6 and N_2 are the available gases in the system. Directional polymer etching by O_2 plasma and SiN_x etching are achieved by this system. For polymer etching, the parameter setting is chosen according to specific requirement which can be found in the thesis. SiN_x RIE recipe is employed as explored before. The parameters and settings are listed in Table A.3.

In Si cryogenic etching, Alcatel/Adixen AMS 100 SE deep reactive ion etching (DRIE) system was used. It is a dual source DRIE system with maximum ICP of 2500 W and two CCP sources, which are 300 W radio frequency (RF, operating at 13.56 MHz) source and 500 W low frequency (LF, operating between 25 and 460 KHz) source. The system is able to process both cryogenic mixed-mode (down to -180C) and room temperature pulsed-mode etching [6]. Wafer is clamped mechanically and backside cooled by helium which ensures effective heat exchange. The parameters and settings are listed in Table A.4.

		25%KOH, 75°C, [nm/min]	20%KOH, 20°C, [nm/min]	5%TMAH, 75°C, [nm/min]	OPD4262, 20°C, [nm/min]	1%HF	50%HF	H_3PO_4, 180°C
Si	<100>	1000	25	560	3.8 [4]	-	-	0.3 [5]
	<110>	1400	25	740	3.7	-	-	-
	<111>	12.5	1	30	0.7	-	-	-
SiO_2		3	<0.2	1	<0.01	4.5	>1000	0.29
TEOS	intrinsic	-	-	-	-	31	>1000	2.9
	annealed 900°C	-	-	-	-	12	>1000	0.55
	annealed 1050°C	-	-	-	-	4.6	>1000	0.29
SiN_x (G3)	intrinsic	<0.01	0.01	-	-	-	2.7	4.2
	annealed 900°C	<0.01	-	-	-	-	2.7	4.2
	annealed 1050°C	<0.01	-	-	-	-	1.7	3.9
Si_3N_4		-	0.01	-	-	-	-	4.2

Table A.2: Etch rates of materials in different wet etchants

Parameter	value
System	Elektrotech Twin system PF 340
Gases	CHF_3 25 sccm / O_2 5 sccm
Substrate temperature	10°C
Power	75 W
Chamber pressure	10 mTorr (no shower head implementation)

Table A.3: SiN_x RIE recipe

Parameter	value
System	Alcatel/Adixen AMS 100 SE DRIE system
Gases	SF_6 15 sccm / O_2 30 sccm
Substrate temperature	-100°C
ICP Power	200 W
CCP (LF) power	20W (20 msec ON, 80 msec OFF)
Substrate distance fro source	200 mm
Throttle valve position	100%

Table A.4: Cryogenic Si etching recipe

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Appendix B

Process documents

B.1 SiO_2 nanoridges and nanoridges reinforced with SiN_x deposition

Nr.	Process	Process parameters	Comments
1	Substrate selection -Silicon <110> DSP	CR112B/Wafer Storage Cupboard Supplier: Orientation: <110> Diameter: 100mm ± mm Thickness: 380m ± 10 μm Polished: Double side polished (DSP) Resistivity: 5-10 Ωm Type: p	
2	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
3	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	

4	LPCVD SiN_x -uniform thickness	CR125C/Tempress LPCVD G3 Program: SiRN01 • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • temperature: 820/850/870°C • pressure: 150 mTorr • N_2 low: 250 sccm • deposition rate: 4 nm/min • reflective index (n): 2.180	15 nm
5	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
6	LPCVD TEOS	CR112B/Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0°C Temperature: 700°C • program: TEOS05 • deposition rate: 10.7 nm/min • Uniformity/wafer: 3% • pressure: 150 mTorr • N_2 low: 250 sccm • reflective index (n): 1.44 • stress after deposition: -5 Mpa • stress after two weeks: -20 Mpa • stress after anneal of 700°C: +5 Mpa	40 nm
7	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
8	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
9	Lithography -Priming (liquid)	CR112B/Suss Micro Tech Spinner (Delta 20) Hotplate 120°C HexaMethylDiSilazane (HMDS) • Dehydration bake (120°C): 5min • Spin program: 4 (4000rpm, 20sec)	
10	Lithography	CR112B/Suss Micro Tech Spinner	

	-Coating Olin907-12	(Delta 20) Hotplate 95°C Olin 907-12 • Spin Program: 4 (4000 rpm, 20 sec) • Prebake (95°C): 60s	
11	Lithography Alignment & Exposure Olin 907-12 (EV)	CR117B/EV620 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Exposure Time: 3.5 sec	
12	Lithography Development Olin Resist	CR112B/Wet-Bench 11 Developer: OPD4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60 sec Development: • Time: 30 sec in Beaker 1 • Time: 15-30 sec in Beaker 1 • Quick Dump Rinse <0.1μS • Spin drying	
13	Lithography -Postbake standard	CR112B/Hotplate 120°C • Time: 30 min	
14	Ozone anneal of Olin 907 (to improve wetting)	CR116B-1/UV PRS-100 • Time: 300 sec	
15	Etching BHF (7:1) SiO_2	CR112B/Wet-Bench 3-3 NH_4F/HF (7:1) VLSI: BASF • Quick Dump Rinse <0.1μS • Spin drying Etch rate thermal SiO_2 = 60-80 nm/min Etchrate PECVD SiO_2 = 125 nm/min Etchrate TEOS = 180 nm/min	
16	Stripping of Olin PR - standard	CR112B/Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20 min • Quick Dump Rinse <0.1μS • Spin drying Visual microscopic inspection	
17	Etching of SiN_x (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	
18	Etching 1%HF -user made	CR116B/Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1μS	Strip TEOS

		• Spin drying	
19	Anisotropic etching of Si	CR116B/Wet-Bench 1&2 OPD 4262 Arch developer solution • Si etch rate: <110> 3.5 nm/min • Quick Dump Rinse <0.1μS • Spin drying	
20	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
21	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
22	Dry Oxidation at 950°C of Si	CR112B/Furnace A2 Standby temp.: 700°C • Program: Dry950 • Temp.: 950°C • Gas: O_2	LOCOS
23	Etching of SiN_x (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	
24	Anisotropic etching of Si	CR116B/Wet-Bench 1&2 OPD 4262 Arch developer solution • Si etch rate: <110> 3.5 nm/min • Quick Dump Rinse <0.1μS • Spin drying	
25	LPCVD SiN_x -uniform thickness	CR125C/Tempress LPCVD G3 Program: SiRN01 • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • temperature: 820/850/870°C • pressure: 150 mTorr • N_2 low: 250 sccm • deposition rate: 4 nm/min	For SiN_x over -deposition

		• reflective index (n): 2.180	

B.2 Si nanoridge fabrication

Nr.	Process	Process parameters	Comments
1	Substrate selection -Silicon <110> DSP	CR112B/Wafer Storage Cupboard Supplier: Orientation: <110> Diameter: 100mm ± mm Thickness: 380m ± 10 μm Polished: Double side polished (DSP) Resistivity: 5-10 Ωm Type: p	
2	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
3	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
4	LPCVD SiN_x -uniform thickness	CR125C/Tempress LPCVD G3 Program: SiRN01 • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • temperature: 820/850/870°C • pressure: 150 mTorr • N_2 low: 250 sccm • deposition rate: ± 4 nm/min • reflective index (n): 2.180	15 nm
5	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
6	LPCVD TEOS	CR112B/Tempress LPCVD B4 Tube: B4-TEOS	

		Bubbler: 40.0°C Temperature: 700°C • program: TEOS05 • deposition rate: 10.7 nm/min • Uniformity/wafer: 3% • pressure: 150 mTorr • N_2 low: 250 sccm • reflective index (n): 1.44 • stress after deposition: -5 Mpa • stress after two weeks: -20 Mpa • stress after anneal of 700°C: +5 Mpa	80 nm
7	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
8	Annealing at 900°C with N2	CR112B/Furnace A2 Standby temp.: 700°C • Program: Anneal900 • Temp.: 900°C • Gas: N_2	1 h
9	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse $<0.1\mu$S • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse $<0.1\mu$S • Spin drying	
10	Lithography -Priming (liquid)	CR112B/Suss Micro Tech Spinner (Delta 20) Hotplate 120°C HexaMethylDiSilazane (HMDS) • Dehydration bake (120°C): 5min • Spin program: 4 (4000rpm, 20sec)	
11	Lithography -Coating Olin907-12	CR112B/Suss Micro Tech Spinner (Delta 20) Hotplate 95°C Olin 907-12 • Spin Program: 4 (4000rpm, 20sec) • Prebake (95°C): 60s	
12	Lithography Alignment & Exposure Olin 907-12 (EV)	CR117B/EV620 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2	

		• Exposure Time: 3.5sec	
13	Lithography Development Olin Resist	CR112B/Wet-Bench 11 Developer: OPD4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30 sec in Beaker 1 • Time: 15-30 sec in Beaker 1 • Quick Dump Rinse <0.1μS • Spin drying	
14	Lithography -Postbake standard	CR112B/Hotplate 120°C • Time: 30 min	
15	Ozone anneal of Olin 907 (to improve wetting)	CR116B-1/UV PRS-100 • Time: 300 sec	
16	Etching BHF (7:1) SiO_2	CR112B/Wet-Bench 3-3 NH_4F/HF (7:1) VLSI: BASF • Quick Dump Rinse <0.1μS • Spin drying Etch rate thermal SiO_2 = 60-80 nm/min Etchrate PECVD SiO_2 = 125 nm/min Etchrate TEOS = 180 nm/min	
17	Stripping of Olin PR - standard	CR112B/Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20 min • Quick Dump Rinse <0.1μS • Spin drying Visual microscopic inspection	
18	Etching of SiN_x (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	
19	Anisotropic etching of Si	CR116B/Wet-Bench 1&2 OPD 4262 Arch developer solution • Si etch rate: <110> 3.5 nm/min • Quick Dump Rinse <0.1μS • Spin drying	
20	Etching of SiN (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	SiN_x under- cut etching

21	Etching 1%HF user made	CR116B/Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1μS • Spin drying	Strip TEOS
22	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
23	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
24	Dry Oxidation at 950°C of Si	CR112B/Furnace A2 Standby temp.: 700°C • Program: Dry950 • Temp.: 950°C • Gas: O_2	LOCOS 5 min
25	Etching of SiN_x (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	Strip SiN_x
26	Anisotropic etching of Si	CR116B/Wet-Bench 1&2 OPD 4262 Arch developer solution • Si etch rate: <110> 3.5 nm/min • Quick Dump Rinse <0.1μS • Spin drying	
27	Etching 1%HF user made	CR116B/Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1μS • Spin drying	Strip SiO_2

B.3 Multi-Si nanoridge fabrication

Nr.	Process	Process parameters	Comments
1	Substrate selection -Silicon <110> DSP	CR112B/Wafer Storage Cupboard Supplier: Orientation: <110> Diameter: 100mm ± mm Thickness: 380m ± 10 μm Polished: Double side polished (DSP) Resistivity: 5-10 Ωm Type: p	
2	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
3	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
4	LPCVD SiN_x -uniform thickness	CR125C/Tempress LPCVD G3 Program: SiRN01 • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • temperature: 820/850/870°C • pressure: 150 mTorr • N_2 low: 250 sccm • deposition rate: ± 4 nm/min • reflective index (n): 2.180	200 nm
5	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
6	LPCVD TEOS	CR112B/Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0°C Temperature: 700°C • program: TEOS05 • deposition rate: 10.7 nm/min • Uniformity/wafer: 3%	50 nm

		• pressure: 150 mTorr • N_2 low: 250 sccm • reflective index (n): 1.44 • stress after deposition: -5 Mpa • stress after two weeks: -20 Mpa • stress after anneal of 700°C: +5 Mpa	
7	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
8	Annealing at 1050°C with N2	CR112B/Furnace A2 Standby temp.: 700°C • Program: Anneal1050 • Temp.: 1050°C • Gas: N_2	1 h
9	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
10	Lithography -Priming (liquid)	CR112B/Suss Micro Tech Spinner (Delta 20) Hotplate 120°C HexaMethylDiSilazane (HMDS) • Dehydration bake (120°C): 5min • Spin program: 4 (4000rpm, 20sec)	
11	Lithography -Coating Olin907-12	CR112B/Suss Micro Tech Spinner (Delta 20) Hotplate 95°C Olin 907-12 • Spin Program: 4 (4000rpm, 20sec) • Prebake (95°C): 60s	
12	Lithography Alignment & Exposure Olin 907-12 (EV)	CR117B/EV620 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Exposure Time: 3.5sec	
13	Lithography Development Olin Resist	CR112B/Wet-Bench 11 Developer: OPD4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development:	

		• Time: 30 sec in Beaker 1 • Time: 15-30 sec in Beaker 1 • Quick Dump Rinse <0.1μS • Spin drying	
14	Lithography -Postbake standard	CR112B/Hotplate 120°C • Time: 30 min	
15	Ozone anneal of Olin 907 (to improve wetting)	CR116B-1/UV PRS-100 • Time: 300 sec	
16	Etching BHF (7:1) SiO_2	CR112B/Wet-Bench 3-3 NH_4F/HF (7:1) VLSI: BASF • Quick Dump Rinse <0.1μS • Spin drying Etch rate thermal SiO_2 = 60-80 nm/min Etchrate PECVD SiO_2 = 125 nm/min Etchrate TEOS = 180 nm/min	
17	Stripping of Olin PR - standard	CR112B/Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20 min • Quick Dump Rinse <0.1μS • Spin drying Visual microscopic inspection	
18	Etching of SiN_x (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	
19	Etching 1%HF user made	CR116B/Wet-Bench 2 HF (1%) VLSI: MERCK 112629.500 • Quick Dump Rinse <0.1μS • Spin drying	Strip TEOS
20	Anisotropic etching of Si by 20%KOH	CR116B/Wet-Bench 1&2 KOH: MERCK 105019.500 KOH:DI = (1:4) • Temp.: 20°C • Si etch rate: <110> 25 nm/min • Quick Dump Rinse <0.1μS • Spin drying	
21	Cleaning RCA-2 $HCl/H_2O_2/H_2O$	CR112B / Wet-Bench 130 HCL (36%) Selectipur, BASF H_2O_2 (31%) VLSI, BASF $HCl:H_2O_2:H_2O$ = 1:1:5 vol% • add HCl to H_2O • add H_2O_2 when mixure at 70°C	

		• Temp.: 70-80°C • cleaning time 10-15min • Quick Dump Rinse <0.1μS • Spin drying	
22*	Etching 50%HF user made	CR116B/Wet-Bench 2 HF (50%) VLSI: MERCK 100373.2500 • Quick Dump Rinse <0.1μS • Spin drying	SiN_x retraction
23*	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
24*	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
25*	Dry Oxidation at 950°C of Si	CR112B/Furnace A2 Standby temp.: 700°C • Program: Dry950 • Temp.: 950°C • Gas: O_2	LOCOS 15 min
26*	Etching of SiN (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	SiN_x under- cut etching
27*	Anisotropic etching of Si by 20%KOH	CR116B/Wet-Bench 1&2 KOH: MERCK 105019.500 KOH:DI = (1:4) • Temp.: 20°C • Si etch rate: <110> 25 nm/min • Quick Dump Rinse <0.1μS • Spin drying	
28*	Cleaning RCA-2 $HCl/H_2O_2/H_2O$	CR112B / Wet-Bench 130 HCL (36%) Selectipur, BASF H_2O_2 (31%) VLSI, BASF	

		$HCl:H_2O_2:H_2O$ = 1:1:5 vol% • add HCl to H_2O • add H_2O_2 when mixure at 70°C • Temp.: 70-80°C • cleaning time 10-15min • Quick Dump Rinse <0.1μS • Spin drying	

The steps marked with * are repeated to fabricate multi-Si nanoridges.

B.4 Plasma etching scheme: Si nanoridge fabrication by positive photoresist and Cr as the mask

Nr.	Process	Process parameters	Comments
1	Substrate selection -Silicon <100> OSP	CR112B/Wafer Storage Cupboard Supplier: Orientation: <100> Diameter: 100mm ± mm Thickness: 550m ± 10 μm Polished: Single side polished (OSP) Resistivity: 5-10 Ωm Type: p	
2	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
3	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
4	LPCVD SiN_x -uniform thickness	CR125C/Tempress LPCVD G3 Program: SiRN01 • SiH_2Cl_2 flow: 77.5 sccm	60 nm

		• NH_3 flow: 20 sccm • temperature: 820/850/870°C • pressure: 150 mTorr • N_2 low: 250 sccm • deposition rate: ± 4 nm/min • reflective index (n): 2.180	
5	Ellipsometer Measurement	CR118B/Plasmos Ellipsometer	
6	Evaporation of Cr -BAK600	CR106A / Balzers BAK600 • Crucible: 3 (Chromium) • Voltage: 8kV • Emission current: see mis logbook % • Base pressure: <1e-6 mBar Density: 7.2 Deposition rate: 1-20 Å/s	
7	Lithography -Coating Olin907-17	CR112B/Suss Micro Tech Spinner (Delta 20) Hotplate 95°C Olin 907-17 • Spin Program: 4 (4000rpm, 20sec) • Prebake (95°C): 60s	
8	Lithography Alignment & Exposure Olin 907-17 (EV)	CR117B/EV620 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Exposure Time: 4 sec	
9	Lithography Development Olin Resist	CR112B/Wet-Bench 11 Developer: OPD4262 Hotplate 120°C (CR112B or CR117B) • After Exposure Bake (120°C): 60sec Development: • Time: 30 sec in Beaker 1 • Time: 15-30 sec in Beaker 1 • Quick Dump Rinse <0.1μS • Spin drying	
10	Ozone anneal of Olin 907 (to improve wetting)	CR116B-1/UV PRS-100 • Time: 300 sec	
11	Etching of Cr Wet	CR116B/Wet-Bench 2 Chromium etch LSI Selectipur: MERCK 111547.2500 • Quick Dump Rinse <0.1μS • Spin drying Etch rate: 100 nm/min	
12	Plasma etching PR -Eske	CR102A/Elektrotech PF310/340 Clean chamber	PR retraction

		Aluminium electrode, quarts substrate Showerhead • Electrode temp.:10°C • O_2: 20 sccm • pressure: 100 mTorr • power: 50 W Etch rate: 100 nm/min	etching 90 sec
13	Plasma etching SiN_x -Eske	CR102A/Elektrotech PF310/340 Clean chamber Aluminium electrode, quarts substrate • Electrode temp.:10°C • CHF_3 flow: 25sccm • O_2: 5 sccm • pressure: 10 mTorr • power: 75 W	
14	Lithography -Postbake standard	CR112B/Hotplate 120°C • Time: 30 min	
15	Plasma etching Si -Adixen	CR125c/Adixen SE Cleaning before etching • Temp.:-100°C • SF_6 flow: 15sccm • O_2: 30 sccm • Valve: 100 % • ICP: 200 W • CCP: 20 W (20/80 msec, on/off) • SH: 200 mm	
16	Stripping of Olin PR -user made	CR112B/Wet-Bench 3-2 HNO_3 (100%) Selectipur: MERCK 100453 • Time: 20 min • Quick Dump Rinse <0.1μS • Spin drying Visual microscopic inspection	
17	Etching of Cr Wet	CR116B/Wet-Bench 2 Chromium etch LSI Selectipur: MERCK 111547.2500 • Quick Dump Rinse <0.1μS • Spin drying Etch rate: 100 nm/min	Strip Cr
18	Cleaning RCA-2 $HCl/H_2O_2/H_2O$	CR112B / Wet-Bench 130 HCL (36%) Selectipur, BASF H_2O_2 (31%) VLSI, BASF $HCl:H_2O_2:H_2O$ = 1:1:5 vol% • add HCl to H_2O • add H_2O_2 when mixure at 70°C	

		• Temp.: 70-80°C • cleaning time 10-15min • Quick Dump Rinse <0.1μS • Spin drying	
19	Etching 50%HF user made	CR116B/Wet-Bench 2 HF (50%) VLSI: MERCK 100373.2500 • Quick Dump Rinse <0.1μS • Spin drying	SiN_x retraction
20	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
21	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
22	Dry Oxidation at 950°C of Si	CR112B/Furnace A2 Standby temp.: 700°C • Program: Dry950 • Temp.: 950°C • Gas: O_2	LOCOS 30 min
23	Etching of SiN (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	
24	Plasma etching Si -Adixen	CR125c/Adixen SE Cleaning before etching • Temp.:-100°C • SF_6 flow: 15sccm • O_2: 30 sccm • Valve: 100 % • ICP: 200 W • CCP: 20 W (20/80 msec, on/off) • SH: 200 mm	
25	Etching 50%HF user made	CR116B/Wet-Bench 2 HF (50%) VLSI: MERCK 100373.2500	remove SiO_2

		• Quick Dump Rinse <0.1μS • Spin drying	

B.5 Plasma etching scheme: Si nanoridge fabrication using SU-8

Nr.	Process	Process parameters	Comments
1	Substrate selection -Silicon <100> OSP	CR112B/Wafer Storage Cupboard Supplier: Orientation: <100> Diameter: 100mm ± mm Thickness: 550m ± 10 μm Polished: Single side polished (OSP) Resistivity: 5-10 Ωm Type: p	
2	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS • Spin drying	
3	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
4	LPCVD SiN_x -uniform thickness	CR125C/Tempress LPCVD G3 Program: SiRN01 • SiH_2Cl_2 flow: 77.5 sccm • NH_3 flow: 20 sccm • temperature: 820/850/870°C • pressure: 150 mTorr • N_2 low: 250 sccm • deposition rate: ± 4 nm/min • reflective index (n): 2.180	60 nm
5	Ellipsometer	CR118B/Plasmos Ellipsometer	

	Measurement		
6	Cleaning Piranha H_2SO_4/H_2O_2	CR112B/Wet-Bench 130 H_2SO_4 VLSI, BASF H_2O_2 VLSI, BASF H_2SO_4:H_2O_2=3:1 add H_2O_2 slowly into H_2SO_4 stirrer on, heater on • Temp.: 100°C • Time: 10-15 min • Quick Dump Rinse <0.1μS • Spin drying	
7	Lithography-Coating SU-8 2000.5 (Delta 20)	CR112B/Suss Micro Tech Spinner (Delta 20) Microchem NANO SU-8 2000.5 • Program: 3000 rpm	
8	Lithography-Soft bake SU-8 2000.5	CR112B or CR117B/Hotplate • Hotplate starts at 25°C • Ramp up to 65°C: 1 min • Ramp up to 95°C: 2 min • Ramp down to 25°C	
9	Lithography Alignment & Exposure SU-8 2000.5 (EV)	CR117B/EV620 Electronic Vision Group 20 Mask Aligner • Hg lamp: 12 mW/cm^2 • Use UV filter • Exposure Time: 20 sec • Hard contact	
10	Lithography -PEB SU-8 2000.5	CR112B or CR117B/Hotplate • Hotplate starts at 25°C • Ramp up to 65°C: 1 min • Ramp up to 95°C: 2 min • Ramp down to 25°C	
11	Lithography Development SU-8 2000.5	CR112B/Wet-Bench 9 TCO Spray Developer Developer: PGMEA (RER 600 , ARCH Chemicals) • Time: 1 min immersion in PGMEA • Time: 1 min immersion in IPA • Spin drying	
12	Lithography -hard bake SU-8	CR112B/Hotplate 120°C • Time: 2 h	
13	Plasma etching SU-8 -Tepla 300E	CR102A / Tepla 300E Barrel Etcher (2.45 GHz) Multipurpose system • O_2 flow: 200 sccm	loading- dependent 5-wafers per run

		• Power: 300 W • Pressure: 1.2 mbar • Time: 5 min	
14	Plasma etching SiN_x -Eske	CR102A/Elektrotech PF310/340 Clean chamber Aluminium electrode, quarts substrate • Electrode temp.:10°C • CHF_3 flow: 25sccm • O_2: 5 sccm • pressure: 10 mTorr • power: 75 W	
15	Plasma etching Si -Adixen	CR125c/Adixen SE Cleaning before etching • Temp.:-100°C • SF_6 flow: 15sccm • O_2: 30 sccm • Valve: 100 % • ICP: 200 W • CCP: 20 W (20/80 msec, on/off) • SH: 200 mm	
16	Strip SU-8 Piranha H_2SO_4/H_2O_2	CR112B/Wet-Bench 130 H_2SO_4 VLSI, BASF H_2O_2 VLSI, BASF H_2SO_4:H_2O_2=3:1 add H_2O_2 slowly into H_2SO_4 stirrer on, heater on • Temp.: 100°C • Time: 10-15 min • Quick Dump Rinse <0.1μS • Spin drying	
17	Etching 50%HF user made	CR116B/Wet-Bench 2 HF (50%) VLSI: MERCK 100373.2500 • Quick Dump Rinse <0.1μS • Spin drying	SiN_x retraction
18	Cleaning Standard	CR112B/Wet-Bench 131 HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK • Beaker 1: fumic HNO_3 (100%), 5min • Beaker 2: fumic HNO_3 (100%), 5min • Quick Dump Rinse <0.1μS • Beaker 3: boiling (95°C) HNO_3 (69%), 10min • Quick Dump Rinse <0.1μS	

		• Spin drying	
19	Etching HF (1%) Native Oxide	CR112B/Wet-Bench 3-3 HF (1%) VLSI: MERCK 112629.500 • Etch time: 1 min • Quick Dump Rinse <0.1μS • Spin drying	
20	Dry Oxidation at 950°C of Si	CR112B/Furnace A2 Standby temp.: 700°C • Program: Dry950 • Temp.: 950°C • Gas: O_2	LOCOS 30 min
21	Etching of SiN (Hot H_3PO_4)	CR112B/Wet-Bench 3-1 H_3PO_4 (100%) Merck VLSI 1.00568.2500 • Temp.: 180°C (caution!) • Quick Dump Rinse <0.1μS • Spin drying	
22	Plasma etching Si -Adixen	CR125c/Adixen SE Cleaning before etching • Temp.:-100°C • SF_6 flow: 15sccm • O_2: 30 sccm • Valve: 100 % • ICP: 200 W • CCP: 20 W (20/80 msec, on/off) • SH: 200 mm	
23	Etching 50%HF user made	CR116B/Wet-Bench 2 HF (50%) VLSI: MERCK 100373.2500 • Quick Dump Rinse <0.1μS • Spin drying	remove SiO_2

Summary

The aim of the project was to create high resolution stamps for thermal nanoimprint applications. The creation of nanoridges with sub-100 nm resolutions was explored by means of edge lithography via top-down routes, i.e. in combination with micromachining technology. Edge lithography is an add-on technology which allows to use any lithographic techniques for primary pattern definition.

The project started from the fabrication of SiO_2 nanoridges by oxidizing vertical Si edges using SiN_x as the mask. Vertical Si sidewalls were created taking advantage of Si <110> wafers and anisotropic Si etching by OPD4262. SiO_2 nanoridges with sub-20 nm width were fabricated. In Chapter 2, we have presented the idea of reinforcing the SiO_2 nanoridges by an additional SiN_x deposition to make the stamps reusable in T-NIL; however, the over-deposition led to the loss of sub-20 nm resolution.

The fabrication of monocrystalline Si nanoridges by advanced edge lithography is demonstrated in Chapter 3. The width of Si nanoridges was co-determined by Si anisotropic etching, lateral retraction of SiN_x and LOCOS. We have demonstrated the capability of fabricating Si nanoridges with a width down to 10 nm by the advanced edge lithography. In Chapter 4, the fabrication of multi-Si nanoridges has been explored and triple Si nanoridges of 120 nm high and 40 nm wide with ca. 40 nm spacing have been created by a repeated advanced edge lithography scheme. In this case, OPD 4262 was replaced by 20% KOH used at room temperature and selective etching of SiN_x and SiO_2 was alternately performed using 50% HF and hot H_3PO_4.

In Chapter 5, the fabrication of nanoridges was extended to arbitrary contours using dry plasma etching methods to avoid the dependence of Si crystal orientation. A cryogenic Si etching recipe was developed according to black silicon method. Two fabrication schemes have been demonstrated capable of producing nanoridges with circular contours with a width down to 60 nm. In the scheme where photoresist and Cr function as the masking layers, Si nanoridges with perfect vertical sidewall profile but rough sidewall

surface finish have been produced. Although Si nanoridges with slightly positive tapered sidewalls are fabricated in the SU-8 scheme, the sidewall surface finish is smooth which is beneficial for nanoimprint applications.

We demonstrated the successful implementation of the monolithic Si nanoridges to alternative nanofabrication approaches in Chapter 6. Assemblies of light harvesting antenna complexes with a resolution of 80 nm have been created by thermal nanoimprint lithography and self-assembly techniques. Composite PDMS-glass stamps with high resolution line structures have been fabricated by both thermal nanoimprint lithography and capillary force lithography. By using the high resolution composite PDMS-glass stamp, we have demonstrated the fabrication of Au nanolines with a width of ca. 80 nm by microcontact printing.

Samenvatting

Het doel van het project is het maken van hoge-resolutie-stempels voor toepassingen die gebruik maken van de thermische nano-imprinttechnologie. Het maken van nano-richels met een resolutie kleiner dan 100 nm is onderzocht. Deze nano-richels zijn als een miniatuur-bergkam met aan beide zijden een klif. Voor het maken van de nano-richels is gebruik gemaakt van 'edge'-lithografie via top-down-routes gebaseerd op microsysteem-technologie. 'Edge'-lithografie maakt het mogelijk om structuren te maken die veel kleiner zijn dan de afbeelding die verkregen kan worden met een simpel lithografie-proces.

Het project is begonnen met de fabricage van nano-richels van SiO_2 door het oxideren van de verticale zijwanden van Si met SiN_x als masker. Verticale Si-zijwanden werden verkregen door op Si <110>-wafers een anisotrope etsstap toe te passen met OPD 4262. Nano-richels van SiO_2 met een breedte kleiner dan 20 nm zijn hiermee verkregen. In hoofdstuk 2 wordt een idee gepresenteerd om de SiO_2-nano-richels te verstevigen door een extra laag SiN_x erop te deponeren zodat de stempels meerdere malen gebruikt kunnen worden. Een nadeel hiervan is dat de richel breder wordt en de resolutie dus achteruit gaat.

De fabricage van monokristallijn Si-nano-richels door geavanceerde 'edge'-lithografie is getoond in hoofdstuk 3. De breedte van de Si-nano-richels wordt hierbij mede bepaald door de anisotrope etsstap van Si, de laterale terugtrekking van SiN_x en het LOCOS-proces. We hebben aangetoond dat het mogelijkheid is om op deze manier Si-nano-richels te maken met een breedte van 10 nm.

In hoofdstuk 4 is de fabricage van meervoudige Si-nano-richels onderzocht. Drievoudige Si-nano-richels van 120 nm hoog en 40 nm breed met een tussenruimte van ongeveer 40 nm zijn verkregen door een herhaald toepassen van de geavanceerde 'edge'-lithografie-techniek. In dit geval is er, i.p.v. OPD 4262, gebruik gemaakt van KOH om Si op kamertemperatuur te etsen. SiN_x is geëtst met 50% HF in het geval dat SiO_2 tevens verwijderd mag worden, anders wordt H_3PO_4 gebruikt voor een betere selectiviteit. Deze

etsstappen worden meerdere malen afgewisseld.

In hoofdstuk 5 is de fabricage van nano-richels uitgebreid naar willekeurige contouren door gebruik te maken van droog plasma-etsen om de afhankelijkheid van de Si-kristal-orintatie te vermijden. Een cryogeen etsrecept voor Si is ontwikkeld volgens de 'black silicon method'. Twee fabricageschema's zijn ontwikkeld die het mogelijk maken om nano-richels met ronde contouren te maken met een breedte tot minimaal 60 nm. In het geval dat fotoresist en Cr als maskerlaag worden gebruikt, kunnen Si-nano-richels met perfect verticale zijwanden worden gemaakt, maar de oppervlakteafwerking is ruw. Hoewel de Si-nano-richels die gemaakt worden met SU-8 als masker, licht taps toelopen, is de oppervlakteafwerking van de zijwand glad hetgeen bevorderlijk is voor nano-imprinttoepassingen.

We hebben het succesvol implementeren van de monolitische Si nano-richels in alternatieve nanofabricage-benaderingen aangetoond in hoofdstuk 6. Assemblages van 'light harvesting'-antennacomplexen met een resolutie van 80 nm zijn gemaakt d.m.v. thermische nano-imprintlithografie en zelfassemblage-technieken. Samengestelde PDMS-glas-stempels met hoge-resolutie lijnstructuren zijn gefabriceerd zowel m.b.v thermische nano-imprintlithografie als ook capillaire-krachtlithografie. Door gebruik te maken van de hoge-resolutie PDMS-glas-stempels, hebben we laten zien dat het mogelijk is om gouden nanolijnen te maken met een breedte van ongeveer 80 nm door middel van microcontact-druk.

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Yiping Zhao
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About the author

Yiping Zhao was was born on February 1^{st}, 1982 in Beijing, China. After graduation from the Experimental High School attached to Beijing Normal University in the year 2000, she went to study Guidance and Control in the Mechatronics Department of Beijing Institute of Technology. She obtained her bachelor degree in June 2004. From September 2004 to May 2006, she did her master study of Mechatronics in the University of Twente, The Netherlands. She finished her master project, named ″Design, fabrication and testing of a pressure wave generator used in a regenerator-based microcryocooler″, in the Transducers Science and Technology group(better known as MicMec). From May 2006, she started her PHD project under the supervision of Dr. H. V. Jansen, Dr. N. R. Tas and Prof. M. C. Elwenspoek from the Transducers Science and Technology group and Prof. J. Huskens from the Molecular Nanofabrication group. The results obtained from her PhD project are described in this thesis.

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