High-Speed Data Processing Module for LLRF

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***Abstract*—Linear accelerators, like the Free-electron LASer in Hamburg (FLASH) or the European X-Ray Free Electron Laser (E-XFEL) take advantage of the digital Low Level Radio Frequency (LLRF) system to control the phase and amplitude of an electromagnetic field inside superconducting cavities. The real-time control LLRF system, processing data within a few microseconds, has to fulfil performance requirements and provide comprehensive monitoring and diagnostics. The AMC-based controller (DAMC-TCK7) board was developed as a general purpose high-performance low-latency data processing unit designed according to the PICMG MTCA.4 spec. The module provides the processing power, data memory, communication links, reference clock, trigger and interlock signals that are required in modern LLRF control systems. The module was originally designed as a cavity field stabilizing controller for standing-wave linear accelerators. However, the application of the board is much wider because it is a general purpose data processing module suitable for systems requiring low latency and high-speed digital signal processing. According to authors' knowledge this is the first MTCA.4 module offering 12.5 Gbps links, unified Zone 3 connectivity and advanced Module Management Controller proposed by DESY. The DAMC-TCK7 card was used as a hardware template for the development of the other AMC modules of the XFEL accelerator's LLRF system. This paper discusses the requirements for the digital real-time data processing module, presents the laboratory performance evaluation and verification in Cryo-Module Test Bench (CMTB) at DESY.**

***Index Terms*—Low Level Radio Frequency Control System, Linear Accelerator, Data Processing module, Micro Telecommunications Computing Architecture, MicroTCA Enhancements for Rear I/O and Precision Timing, High-Energy Physics, Zone 3 connector classes**

I. Introduction

THE European X-ray Free Electron Laser (XFEL) is the 4^{th} generation synchrotron light source capable of producing high-intensity ultra-short wavelength X-ray laser light [1], [2]. The machine produces X-ray flashes in the wavelength range from 0.05 to 4 nm that are shorter than 100 fs (rms). The laser is composed of an injector, accelerating section with the final electron energy of 17.5 GeV and undulators producing laser light. The layout of the accelerator is presented in Figure 1. The linear accelerator of the European XFEL is composed of 800 super-conducting cavities operating at 1.3 GHz [3]. The accelerating section, consisting of 100 cryo-modules, is controlled by 25 RF (Radio Frequency) sections (A1–A25 as presented in Figure 1).

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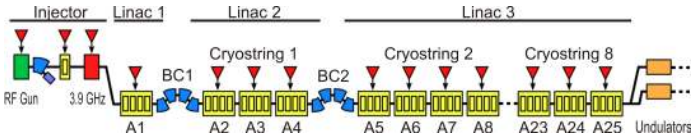

Fig. 1. The layout of the European XFEL accelerator

The injector section is composed of a normal conducting RF gun and two cryo-modules: one working with 1.3 GHz and the other with 3.9 GHz (third-harmonic). The main accelerating section consists of three Linacs (L1, L2, L3) and two Bunch Compressors (BC1, BC2). A single RF station, powered from a 10 MW klystron, supplies 32 superconducting TESLA cavities, grouped in 4 cryomodules [4], [5].

A powerful Low Level Radio Frequency (LLRF) control system is required to obtain a high quality electron beam and laser light [6]–[9]. The system has to control the phase and amplitude of the electromagnetic field inside the superconducting cavities of the linear accelerator with the accuracy of the order of 0.01% for the amplitude and up to 0.01° in the phase at 1.3 GHz [8], [10].

A digital control system, designed with the application of the state-of-the-art technology, is essential to obtain such a challenging stability of phase and amplitude parameters. The key element of the system is a low-latency digital data processing module with fast feedback and adaptive feed-forward algorithms [11].

Since, the LLRF system is being built using the Micro-Telecommunications Computing Architecture (MTCA) standard, the data processing module was designed as an Advanced Mezzanine Card (AMC) that is compliant with the MTCA.4 specification [12]–[14].

The paper has the following structure: Section II presents the LLRF control system of the XFEL accelerator implemented using MTCA.4. Section III describes the design of the data processing module. The performance evaluation and the first results from the Cryo-Module Test Bench (CMTB) facility tests are discussed in the section IV.

II. LLRF System of the Linear Accelerator

The LLRF system measures probe signals in accelerating cavities, digitises them and sends to the data processing module. This module executes the feedback algorithm and generates a signal which is then sent to the Vector Modulator (VM). The upconverted signal drives the klystron and closes the feedback loop. The LLRF feedback loop should be processed within 2 µs to ensure the correct operation of the feed-forward field control algorithm.

Hardware of the LLRF control system is usually built in the form of electronic modules housed in a chassis. Various form-factors and standards can be used to implement the LLRF system electronics [15]–[21].

A. LLRF Control System Implemented in MTCA.4

A single RF station of the XFEL LLRF is designed as a semi-distributed system composed of two MTCA.4 chassis controlling 32 cavities. A detailed description of the system can be found in [4]. In such a configuration, a single RF system requires two data processing modules that are installed in two MTCA.4 chassis (Master and Slave systems). A Slave system collects data from the first 16 cavities. The calculated partial vector sum is sent to the Master system via a low latency, Peer-to-Peer (P2P), optical fibre link. The Master system calculates the final vector sum, executes control algorithms, and finally, transfers the data to the Vector Modulator which performs the required phase and amplitude correction [22], [23].

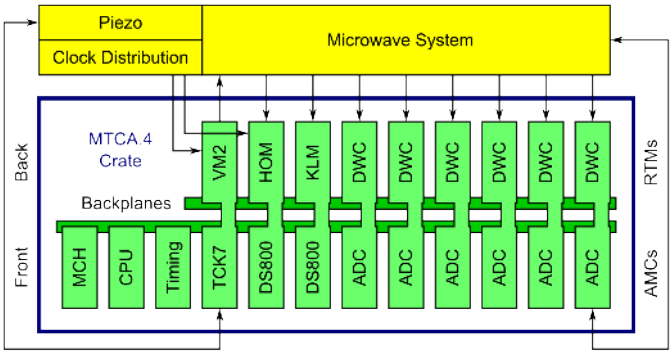

Fig. 2. A block diagram of the Master chassis of LLRF System

The structure of the Master MTCA.4 chassis is presented in Figure 2 [4], [24], [25].

All modules are controlled by the Central Processing Unit (CPU) installed in the chassis. It communicates with AMC modules using the PCIe and the switch provided by the MicroTCA Carrier Hub (MCH) [14]. Slots 3 and 4 have direct connections to slots 5–12. The controller module (DAMC-TCK7), located in the slot 3, processes the data from digitizer cards (ADC, DS800 in slots 5–12) delivered via the backplane connectivity and generates the output signal to the Vector Modulator. The VM module is implemented as an RTM module connected via the Zone 3 to the TCK7 to reduce the latency. Auxiliary systems, e.g. a slave crate, n-1 and n+1 station, piezo controller, are connected through SFP+ (Small Form-factor Pluggable) optical fibre connections.

A low-latency connectivity is required for the communication between the data acquisition modules (ADC), data processing unit (DAMC-TCK7 or TCK7) and the VM. The latency of P2P communication channels between the system components should be in range of 150 ns [26], [27].

The MTCA.4 specification defines Enhancements for the Rear I/O and Precision Timing [13], [28], [29]. The MLVDS multi-drop bus, realized on backplane channels 17–20, is used for the trigger, interlock, synchronous reset and LLRF alarm signals. The PCIe clock (100 MHz) is distributed using a FCLK star connection. The low-jitter LLRF clock (1.3 GHz or 81.25 MHz) is distributed using an RF backplane assembled on the rear side of the chassis [30]–[32].

III. Data Processing Module

The data processing module (DAMC-TCK7) of the LLRF system should provide resources for the feedback control and diagnostic algorithms. The module is the main controller of the LLRF system. It receives data from the RF station modules using high-speed serial interfaces, performs MIMO control algorithms, Learning Feed Forward (LFF) and Beam Loading Compensation (BLC) calculations. Details concerning the control algorithms can be found in [33], [34].

The data processing module was designed as an AMC blade. The assembled card with an attached Vector Modulator is presented in Figure 3.

The DAMC-TCK7 module has to provide data processing resources, data communication interfaces, synchronisation and interlock signals. For this purpose, a dedicated FPGA-based computation blade with high-throughput memories, dozens of high-speed low-latency links and an interlock controller were developed.

A. Requirements for the Controller Module

The processing module should be able to support high-performance complex number computations. The worst case computation time should not exceed 1 µs to assure a stable regulation. The IQ detection (ca. 300 ns) and data transmission (ca. 600 ns) consume almost 1 µs.

It was estimated that the current feedback and diagnostic algorithms require an FPGA device with at least 900 DSP slices. The computations and diagnostic data storage need an access to an external memory of the capacity not less than 256 MB and a throughput not lower than 50 Gbps. The non-volatile memories should allow the booting of the FPGA using one of two firmware versions. The system should support an on-line upgrade of the firmware, preferably using the PCIe link.

The user communication link to the FPGA should provide the min. 16 Gbps (PCIe x4 gen. 2) and min. 1 Gbps Ethernet. Data transmission with other components of the LLRF system is implemented using P2P connections and a low latency (ca. 200 ns) proprietary protocol. The transmission of control (e.g. vector sum, IQ data) and diagnostic (e.g. virtual probes) data requires at least 5 Gbps of the data throughput. Eight P2P links should be provided to the backplane (six digitizer modules, HOM and KLM), further eight to the SFP+ transceiver's on the front panel (connections to other LLRF stations) and min. 2 links to the Zone 3 connector (Vector Modulator), see Figure 2. In addition, the module should allow the communication on ports 2 and 3 for the multi-controller operation.

To support the variety of communication links, the module has to contain several low-jitter clock generators, that can be set to specified frequencies in range of 50–325 MHz. To synchronize the board with the LLRF system, it is also required to receive and distribute several dedicated clocks from VM via the Zone 3 connector.

Fig. 3. The photograph of the DAMC-TCK7 data processing module (on the left) connected with a Vector Modulator (on the right)

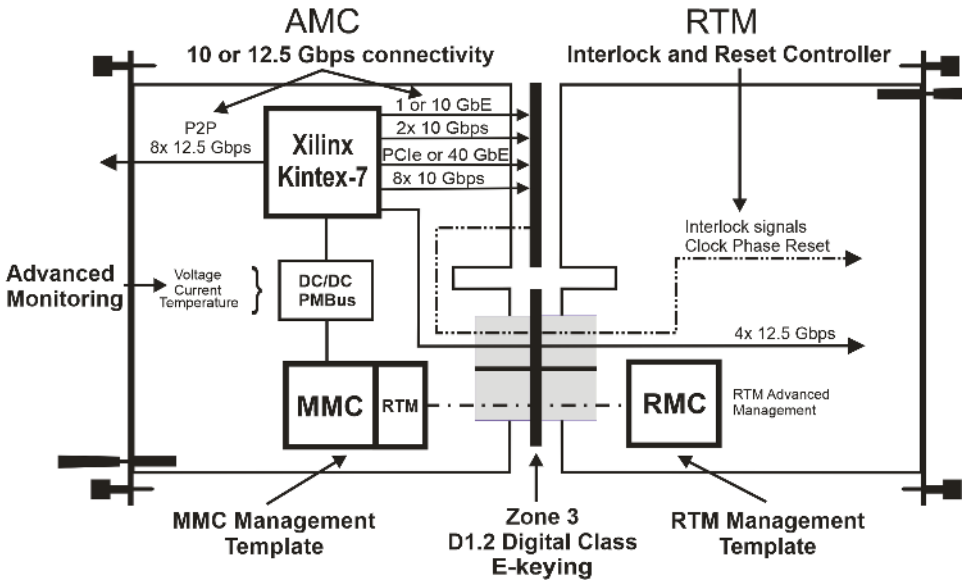

Fig. 4. The novel ideas introduced during the TCK7 development

B. Data Processing Module - Implementation

The design should also deliver additional resources for the further development of algorithms and diagnostics. A number of dedicated hardware solutions was provided to fulfil the requirements of the XFEL LLRF system. The novel ideas applied during the design of the DAMC-TCK7 are collected and depicted in Figure 4. The following subsystems of the TCK7 module became adopted as DESY standards:

- MMC and RTM management.
- Interlock and clock phase reset controller.
- Zone 3 connector signals (D1.2 class).
- E-keying for Zone 3 connector.
- PMBus-based power supply.

These solutions are currently used at DESY as templates of circuits for the development of new AMC and RTM modules [35]. The templates are also widely used by research institutions and industry partners providing MTCA.4 hardware. Signal classes created for the Zone 3 interconnections are currently under the PCI Industrial Computer Manufacturers Group (PICMG) standardisation [36]. The presented solutions are further discussed in the following sections.

C. Mechanical and Thermal Aspects

The double-width mid-size AMC module board, together with Rear Transition Module (RTM), can consume up to 80 W. The DAMC-TCK7 module should provide 30 W of power supply for the VM. In this case, the module can consume up to 50 W. The limited AMC power is the important factor for selecting the FPGA device.

D. Data Processing Power

The data processing power is provided by the Xilinx Kintex-7 FPGA device. The application of the Kintex FPGA allows designing a cost-effective and still powerful controller. Two versions of the FPGA are supported: XC7K355T (55650 slices, 1440 DSP slices and 25740 kb of block RAM) XC7K420T (65150 slices, 1680 DSP slices and 30060 kb of block RAM). Both versions of the FPGA devices fulfil

the basic requirements for digital resources and provide spare logic for further development.

The module provides 4 GB of the DDR3 SDRAM. The memory has a 64-bit wide data bus offering a 68 Gbps throughput and also fulfils the requirements.

E. High-Speed Connectivity

The FPGA device should communicate with other devices using a high-speed low-latency P2P connections provided by the FPGA serial transceivers. The applied Kintex-7 FPGA allows transferring data with a maximum throughput up to 12.5 Gbps (speed grade -3). The measured latency for the 6.25 Gbps P2P connection for the 125 MHz reference clock is equal to 105 ns. The performance of GTX transceivers exceeds the LLRF requirements. The Xilinx chip provides a hardware IP block for the PCIe gen. 2 with a further possibility to upgrade to the PCIe gen. 3 via a software solution. The TCK7 board supports 1 or 10 Gb Ethernet connection on channels 0 and 1 (the 10 Gb Ethernet is currently under the PICMG standardisation).

F. Module Management Controller

The Module Management Controller is an important subsystem required by the MTCA specification. The MMC communicates with the MTCA Carrier Manager and is responsible for the activation and deactivation of the module, power supply control and monitoring of operating parameters. It is also responsible for the E-keying process for backplane interfaces [37]. In the MTCA.4 systems, the MMC also manages the RTM module. It represents the RTM as an additional Field Replaceable Unit (FRU) of the system, controls it operation and monitors all sensors.

The MMC on the DAMC-TCK7 board is based on the ATxmega128A1 microcontroller. It implements all functionality necessary to meet the requirements of the MTCA.4 standard. The microcontroller is connected to the IPMB-L bus, and it implements all IPMI commands necessary for the communication with the supervising system. It controls all DC/DC converters that provide the power supply for the FPGA and other payload components of the board. It is also responsible for temperature and voltage monitoring. The temperatures are measured in 4 locations on the PCB and also directly on the FPGA circuit die. The power supply voltages are monitored with built-in ADCs while the current consumption is measured via PMBus sensors. The MMC allows controlling the FPGA (payload reset, firmware reload, check status of booting, select active PROM) using custom IPMI commands. The block diagram of the MMC is depicted in Figure 5.

The mentioned ATxmega microcontroller manages the RTM module that can be connected to the board. The device controls the inrush current of the RTM, monitors the voltage and current on both management and payload power. The controller also provides the management of the FPGA present on the VM (RTM).

The MMC controller of TCK7 is also responsible for the E-keying of analogue (A.xx) and digital (D.xx) classes of the

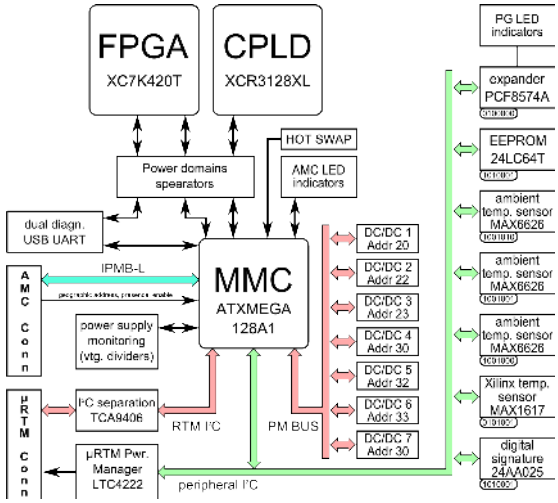

Fig. 5. A block diagram of the MMC

Zone 3 connector. The MTCA.4 defines a hardware keying that depends only on voltage levels. However, the improper Zone 3 connection between the analogue and digital class signals (e.g. AMC-digital, RTM-analogue) or a collision of two outputs could damage the hardware. The E-keying routine reads the class identifier from AMC and RTM FRUs and verify if the boards are compatible. If not, the MMC will stop the further activation of the RTM and will not enable the Payload Power for it.

The MMC device supports the firmware upgrade of the ATxmega microcontroller and the FPGA using the HPM.1 protocol.

The firmware for the MMC of DAMC-TCK7 module was written at Lodz University of Technology. More information concerning the MMC code could be found in [37]–[39]. The MMC was verified to operate properly with NAT and VadaTech MCHs.

G. Zone 3 Connectivity

The Zone 3 connector provides low-latency links to the RTM (Vector Modulator), general purpose differential signalling parallel bus, output signals (interlocks), reference clock I/Os and several more signals required by the MTCA.4 specification.

The DAMC-TCK7 connects with the RTM module using two 30-pair ADF connectors J30/J31. To improve the compatibility and modularity of the AMC and RTM boards, DESY developed a classification recommendation for the Zone 3 connector pin assignment for the MTCA.4 standard for different classes of applications (analogue and digital) [36]. This implies a zone description, electrical specification, electrical protection sequence, electronic keying, grounding and shielding options.

The Zone 3 connectivity of DAMC-TCK modules was used to define the DESY D1.2 Digital Class. The D1.2 class defines 4 high-speed links, 36 digital I/Os, 3 output signals and 4 reference clocks [36].

H. Interlocks Signals

The interlock controller is another important circuit of the TCK7 module. Expensive hardware of an accelerator (e.g. klystron) could be damaged in the case of a failure of this circuit. Therefore, the device was designed using non-programmable, discrete logic. The device, composed of two identical channels, provides redundant interlocks used to control the RF gate switches of the Vector Modulator (RF Gate 0 and RF Gate 1). The RF Gate switch is closed (RF present) when all interlock signals (FPGA interlock, backplane interlocks 0 and 1) are de-asserted. The RF Gate is open when at least one of the signals is asserted. The interlock 0 (channel Tx 19) and interlock 1 (channel Rx 20) signals present on the backplane are connected to the interlock controller.

The interlock signals on the Zone 3 are asserted with high LVDS levels. The LVDS receiver on the DRTM-VM2 module is operating in a fail-safe mode. When there is no signal from the AMC driver, the output of the LVDS receiver is asserted and the RF Gate is open.

The interlocks use fixed direction Out 0 and Out 1 signals according to the D1.2 digital class [36]. The fixed direction signals simplify the implementation and increase the reliability of the interlock subsystem, as the signal flow direction cannot change during the operation of the system.

The developed and tested interlock circuit was standardised at DESY and it is currently used as a template for new designs.

I. Firmware Upgrade Support

The reprogramming of FPGA devices without using the JTAG programmer connected directly to the module is a desirable feature in control systems of complex machines. The TCK7 module supports an upgrade of the FPGA firmware via the PCIe. The module is equipped with two non-volatile SPI PROMs that may be accessed by the FPGA (reading and writing). They are used for storing the FPGA firmware bitstreams. Memories may be reprogrammed by the FPGA using the PCIe and then used for the FPGA booting. Selection of an active memory and FPGA reconfiguration is controlled by the MMC using custom IPMI commands. The completion status of the programming can be monitored via the MMC. The firmware upgrade is executed by the dedicated software that controls all necessary components and implements a complete algorithm of the procedure. The firmware upgrade controller also allows updating the FPGA firmware on the RTM. More details about the applied firmware upgrade procedure may be found in [38]. The main FPGA can be reprogrammed via the MMC (HPM.1) when both PROMs are improperly programmed.

J. Power Supply Subsystem

The applied Kintex-7 FPGA can consume the current up to 25 A on 1 V supplying the core. The core voltage should not differ by more than 3 % (30 mV) and should have less than 10 mV voltage ripple. To meet these requirements, the power supply subsystem must be carefully designed. Despite that the power supply is provided via a wide power plane to the FPGA, the voltage on its pins could significantly drop when high a current is consumed. The Point of Load (PoL) voltage regulation was applied to compensate for voltage drop on the core power supply.

The power distribution system of the TCK7 module consists of seven DC/DC converters accompanied by several LDO voltage regulators to provide several various power supply voltages. All seven DC/DC converters are equipped with the PMBus interface. Such a solution allows reading the value of the converter's currents and voltages on both input and output terminals, monitoring the thermal conditions, and tuning the converter parameters.

The MMC sensors provide a convenient way to read not only voltages but also currents for power supplies (FPGA core, GTX and IO banks).

IV. Experimental Results

The DAMC-TCK7 module was initially tested in the laboratory. Firstly, all sub-modules were evaluated and measured using a test firmware loaded to the MMC. The board was supplied from an external power supply and fully activated. All voltages and currents including the RTM have been measured. Next, the SDRAM memory and high-speed SPF+ links were evaluated. The debugged module was programmed with the MMC firmware developed at Lodz University of Technology and tested with MTCA.4 chassis.

Finally, the FPGA was programmed with the LLRF firmware and the tests in the CMTB facility were performed [40]. Some of the TCK7 modules are currently installed in the FLASH accelerator tunnel at DESY.

A. Tests in MTCA.4 Shelves

The debugged module was programmed with the MMC firmware and tested in crates from three different vendors: Schroff, ELMA and VadaTech. The NAT-MCH-PHYS MCH, fabricated by NAT was used for Schroff and ELMA and UTC001 MCH was used for the VadaTech crate.

1) Module Management Controller: The DAMC-TCK7 module cooperating with the NAT MCH is properly activated (M4 state) within less than 1 s. The module is equipped with correct FRU and all sensors are accessible. Tests of the RTM support were done with the use of the Vector Modulator and RTM Eval-kit. Both boards were correctly activated and all sensors were successfully read. All observed sensors (voltages, currents, temperatures) indicated correct values. Similar tests were performed with the VadaTech UTC001 MCH.

2) High-speed Connectivity Tests: The tests cover all GTX links available on the MTCA.4 backplane: direct connections on ports 2 and 3 (SATA) and ports 8–15 (low latency links). The topology of the LLRF backplane is presented in Figure 6.

The Bit Error Rate (BER) was evaluated using the Xilinx IBERT analyser. The tests were executed for three data throughputs: 6.25, 10 and 12.5 Gbps (the maximum throughput of the Kintex-7 devices). A PRBS-31 pattern and default setting of transceivers were used during the measurements. The registered BER for all three chassis is presented in Table I.

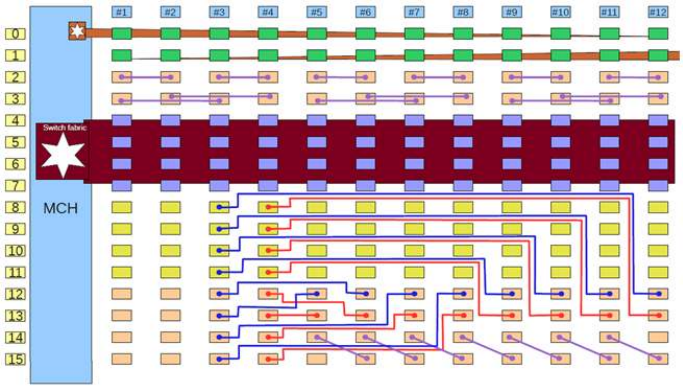

Fig. 6. The topology of the LLRF backplane

TABLE I
BIT ERROR RATE MEASURED FOR BACKPLANE LINKS

MTCA Port	Gbps	Schroff	ELMA	VadaTech
2–3	6.25	$<10^{-15} \cdot bit^{-1}$	$<10^{-15} \cdot bit^{-1}$	–
	10.0	no link	no link	–
	12.5	no link	no link	–
7–15	6.25	$<10^{-15} \cdot bit^{-1}$	$<10^{-15} \cdot bit^{-1}$	$<10^{-15} \cdot bit^{-1}$
	10.0	$<10^{-15} \cdot bit^{-1}$	$<10^{-15} \cdot bit^{-1}$	$<10^{-15} \cdot bit^{-1}$
	12.5	$10^{-10} \cdot bit^{-1}$	$10^{-8} \cdot bit^{-1}$	–

The Schroff chassis was equipped with two DAMC-TCK7 modules installed in slots 3, 4 and with eight SIS8300L digitizer cards inserted into slots from 5 to 12. This is a typical LLRF configuration when digitizers send a vector sum to the data processing module. This setup helps detecting potential problems, like cross-talk and inter-symbol interferences during the transmission between various modules. The BER measured for 6.25 Gbps was better than $<10^{-15} \cdot bit^{-1}$. No errors were detected during the tests.

Two DAMC-TCK7 modules were installed in slots 3 and 4. Both cards were populated with 16 SFP+ AFBR-703SDZ modules manufactured by Avago (10 Gb, 850 nm SFP+ Transceiver). Various configurations of SFP+ connections proved an error-free transmission with the BER better than $10^{-15} \cdot bit^{-1}$. The tests with 12.5 Gbps were performed using SFP+ copper cables. The BER measured with 2-m-long cables was better than $10^{-15} \cdot bit^{-1}$.

The Zone 3 4-lane connectivity was verified with a simple loopback. The BER better than $10^{-15} \cdot bit^{-1}$ was measured. Next, the VM module was tested. The Zone 3 links on the VM have a direct connection to the Spartan 6 FPGA (2 lanes) and SFP+ cages (also 2 lanes). The SFP+ BER measured for 6.25, 10 and 12.5 Gbps was better than $10^{-15} \cdot bit^{-1}$. The Spartan 6 allows for the maximum transmission rate of 3.125 Gbps. No errors were detected during 1 hour tests of these links.

3) Tests of PCIe Links: The NAT MCH with the PCIe gen. 3 switch and the Concurrent AM 900/412-12 CPU (Intel Core-i7) were used for all tests with the PCIe. The tests were executed for Schroff and ELMA chassis. The PCIe links on ports 4–7 were tested with the native Xilinx PCIe x4, gen. 2 endpoint. The measured throughput for the read operation was equal to 12.8 Gbps (10 GB transfer, 100 block with 100 MB each). No errors were observed. The Kintex-7 does not offer the hardware PCIe gen. 3 endpoint. To test the gen. 3 link performance the PLDA XpressRICH3 the IP-core was used. The throughput measured during the read operation was 16.6 Gbps and 24.5 Gbps for the write operation. Again, no errors were observed.

4) DDR3 SDRAM Performance Evaluation: The SDRAM memory was tested with a reference clock frequency of 533 MHz. The Double Data Rate transmission with a 64-bit wide bus results in 64 Gb throughput. Test programs write the memory with various patterns, then read and verify the results. No errors were detected.

5) Power Supply and Thermal Tests: The DAMC-TCK7 module was tested with various programs loaded to the FPGA to evaluate the power consumption and heat dissipation. The tests were carried out with the Schroff 5U 42HP 7-slot MTCA.4 chassis and the NAT MCH.

The management power supply consumption for a not activated board is 51 mA. The activated board consumes 81 mA. Connecting the VM RTM card to the TCK7 module increases this figure further to 122 mA. The payload power consumption depends heavily on the algorithms loaded to the FPGA. The module uses 0.6 A when the FPGA is not configured and up to 3.5 A (42 W, all GTX links active, DDR3 and 90% of logic resources are used). A programmed VM consumes 2 A (24 W), therefore the total payload current amounts to 5.5 A (66 W).

The temperature measured on the PCB and in the FPGA during the power consumption tests was 40°C and 55°C respectively.

B. Tests in CMTB Facility

The Cryo-Module Test Bench (CMTB) facility at DESY is used for the evaluation of Superconducting RF (SRF) modules and cavities. In addition, the CMTB allows performing high and low power RF tests, in particular the LLRF system.

The setup for the LLRF evaluation was built using a single 12-slot ELMA chassis with the LLRF backplane, the NAT-MCH, the Concurrent CPU, a timing module, one DAMC-TCK7 with VM board, three SIS8300-L boards, three DWC10 RTMs and a piezo driver box PZM16.

Field detection is done with the SIS8300-L digitizer boards. The calculated vector sum and phases of signals are sent to the data processing DAMC-TCK7 module over the LLL available on the backplane. The DAMC-TCK7 is working as a main LLRF controller. The CMTB was able to work in a continuous wave (CW) or long pulse operation during the tests. Controller tables for the set point, feed forward and correction are 16 k samples long and are for 1 s of the operation time. The proportional controller was used during the tests. The controller works with the 9 MHz internal timing. A calculated driving signal is sent to the VM board over the Zone 3 low latency link. The DAMC-TCK7 additionally computes the detuning of the cavity. This information is sent via the front SFP optical link to the piezo box. It was possible to close two

feedbacks, one for driving the RF amplifiers and the second for piezo drivers, using signals from the SIS8300-L cards. Data from acquisition modules is stored in the DDR memory and is accessible over the PCIe using DMA transfers. The hardware setup was used for two-week-long tests. During that time the LLRF system was stable and no problems were observed.

V. Conclusions and Plans for Future

The DAMC-TCK7 module based on the Kintex-7 FPGA is a powerful and cost effective data processing module designed for the LLRF application. The module was intensively tested and performance of various components was evaluated. The module allows transmitting data with a maximum throughput of 12.5 Gbps and therefore fulfils the requirements of the LLRF system.

All the backplane links were carefully designed on the PCB. Therefore, the links on channels 0 and 1 (GbE) should also work with 10 Gbps. It gives the possibility to use the 10 Gb Ethernet that is currently under the PICMG standardisation. Similarly, the links on channels 4–7 (currently PCIe) can be used to implement the 40 Gb Ethernet. Therefore, the TCK7 is an attractive module, useful during the development of hardware supporting the 10 and 40 Gb Ethernet (MCH, MTCA.4 backplane).

Many circuits developed and tested on the TCK7 module were standardised at DESY and are currently used as templates for new AMC and RTM designs. The internal standardisation simplifies the design, decreases the development time as well as significantly improves the compatibility of all designed components. Some of the solutions introduced as a part of the TCK7 module were adopted by the PICMG and are now under standardisation.

Two versions of the FPGA (355T and 420T) provide enough resources for the implementation of complex LLRF control and diagnostic algorithms.

The module supports a dedicated low-jitter clock via the Zone 3 connector and interlocks, trigger and synchronization signals via MLVDS signals defined by the MTCA.4.

The module was tested with various MTCA.4 chassis and MCHs from NAT and VadaTech. The MMC firmware properly activated the card during all tests.

The DAMC-TCK7 has a sufficient thermal and power consumption margin even for complex algorithms, consuming many FPGA resources and GTX links. The VM module consumes a significant amount of power, which is close to the limit of 30 W.

Tests with digitizer modules and the initial usage in the CMTB facility proved that the design is well suited for accelerator applications.

A. Plans for future

The currently fabricated boards were successfully tested. The next step is the pre-production and then the final production of modules for the XFEL accelerator. More tests are required to evaluate a long-term operation, especially in corner cases (high ambient temperature, minimum and maximum power supply voltage).

Further testes are planned and the installation of the module in other test facilities at DESY: the AMTF, FLASH and finally in the XFEL accelerator.

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