High Speed Flash Memory and 1T-DRAM on Dopant Segregated Schottky Barrier (DSSB) FinFET SONOS Device for Multi-functional SoC Applications

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ABSTRACT

A novel dopant segregated Schottky barrier (DSSB) FinFET SONOS device is demonstrated in terms of multifunctioning in a high speed NAND-type Flash memory and capacitorless 1T-DRAM. In addition, a novel program mechanism that uses energy band engineered hot electrons (EBEHE) energized by sharp energy band bending at the edge of source/drain (S/D) is proposed for a high speed Flash memory programming operation. A short program time of 100ns and a low program voltage of 12V yield a V_{th} shift of 3.5V and a retention time exceeding 10years. For multifunctioning, the operation of a capacitorless 1T-DRAM is also demonstrated with a partially silicided DSSB in the same device.

INTRODUCTION

Ever since multifunctional devices with a high performance and embedded memories were proposed for SoC applications, such as SOONO and Unified-RAM on a single transistor **[1, 2]**, there have been expectations of a reduction in process complexity and chip cost. A primary goal in this work is to propose a novel multifunctioning device based on a DSSB FinFET SONOS device with a high speed NAND-type nonvolatile memory and capacitorless 1T-DRAM. **Fig. 1** shows the schematics of a DSSB FinFET SONOS device.

In general, the increasing density and program speed of NAND Flash memory have been challenging tasks because the diffusion-based S/D and Fowler-Nordeim (FN) tunneling needed for program obstructed aggressive scaling and fast program speed. We therefore demonstrate a fast program for Flash memory with superior short-channel immunity in the FinFET SONOS structure. As shown in **Fig. 2**, a hot carrier with high kinetic energy triggered by a sharp energy band at the S/D enhances the speed of the nonvolatile memory.

On the other hand, the SB-MOSFET has not been used for a capacitorless 1T-DRAM due to difficulty of hole accumulation at the floating body **[3]**. To benefit from the superiority of the SB-MOSFET in a capacitorless 1T-DRAM, we used a dopant segregation technique to develop a partial silicidation process at the S/D, which, as shown in **Fig. 3**, allows hole storage at the floating body.

DEVICE FABRICATION

The process sequence is summarized in **Fig. 4**. The process flow of the DSSB FinFET SONOS device is the same as that of our previous work **[2]** except for the gate spacers and the silicided S/D formation. Using a shallow implantation of arsenic (As) after formation of gate spacers, we effectively modulated the SB height by using the segregated dopants. During the formation of the gate spacers, the S/D regions are recessed so that they subsequently provide a uniform S/D along the fin depth (vertical direction). This task is challenging with only an S/D implantation and activation. Finally, the DSSB S/D was formed by means of nickel silicidation (NiSi) in a two-step RTP, which can minimize the lateral diffusion of NiSi. The SEM photograph in **Fig. 5(a)** shows a bird's-eye view of the fabricated DSSB FinFET SONOS device. **Fig. 5(b)**, **5(c)**, and **5(d)** are cross-sectional TEM images from various points of view of the DSSB FinFET SONOS device. The device has a gate length of 220nm and a fin that ranges in width from 30nm to 100nm. For the control group, we fabricated a conventional FinFET SONOS device with a diffused p-n junction was also fabricated.

RESULTS AND DISCUSSIONS

Fig. 6 shows the I_{ds}-V_{gs} characteristics of the DSSB FinFET SONOS device with a gate length (L_g) of 220nm and a fin width (W_{fin}) of 30nm. As shown in **Fig. 7**, a low parasitic resistance is achieved due to the metallic silicided S/D in the DSSB FinFET device. The DSSB FinFET with low parasitic resistance at the S/D is therefore expected to be a promising candidate for a high performance device, especially with a short gate length. Moreover, as shown in **Fig. 8**, even though the thickness of gate oxide is thick due to the O/N/O triple-layered structure, the short-channel effects are effectively suppressed in the DSSB FinFET device.

A. Nonvolatile memory characteristics

Fig. 9 shows the novel EBEHE program and the typical FN erase characteristics of the DSSB FinFET SONOS device. Excellent program efficiency is achieved. The V_{th} shift of 4.5V and 3.5V was achieved with 1μs/12V and 100ns/12V for program, respectively. And 100μsec/-14V was used for erase. The difference in the V_{th} shift between the DSSB FinFET

SONOS device and the conventional one for programming is approximately 2.5V at a program time of 100ns. This result is attributed to the hot carrier injection triggered by the sharp band bending at the DSSB S/D junction edge, which results in a larger V_{th} shift than in the conventional FinFET SONOS device with the same program voltage. In contrast, there is no significant difference in the erase characteristics between the DSSB FinFET SONOS device and the conventional one because of the same FN erase operation. However, unimproved erase characteristics can be circumvented by BE-SONOS technology **[4]**. As shown in **Fig. 10**, a parallel shift among programmed states was found in the DSSB device but not in the conventional device. This difference implies that the two-sided charge injection at the S/D prevails in the DSSB FinFET SONOS device. Note on the other hand that an unwanted non-uniform charge injection by FN tunneling occurs in the conventional FinFET SONOS device, resulting in an oblique shift and degradation of the slope. **Fig. 11** shows the V_{th} distribution of both the program/erase (P/E). The large V_{th} window of almost 5V is attractive for multilevel cell applications with a short programming time. **Fig. 12** shows a novel divided bit-line (BL) NAND array architecture that was designed for the implementation of the EBEHE program. The selected cell is programmed by simultaneously applying the ground bias for the top BL and the bottom BL. The word-line (WL) disturbance window, as shown in **Fig. 13,** is determined by a disturbed V_{th} of 1.5V in unselected cells. This reference value means that unselected cells can tolerate more than 100 times of program operation (t_{PGM}=1μs). A positive BL voltage is used in unselected cells because it can reduce the hot electron generation due to the reduced electric field at the edge of the S/D. Thus, the increased BL voltage in the unselected cells can enlarge the WL disturbance window. **Fig. 14** shows data retention results after the 1k P/E cycling and endurance behavior. For a program time of 100ns, we found that, in comparison with the conventional FinFET SONOS device, the DSSB FinFET SONOS device had a more rapid degradation of the retention characteristics as a result of the charge loss; this output can be attributed to the fact that the hot carriers degrade tunneling oxide quality. Nevertheless, we can extrapolate the V_{th} window to be 2V after 10 years because of the high efficiency programming. The V_{th} window is estimated to be 4V after 10^7 P/E cycles for a program time of 1μs and an erase time of 100μsec. These values ensure sufficient reliability.

B. Capacitorless 1T-DRAM characteristics

In **Fig. 15**, as evidence of hole accumulation, the kink effect is only observed in the DSSB FinFET SONOS device with a partially silicided S/D. A partially silicided S/D can be easily achieved by adjusting the deposited metal thickness during the silicidation process. The program, erase, and read conditions for the 1T-DRAM operation are summarized in **Fig. 16**. **Fig. 17** shows the P/E characteristics set by the P/E voltages for 50ns and 100ns, respectively. The P/E states are clearly distinguished in the DSSB FinFET SONOS device with the partially silicided S/D, whereas the P/E states for the fully silicided S/D are not clearly distinctive. The reason for this difference is that the accumulated hole can easily leak out to the fully silicided S/D. One of the advantages of a capacitorless 1T-DRAM is that excess holes are retained in the floating body during the P/E states. Consequently, a nondestructive readout is feasible and saves the refresh process, which can be required in a conventional DRAM (1T/1C structure). **Fig. 18** shows a 70ms nondestructive readout of the fabricated DSSB FinFET SONOS device. **Fig. 19** shows the schematics of the capacitorless 1T-DRAM cell array. Note that the cell architecture of the capacitorless 1T-DRAM is exactly the same as that of NOR-type Flash memory. This sameness shows the feasibility of multifunctions such as Flash memory and DRAM operations, without the risk of changing the cell architecture. This multifunctioning device can therefore be extended to embedded memory and a hybrid CMOS through integration with a FinFET, Flash memory, and DRAM, where the integration is based on the DSSB structure of SoC applications. Moreover, DC stresses were applied to evaluate how the V_{th} stability depends on the writing time, especially because the use of impact ionization can degrade device reliability. The extrapolation results in **Fig. 20** show that the V_{th} shift is smaller than 0.1V after a 10^8 sec of DC stress.

CONCLUSIONS

We propose a multifunctional DSSB FinFET SONOS device and demonstrate its multi-functional characteristics for high speed Flash memory with a novel NAND Flash architecture and capacitorless 1T-DRAM with the partially silicided as well as dopant segregated S/D in a single transistor.

In a Flash memory operation, hot electrons energized by an energy band engineered at the edge of the S/D are used for a fast program. The DSSB FinFET SONOS device not only inherits the merit of Schottky-barrier FinFET through high immunity of short-channel effect but also endows the high programming speed. A capacitorless 1T-DRAM operation was also achieved by utilizing the dopant segregated region in the same device. These results confirm that the DSSB FinFET SONOS device has great potential for multifunctional SoC applications.

ACKNOWLEDGEMENT

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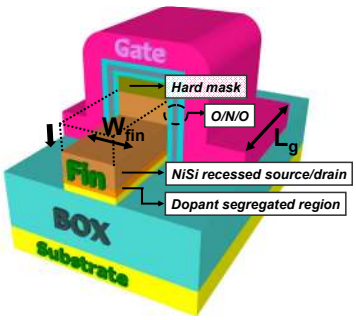
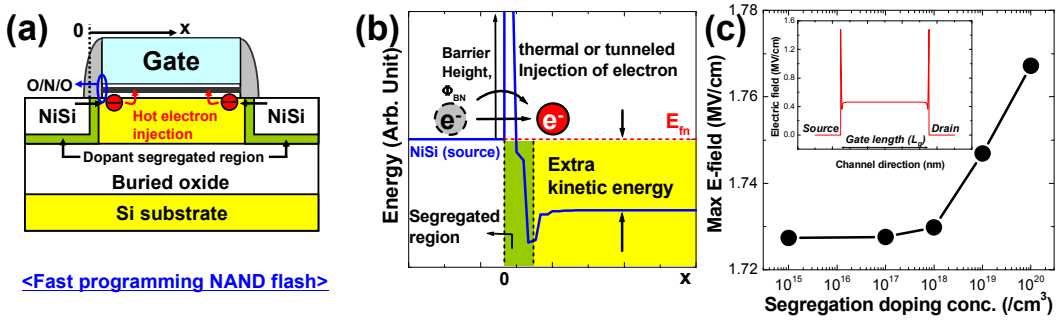
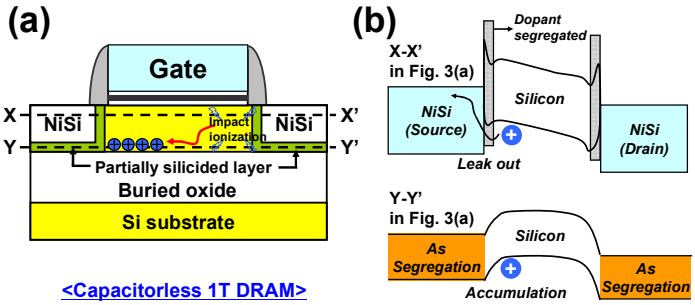


Fig. 1 : Schematics of the DSSB FinFET SONOS device. For multifunctioning memory, an O/N/O structure and a partially silicided S/D are used on an SOI substrate.



<Fast programming NAND flash>

Fig. 2 : Schematic of high speed NVM operation for multifunctioning. (a) The hot electrons energized by a DSSB are used to program a NVM application. Because of the hot electrons energized by the energy band engineered DSSB, a new programming method for Flash memory is possible with low voltage and high speed. (b) A simulated band diagram in the S/D edge. Electrons injected from the S/D have extra kinetic energy, enabling high-speed low-voltage programming for Flash memory operation. (c) Simulation data of an electric field caused by a concentration of segregated doping.



<Capacitorless 1T DRAM>

Fig. 3 : (a) Holes generated by impact ionization accumulate on the floating body due to partially dopant segregation layer. This accumulation can enable the operation of an 1T-DRAM. (b) In 1T-DRAM operation, holes accumulate in a partially segregated layer.

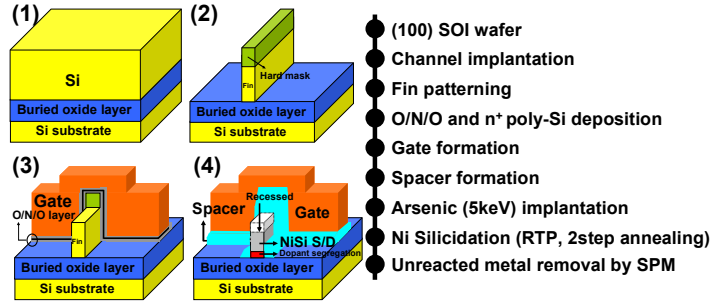


Fig. 4 : Flowchart of the DSSB FinFET SONOS device. In the silicidation process, a two-step RTP is used to reduce any overgrowth of NiSi or severe lateral diffusion. Since SB height is effectively modulated by the dopant concentration, a shallow implantation (5keV) of As was applied.

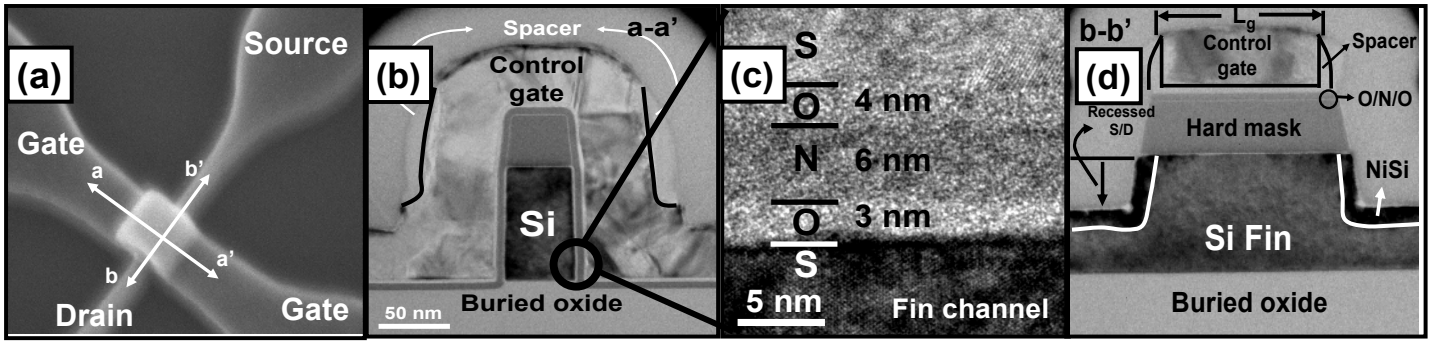


Fig. 5 : The fabricated DSSB FinFET SONOS device: (a) A SEM image of the DSSB FinFET SONOS device, (b) A TEM image across the a-a' direction in Fig. 5(a). The sidewall spacers are observed as shown in Fig. 5(b). The fabricated fin widths vary from 30nm to 100nm and the height of the fin is 75nm. (C) A TEM image of the O/N/O layer for Flash memory. (d) A TEM image across the b-b' direction in Fig. 5(a). The recessed S/D is feasible for making a uniform S/D along the fin depth

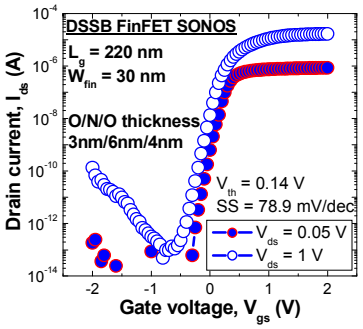


Fig. 6 : The I_{ds}-V_{gs} characteristics of the DSSB FinFET SONOS device.

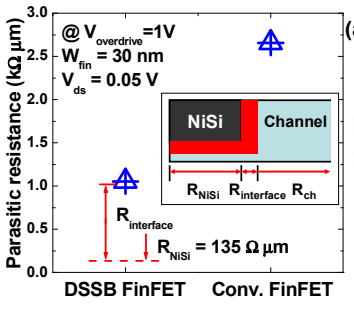


Fig. 7 : The measured parasitic resistance (R_{para}), where R_{para} is normalized by W_{fin}.

$$(R_{para,DSSB\ FinFET} < \frac{1}{3} \cdot R_{para,conv.FinFET})$$

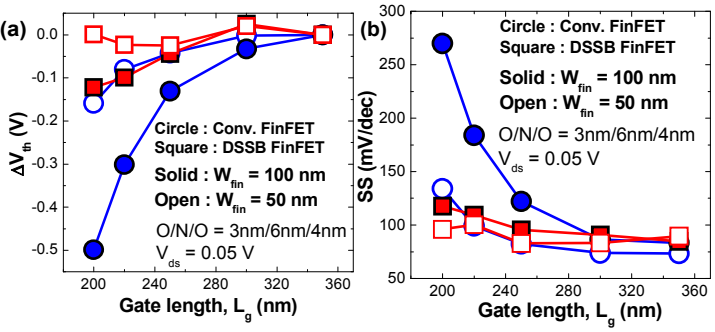


Fig. 8 : (a) The V_{th} roll-off characteristics of the DSSB FinFET SONOS device. These characteristics are attractive in terms of applying the DSSB FinFET SONOS device to a scaled memory due to the high immunity of short-channel effects (SCEs). (b) The subthreshold swing versus the gate length. The SCEs of the DSSB FinFET SONOS device are superior to those of a conventional device.

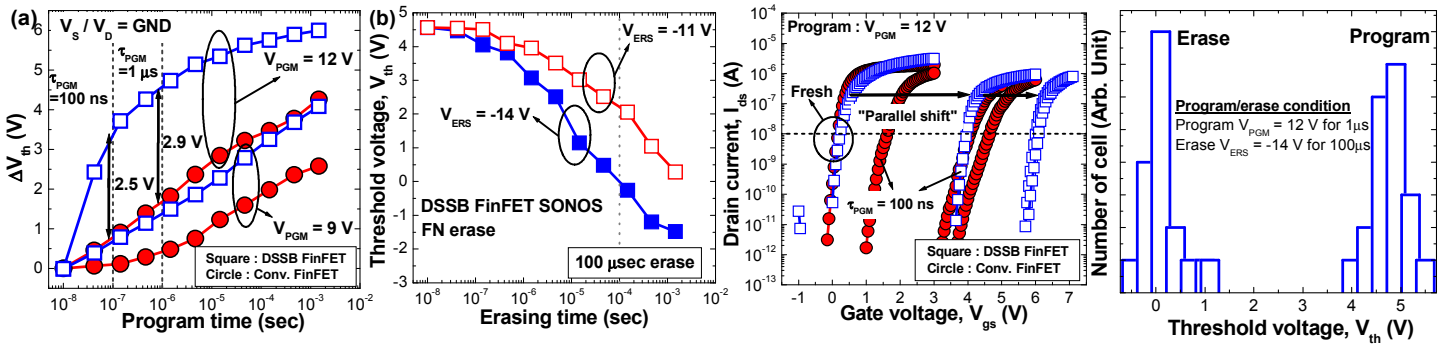


Fig. 9 : (a) The characteristics of the EBEHE-program. Excellent programming efficiency compared to the control group is obtained due to high speed EBEHE programming. Fast programming (V_{th} >4.5V) is demonstrated even at 1μs. (b) The FN erase characteristics with different erasing voltages.

Fig. 10 : Comparison of the I_{ds}-V_{gs} shift among various programmed states. A two-sided injected charge produces a parallel shift of I-V.

Fig. 11 : The V_{th} distribution of the EBEHE program and FN erase of the DSSB FinFET SONOS device in NAND operation.

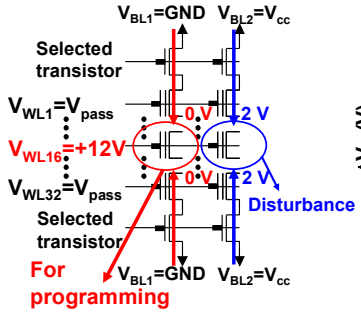


Fig. 12 : A novel divided bit-line NAND architecture for the EBEHE programming. The ground bias of the bit line is applied to the EBEHE programming.

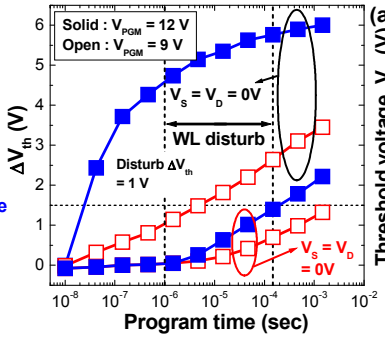


Fig. 13 : A WL disturbance window for the EBEHE programming. A positive S/D voltage can reduce the hot electron generation because of a reduced electric field.

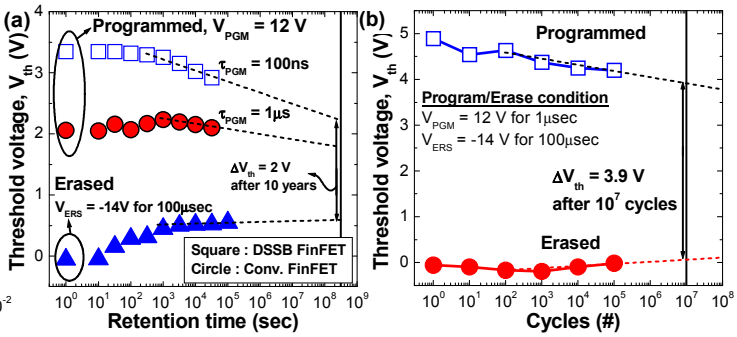


Fig. 14 : (a) Data retention characteristics after 1k P/E cycles. Even for short program times (100ns), a large V_{th} window is obtained due to the EBEHE program. (b) The measured endurance characteristics of the DSSB FinFET SONOS device in Flash memory operation.

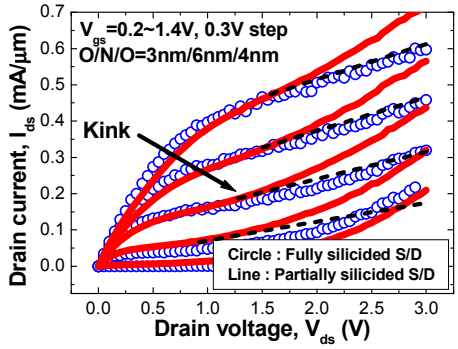


Fig. 15 : The measured I_{ds}-V_{ds} curve. The kink effect caused by the accumulated holes in the floating body is observable only in a partially silicided device.

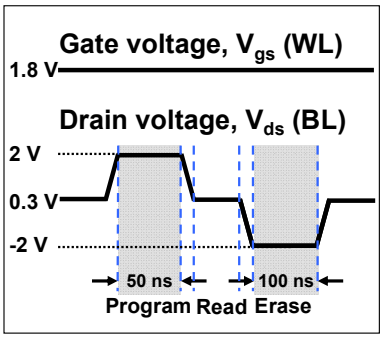


Fig. 16 : The program, erase, and read bias conditions. The program time is 50ns and the erase time is 100ns.

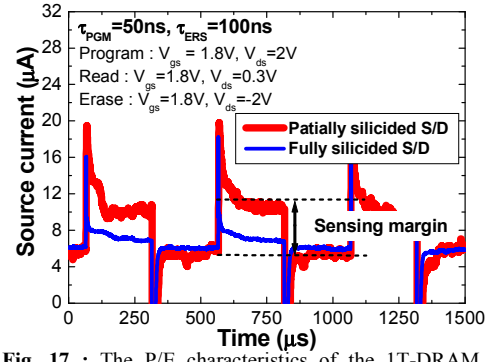


Fig. 17 : The P/E characteristics of the 1T-DRAM operation in the DSSB FinFET SONOS device for multifunctioning. Two separated states are clearly distinguishable but only in the partially silicided case.

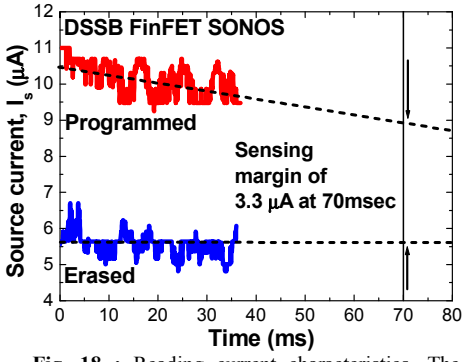


Fig. 18 : Reading current characteristics. The nondestructive readout ensures a sensing margin of 3.3 μA for 70ms.

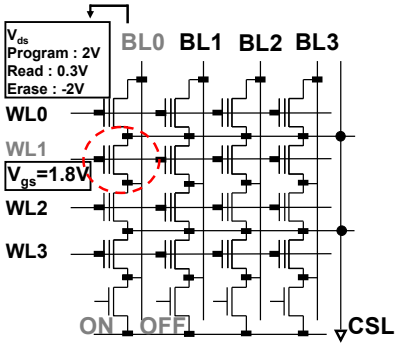


Fig. 19 : The Cell layout for the 1T-DRAM operation. This cell layout is exactly the same as that of the NOR Flash.

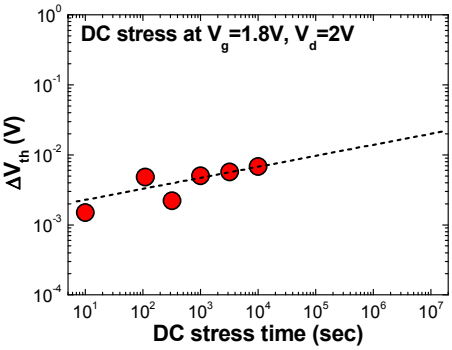


Fig. 20 : The V_{th} shift after DC stress at the 1T-DRAM program voltage in the DSSB FinFET SONOS device. No significant V_{th} shift is observed even after 10^4 s.