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High speed graphene transistors with a self-aligned nanowire gate

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Abstract

Graphene has attracted considerable interest as a potential new electronic material[1–11]. With the highest carrier mobility exceeding 200,000 $cm^2/V{\cdot}s$, graphene is of particular interest for ultra-high speed radio frequency (RF) electronics[12–18]. However, the conventional dielectric integration and device fabrication processes cannot be readily applied to fabricate high speed graphene transistors because they can often introduce significant defects into the monolayer of carbon lattices and severely degrade the device performance[19–21]. Here we report a new approach to fabricate high-speed graphene transistors with a self-aligned nanowire gate to enable unprecedented performance. The graphene transistors are fabricated using a Co_2Si/Al_2O_3 core/shell nanowire as the gate, with the source and drain electrodes defined through a self-alignment process and the channel length defined by the nanowire diameter. The physical assembly of nanowire gate preserves the high carrier mobility in graphene, and the self-aligned process ensures that the edges of the source, drain, and gate electrodes are automatically and precisely positioned so that no overlapping or significant gaps exist between these electrodes and thus minimizes access resistance. It therefore enables transistor performance not previously possible. Graphene transistors with channel length down to 140 nm have been fabricated with the highest scaled on-current (3.32 mA μm^{-1}) and transconductance (1.27 mS μm^{-1}) reported to date. Significantly, on-chip microwave measurements demonstrate that the self-aligned devices exhibit a record high intrinsic cutoff frequency (f_T) in the range of 100–300 GHz, with the extrinsic f_T in the range of a few gigahertz largely limited by parasitic pad capacitance. The reported intrinsic cutoff frequency of the graphene transistors is comparable to that of the very best high electron mobility transistors with similar gate lengths[10]. It therefore marks an important milestone in graphene RF devices and can enable exciting opportunities in high-speed electronics.

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Author Contributions X.D conceived the research. X.D. and L.L. designed the experiment. L.L. performed all the experiments including material synthesis, device fabrication, DC/RF characterization, and data analysis. Y-C.L. contributed to material synthesis, material and device structure characterization, and RF analysis. M.B. contributed to RF characterization and analysis. R.C. and Y.L. contributed to DC/RF analysis. J.B. contributed to device fabrication. Y.Q. contributed to material synthesis. X.D. and L.L. co-wrote the paper. All authors discussed the results and commented on the manuscript.

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With the highest carrier mobility exceeding 200,000 $cm^2/V{\cdot}s$[8], and many other desirable properties including large critical current densities (~2×10^8 A/cm^2)[22] and a high saturation velocity (5.5×10^7 cm/s)[11], graphene is of significant potential for high speed electronics to offer excellent RF characteristics with very high cutoff frequency (f_T). Importantly, recent studies have demonstrated graphene transistors operating in the gigahertz regime[12–14,16–18] with a record of f_T =100 GHz[13]. The reported RF performance to date is however still far from the potential that the graphene transistors may offer, primarily limited by two adverse factors in the device fabrication process.

A first limitation is associated with the severe mobility degradation resulted from graphene-dielectric integration process that introduces substantial defects into pristine graphene lattices[20,23]. To this end, we have recently developed a new strategy to integrate high quality high-*k* dielectrics with graphene using a physical assembly approach without introducing any appreciable defects into the graphene lattices, and demonstrated the top-gated graphene transistors with the highest carrier mobility exceeding 20,000 $cm^2/V{\cdot}s$[24–26]. Another limitation of the top-gated graphene transistors reported to date is the large access resistance due to non-optimum alignment of the source-drain and gate electrodes, which can have particularly adverse impact on short channel devices. With decreasing channel length, there is an increasing demand for a more precise device fabrication process. In the state-of-the-art silicon MOSFET technology, a self-aligned gate structure is used to ensure that the edges of the source, drain, and gate electrodes are precisely positioned so that no overlapping or significant gaps exist between these electrodes. However, these conventional dielectric integration and device fabrication processes used in silicon technology can not be readily employed for graphene-based electronics, as many of them can lead to significant damages in the monolayer of graphene lattices with severe performance degradation.

Here we report an entirely new strategy to fabricate graphene transistors using a Co_2Si/Al_2O_3 core/shell nanowire as the self-aligned top-gate (Figure 1). To fabricate the device, graphene flakes were first mechanically peeled onto a highly resistive silicon substrate (> 18,000 ohm·cm) with a 300 nm thermal silicon oxide. The Co_2Si/Al_2O_3 core/shell nanowires were aligned on top of the graphene through a physical dry transfer process[25,26], followed by e-beam lithography, buffered oxide etching to remove the Al_2O_3 shell and expose the Co_2Si core, and metallization (Ti/Au, 70/50 nm) process to define the external source, drain and gate electrodes. A thin layer of Pt metal (10 nm) was then deposited on top of the graphene across the Co_2Si/Al_2O_3 core/shell nanowire, in which the Co_2Si/Al_2O_3 core/shell nanowire separates the Pt thin film into two isolated regions that form the self-aligned source and drain electrodes precisely positioned next to the nanowire gate. In this device, the Co_2Si/Al_2O_3 core/shell nanowire defines the channel length, with the 5 nm Al_2O_3 shell functioning as the gate dielectrics, and the metallic Co_2Si core functioning as the local top-gate, and self-aligned Pt thin film pads as the source and drain electrodes (Fig. 1a, b).

The Co_2Si nanowires were synthesized through a chemical vapour deposition (CVD) process with the diameters typically in the range of 100–300 nm and the lengths around 10 μm (Fig. 2a)[27]. The composition of Co_2Si was characterized by energy-dispersive x-ray spectroscopy (Supplementary Fig. S1). The Co_2Si/Al_2O_3 core/shell nanowires were grown through atomic layer deposition (ALD) of Al_2O_3 shell on the Co_2Si nanowires with controlled thickness. The relative dielectric constant of the ALD Al_2O_3 is determined to be ~7.5 based on capacitance-voltage measurement using a planar metal/Al_2O_3/Si control structure. Transmission electron microscope (TEM) image shows a uniform coating of the amorphous Al_2O_3 (light contrast) surrounding the single-crystalline Co_2Si core (dark contrast) (Fig. 2b). High resolution TEM image clearly shows the single crystalline Co_2Si core with an amorphous Al_2O_3 shell of lighter contrast (Supplementary Fig. S2). The electrical measurement of a Co_2Si nanowire clearly shows linear current-voltage (I–V)

characteristics (Fig. 2c) with the resistance of a 180 nm diameter and 3 micron long Co_2Si nanowire close to 527 ohm, and an estimated resistivity of 437 μΩ·cm. Our measurements of over 10 nanowires give a resistivity range of 200–500 μΩ·cm, consistent with previous report[27]. The low resistance of the Co_2Si nanowires is particularly important for them to function as effective gate electrodes for RF graphene transistors.

Figure 3a shows an SEM image of a self-aligned graphene transistor and an optical microscope image of the overall device layout (inset, Fig 3a). The cross-sectional SEM image of a typical device shows the self-aligned Pt thin film source and drain electrodes are well separated by the nanowire gate and precisely positioned next to the nanowire gate (Fig. 3b), clearly demonstrating that the self-alignment process can be used to effectively integrate graphene with a nanowire gate and nearly perfectly positioned source and drain electrodes.

Prior to the formation of the self-aligned Pt source and drain electrodes, we have measured the transfer characteristics, drain-source current (I_{ds}) versus top-gate voltage (V_{TG})applied by the local nanowire gate. The I_{ds} -V_{TG} plot clearly shows that the graphene transistor can be modulated by the local nanowire gate, overturning from the hole branch to electron branch within −1 to 3 V range (Fig. 3c), demonstrating the Co_2Si/Al_2O_3 core/shell nanowire can indeed function as an effective local gate for the graphene transistors. However, the gate modulation is less than 10%, smaller than the typical values observed in graphene transistors at room temperature (around 50%). This difference can be attributed to the large access resistance due to the relatively small gated area compared to the entire graphene channel.

The formation of the self-aligned source and drain electrodes allows precise positioning of the source-drain edges with the gate edges, and thus substantially reduce the access resistance and improve the graphene transistor performance. Before transistor characterization of the self-aligned devices, we have first tested the gate leakage across the Co_2Si/Al_2O_3/graphene gate stack. The gate tunnelling leakage current (I_{gs}) from the Co_2Si/Al_2O_3 core/shell nanowire to the underlying graphene is negligible within the gate voltage range of ± 3 V range (Supplementary Fig. S3). This measurement demonstrates that the 5 nm Al_2O_3 dielectrics can function as an effective gate insulator for top-gated graphene transistors and afford high gate capacitance that is critical to the high transconductance.

Importantly, the I_{ds}-V_{TG} transfer curve recorded for a self-aligned device shows a current modulation of about 42 % (Fig. 3d), comparable to the typical values observed in long channel graphene transistors, suggesting that the access resistance in this ultra-short channel device is largely removed through the self-alignment process. The hysteresis of I_{ds}-V_{TG} is about 0.02 V under ambient conditions (Supplementary Fig. S4), demonstrating the relative clean nature of the graphene-dielectric interface. Figure 3e shows the I_{ds}-V_{ds} output characteristics at various gate voltages. The device can deliver a maximum scaled on-current of 3.32 mA/μm at V_{ds} = −1 V and V_{TG} = −1 V. The transconductance $g_m = \left|\frac{dI_{ds}}{dV_g}\right|$ can be extracted from the I_{ds}-V_{TG} curve (Fig. 3f). A peak scaled transconductance of 0.02 mS/μm is obtained at V_{ds} = −1 V for the device prior to the deposition of the self-aligned source and drain electrodes. Significantly, with the self-aligned source and drain electrodes, the peak scaled transconductance at V_{ds} = −1 V reaches 1.27 mS/μm, a more than 60 times of improvement over the non-self-aligned device. This study clearly demonstrates the self-alignment process is a critical to ensure high transistor performance in the short channel devices. To the best of our knowledge, these scaled on-current and transconductance values obtained here represent the highest values reported in bulk graphene transistors to date[11–13,15–17,28]. Higher transconductance was only observed previously in graphene nanoribbon transistors with much larger gate capacitance[25].

To characterize the gate capacitance, we have measured the device conductance as a function of both V_{TG} and back-gate bias (V_{BG}) (Fig. 3g). From these measurements, we can obtain Dirac point shifts in the top-gated configuration as a function of the applied V_{BG} (Fig. 3h), which gives the ratio between top-gate and back-gate capacitances, $C_{TG}/C_{BG} \approx 38$. Using the back-gate capacitance value of $C_{BG} = 11.5$ nF/cm^2, the top-gate capacitance is estimated to be $C_{TG} = 437$ nF/cm[11,24], which is consistent with the results obtained from the finite element calculations, $C_{TG} = \sim 394$ nF/cm^2 (Supplementary Fig. S5).

The above discussions clearly demonstrate our self-aligned nanowire gate can allow us to achieve graphene transistors with unprecedented DC performance. An important benchmark of the transistor RF performance is the cutoff frequency f_T. To assess the RF characteristics of our self-aligned transistors, on-chip microwave measurements were carried out in the range of 50 MHz to 30 GHz using an Agilent 8722ES network analyzer. Due to the extremely small dimension of our devices, the gate capacitance of our device is typically about two orders of smaller than the parasitic pad capacitance. To accurately determine the f_T values requires careful de-embedding procedures (see Methods)[13,14,17].

Figure 4a shows the current gain |h21| derived from the measured S-parameters at $V_{TG} = 1$ V and a drain bias $V_{ds} = -1$ V. It displays the typical *1/f* frequency dependence expected for an ideal FET, yielding a f_T of 300 GHz. We also verified f_T data using Gummel's approach[29], in which the extracted f_T is identical to the aforementioned value (inset, Fig. 4a). This extracted f_T value is also consistent with the projected value (323 GHz) using the well-known relation $f_T = g_m/(2\pi C_g)$ established for conventional FETs[30]. Importantly, the speed of this self-aligned graphene device represents the highest in all graphene devices reported to date[12–14,16–18]. Furthermore, it is about two times faster than that of the best silicon MOSFETs of comparable sizes (e.g. about 150 GHz for a 150 nm Si-MOSFET), and comparable to those of the very best InP high electron mobility transistors (HEMT) and GaAs metamorphic HEMT with similar channel lengths[10]. Figure 4b and 4c further show the results obtained from another two self-aligned graphene transistors with a 182 nm and 210 nm nanowire gate, displaying a f_T of 168 GHz and 125 GHz, respectively, also higher than any graphene transistors reported previously.

It should be noted that the record high intrinsic f_T values reported here are obtained after careful de-embedding procedures using the exact contact pad layout. Without de-embedding procedures, the extrinsic f_T values (2.4, 1.9 and 1.6 GHz) for the three devices described above are substantially lower (Supplementary Fig. S6), due largely to the large ratio between parasitic and gate capacitance. The large intrinsic/extrinsic f_T ratios (125, 88 and 78) call for further scrutiny and validation of our de-embedding procedures. To this end, we have carefully analyzed the second device to extract all device component values based on the equivalent circuit and S-parameter measurements (Supplementary Fig. S7). Importantly, the device component values (including parasitic capacitance, gate capacitance and transconductance etc.) derived from the RF measurements are consistent with those obtained from the DC measurements or electrostatic simulations (Table S1 & S2). In particular, this analysis confirms that the difference between intrinsic and extrinsic f_T can be primarily attributed to the large ratio between parasitic pad capacitance and gate capacitance. Significantly, by re-designing the device layout to reduce the parasitic capacitance, we can significantly reduce the parasitic/gate capacitance ratio and hence the intrinsic/extrinsic f_T ratio (Supplementary Fig. S8). These studies unambiguously validate our de-embedding procedures.

In summary, we have described a novel self-aligned process to fabricate graphene transistors with a nanowire gate. The unique device layout ensures that the edges of the source, drain, and gate electrodes are precisely and automatically positioned so that no overlapping or

significant gaps exist between these electrodes. The fabrication approach allows integration of the top-gate electrodes without introducing appreciable damage into pristine graphene lattices and thus retains the high electronic performance, to enable graphene transistors with several significant advantages, including record high driving current, transconductance and f_T. This study marks an important milestone in the development of high-speed graphene transistors, and opens the exciting potential of graphene-transistors in high-speed high-frequency electronics. With further optimization of graphene growth over large area, nanowire assembly or soft lithography process to precisely control the dimension and location of the self-aligned gate, large arrays of self-aligned high-speed graphene transistors or circuits can be envisioned.

METHODS SUMMARY

The Co_2Si nanowires were synthesized through a chemical vapour deposition process, and Co_2Si/Al_2O_3 core/shell nanowires by atomic layer deposition (ALD) of Al_2O_3 shell on the Co_2Si nanowires. Graphene flakes were first mechanically peeled onto a highly resistive silicon substrate (> 18,000 ohm·cm) with a 300 nm thermal silicon oxide. The Co_2Si/Al_2O_3 core/shell nanowires were aligned on top of the graphene through a physical dry transfer process, followed by e-beam lithography, buffered oxide etching to remove the Al_2O_3 shell and expose the Co_2Si core, and metallization (Ti/Au, 70/50 nm) process to define the source, drain and gate electrodes. A thin layer of Pt metal (10 nm) was then deposited on top of the graphene across the Co_2Si/Al_2O_3 core/shell nanowire, in which the Co_2Si/Al_2O_3 core/shell nanowire separates the Pt thin film into two isolated regions that form the self-aligned source and drain electrodes precisely positioned in close proximity to the nanowire gate. The DC electrical transport studies were conducted with a probe station at room temperature under ambient conditions with a computer-controlled analogue-to-digital converter. The on-chip microwave measurements were carried out in the range of 50 MHz to 30 GHz using an Agilent 8722ES network analyzer. The measured S-parameters were de-embedded using specific “short” and “open” structures with identical layouts, excluding the graphene channel, to remove the effects of the parasitic capacitance, resistance and inductance associated with the pads and connections. The “through” calibration was done with exact pad layout with gate shorted to drain, and the “load” calibration was done with standard calibration pad.

Supplementary Material

Refer to Web version on PubMed Central for supplementary material.

Acknowledgments

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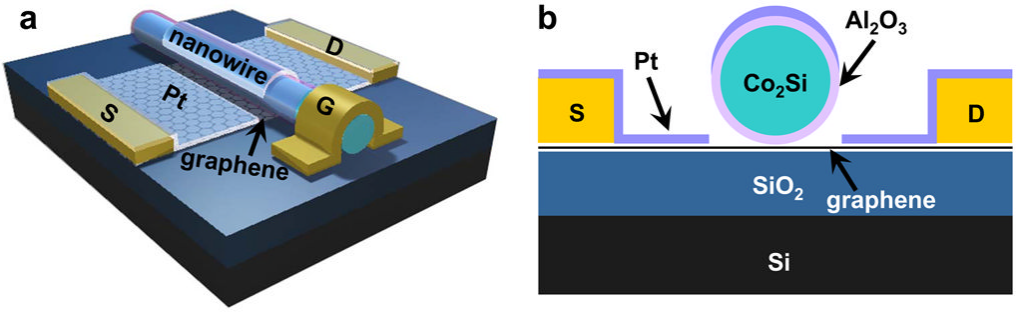

Figure 1. Schematic illustration of a high-speed graphene transistor with a Co_2Si/Al_2O_3 core/shell nanowire as the self-aligned top-gate

a, Schematic illustration of the three-dimensional view of the device layout. **b**, Schematic illustration of the cross-sectional view of the device. In this device, the Co_2Si/Al_2O_3 core/shell nanowire defines the channel length, with the 5 nm Al_2O_3 shell in functioning as the gate dielectrics, and the metallic Co_2Si core functioning as the self-integrated local gate, and the self-aligned Pt thin film pads as the source and drain electrodes

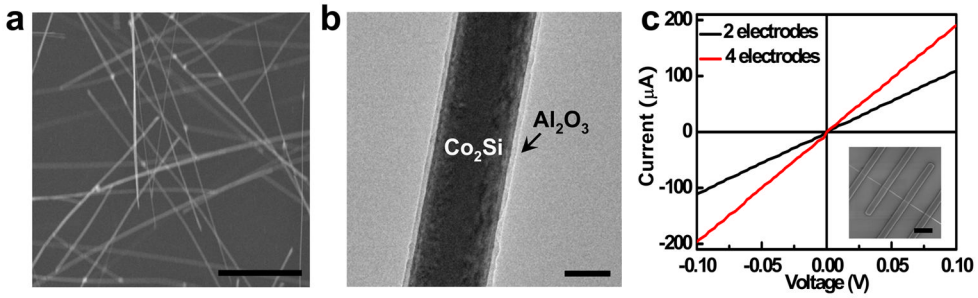

Figure 2. Characterization of Co_2Si and Co_2Si/Al_2O_3 core/shell nanowires

a, SEM image of the Co_2Si nanowires. The nanowires were synthesized through a chemical vapour deposition process with the diameters typically in the range of 100–300 nm and the lengths around 10 μm. **b**, TEM image of a Co_2Si/Al_2O_3 core/shell nanowire shows a uniform coating of the amorphous Al_2O_3 (light contrast) surrounding the single-crystal Co_2Si core (dark contrast). **c**, The I–V characteristic of a single Co_2Si nanowire in two- and four-terminal measurements to determine the nanowire resistance and resistivity. The inset shows an SEM image of the device, the scale bar is 3 μm.

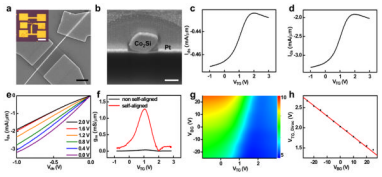

Figure 3. Room temperature electrical characteristics of the graphene transistors with a self-aligned nanowire gate

a, An SEM images of a graphene transistor with a self-aligned nanowire gate, the width of devices of about 2.64 μm. The inset shows an optical microscope image the overall device layout. **b**, The cross-sectional SEM image of a typical device shows the self-aligned Pt thin film source and drain electrodes are well separated by the nanowire gate and precisely positioned next to the nanowire gate. The graphene below the nanowire gate is not clearly visible. **c**, and **d**, I_{ds}-V_{TG} transfer characteristics at V_{ds} = −1 V before and after the deposition of the self-aligned Pt source-drain electrodes. **e**, The I_{ds}-V_{ds} output characteristics at various gate voltages (V_{TG} =0.0, 0.4, 0.8, 1.2, 1.6, and 2.0 V) for the *dIds* self-aligned device. **f**, Transconductance $g_m = \left|\frac{dI_{ds}}{dV_g}\right|$ at V_{ds} = −1 V as a function of top-gate voltage V_{TG} before (black) and after (red) the deposition of the self-aligned Pt source-drain electrodes, highlighting the self-alignment process increases the peak transconductance by a factor of > 60. **g**, Two dimensional plot of the device conductance for varying V_{BG} and V_{TG} bias for self aligned device. The unit in the color scale is mS. **h**, The top-gate Dirac point V_{TG_Dirac} at different V_{BG}, with which we can derive C_{TG}/C_{BG}≈38.

Figure 4. Measured small-signal current gain |h21| as a function of frequency *f* at V_{ds} = −1 V
a, For a device with gate length = 144 nm at V_{TG} = 1 V; **b**, For a device with gate length = 182 nm at V_{TG} = 0.3 V; and **c**, For a device with gate length = 210 nm at V_{TG} = 1.1 V; These different V_{TG} values used are the peak transconductance points for each device. The insets show the f_T extraction by Gummel's method.