High-speed one-dimensional spatial light modulator for Laser Direct Imaging and other patterning applications

Jan-Uwe Schmidt[1a], Ulrike A. Dauderstaedt[a], Peter Duerr[a], Martin Friedrichs[a], Thomas Hughes[a], Thomas Ludewig[a], Dirk Rudloff[a], Tino Schwaten[a], Daniela Trenkler[a], Michael Wagner[a], Ingo Wullinger[a], Andreas Bergstrom[b], Peter Bjornangen[b], Fredrik Jonsson[b], Tord Karlin[b], Peter Ronnholm[b], Torbjorn Sandstrom[b]

[a]Fraunhofer Institute for Photonic Microsystems (IPMS), Maria-Reiche-Str. 2, D-01109 Dresden, Germany; [b]Micronic Mydata AB, Nytorpsvagen 9, SE-18303 Taby, Sweden

ABSTRACT

Fraunhofer IPMS has developed a one-dimensional high-speed spatial light modulator in cooperation with Micronic Mydata AB. This SLM is the core element of the Swedish company's new LDI 5sp series of Laser-Direct-Imaging systems optimized for processing of advanced substrates for semiconductor packaging. This paper reports on design, technology, characterization and application results of the new SLM. With a resolution of 8192 pixels that can be modulated in the MHz range and the capability to generate intensity gray-levels instantly without time multiplexing, the SLM is applicable also in many other fields, wherever modulation of ultraviolet light needs to be combined with high throughput and high precision.

Keywords: Laser Direct Imaging (LDI), Printed Circuit Boards (PCB), Spatial Light Modulator (SLM), Micro Mirror Array (MMA), gray-scale lithography, semiconductor packaging, semi-additive processing, substrate

1 INTRODUCTION

1.1 Laser direct imaging for advanced substrates in semiconductor packaging

Modern electronics packaging increasingly utilizes high-end forms of printed circuit boards called 'substrates' and 'interposers'. The first provide a mechanical support and an electrical interface between integrated circuits and the outside world, the latter act as an intermediate layer used for interconnection routing and as a ground/power plane. Advanced packages require substrates with a high density of interconnects with minimum interconnect line widths and spaces of about 10 µm, in few years even less. Such high density substrates are processed in form of large panels (e.g. 510 mm x 515 mm). To form the interconnect layers, the 'semi-additive metallization' process [1] is used (Figure 1): On a copper seed layer, a layer of dry film resist (DFR) is laminated (1). Next, the whole panel is exposed by ultraviolet (UV) light (2), in order to enable patterning of the DFR (3). The spaces in the patterned DFR act as template for the deposition of copper by electroplating (4). The removal of DFR (5) is followed by a flash etch to remove the Cu seed layer (6). As feature size decreases, several wiring layers and their vertical connections (vias) have to be aligned within smaller tolerances to avoid functional errors. Compared to mask-based steppers an exposure by Laser Direct Imaging (LDI) offers higher flexibility. LDI techniques utilize a programmable micromechanical element, a so-called 'spatial light modulator' (SLM) to print dose-patterns into the resist and have the potential to combine high resolution, high precision of alignment and high throughput. Small variations in the pitch of existing structures induced by strain in the substrates can be measured for each panel and compensated by appropriate algorithms, such that new layers perfectly match the preceding ones. Micronic Mydata AB has developed a novel LDI5sp laser direct imaging system optimized for this field of application. As a cooperation partner, Fraunhofer IPMS contributed to this system a novel fast one-dimensional diffractive spatial light modulator (SLM), which shall be discussed in the present article.

1 Corresponding author: jan-uwe.schmidt@ipms.fraunhofer.de; phone ++49-351-8823-119; fax ++49-351-8823-266; www.ipms.fraunhofer.de

MOEMS and Miniaturized Systems XIII, edited by Wibool Piyawattanametha,
Yong-Hwa Park, Proc. of SPIE Vol. 8977, 89770O · © 2014 SPIE
CCC code: 0277-786X/14/$18 · doi: 10.1117/12.2036533

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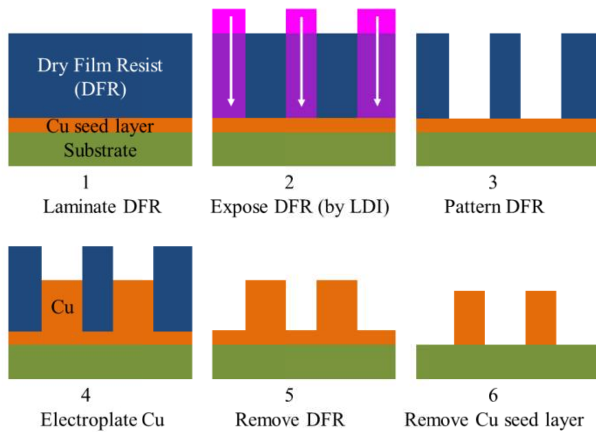

Figure 1: Schematic of semi-additive metallization process (SAP) using a negative tone resist.

Figure 2: Micronic Mydata LDI 5sp system

1.2 Diffractive intensity modulation by means of programmable micro mirror arrays

To motivate the selected SLM design, the principle of diffractive intensity modulation using micro-mirror arrays is briefly summarized. Due to the regular grid of mirrors, any micro mirror array (MMA) acts as an optical grating. While the location of the 0th diffraction order in space is determined by the angle of incidence only, the positions of the higher orders also depend on pitch of micro mirrors, and the optical wavelength [2]. Determined by interference, the fractions of intensity reflected into the different orders of the grating depend on the phase relationship between reflected partial waves. They can be modulated by changing the deflection state of micro mirrors: a light wave approaching a MMA of un-deflected mirrors will be reflected specularly, i.e. all reflected intensity will be in the 0th order (assuming negligible slits and ideally flat mirrors). Already small piston or tilt deflections of micro mirrors modify the phase of light such, that intensity is partly redirected into the higher diffraction orders. The intensity in the 0th order approaches zero for certain deflection conditions [3].

Based on this effect, MMAs can be utilized to modulate the intensity of coherent monochromatic or narrow-band light sources. For this purpose the light reflected by the MMA is collected by an imaging system, that allows only the intensity in the 0th diffraction order (or another single diffraction order) to contribute to the image, while the other diffraction orders are blocked, e.g. by placing an aperture of suitable dimensions in the Fourier plane of the imaging system. In an image generated this way, regions with un-deflected mirrors will appear bright, whereas regions with deflected mirrors will appear gray or even black, depending on the mirror deflection.

The illustrated concept for diffractive intensity is most frequently used with MMA devices that allow for an analog deflection of mirrors (“analog” MMA) [4][5][6][7], because a continuously controlled mirror deflection is converted instantly into gray-scale intensity levels. The described technique allows to use analog MMAs as high-speed spatial light modulators for the generation of monochrome gray-scale patterns. This motivated the commercial application of two dimensional analog MMAs in semiconductor mask writers [3][7][8].

2 SLM DESIGN

The active area of the one-dimensional (1D) modulator is formed by an array of electrostatically addressed micro mirrors capable of analog tilt deflection.

Figure 3 shows a top-view scanning electron microscopy (SEM) image of mirrors in the optically active area. The manually added colors highlight rows of identically addressed and synchronously tilting mirrors. Each of the 8192 mirror rows acts as one “optical pixel” of the SLM. The SLM contains no integrated active driver electronics: an external data path unit provides the required data and auxiliary potentials directly to the SLM. Figure 4 shows a cross-section of the same structure. The three top structural layers (mirror, yoke, interconnect 2) can be seen.

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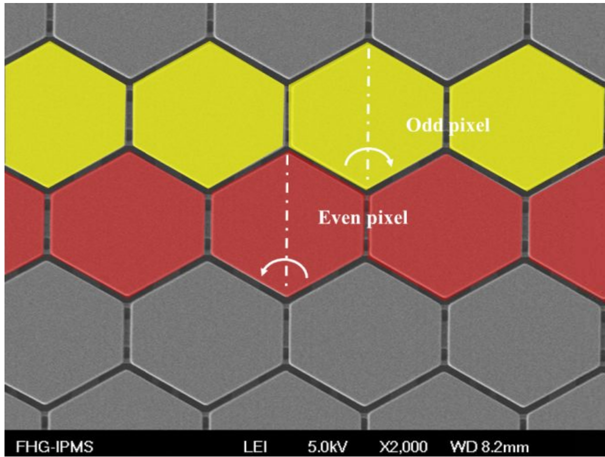

Figure 3: SEM image of tilt mirrors. Colors indicate mirrors belonging to same pixel.

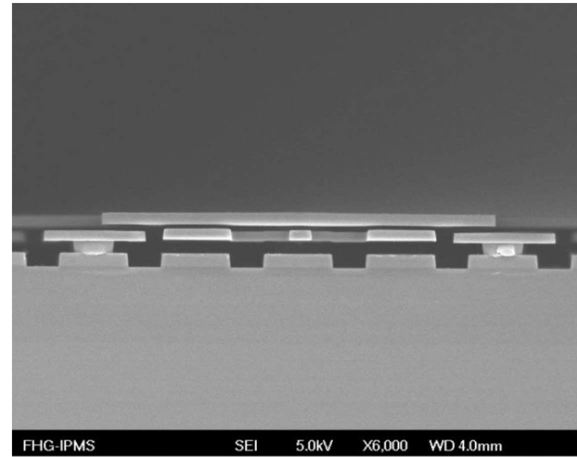

Figure 4: SEM cross-sectional image of tilt mirrors after removal of sacrificial layer.

Figure 5 shows the fully processed SLM to illustrate its layout. The approximate chip dimensions are 15 mm x 88 mm. Bond pads are arranged in 4 rows to both sides of the SLM (1). In the electrode fan out region (2) data-electrodes are routed to the pixel area (3) comprising 2.2 million mirrors grouped to 8192 “optical pixels” (4).
The pixel area has approximate dimensions of 4 mm x 82 mm.
This design was preferred for several reasons: all optical pixels can be updated in parallel at a modulation rate in the MHz range limited only by the fundamental resonance of the micro mirror tilt-movement. This enables highly productive continuous exposure processes and allows an efficient utilization of quasi-continuous, i.e. MHz-repetition rate pulsed ultra-violet lasers. Since a higher repetition rate of the laser also implies a lower energy per laser pulse and hence lower mirror temperatures, the design also helps to minimize laser induced degradation of mirrors.
Building the “optical pixels” of the 1D-SLM from sets of small identically addressed micro mirrors allows to reach a high fundamental resonance of micro mirrors, but also allows to increase the total area per optical pixel without sacrificing modulation speed. This again helps to reduce power density at the SLM and the temperature of the laser-exposed micro mirrors and contributes to a long SLM lifetime [10]. The SLM design without integrated address electronics reduces the complexity of SLM processing, SLM cost and processing time, and increases yield. Upgrades of the control electronics have no impact on SLM technology and can be implemented whenever more powerful components become available at acceptable cost.

Figure 6 shows a single actuator electrostatically addressed via global voltage electrodes (1) and (2) and the data electrode (3). The global electrodes (1) and (2) proceed in vertical direction and supply the common counter potentials to all pixels. The electrodes (1), (2), and (3) are formed from interconnect layer 2. Within one optical pixel, the segmented data electrodes (3) of all micro mirrors are connected by vias to the same data line. The latter proceeds perpendicular to the global electrodes in the hidden interconnect layer 1.
Since actuators in even and odd rows are offset by half the width of an actuator, the positive global electrode (1) and the negative global electrode (2) change sides within the actuator cell for even and odd pixels respectively. This results in reversal of tilt directions for even and odd pixels assuming the same sign of data voltage applied to the data electrodes (3) of the neighboring pixels.
The yoke structure (4) is supported by two posts resting on the data electrode. It is tilted depending on the voltage difference between data and global electrodes (arrows in Figure 6). The restoring force is defined by the narrow spring region (5) of the yoke structure. A post (6) resting on the yoke supports the mirror (7).
Separate structural layers for mirror and springs allow optimizing mechanical and optical characteristics independently. By use of a low-creep hinge material, hysteresis effects are eliminated and the mirror can be optimized for the operating wavelength.

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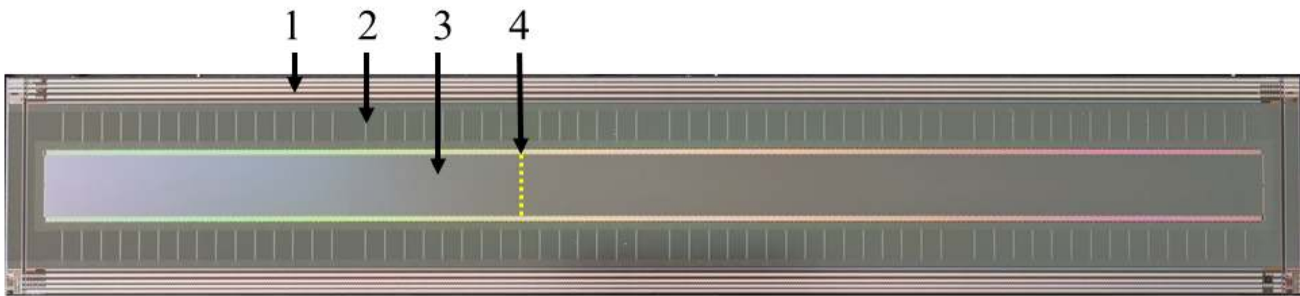

Figure 5: Photograph of the diced chip with removed sacrificial layers. Markers indicate bondpad region (1), electrode fan-out region (2), and active pixel area (3). The dotted line (4) shows the orientation of a single optical pixel.

Applying the variable data potential to the yoke/mirror electrode (3) reduces the required data voltage range by a factor of two compared to the alternative option of addressing electrode (1) while keeping electrodes (2) and (3) at fixed reference potential. Reducing the data voltage range lowers the cost of electronic components for the data path and allows for a higher speed.

For this specific SLM, a hexagonal mirror plate has been used to optimize the modulation characteristics. To illustrate the effect of mirror shape, Figure 7 shows simulated modulation characteristics for (ideally flat) hexagonal and rectangular mirrors at a wavelength of 355 nm. Plotting the intensity in the 0th order vs. tip deflection of a mirror, the side lobe next to the first intensity minimum is clearly less pronounced for the hexagonal mirror shape compared to rectangular or square mirrors with rotation axis parallel to the sides. On the other hand, the deflection required to reach the first intensity minimum is slightly higher for hexagonal mirrors (for the chosen design about 110 nm at a wavelength of 355 nm).

Due to the fact that the slits are very narrow and the mirror post is completely hidden underneath the mirror (Figure 3), the optical fill factor of the pixel area is very high, about 90 %. Scattering losses are thereby reduced, while optical efficiency and achievable contrast are increased. A summary of parameters of the new SLM is given in Table 1.

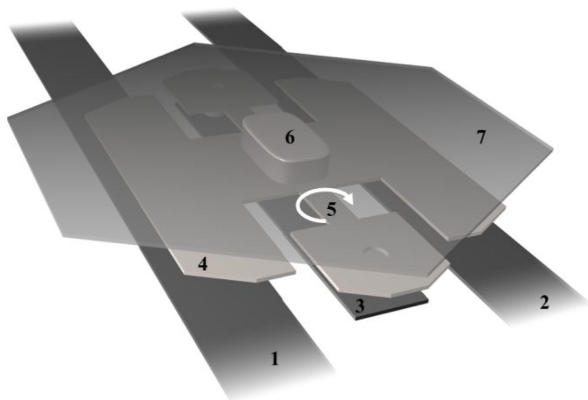

Figure 6: Schematic of single tilting mirror.

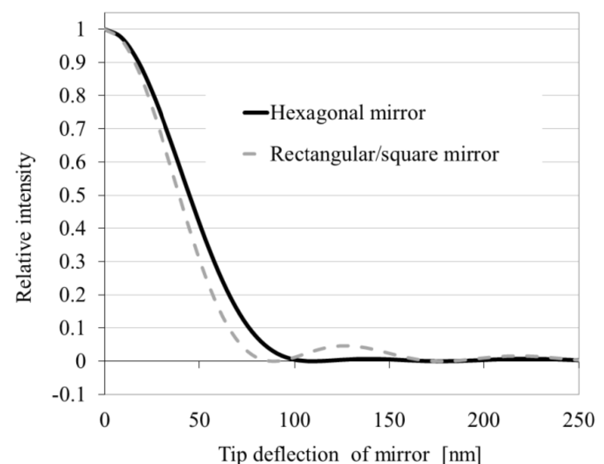

Figure 7: Intensity modulation characteristics for hexagonal and rectangular/square mirrors.

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3 SLM WAFER PROCESSING AND ASSEMBLY

The SLM has been fabricated in the MEMS pilot fabrication line of Fraunhofer IPMS, based on a technology developed for the monolithic integration of analog MMAs on CMOS in a "MEMS-last" technology-scheme using SiO2 as sacrificial layer. Figure 8 schematically illustrates the main steps of the process flow using a cross-section of the actuator (Figure 6) parallel to the springs and through the two yoke posts.

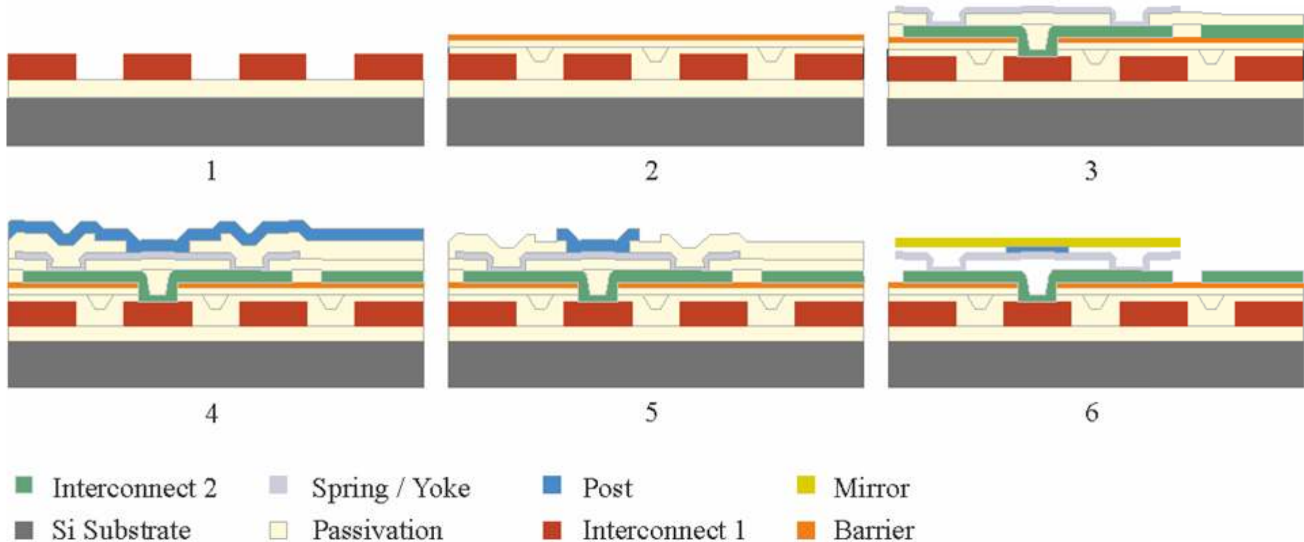

Figure 8: Schematic processing sequence of SLM

After growth of an insulating SiO2 film on the Si substrate, the first interconnect layer is deposited and patterned (1). The first interconnect layer is covered with SiO2 interlayer-dielectric (ILD) and planarized. On top of the ILD, an inert barrier layer (2) is deposited to protect the underneath SiO2 layers against attack of Hydrogen Fluoride gas used to finally remove SiO2 sacrificial layers. Vias down to interconnect 1 are formed, and interconnect layer 2 is deposited, patterned and planarized. The first sacrificial SiO2 layer is deposited, vias for the hinge posts are etched and the hinge metal is deposited and patterned (3). A second sacrificial SiO2 layer is deposited and vias for the mirror post are etched. The post material is deposited such that it completely fills the post via (4). The post material is removed anywhere, apart from the region next to the post (5). The wafer surface is planarized and the final thickness of the second sacrificial SiO2 layer, i.e. the distance between mirror and stoppers (not shown in Figure 8) is defined. At the same time the protruding mirror post and the sacrificial layer are leveled. Next, the mirror is deposited and patterned. The wafers are then diced to chips. The sacrificial SiO2 layers are removed by a Hydrogen Fluoride gas-phase etch, in order to release the actuators (6). Figure 9 shows an image of a completed product wafer just before dicing. Figure 10 is a differential interference contrast (DIC) microscopy image of the boundary of the pixel area. Individual pixels are just resolved, to maximize sensitivity of DIC to pre-deflection of mirrors. The image illustrates the extremely uniform deflection of non-addressed mirrors.

After the release etch, the SLM chip is glued to a highly planar ceramic carrier, which is then mounted to a metal plate. A metal holder for a quartz glass is mounted to the ceramic carrier. The quartz glass window is fitted into the aperture of the metal holder to protect the SLM against particle-contamination during further assembly and use.
Next, metal carrier plates for two multi-layer printed circuit boards are mounted. These "Fan-In-Adapter" boards (FIA) are then mounted to the carrier plates, such that bond pads on SLM and FIAs are aligned and leveled to each other. Bond pads on SLM and FIA boards are connected by 4 layers of fine-pitched wire bonds. Each FIA board holds connectors for 4096 data channels, the global voltages and test potentials. During a later use, flexible ribbon cables plugged into the FIA connectors establish the link to the digital-analog converter (DAC) boards of the data path unit controlling the SLM.
Figure 12 shows the wire bonded SLM-unit. The wire bond protection cap has been removed to enable an unobstructed view on the SLM.

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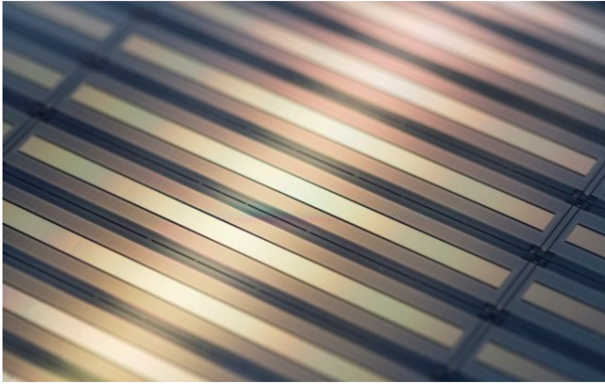

Figure 9: Image of completed product wafer

Figure 10: DIC microscopy image of pixel area after sacrificial layer etch. Minimal and homogeneous tilt of idle mirrors.

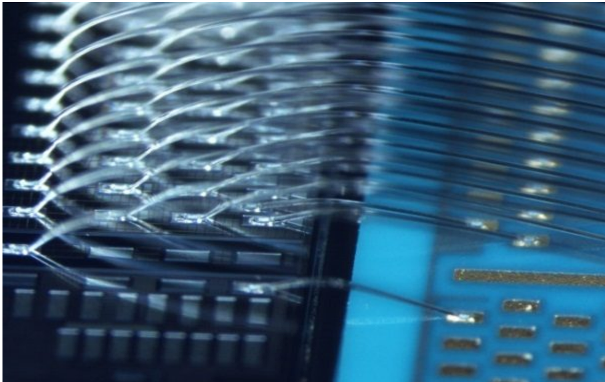

Figure 11: Close-up onto the wire bonds on one side of the SLM.

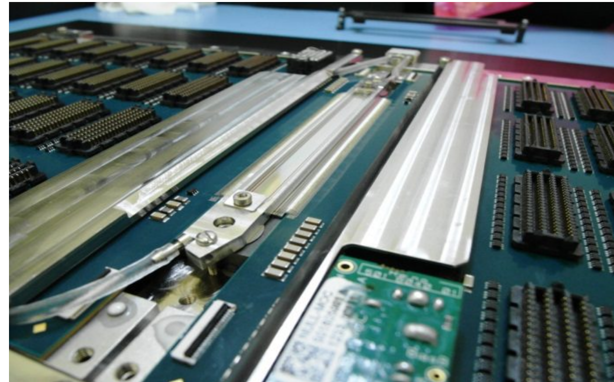

Figure 12: Close-up image of the assembled SLM unit showing the wire bonds connecting SLM and FIA boards.

4 SLM CHARACTERIZATION

4.1 Fundamental resonance of mirror tilt movement

For a current spring design the resonance frequency has been measured at ambient pressure using a MSV-300 Microscope Scanning Vibrometer (Polytec) by modulating the data-voltage with a rectangular voltage function. The resonance frequency has been determined to be higher than 1.3 MHz.

4.2 Planarity of chip within pixel area

An imperfect planarity of the SLM within the pixel area will lead to errors of the generated SLM image. The imaging system and software of an LDI system may compensate or correct for certain errors of SLM shape: e.g. a cylindrical bow of the MMA can be compensated by the imaging optics. Planarity specifications therefore have to be considered with respect to the specific imaging system. The planarity within the large pixel area is measured using a Wyko® NT9800 optical profiler. Single measurements covering an area of 1.2 mm x 1.6 mm sampled with 4.7 µm resolution are stitched together to cover the whole pixel area. Figure 13 shows a typical height map of the pixel area after subtraction of bow.

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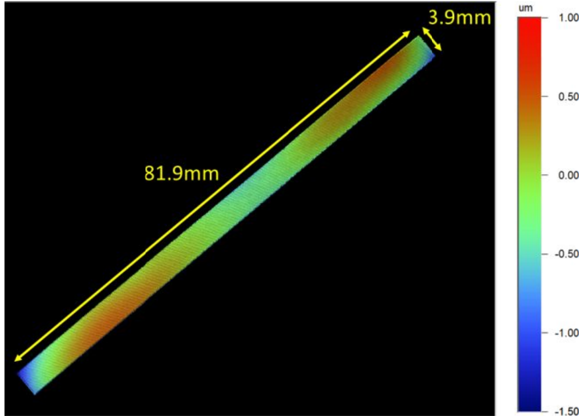

Figure 13: Planarity measurement of pixel area.

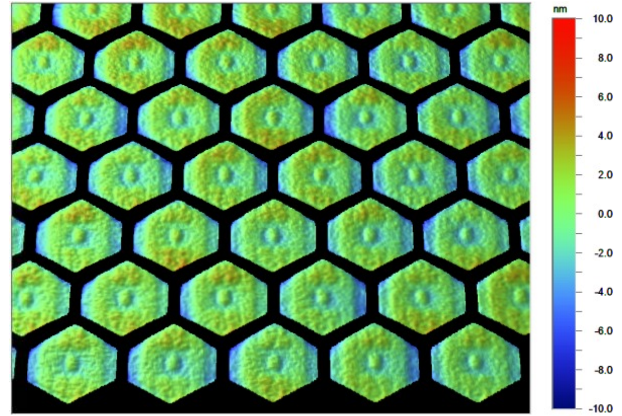

Figure 14: Surface planarity of released mirrors. RMS value 1.5±0.2nm

4.3 Mirror planarity

To obtain a sufficiently high contrast (here defined as ratio of "white" and "black" intensity), the planarity of mirrors must be kept within a narrow range (less than about 7 nm surface RMS). After removal of sacrificial layers the mirror planarity is measured using a Wyko® NT8000 optical profiler. An exemplary test using a control sample of 10 test-sites on 3 arbitrarily chosen wafers (in total 2416 mirrors) resulted in a mean RMS of 1.5±0.2nm, which is well within target range. Figure 14 shows a representative height map of mirrors.

4.4 Deflection characteristic

The deflection characteristic of micro mirrors is measured using a Wyko® NT9800 optical profiler. For that purpose the voltages of global electrodes (1 and 2 in Figure 6) are set to same absolute value but opposite polarity for all pixels. To deflect the mirrors, the voltage of the data-line connected to yoke/mirror and stoppers is varied. Figure 15 shows the resulting deflection response curve for different values of global voltage used as parameter. The target deflection for the "black state", 110 nm (according to Figure 7) is reached at a global voltage of 15.5 V and a data voltage of about 14.5 V.

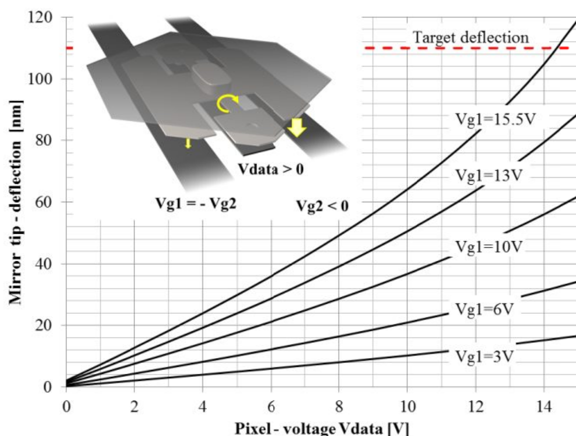

Figure 15: Mirror tip-deflection vs. data voltage

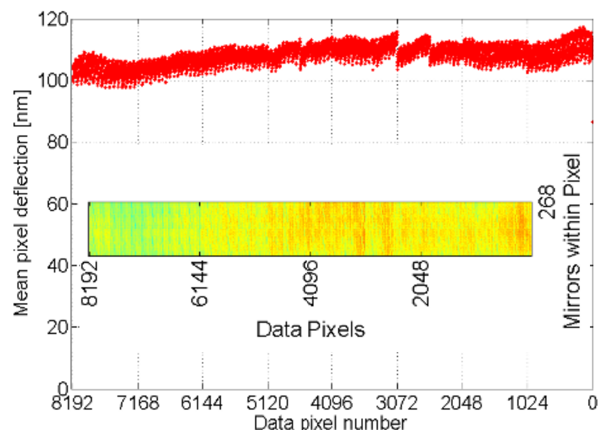

Figure 16: Full-matrix deflection test. The MMA is addressed with a common bias for all pixels. Plot of mean deflection vs. pixel number. Inset: Deflection map for all mirrors (same data set).

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Table 1: Summary of SLM parameters.

LDI SLM Parameter	Value
Chip dimensions [mm]	15 x 88
Dimensions of pixel area [mm]	4 x 82
Fill grade of active area [%]	> 90
Number of pixels	8192
Mirrors per pixel	268
Mirror shape	hexagonal
Mirror material	Al-alloy
Operating wavelength [nm]	355
Mirror reflectance at 355nm [%]	> 85
Max. mirror deflection [nm]	> 110
Pixel resonance frequency [MHz]	> 1.3
Achieved contrast	Up to 1000
Mirror RMS planarity [nm]	< 7

4.5 Deflection test of assembled SLM-unit

The functionality of the completely assembled and wire bonded SLM-units is verified by a deflection test using a Wyko® NT9800 optical profiler. Herein the SLM unit is addressed through the FIA boards to include FIAs and wire bonds in the test. All pixels are addressed with the same voltages to check for non-working pixels. The lateral resolution for the interferometric measurement is chosen such that the deflection amplitude of each individual mirror can be determined. The pixel area is covered by stitching a set of subsequent measurements.

Figure 16, a plot of mean pixel deflection vs. pixel number, illustrates a typical result. All pixels are functioning. Due to design-related systematic differences in the routing of data electrodes, the observed deflection values vary slightly with pixel number in a systematic way. Irregular features, like the one at pixel 3072, are attributed to small variations in hinge width caused by small tolerances of lithography.

Before the SLM is finally used in a LDI system, the mentioned systematic effects are compensated by a calibration procedure. After calibration for all individual pixels the voltages required to reach certain deflection values can be retrieved from look-up tables.

A two-dimensional representation of the same data, i.e. a map of deflection for each individual mirror of the SLM (inset in Figure 16) can be used to check for possible non-working mirrors and to retrieve their positions.

5 SLM PERFORMANCE IN LDI EXPOSURE SYSTEM

5.1 Description of exposure system

Figure 17 is a schematic of the LDI5sp system developed by Micronic Mydata AB. The coherent light source of the exposure system is a high-power, 355 nm diode-pumped solid state laser. The SLM is illuminated by the rectangular laser beam. Light reflected into the 0th diffraction order passes the aperture in the Fourier plane of the optical system, while the higher diffraction orders of the SLM are blocked. Behind the lens system, the beam is reflected via a rotating prism into one of four imaging arms rotating in synch with the prism before it is imaged onto the substrate.

During exposure the intensity modulated line focus is laterally scanned in an arc across the substrate panel, always keeping the same orientation similar to a windscreen wiper. After it has passed the panel edge, the laser beam hits the next facet of the prism and is directed into the next imaging arm to expose the next arc. Since at the same time the panel is steadily moved, subsequently exposed arcs are seamlessly stitched together until the whole panel has been exposed.

To maximize throughput, the twin table system aligns the next panel already while the preceding panel is being exposed. After exposure, the aligned panel is briefly flipped upwards to enable the passage and unloading of the already exposed panel. The tool exposes dry film resist on substrate panels with dimensions up to 510 x 612 mm^2 at a resolution better than 10 µm L/S.

The constant-speed operation of both rotor arms and panel stage contribute to a highly precise pattern placement. Feature edges can be smoothly shifted laterally utilizing the gray-leveling capability of the presented SLM. An adjustment of exposure dose is possible by tuning the speed of rotation for the imaging arms. Based on the high SLM modulation rate and high optical efficiency of the SLM, a high write speed and efficient use of laser power are achieved.

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5.2 Exposure results

Examples of patterned substrates are shown to illustrate the successful utilization of the presented SLM in Micronic Mydata's LDI5sp Laser Direct Imaging systems. Figure 18 shows a 15 µm high dry film resist on a copper seed layer patterned with 6 µm minimum line/space dimensions. Figure 19 shows a 25 µm high dry film resist on a copper seed layer structured with a pattern typical for the routing of interconnects around a pad. The minimum line/space dimensions in this image are 10 µm. Using the presented new SLM, contrast values (here defined as ratio of maximum and minimum intensity at the exposed substrate) of up to 1000 have been measured.

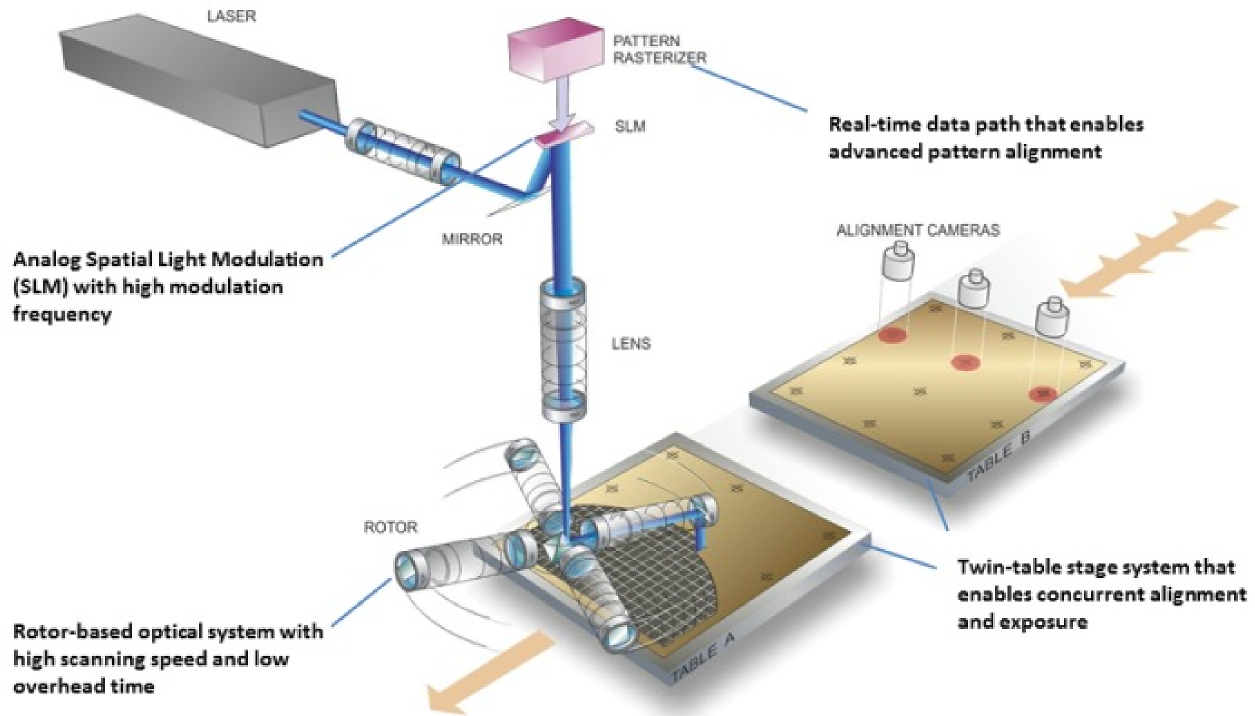

Figure 17: Schematic of Micronic Mydata's LDI5sp system

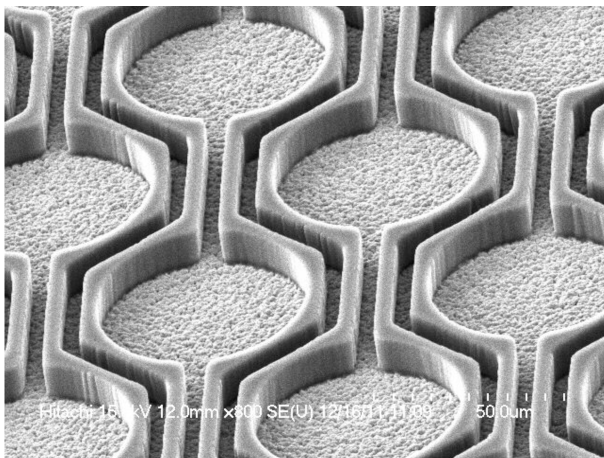

Figure 18: 15 um DFR on Cu seed layer, patterned with a micro-VIA interconnect test pattern. Minimum line/space feature size is 6 um.

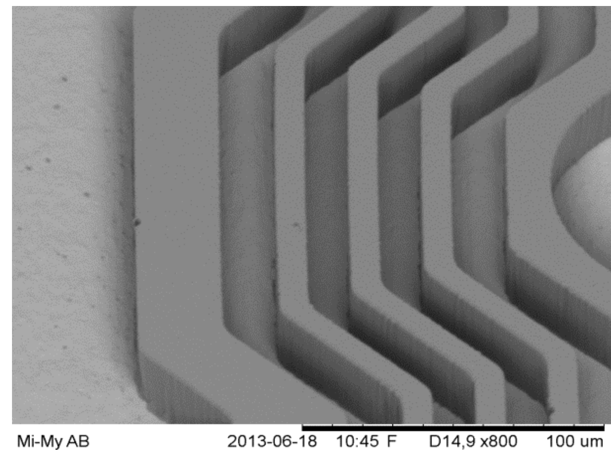

Figure 19: 25 um DFR on Cu seed layer, patterned with a structure typically used in the pad region of a substrate. Minimum line/space feature size is 10 µm.

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6 SUMMARY

Fraunhofer IPMS has developed a fast one-dimensional analog spatial light modulator (SLM) in collaboration with Micronic Mydata AB. The SLM supports a pixel rate of >10 billion grayscale-pixels per second and handles tens of Watt of laser power at a wavelength of 355 nm.

The SLM has successfully passed all performance tests and is now utilized in Micronic Mydata's novel LDI5sp series of Laser Direct Imaging systems optimized for the processing of advanced substrates for semiconductor packaging. A first Micronic-Mydata LDI5sp tool equipped with the IPMS-SLM has reached acceptance status at a final customer.

7 ACKNOWLEDGEMENTS

The authors wish to acknowledge Per Askebjer and Jarek Luberek for their valuable contributions to this development.

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