High Speed PFD with Charge Pump and Loop Filter for Low Jitter and Low Power PLL

[1]Kruti P. Thakore, [2]Harikrishna C. Parmar, [3]Dr.N.M. Devashrayee
[1]Dept. of EC, L.D.R.P. Institute of Technology, Gandhinagar, India
[2]Dept. of ECC, C.K.Pithawalla College of Engg. & Technology, Surat, Gujarat
[3]VLSI Design, EC Branch, Nirma University, Ahmedabad, Gujrat, India

Abstract
This paper presents a high speed phase frequency detector with charge pump and second order loop filter for low jitter and low power phase lock loop. The high speed phase frequency detector with dead zone compensation has been proposed. The paper contains the detailed circuit diagram of PFD, charge pump and loop filter with 1.2v power supply, 2ps jitter, and 1GHz input frequency, 22µwatt power dissipation. The design has been realized using .18um CMOS technology.

Keywords
Low Power, Low Jitter, PLL, PFD

I. Introduction

Low jitter and low power phase lock loop is becoming essential for portable and battery operated compact electronic devices, which decreases the risk of reliability problems. So power and jitter have been major big concern in circuit designs from last decade. In recent years, the design of low power and low jitter PLL for the different application has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power and reduction in jitter of new VLSI circuits.

The phase-locked loop (PLL) plays the versatile roles in the applications of clock generation, time synchronization and clock multiplication. A typical Phase Lock Loop block architecture is depicted [2]. Very basic block diagram of PLL is introduced in Fig. 1.It consists of a phase frequency detector (PFD), a charge pump, a loop filter, a voltage-controlled oscillator (VCO) and a frequency divider. [6,7,9] Each building block contributes to the PLL output timing jitter, [1] so improved circuit of phase frequency detector, charge pump and second order loop filter [8] is proposed in this paper for low jitter and low power PLL. Power and jitter are the main concern when designing the PLL. The average difference in time between the phases of the two signals when the PLL has achieved lock is called the static phase offset (steady-state phase error) and this variance is called jitter [10].

Power is also a limiting factor in VLSI integration for portable applications. The resulting heat dissipation also limits the feasible packaging and performance of the VLSI chip [5]. Since the dynamic power dissipation in synchronous digital integrated circuit is determined by CV2f, reducing the supply voltage is an effective way to reduce power [4].

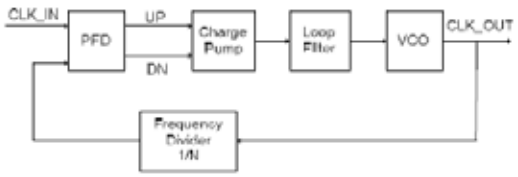

Fig. 1: Basic Block Diagram of PLL

The paper is organized as follows. Section II contains high speed phase frequency detector circuit with simulated results. Section III contains charge pump and loop filter with detailed circuit diagram and simulated output. Section IV contains the specification table with results. Section V concludes the best PFD with charge pump and loop filter for low jitter and low power PLL.

II. High speed pfd

The phase frequency detector, which is the first block of PLL, is very important for designing the PLL. In this paper the high speed phase frequency detector is presented instead of traditional phase frequency detector [3], which detects the phase and frequency difference between two inputs. High speed PFD detects both the edges of the PFD and so called the high speed PFD. PFD having two inputs – clock reference (clkref) and clock from voltage control oscillator (clkvco).Two outputs – UP signal and DWN signal. Input to the PFD is from the reference clock and second input is from the feedback signal coming from VCO. The outputs are connected to the charge pump to generate the related control signal for VCO.

Input to the PFD is from the reference clock which is the system clock or the processor clock. The range of the clock is normally mega hertz .The high speed PFD in this paper is operated at 1GHz frequency.

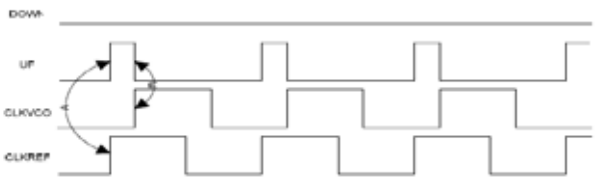

Fig. 2: Signal Transaction

From the fig. 2, signal transaction, when clkref signal is going high it will charge the upper D flip flop and resulting in changing the UP signal to high. Same for clkvco, when clkvco signal is going high it will result the DWN signal changing to high. This will result both the inputs of AND gate high and make the reset signal high to make both outputs low. It is known as the lock condition for the PFD when both the outputs of PFD – UP signal and DWN signal are low. When clkref is leading it will result the UP signal high as shown in fig. 1, same for clkvco result the DWN signal high. The width of the UP signal or DWN signal is the measure of error. With the use of this error the control voltage is generated and then that will correct out the frequency difference between input CLK and the clock coming from the VCO from feedback path of the PFD.

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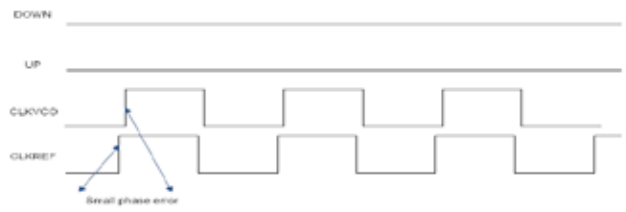

Fig. 3: Dead Zone

Fig. 3 shows the lock condition of the PFD with dead zone. Dead zone is due to small phase error, when both the input signals of PFD are very close to each other but output signals are not able to generate this error it will create the dead zone problem. Dead zone is due to the delay time of the logic components of digital circuit and the reset time that requires by the reset path to reset the flip flop of the PFD. Due to this dead zone problem at the out put jitter will create and the sensitivity of the PFD is affected.In this case the sensitivity of the means the smallest difference the PFD can detect and produce at the output UP or DOWN signal. This lead to the conclusion that the higher the sensitivity the better the PFD.

One of the disadvantages of the tradition PFD suffers is dead-zone. Dead-zone is a small difference in the phase of the inputs that a PFD will not be able to detect. Due to dead zone jitter will produce at the output. Traditional PFD has very big dead zone and so the jitter. The power consumption of the traditional PFD is quit high. So as a solution in this paper high speed PFD is used with lower jitter and power.

In the high speed PFD the feedback path is totally eliminated compared to traditional PFD. So improvement is possible with high speed PFD which is another way to reduce the power consumption and the jitter but addition of two invertors and NAND gates. The implementation of the high speed PFD with CMOS .18µm technology is as shown in the Fig. 4.The pre-simulated output of this high speed PFD is shown in Fig.5, 6, and 7. Pre-simulation is done with the MENTOR GRAPHIC TOOL. From the Fig. 5, the lock condition of the PFD, both the output signals UP and DWN signals are low.

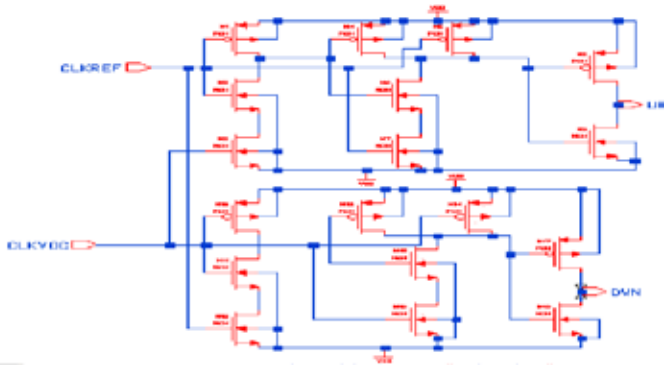

Fig. 4: Implementation of High Speed PFD

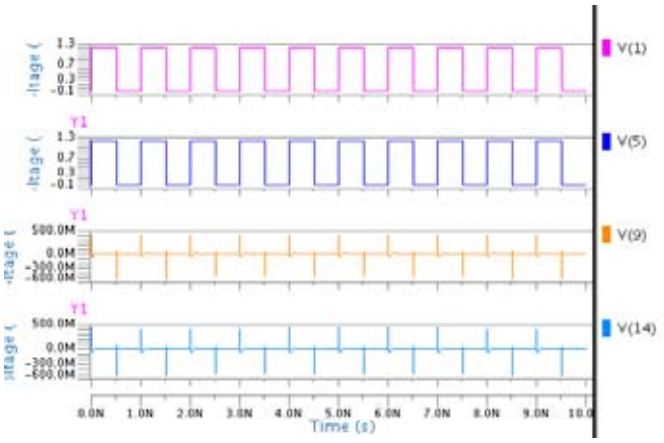

Fig. 5: High Speed PFD at 1GHz (Lock Condition)

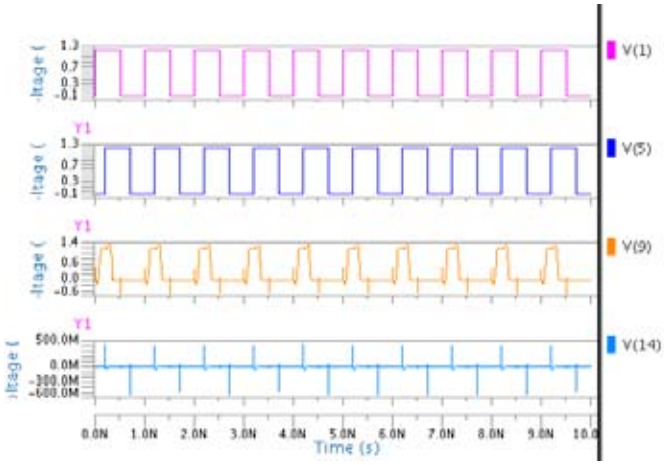

Fig. 6: High Speed PFD at 1GHz (Clkref leading)

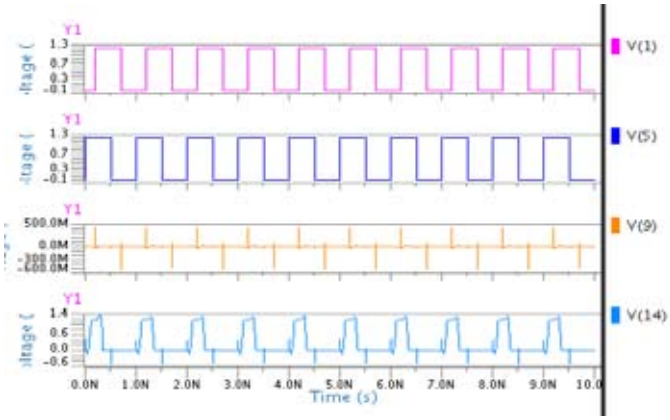

Fig. 7: High Speed PFD at 1GHz (Clkvco leading)

From the pre - simulated results as shown in Fig. 6 and 7 the clkref leading condition and the clkvco leading condition, the pulse width of the UP signal or DWN signal shows the relative value of the error generated between two inputs of the PFD. This error value is applied to the charge pump.

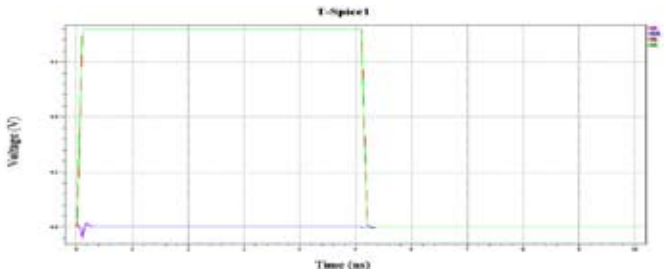

Fig. 8: Dead Zone of High Speed PFD

As shown in Fig. 8 , the dead zone of the high speed PFD is only 2 ps and the power consumption is only .87nw. so the dead zone is approximately zero and very small power consumption. So this is the best candidate for the PLL for low power and low jitter PLL.
Now in this paper with the same PFD, high speed PFD the charge pump and loop filter are connected with the same input frequency of 1 GHz.

III. Charge pump with loop filter

Charge pump and the loop filter both the blocks are working together to generate control voltage for VCO. This control voltage will adjust the output frequency of the VCO.

A. Charge pump

Charge pump is the next block to the phase frequency detector. The output signals - UP signal and DWN signal generated by the PFD is directly connected to the charge pump.
The main purpose of a charge pump is to convert the logic states of the phase frequency detector into analog signals suitable to control the voltage-controlled oscillator (VCO). Basically, the charge pump consists of current sources and switches. The output of the charge pump is connected to a low pass filter that integrates the charge pump output current to an equivalent VCO control voltage (Vcntl).

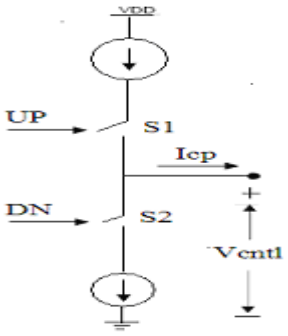

Fig. 9: Basic Block Diagram of Charge Pump

Three states in the charge pump correspond to its output to the loop filter:
State 1: Charging current: +ICP
State 2: Discharging current: -ICP
State 3: Zero current
As mentioned earlier, the PFD needs to produce a certain amount of pulse width of the UP and DN signal in the beginning of the period. In this condition, ideal charge pump will give zero current which is state 3 since the charging current is equal to the discharging current.
When the VCO output frequency is leading the reference frequency, the PFD will activate the DOWN signal and deactivate the UP signal. Hence, switch S_1 will be opened and switch S_2 will be closed. This time, current ICP will flow out from the filter and reduce the Vcnt. Consequently, the VCO output frequency is decreases.
The lock condition of the PLL is established when the VCO output frequency is the same as the reference frequency. During this period, the PFD will deactivate both up and down signals. Hence switches S_1 and S_2 will be opened until the VCO output frequency changes. Since switches are open, there is no current path formation, hence no current will flow into or out from the filter.

UP signal	DN signal	Condition	Note
1	0	Charging	Icp flows into filter
0	1	Discharging	Icp flows out from filter
0	0	V_{cntl} constant	Icp = 0
1	1	V_{cntl} constant	Icp ≠ 0

Fig. 10: Operation of Ideal Charge Pump

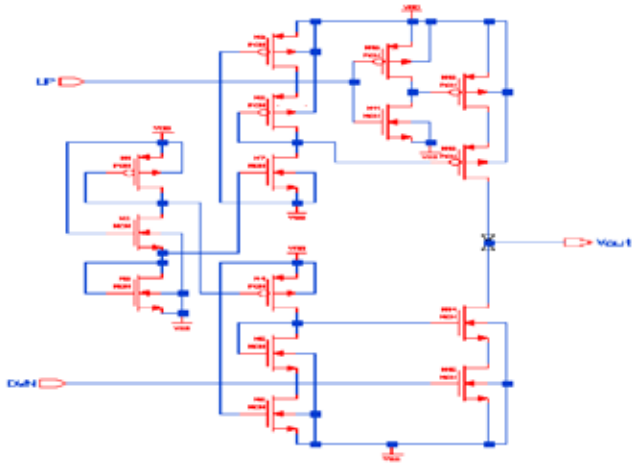

Fig. 11: Implementation of Charge Pump

Implementation of charge pump is with the .18 um CMOS technology it can be observed in Fig. 11. The overall operation of the charge pump can be observed in Fig. 12, which is the ideal behavior of the charge pump. It shows both the conditions of the charge pump. It charges or discharges the current of the charge pump related to the value of the error signal (pulse width of the UP signal or DWN signal) generated by the PFD.

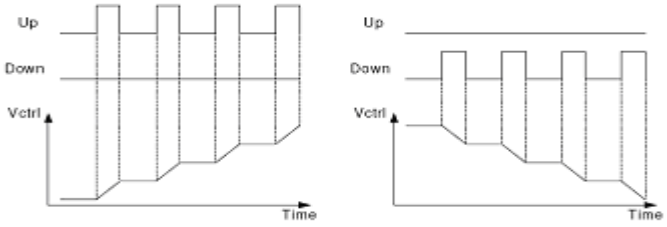

Fig. 12: Ideal Behavior of Charge Pump

B. Loop filter

A second order low pass filter is used as Loop filter. The main function of the loop filter is to convert the current coming form charge pump to control voltage that is directly connected to VCO to control the frequency of VCO.
The inclusion of a loop filter at the output of the Charge Pump

serves two functions. First, the loop filter integrates the pulses to produce a time-average, or continuous value. Second, it defines the loop bandwidth, which in turn affects the capture range, jitter and bandwidth. The dynamic characteristics of the phase-locked loop are therefore governed principally by the loop filter. Therefore, choosing the best loop filter is a critical step in a PLL design.

Furthermore, the loop filter values should be chosen to optimize the overall loop performance instead of a particular characteristic. For example, the output jitter is reduced to some extent by decreasing the loop bandwidth. This, however, reduces speed of the response.

The first-order loop filter design consists of a single resistor and capacitor. This filter can also be constructed by only a capacitor which will add only a pole in the transfer function. Adding a resistor in series with the capacitor will add a zero in transfer function. This will enhance the stability of the system.

The first-order loop filter does not have a second capacitor to smooth out current spikes. The second-order loop filter has the second capacitor to smooth out current spikes. This type of filter has two poles one at low frequency and one have high frequency and a zero which will add the stability of the system.

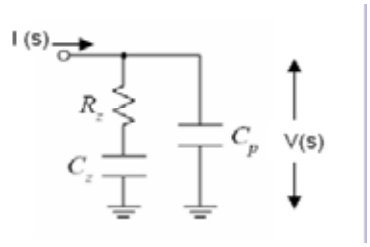

Fig. 13: Second Order Loop Filter

Here in this paper second order loop filter is shown in Fig. 13. In this paper the value of capacitor Cp is 5 times less than capacitor Cz. The range of resister is MEGA OHMS and capacitor is PICO FERADE. At the output of loop filter the generated voltage is connected to the voltage control oscillator that is used to control the output frequency of the VCO.

Total simulation from high speed phase frequency detector to loop filter is shown in Fig. 14. Pre simulation with the use of MENTOR GAFIC TOOL is at 1.2v, 1GHz frequency and .18um CMOS technology.

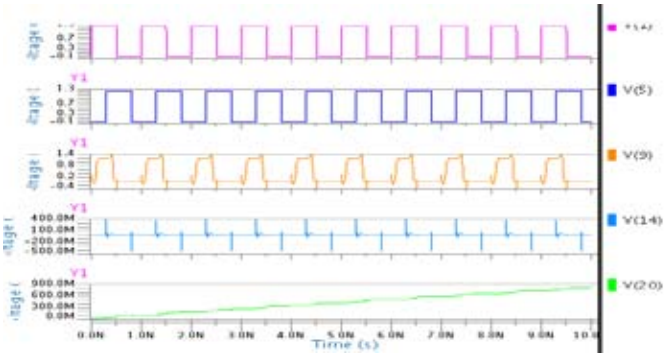

Fig. 14: Simulated output of PFD with Charge Pump and Loop Filter

IV. Results with specification table

Results generated by charge pump

Icp = 18.6μamp

Gain of Charge Pump –

Kcp = Icp/2Π A/rad

= 18.6μamp / 2Π

= 2.96 A/rad

Table 1: Results generated by the charge pump and loop filter

UP signal	DWN signal	Vcnt
0	0	10mv
0	1	-90mv
1	0	90mv
1	1	20.5mv

Table 2: Specification of PFD, Charge pump and Loop filter

Input frequency	1 GHz
VDD	1.2V
VSS	0V
Output Jitter	2ps
Power dissipation	22μwatt
Technology	.18um

V. Conclusions

A high speed phase frequency detector , charge pump and second order low pass filter as loop filter is designed with 0.18μm CMOS technology , 1.2v power supply and 1GHz input frequency. The jitter of the proposed design is reduced only to 2ps and the total power consumption of the circuit is 22μwatt.

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Kruti P. Thakore received her B.E. Degree in electronics and communication engineering from North Gujarat University. She is pursuing her M.Tech. Degree in VLSI Design-EC Engineering from Nirma University, Ahmedabad. Currently she is Assistant Professor in electronics and communication engineering department at LDRP Institute of Technology collage, Gandhinagar, Gujarat, India.

Harikrishna C. Parmar received his B.E. degree in Electronics & Communication engineering from south Gujarat university. He is pursuing his M.Tech.Degree in VLSI design – EC engineering from Nirma University, Ahmedabad. Currently he is Assistant professor in electronics and communication engineering department at C.K. Pithawalla College of engg. and technology. Surat, Gujarat, India.

Dr. N. M. Devashrayee is currently P.G. Co-ordinator for VLSI design course and an associate professor in department of electronics & communication engineering at the institute of technology, Nirma University, Ahmedabad. Earlier he has served as a senior scientist at central electronics engineering research institute (CEERI), Pilani which is a pioneer research institute in the country. He holds his Ph.D. Degree in VLSI design. His research interests include IC fabrication and VLSI Testing.