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High-temperature characterisation and analysis of leakage-current-compensated, low-power bandgap temperature sensors

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Abstract This paper analyses leakage current compensation techniques for low-power, bandgap temperature sensors. Experiments are conducted for circuits that compensate for collector-substrate, collector-base, body-drain and source-body leakage currents in a Brokaw bandgap sensor. The sensors are characterised and their failure modes are analysed at temperatures from 60 to 230 °C. It is found that the most appropriate compensation circuit depends on the accuracy requirements of the application and on whether a stable reference voltage is required by other parts of the circuit. Experiments show that the power consumption is dominated by leakage current at high temperatures. One type of sensor was seen to consume 260 nW at 60 °C, 2.1 µW at 200 °C and 14 µW at 230 °C. This work is motivated by the need to accurately monitor the temperature of power semiconductors in order to predict emerging faults in power semiconductor modules, a task for which cheap, single-chip, low-power, high-temperature, wireless bandgap temperature sensors are appropriate.

Keywords Bandgap · Condition monitoring · High temperature · Leakage current · Low power · Power semiconductor · Temperature sensor · Voltage reference

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1 Introduction

High-temperature sensors are used in power electronic equipment to monitor the temperature of power semiconductors [17], and their use in this area is the main motivation behind this work. The ageing of the solder interface between power semiconductor and cooling baseplate causes an increase in operating temperature of the device over time and can eventually result in the device's destruction [4]. If a temperature rise can be detected before a device fault occurs, preventive maintenance can be performed, and catastrophic failure can be avoided.

Systems that measure the temperature of power semiconductors by using direct-contact sensors are not known by the authors to exist, but would provide advantages in terms of accuracy and portability between modules [7]. This work aims to enable the manufacturing of such a system by demonstrating a low-power integrated circuit (IC) temperature sensor that is able to operate up to at least 230 °C.

Low-power, high-temperature sensors can be used in conjunction with on-chip coils for power transfer to monitor the temperature of power semiconductors [8]. The concept is illustrated in Fig. 1. Here, the temperature sensors are glued in direct contact with the power semiconductors to provide accurate measurements while being galvanically isolated from the main measurement system, as communication and power supply are implemented wirelessly through radio-frequency identification (RFID) technology.

One challenge in designing low-power, high-temperature bandgap temperature sensors is the exponential increase in leakage current with increasing temperature [7]. These leakage currents arise in reverse-biased p-n junctions [15]. Unless compensated for, this effect will set the upper operating temperature limit of a sensor.

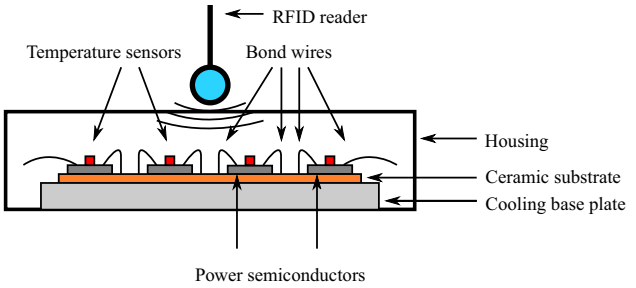

Fig. 1 Schematic view of the cross-section of a wire-bond power semiconductor module whose devices are being monitored by single-chip temperature sensors powered by a nearby RFID reader [8]

This paper presents high-temperature characterisations of low-power temperature sensors by providing and analysing measured data of manufactured ICs in a 0.18 µm p-substrate CMOS process with vertical bipolar junction transistors (BJTs). The sensors are Brokaw bandgap temperature sensors with collector-substrate (CS) leakage current compensation from [11] for bipolar transistors. We also include circuitry for collector-base (CB) leakage current compensation as well as for body-drain (BD) and source-body (SB) leakage current compensation for metal-oxide semiconductor field effect transistors (MOSFETs). In these circuits, the NMOS and PMOS bodies are p-wells and n-wells connected to ground and supply voltage, respectively. Experiments are performed for temperatures up to 230 °C to characterise circuits with no leakage current compensation circuitry, with the compensation circuit found in [11] (previously characterised up to 175 °C) and with said compensation circuit plus the compensation circuit demonstrated in [7], which has previously only been characterised through simulation up to 175 °C.

The experiments show that the use of CB/BD/SB leakage current compensation circuits enable operation up to at least 230 °C. They further show that many of the sensors that do not use this type of compensation circuit fail at temperatures around 200 to 210 °C.

In Sect. 2, we present a survey of previous work on leakage current compensation techniques for bandgap circuits as well as the theory behind the sensor presented in this work. In Sect. 3, the experimental set-up is described, with the experimental results presented in Sect. 4. Section 5 presents a discussion of the results and compares them to the results of other works. Conclusions are presented in Sect. 6.

2 Low-power bandgap temperature sensors

The Brokaw bandgap reference [3] is commonly used to measure temperatures. One implementation is depicted in Fig. 2. The basic idea is that the base-emitter (BE) voltage, V_{BE}, of a BJT has a negative temperature coefficient, whereas the difference in voltage between a larger and smaller BJT, ΔV_{BE}, has a positive temperature coefficient and is thus proportional to absolute temperature (PTAT). V_{BE} is given in [5] as

$$V_{BE} = V_{G0} - c_T T + VNL(T). \quad (1)$$

Here, $V_{G0} \approx 1.2\,\text{V}$ is the extrapolated bandgap voltage at 0 K, c_T is a constant temperature coefficient, T is the temperature, and $VNL(T)$ represents temperature-dependent, non-linear terms. In this work, we ignore $VNL(T)$ because it is insignificant considering our desired accuracy and substantially smaller than the errors introduced due to leakage at high temperatures.

By summing and scaling ΔV_{BE} and V_{BE}, two new voltages are generated; one voltage that is constant over temperature, $VREF$, and one that is PTAT, $VPTAT$. The ratio of these voltages, $VPTAT/VREF$, can be used in conjunction with an analog-to-digital converter (ADC) to obtain temperature measurements.

2.1 Operation of the Brokaw bandgap reference

Ignoring the effects of Q_3 for now, the circuit of Fig. 2 operates by having the current mirror M_1–M_2 force equal collector currents I_{C1} and I_{C2} through Q_1 and Q_2 using the common source transistor M_3 to feedback an error signal into the bases of Q_1 and Q_2.

Because Q_1 and Q_2 differ in size and carry equal collector currents, they are biased at different current densities, and thus, a voltage ΔV_{BE} develops across their emitters, that is, over R_1. Because ΔV_{BE} is PTAT, the current through R_1, I_{E2}, will be PTAT. Assuming equal emitter currents, $I_{E1} = I_{E2} = I_E$, the current through R_2 ($2I_E$) will also be PTAT, and therefore $VPTAT$ will be

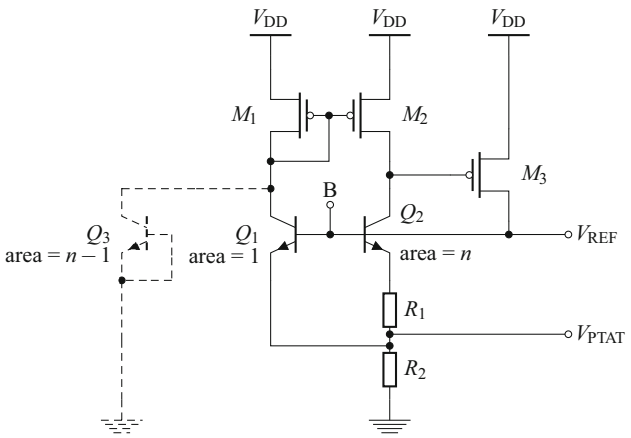

Fig. 2 Brokaw bandgap reference circuit as implemented in [11]. For simplicity, the start-up circuit is shown sepearately in Fig. 3 and is connected to this circuit through their common node B

PTAT. The voltage $VREF$ will be the sum of $VPTAT$ and the base-emitter voltage of Q_1, V_{BE1}. Thus, scaling the ratio of R_2/R_1 appropriately makes $VREF$ independent of temperature and equal to V_{G0} because the first-order temperature-dependent terms are cancelled.

An expression for $VPTAT$ is given in [3] as

$$VPTAT = 2\frac{R_2}{R_1}\frac{kT}{q}\ln\frac{J_{C1}}{J_{C2}}, \tag{2}$$

where k is Boltzmann's constant, T is the temperature and J_{C1} and J_{C2} are the respective collector current densities of Q_1 and Q_2. If $I_{C1} = I_{C2}$, we can write

$$VPTAT = 2\frac{R_2}{R_1}\frac{kT}{q}\ln\left(n\frac{I_{C1}}{I_{C2}}\right), \tag{3}$$

where n is the area ratio between transistors Q_2 and Q_1.

To avoid the operating point at which no current flows through Q_1 and Q_2, a start-up circuit must be introduced. This circuit is shown in Fig. 3 and is connected to the circuit of Fig. 2 through their common node B. It operates by having the pull-up network M_{S3}–M_{S4} turn M_{S2} on unless there is a voltage $VREF$ at node B to turn M_{S1} on, which then in turn drives M_{S2} off. This arrangement enforces a non-zero voltage, $VREF$ at node B.

2.2 Effects of collector-substrate leakage current in bandgap circuits

Leakage current poses a challenge in high-temperature IC design [15]. Figure 4 shows an extended version of the schematic in Fig. 2, where major sources of leakage current due to reverse-biased p-n junctions are shown and indicated as current sources. In this figure, CS leakage occurs in Q_1, Q_2 and Q_3. Because leakage current in reverse-biased p-n junctions increases exponentially with increasing temperature [14], at high temperatures, the leakage currents of a low-power bandgap temperature sensor become significant as their magnitudes become comparable to that of the sensor's quiescent current. One aspect of how leakage current adversely affects bandgap circuits has been studied by Radoiaş et al. [10, 11]. They found that, at high

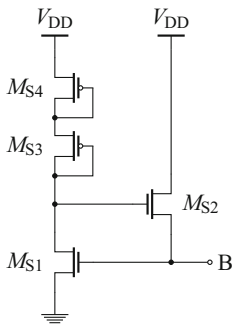

Fig. 3 Start-up circuit for the Brokaw bandgap circuit of Fig. 2. This circuit is connected to the bandgap circuit through their common node B

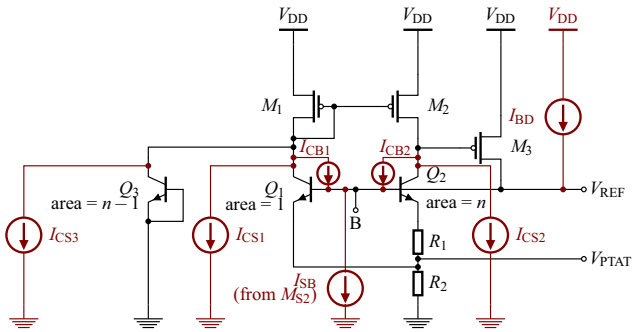

Fig. 4 Brokaw bandgap circuit with leakage current caused by reverse-biased p-n junctions represented as current sources. The subscripts CS, CB, BD and SB indicate CS, CB, BD and SB leakage current, respectively

temperatures, CS leakage in the main bipolar pair causes the collector currents I_{C1} and I_{C2} to become mismatched due to differing sizes of the respective transistors.

The source-drain currents of M_1 and M_2 are the sum of their respective associated collector currents, I_{C1} and I_{C2}, and leakage currents, I_{CS1} and I_{CS2}, being drawn from the collectors of Q_1 and Q_2. Because Q_2 is larger than Q_1, $I_{CS2} > I_{CS1}$. The current mirror M_1-M_2 and the feedback loop through M_3 will keep $I_{C1} + I_{CS1} = I_{C2} + I_{CS2}$, by increasing the drain current of M_3, I_{D3}, supplied to the bases of Q_1 and Q_2. As the BE junction of Q_1 has a lower impedance than that of Q_2, I_{C1} will increase more than I_{C2}. Thus, taking leakage currents into account, the ratio I_{C1}/I_{C2} increases.

It can be seen from Eq. (3) that $VPTAT$ will increase from an increase in collector current ratio, I_{C1}/I_{C2}. This increase will also be seen in $VREF$ because $VREF$ is the sum of $VPTAT$ and V_{BE1}. Thus, at high temperatures, $VPTAT/VREF$ increases beyond the level predicted if leakage current is not considered.

When the temperature, and hence CS leakage currents, become large enough, the collector voltages of Q_1 and Q_2 decrease and eventually the CB junctions of Q_1 and Q_2 become forward-biased. This causes a part of I_{D3} to go through the CB junctions of Q_1 and Q_2, reducing the current through their BE junctions. Thus, I_{C1} and I_{C2} are reduced, effectively reducing $VPTAT$ and $VREF$. At sufficiently high temperatures, this effect prevents the circuit from operating as a bandgap reference, thus disabling its ability to function as a temperature sensor.

Radoiaş et al. compensated for unequal CS leakage by introducing another transistor in cut-off mode with a size equal to the difference in size between the main bipolar pair, Q_1 and Q_2 [11]. This new transistor is Q_3 in Fig. 2. The sole purpose of this transistor is to ensure that CS leakage currents in both half circuits are matched, therein keeping collector currents equal even at high temperatures and thus compensating for the non-linearities arising from CS leakage.

Note that Radoiaş et al. connected the emitter and base of Q_3 to $VPTAT$ [11]. In contrast, in this work, we connect it to ground to avoid introducing non-linearities in $VPTAT$ (and subsequently in $VREF$) caused by the CB leakage of Q_3.

2.3 Effects of collector-base, body-drain and source-body leakage current in bandgap circuits

Excess current introduced in the bases of the bipolar pair, node B in Fig. 2, may adversely affect circuit operation, especially for low-power circuits [7]. Such an excess current arises at high temperatures due to CB, BD or SB leakage introduced by reverse-biased p-n junctions in Q_1, Q_2, M_3 and M_{S2}, see Figs. 3 and 4. In these figures, CB leakage occurs in Q_1, Q_2, and Q_3; BD leakage occurs in M_3, while SB leakage occurs in M_{S2}. Note that M_{S2} is leaking current out of node B, while the other leakages are leaking current into node B. However, summing all leakages from/to node B results in a net outflow of current from the node because the leaking junction area of the bipolar transistors are significantly bigger than that of M_{S2}.

Because Q_1 is biased at a higher current density than is Q_2 and has no series resistor, the majority of excess current injected in node B will take the path through the BE junction of Q_1, be amplified by Q_1 and mirrored by the current mirror M_1–M_2. The gate voltage of M_3 will increase, whereby the current from M_3 supplied to node B will be reduced, counteracting the initially introduced current. However, if the loop gain of the M_1–M_2–M_3 feedback loop is low, non-negligible current imbalance between Q_1 and Q_2 will remain. Such an imbalance introduces non-linearities with respect to temperature in $VREF$ and $VPTAT$. Because the CB junction of Q_3 is biased at a higher reverse voltage than are Q_1 and Q_2, the magnitude of its CB leakage current is slightly higher than that of Q_1 and Q_2. Thus, M_3 will subtract more current than are added in the form of CB/BD/SB leakage. At sufficiently high temperatures, M_3 will be turned completely off, whereas $VREF$ and $VPTAT$ will only be driven by leakage current, thus dropping to very low voltages.

Because CB/BD/SB leakage limits the high temperature range in which a bandgap sensor can operate, it is desirable to compensate for such leakage. Such compensation can be realised by adding artificial leakage sources in the form of transistors in cut-off with dimensions identical to that of the leaking transistors. This leakage can then be mirrored so that equal amounts of leakage is leaking into a node as is leaking out of it. Mizuno *et al* demonstrated such a compensation circuit in [6]. Because the direction of net leakage current in the Mizuno circuit (towards ground) is different from that in this work (towards supply), a modified circuit was presented in our previous work [7] and further extended in this work to compensate for one additional leaking transistor, M_{S2}. This circuit is presented in Fig. 5. Here, sources of artificial leakage are generated by Q_1', Q_1'', Q_2', Q_2'', M_3' and M_{S2}' operating in cut-off, while the current mirror consists of M_{C1}, M_{C2}, M_{C3}, M_{C4} and M_{C5}. See [6] for details of how this circuit operates. A discussion of failure modes for the circuits of Figs. 4 and 5 is presented in Sect. 4.1.

2.4 Matching of leakage currents

The success of leakage current compensation techniques are highly dependent on the matching that can be achieved between the compensated and the compensating device. In their work, Mizuno *et al* have demonstrated matching of leakage currents with an error of 5% [6]. This increased the temperature operating range by 20 °C compared to using a simple current mirror as compensation circuit, by 40 °C compared to using a diode directly and by 60 °C compared to not using any leakage current compensation at all.

Because we use the same underlying compensation technique in this work for CB/BD/SB leakage current compensation, we expect a similar level of matching. Thus, we also expect the failure mechanisms involving by CB/BD/SB leakage to be shifted up in temperature by approximately 60 °C.

2.5 Power consumption of low-power, high-temperature bandgap sensors

The power consumption, P, of a Brokaw bandgap reference with the two leakage current compensation circuits

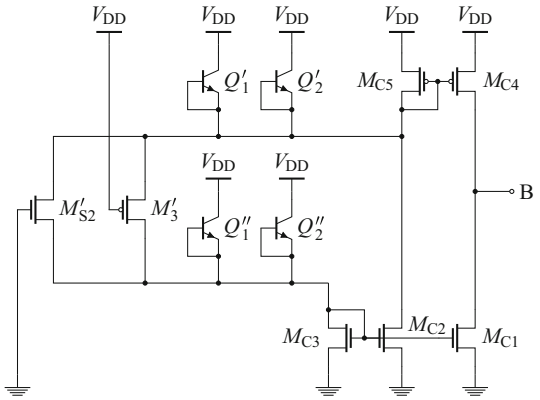

Fig. 5 Leakage current compensation circuit connected to the Brokaw bandgap circuit of Fig. 2. The prim/bis notation denotes devices with identical dimensions as similarly named devices from the Brokaw bandgap circuit depicted in Fig. 2. M_{C1}, M_{C2}, M_{C3}, M_{C4} and M_{C5}, all have a width of 2 µm and a length of 360 nm. This circuit has been designed for a nominal supply voltage of $V_{DD} = 2.0$V. The only currents flowing in the circuit are leakage current and compensation current (mirrored leakage current). The circuit is based on the work of Mizuno et al. [6]

described earlier in this section consists of two temperature-dependent components; a linear part, due to bias current, and an exponential part, due to leakage current [7]. The power consumption can be written as

$$P = c_1 T + c_2 e^{b_2 T}, \quad (4)$$

where T is the temperature and c_1, c_2 and b_2 are linear and exponential temperature coefficients.

At low temperatures, the magnitudes of leakage currents are small and the linear part will dominate. At higher temperatures, the exponential part becomes significant and rapidly becomes the dominant term in the expression for the power consumption. Thus, there is a limit below which a reduction in bias current is not effective for reducing the power consumption at high temperatures where the exponential term is dominant.

3 Experiments

To assess the contribution of each compensation technique presented in Sect. 2, measurements were performed on three types of bandgap sensors:

- Type 0: With no leakage current compensation; that is, the circuit of Fig. 2 excluding Q_3.
- Type R: With the leakage current compensation circuit of Radioaş *et al* [11]; that is, the circuit of Fig. 2 including Q_3.
- Type RN: With the leakage current compensation circuit of Radioaş *et al* [11] and the leakage current compensation circuit of Nilsson et al. [7]; that is, the circuit of Fig. 2 including Q_3 with the circuit of Fig. 5 connected to it (node B to node B).

Because of the high operating temperatures and relatively high output impedance of $VREF$ and $VPTAT$, bootstrapped guard rings [1] were implemented on the printed circuit board (PCB) where the device under test was bonded, and polytetrafluoroethylene-insulated (PTFE) wires were used for connecting this board to the remainder of the measurement set-up. The guard rings were implemented because surface leakage currents in the PCB were observed at high temperatures. Driving a guard ring to the same potential as that of the trace which it surrounds minimises this leakage. For each measurement the temperature was required to remain within $\pm 1\,^{\circ}\mathrm{C}$ (as measured using a Pt100 resistance thermometer) for 90 s, after which 50 measurements were taken. Because of problems with tuning the oven temperature regulator at high temperatures, several devices were damaged by epoxy leaking from the PCB, thus limiting the number of samples that could be fully characterised.

4 Measurement results

A batch of 2.25 mm^2 chips containing Type 0, Type R and Type RN circuits were manufactured in a 0.18 µm CMOS process with vertical npn BJTs. The dimensions used for the transistors are specified in Table 1. Temperature sweeps were performed on each type of circuit, and data for all the sweeps of $VREF$ and $VPTAT$ for the different types of circuits is presented in Fig. 6. Due to the difficulties encountered during the characterisations (as described in Sect. 3), we were only able to successfully complete temperature sweeps on 3 different Type 0 circuits, 5 different Type R circuits and 5 different Type RN circuits. Due to the limited sample size, we do not present standard deviations for the measured data.

Different properties of the different types of compensation circuits are analysed in the remainder of this section. Unless otherwise noted, the presented data is for a supply voltage V_{DD} of 2.0 V.

4.1 Failure modes

From Fig. 6(a) it can be seen that the failure mode for Type 0 circuits follows the theory presented in Sect. 2.2. At moderately high temperatures both $VREF$ and $VPTAT$ increase, whereas at higher temperatures, they rapidly decrease to very low values.

For Type R circuits, it can be seen from Fig. 6(b) that for most circuits $VREF$ and $VPTAT$ become very low voltages at high temperatures. This is in agreement with the theory presented in Sect. 2.3. When M_3 is turned off, $VREF$ is reduced to the point at which it triggers the start-up circuit of Fig. 3. Because the start-up circuit is triggered at the threshold voltage of M_{S1}, $VREF$ attains the value of said threshold voltage and because threshold voltage

Table 1 Dimensions of transistors from the circuits of Figs. 2, 3 and 5 for a 0.18 µm design

Device		
MOSFETs	Width (nm)	Length (nm)
M_1, M_2	2000	360
M_3	2000	720
M_{S1}, M_{S2}	2000	360
M_{S3}, M_{S4}	220	20000
M_{C1}, M_{C2}, M_{C3}, M_{C4}, M_{C5}	2000	3600
BJTs	Emitter area (µm^2)	
Q_1	6.8 (1 device)	
Q_2	40.8 (6 devices)	
Q_3	34.0 (5 devices)	

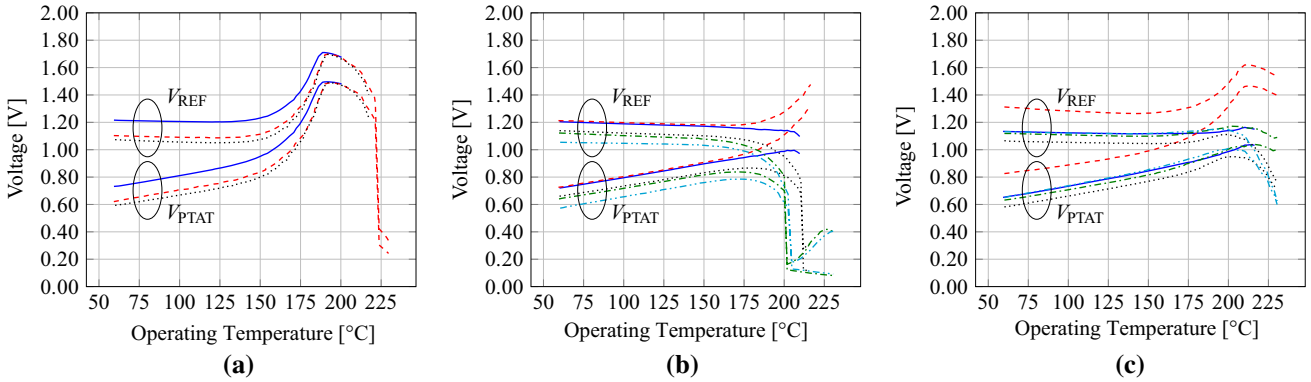

Fig. 6 Measurement results of *VREF* and *VPTAT* as functions of temperature for different types of leakage current compensation circuits. Each *plot* contains data from multiple temperature sweeps from different chips. *Identical line* styles in a plot indicate voltages from the same chip. **a** Type 0. **b** Type R. **c** Type RN

decreases with temperature [15], *VREF* also decreases with temperature.

As *VREF* decreases in Type R circuits, it can be seen from Fig. 6(b) that *VPTAT* starts to increase beyond *VREF*. Because *VPTAT* is larger than *VREF* it can no longer be driven by *VREF*. Thus, the current through R_2 must come from another place than node B. Looking at the circuit of Fig. 2, it can be seen that the current can only come from one or both of the bipolar transistors, Q_1 and Q_2. One feasible explanation for this behaviour is collector-emitter (CE) leakage current from pipe formation or surface inversion in the base [2]. Although surface inversion in bipolar devices is uncommon in modern processes, a reduced threshold voltage due to the unusually high operating temperature of the devices under test might trigger the phenomenon. Another source of CE leakage could be minority holes from the CB junction diffusing over to the BE junction instead of exiting through the base. This effect would be more prominent when the BE junction is reverse-biased, which it is at this operating point, because a reverse biased BE junction would decrease the effective base width. For the two temperature sweeps on Type R circuits where this effect could be observed, around 450 nA was seen to run through R_2 at 225 °C.

One exception to the behaviour discussed above is the red, dashed line of Fig. 6(b). Here, *VREF* and *VPTAT* increase instead. One explanation for this deviation from the theory could be that for that particular circuit, a mismatch in the bipolar transistors occurred so that the left half-circuit of Fig. 2 (Q_1 and Q_3) generates significantly less CS leakage current than the right half-circuit (Q_2). The failure mode of this circuit then becomes similar to that of Type 0 circuits except that it occurs at higher temperatures because the CS leakage for each half-circuit is still better matched compared to Type 0 circuits.

From Fig. 6(c) it can be seen that for Type RN circuits similar non-linearities as for the Type R circuit are present, although at higher temperatures compared to the Type R circuits. No rapid voltage reductions as seen in Type R circuits was seen in Type RN circuits at the examined temperatures. However, due to mismatches in compensated leakage currents resulting from process mismatches and/or the limitations of the compensation circuits used, it is likely that the Type RN circuits would fail in a manner similar to the other circuits, but that the failures occur at temperatures higher than the temperature range of the experiments performed in this work. As concluded in Sect. 2.4, if similar matching to that of [6] was achieved, this failure mode should occur for Type RN circuits at a temperature approximately 60 °C higher than the temperature at which this happens for Type R circuits. However, the temperature sweeps performed in this work do not examine such high temperatures. Thus, this hypothesis has yet to be confirmed.

4.2 Linearity, accuracy and temperature range

For Type 0 circuits (Fig. 6(a)) significant non-linearities are introduced in *VREF* and *VPTAT* at temperatures as low as 150 °C. For Type R and Type RN compensations, it can be seen from Fig. 6(b), (c) that the same magnitude of non-linearities do not occur until above 175 °C.

Figure 7 shows a *VPTAT*/*VREF* ratio for different types of compensation circuit based on data of selected curves from Fig. 6. The curves were not chosen to quantify performance, but rather to illustrate the characteristic behaviour of each of the different types of compensation circuit. The selected graphs are from sweeps from which the highest temperature ranges were obtained. For the Type 0 circuit, the curve is highly non-linear and experiences a rapid decrease at 220 °C, where both *VREF* and *VPTAT* are reduced rapidly. The Type R circuit achieves good linearity up to 210 °C, followed by a rapid increase in *VPTAT*/*VREF* where both *VREF* and *VPTAT* fall off

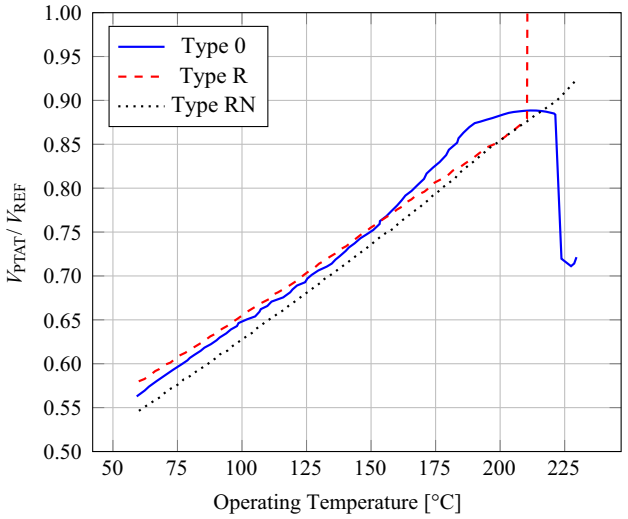

Fig. 7 Measurement results of $VPTAT/VREF$ as functions of temperature for different types of leakage current compensation circuits for a Brokaw bandgap circuit. The Type 0 curve is derived from the *red dashed curve* from Fig. 6(a), and the Type R and RN curves are derived from the *black dotted curves* of Fig. 6(b), (c), respectively (Color figure online)

sharply. The Type RN circuit, on the other hand, presents good linearity over the entire 60–230 °C temperature range.

The data of the $VPTAT/VREF$ ratio was used to assess the linearity of the different types of compensation circuits and to relate the linearity to how it affects the temperature range for a given accuracy. Table 2 presents the best-case, median and worst-case ranges over which a least-squares fit to measured data in the 60–90 °C temperature range produced a maximum deviation of 3, 5 and 10 °C. We denote this deviation as the accuracy of the circuit. Examining the median upper temperature limits, it can be seen that the Type 0 circuit has the lowest upper temperature limit for all values of accuracy. For the 3 and 5 °C accuracy requirements, the Type R circuit achieves the highest upper temperature limit, and the Type RN circuit achieves the highest upper temperature limit for an accuracy of 10 °C.

To further assess the accuracy of the circuits, histograms presenting the amount of chips which achieved a given accuracy at different temperatures are presented in Fig. 8. It can be seen from Fig. 8(a) that at 195 °C, all of the 5 measured Type R circuits achieve an accuracy better than 7.5 °C. This is in contrast to the Type RN circuits for which the accuracies are generally worse and varies more. Fig. 8(b) shows that 4 of the 5 measured Type RN circuits achieve an accuracy between 2.5 and 10.0 °C whereas 3 of those stay below 7.5 °C. The histograms are shown at 195 °C because several of the Type R circuits experienced malfunction at around 200 °C. Looking at a higher temperature of 216 °C, it can be seen from Fig. 8(c) that the accuracy for Type RN devices is slightly reduced but still stays better than 7.5 °C for 3 of the 5 tested chips. Data of Type R devices for 216 °C is not presented because the Type R devices that were characterised up to that temperature experienced malfunction at 210 °C or lower.

4.3 Reference voltage stability

Table 2 also shows the maximum $VREF$ variation over the temperature range where the accuracy requirement is not exceeded. For the chips with median upper temperature limit, it can be seen that the Type RN circuit has a generally more stable $VREF$ over temperature than has the Type R circuit.

The obtained results were compared to the simulations of [7]. For Type RN circuits with an accuracy of 3 °C the median upper temperature limit is 168 °C for which $VREF$ varies by 16 mV. This result is in agreement with expected values based on simulation results from [7]. There, a Monte Carlo simulation showed a variation of $VREF$ of 9.4 mV over the 0 to 175 °C temperature range, with a standard deviation of 6.8 mV.

As can be seen from Fig. 6(a), the $VREF$ stability of the Type 0 circuit is generally low. However, we do not compare it to the other types of circuits because its upper temperature limit is significantly lower than that of the other circuits.

4.4 Supply voltage requirements

When repeating the above experiments for a supply voltage $V_{DD} = 2.5$ V, $VREF$ and $VPTAT$ were largely unaffected for most sweeps. However, for two out of thirteen measurements, a difference was seen at high temperatures. One possible explanation is that the hole mobility decreases with increasing temperature and a larger overdrive voltage over the M_1–M_2 mirror is required for a given current for the mirror to remain in saturation. In addition, leakage currents from the collectors of Q_1 and Q_2 must be resupplied by the current mirror, further increasing the required overdrive voltage. This phenomenon was seen for one of the Type 0 circuits, none of the Type R circuits and one of the Type RN circuits.

4.5 Power consumption

A plot of the mean power consumption based on four temperature sweeps of the Type RN circuit is shown in Fig. 9. In accordance with the theory presented in Sect. 2.5, the power consumption consists of a linear term and an exponential term. The exponential coefficient b_2 was obtained from the exponential part of the plotted data and found to be 0.064 C^{-1}. This supports the theory that the

Table 2 Upper temperature limits for different types of leakage current compensation circuits for different values of accuracy (Color table online)

Accuracy (°C)	Upper Temperature Limit (°C)		
	Type 0	Type R	Type RN
10	171/162/161	216/210/200	228/216/181
5	156/155/153	208/200/184	202/182/158
3	150/147/144	200/170/162	182/168/147
	Maximum V_{REF} Variation (mV)		
	Type 0	Type R	Type RN
10	140/74/65	258/303/283	257/46/53
5	42/30/28	270/283/36	22/22/48
3	24/22/16	283/36/32	17/16/48

For each type of compensation and for a certain accuracy, the best, median and worst chips in terms of highest upper limits are shown in the following format: "<best-case> / <median> / <worst-case>". The maximum *VREF* variation over the range where the accuracy is not exceeded is also shown. An identical position or colour for a given accuracy indicates data from the same chip

exponential term is due to reverse leakage current, which approximately doubles for every 10 °C increase in temperature [13].

At 60 °C, the power consumption of the different chips ranged from 230 to 320 nW (mean 260 nW), which is a relative variation of 32%. At 200 °C, the power consumption ranged from 1.5 to 2.8 µW (mean 2.1 µW), reaching the higher relative variation of 60%, and at 230 °C, the power consumption ranged from 9.5 to 19 µW (mean 14µW), reaching a relative variation of 67%. This variation of power consumption between different regions of operation suggests that the power consumption generated by leakage current is more sensitive to process variation than is the power consumption generated by bias current.

5 Discussion

From the results presented in Sect. 4.2, it can be seen that two aspects play an important role when determining which compensation type to use when designing a low-power, high-temperature bandgap temperature sensor: how important it is to generate a stable reference voltage and how high of a measurement accuracy that is required.

5.1 Stable reference voltage

An advantage of using a bandgap circuit as a temperature sensor is that one of the generated output voltages is a relatively temperature-invariant reference voltage that can be used by other parts of the circuit that is not directly taking ratiometric temperature measurements. For example, an ADC may be needed to obtain digital samples of the measured voltages, or a voltage regulator in a mixed-signal design may need a stable voltage reference to operate properly. Thus, depending on the system specifications, because a Type RN circuit outperforms a Type R circuit in terms of *VREF* stability, it may be preferable to use a Type RN circuit even though its temperature range is generally lower for an accuracy of 5 °C or better.

5.2 Accuracy and temperature range

If an accuracy better than 5 °C is required, it has been demonstrated that the Type R circuit provides the highest operating temperature range. However, if the accuracy requirement is relaxed to 10 °C, which may be acceptable for a condition monitoring system, the Type RN circuit achieves the higher range.

Although most samples of the Type R circuit outperforms the Type RN circuit in terms of temperature range at better accuracies than 5 °C, some Type R chips were shown to suffer from rapid reductions in output voltage at a specific temperature where both *VREF* and *VPTAT* fall off sharply. If *VREF* becomes small, voltage regulators and subsequently digital subsystems requiring a regulated voltage in order to operate will shut down, reducing the possibilities for the system to signal that there is a problem. This behaviour was not seen for any of the Type RN chips in the temperature range where the experiments were performed, that is, from 60 to 230 °C. Thus, it would appear that Type RN circuits could operate at a higher temperature range, although with lower accuracy, while keeping a digital subsystem operational.

Another aspect of the fact that no such malfunction was seen for Type RN circuits is that the accuracy can be significantly improved if the system is calibrated digitally, and the difference in accuracy between a Type R and Type RN compensation circuit can be minimised, and thus, the operating range for a certain amount of accuracy can be extended. For circuits suffering from this type of malfunction, such a calibration will not improve the accuracy after the rapid voltage reduction point because too severe non-linearities are introduced there.

5.3 Comparison to other work

Table 3 presents a comparison of the sensor in this work in terms of different requirements on accuracy with state-of-the-art low-power, high-temperature sensors. The sensors in this work have no integrated ADC, and thus no power consumption value for those positions. Future work

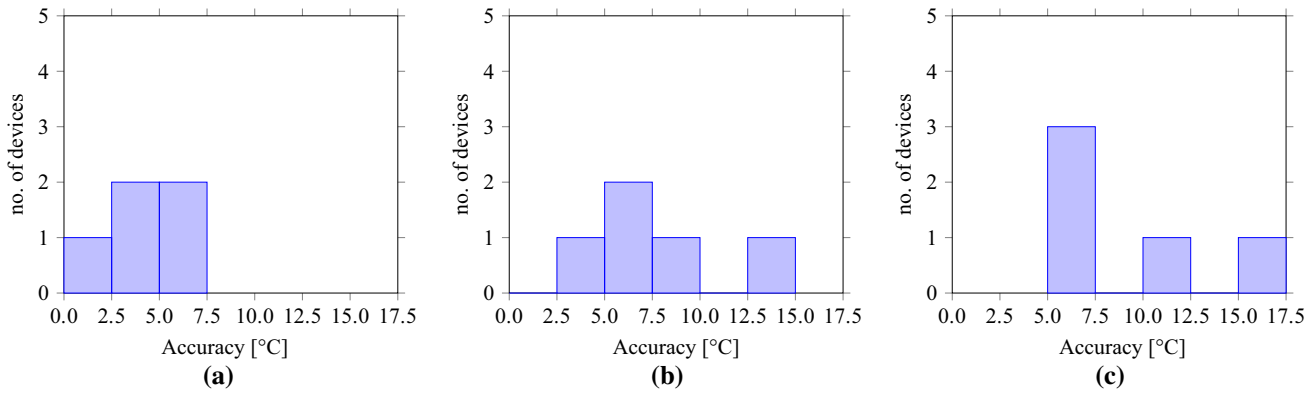

Fig. 8 Histograms of the accuracy for Type R and Type RN circuits for 195 °C and 216 °C. Data for each *plot* is derived from 5 temperature sweeps of different chips for both Type R and Type RN circuits. Data for Type R circuits at 216 °C has been omitted because all Type R devices characterised at said temperature experienced malfunction at 210 °C or lower, as can be seen from Fig. 6(b). **a** Type R, 195 °C. **b** Type RN, 195 °C. **c** Type RN, 216 °C

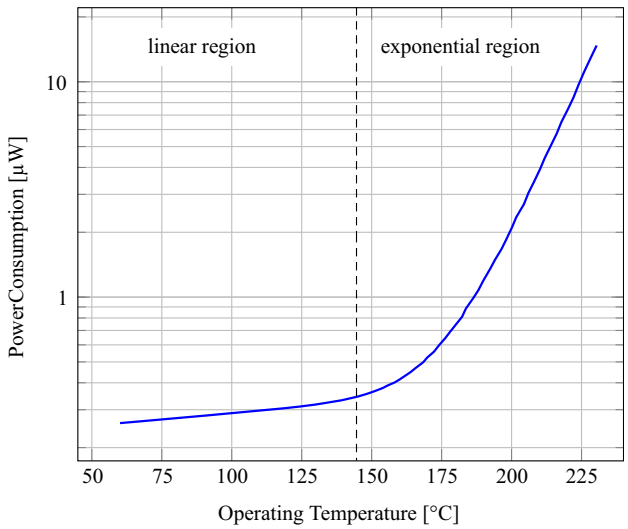

Fig. 9 Mean power consumption of the Type RN circuit based on measured data from four temperature sweeps

includes investigating how to combine a power-efficient ADC with the circuits presented in this work.

The sensors from this work show a higher or equal upper temperature limit compared to all other sensors with a bandgap as the sensing element. However, this is achieved at the expense of accuracy. For the case of a sensor in this work with an accuracy of 5 °C, the same upper temperature limit is obtained as in [16], and the power consumption is smaller by a factor of 17. However, [16] achieves an accuracy as high as 0.4 °C.

The only non-bandgap sensor in this comparison, [12], achieves an upper temperature limit as high as 250 °C. This is significantly higher than the sensor of this work even if an accuracy of only 10 °C is accepted. However, this is achieved with the power consumption increased by a factor of 18 compared to the sensors of this work.

In contrast to the other sensors in this comparison, the sensors from this work were not manufactured in an

Table 3 Comparison of the performance of different temperature sensors

Parameter	This work[a]	This work[b]	This work[c]	[9]	[16]	[12]
Sensing element	Bandgap	Bandgap	Bandgap	Bandgap	Bandgap	PIN diode
SOI	No	No	No	Yes	Yes	Yes
Calibration points	2	2	2	1	1	2
Process technology node (µm)	0.18	0.18	0.18	1.0	0.16	Not available
Power consumption (including ADC) (µW)	Not available	Not available	Not available	90	40	150
Power consumption (excluding ADC) (µW)	5.7	2.1	0.53	45	22	12
Accuracy (°C)	10	5	3	1.6	0.4	3
Temperature range (°C)	0–216	60–200	60–170	40–170	−55–200	25–250

This work is included three times to demonstrate how the performance parameters change with changing requirements on accuracy. Power consumption is taken as the highest value over the entire temperature range. This table is based on the comparison table found in [9]

[a] The Type RN circuit corresponding to the measurements of the blue solid line of Fig. 6(c).

[b] The Type R circuit corresponding to the measurements of the green dashed-dotted line of Fig. 6(b).

[c] The Type R circuit corresponding to the measurements of the red dashed line of Fig. 6(b)

silicon on insulator (SOI) process to achieve a high upper temperature limit. Because leakage currents are generally smaller in SOI processes, it is possible that the temperature range could be further extended and/or the power consumption could be reduced using such a process.

6 Conclusion

Experiments show that Type R and Type RN circuits extend the temperature range compared to the Type 0 circuit by 20– 50 °C. For an accuracy of 10 °C or more, the Type RN circuit achieves a higher upper temperature limit compared to the Type R circuit, and for an accuracy of 5 °C or less, the Type R circuit achieves the higher limit. Some of the examined Type R circuits were seen to experience a total circuit malfunction above a certain temperature where no temperature readings can be conducted. This phenomenon was not seen for any of the Type RN circuits over the entire temperature range from 60 to 230 °C.

At high temperatures, the power consumption of the temperature sensors was found to be highly dependent on leakage current. It was seen to increase exponentially with increasing temperature, setting a limit at which it is no longer effective to reduce the power consumption by reducing bias current.

The sensors presented in this work are suitable for use in the field of condition monitoring of power semiconductors. Their high upper temperature limit and low power consumption make direct-contact sensors suitable for wireless single-chip designs. A drawback to using these types of sensors is their low accuracy; however, the trade-off between high temperature operation and high accuracy may be acceptable depending on the system requirements. Furthermore, the accuracy may be improved by calibrating the sensors digitally.

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