High-Temperature Recessed Channel SiC CMOS Inverters and Ring Oscillators

Mattias Ekström, Bengt Gunnar Malm, *Senior Member, IEEE*, and Carl-Mikael Zetterling, *Senior Member, IEEE*

***Abstract*— Digital electronics in SiC find use in high-temperature applications. The objective of this study was to fabricate SiC CMOS without using ion implantation. In this letter, we present a recessed channel CMOS process. Selective doping is achieved by etching epitaxial layers into mesas. A deposited SiO_2-film, post-annealed at low temperature and re-oxidized in pyrogenic steam, is used as the gate oxide to produce a conformal gate oxide over the non-planar topography. PMOS, NMOS, inverters, and ring oscillators are characterized at 200 °C. The PMOS requires reduced threshold voltage in order to enable long-term reliability. This result demonstrates that it is possible to fabricate SiC CMOS without ion implantation and by low-temperature processing.**

***Index Terms*— Inverter, recessed channel, ring oscillator (RO), silicon carbide (4H-SiC), static CMOS.**

I. Introduction

SEVERAL different transistor and circuit technologies have been demonstrated in silicon carbide (4H-SiC) technology. SiC circuit technology is suitable for extreme environments, such as high temperature [1] and high radiation [2]. The bipolar junction transistor (BJT) technology have been demonstrated for use in emitter-coupled logic (ECL) [3], [4] and transistor-transistor logic (TTL) [5], [6]. The field-effect transistors (FETs) include impressive results in the use of metal-semiconductor FETs (MESFETs) [7], [8], junction FETs (JFETs) [9]–[11] and metal oxide semiconductor FETs (MOSFETs) [12]–[15]. Of these transistors and circuit families, the static complementary MOSFET (CMOS) circuit family offers high input impedance, high fan-out, rail-to-rail swing output, low static power consumption, dense and simple digital circuit design and compatibility with all state-of-the-art memory technologies. SiC CMOS together with integrated ferroelectric memory devices [16], [17] could give non-volatile memory operational at high temperatures.

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The authors are with the School of Electrical Engineering and Computer Science, KTH Royal Institute of Technology, SE-164 40 Kista, Sweden (e-mail: mekstr@kth.se).

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The state-of-the-art SiC NMOS devices uses nitridation in either N_2O or NO to achieve high channel mobility (μ_n), typically in the range 25–35 cm^2/Vs [18], [19]. Nitridation has been reported to produce high hole mobility (μ_p), about 7–10 cm^2/Vs [20], although the highest hole mobility was reported for pyrogenic steam grown oxides, with μ_p of 15.6 cm^2/Vs [21]. However, μ_n is reportedly low in this process (1 cm^2/Vs) [12].

Previous demonstrations of SiC CMOS have used ion implantation to achieve selective doping. Ion implantation is continually improving in SiC technology [22], but the p^+-type implant requires excessively high annealing (∼1700 °C) to activate the dopants. Self-aligned PMOS transistors are currently not possible. A considerable amount of point defects remain even after high temperature annealing. Based on our previous experience in SiC BJT technology [3]–[6], which did not require ion implantion, it was of interest to determine if SiC CMOS could also be done without ion implantation. A few previous works have presented recessed channel SiC NMOS transistors [23]–[25], a technology that does not require ion implantation. The recessed channel transistor can be processed by etching epitaxially grown layers to achieve selective doping. In this letter, we present the first results of our SiC CMOS process, which is the first time demonstration of a recessed channel SiC CMOS process that does not require ion implantation. We demonstrate inverters and ring oscillators (ROs) with this process. The results of this study can prove beneficial for others working with SiC CMOS, regardless of if ion implantation or epitaxy-only process is used. Both nitridation and steam process were tested, but only the steam process produced PMOS transistors that could be used for CMOS applications. Only the steam process is presented here. The presented process is intended for high temperature applications.

II. Experimental Details

The devices were fabricated in our in-house 100 mm wafer SiC processing flow. The epitaxy was grown by Norstel [26], and was, from top to bottom, $n^+/p/p^+/n/n^+/p^+/n$-substrate. The lightly doped regions (n and p) served as the body of the transistors, and had a graded doping profile. The highly doped regions (n^+ and p^+) served as the source/drain or body contact region (depending on transistor polarity). The final p^+-layer isolates the PMOS transistors from the n-type substrate. The doping profile, with thickness

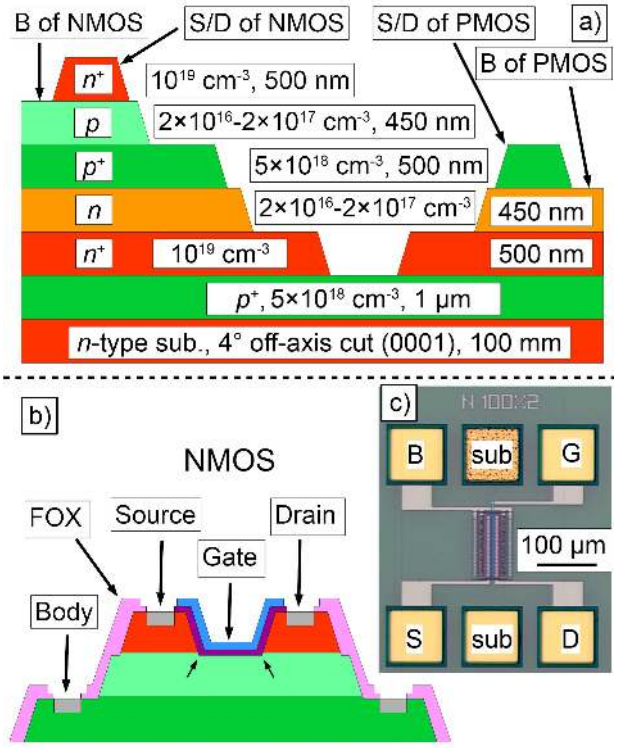

Fig. 1. a) Half-pitch cell of NMOS and PMOS epitaxy after etching. The body dopings are graded, with higher doping (125 nm, 2×10^{17} cm^{-3}) at the surface compared to deeper in the body (325 nm, 2×10^{16} cm^{-3}). b) Cross-section of an NMOS, illustrating the four terminals (without metallization). The etch recesses the channel and exposes the *p*-type region. The poly-gate controls electron flow from the raised source to the raised drain through field-effect modulation of charge-carriers in the recessed channel. The corners at the edges of the channel are pointed out. c) Photograph of fabricated NMOS (100 μm width, 2 μm length). The two sub. connections are to the bottom p^+-layer to isolate the transistors from the substrate.

and doping values, is shown in Fig. 1a). The epitaxial layers were etched into mesas by magnetically enhanced reactive ion etching (MERIE, SF_6-based, 300 W, 5.3 Pa, 3 mT) in five steps, as shown in Fig. 1a). Photoresist was used, which gives sloped mesa sidewalls. The surface etch damage was removed by sacrificial oxidation. The field oxide (FOX) was formed in a sequence of depositing polysilicon films (poly), patterning the poly and oxidizing the patterned poly into polyoxide. A thin blanket polyoxide prevented SiC etch damage during the poly etch. The FOX was thinned in buffered HF to open the active regions. The oxidations were performed at 1000 °C in pyrogenic steam. The final FOX thickness was 230 nm. The merits of using polyoxide in SiC technology was recently evaluated [27]. Radio Corporation of America (RCA) clean was performed prior to depositing 33 nm SiO_2 by atomic layer deposition (ALD). This ALD-film sets the bulk thickness of the gate oxide. After deposition, the gate oxide interface was oxidized in O_2 for 10 min at 1050 °C, followed by annealing the oxide in N_2 for 1 h, ended by steam for 10 min at 950 °C. The low temperature and short time was used to prevent excessive oxide growth on the exposed *a*-faces [28]. In-situ doped poly (*n*-type) was used as gate electrode. Contacts were formed as detailed in our previous work [29], [30]. The NMOS transistor without metallization is shown in Fig. 1b). A chemical-mechanical

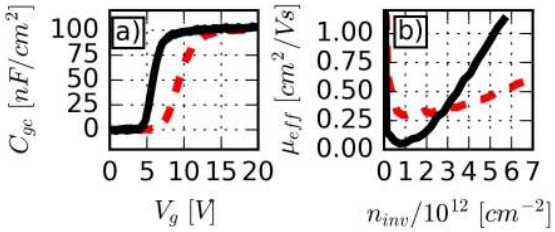

Fig. 2. NMOS (100 × 10) transistor, measured at RT (dashed) and at HT (solid). a) $C_{gc} - V_g$, measured at 100 kHz, 30 mV (root-mean square, RMS). b) $\mu_{eff} - n_{inv}$, with n_{inv} the inversion charge number density.

polishing (CMP) enabled 2-level TiW-metallization was used to connect the transistors. The metallization was covered with a plasma enhanced CVD (PECVD) SiO_2/SiN_x passivation and the measurement pads were covered with Au/Pt/Ti to prevent oxidation at high temperature [9], [31]. A processed NMOS transistor can be seen in Fig. 1c).

Electrical characterization was performed using a Keithley SCS parameter analyzer, equipped with $I - V$, $C - V$ and pulse measurement units. A Cascade 12000 semi-automatic probestation with a 200 °C hotchuck enabled full wafer statistical measurements. The threshold voltage (V_t) was mapped across the wafer by using constant current (CC) method, with the threshold current (I_t) set to 1 nA with a drain-source voltage (V_{ds}) of 1 V. The CC method gives somewhat higher V_t than $C - V$ based estimation, but lower than other $I - V$ based estimates. Effective mobility (μ_{eff}) is estimated by using split $C - V$ and pulsed $I - V$. Density of interface traps (D_{IT}) was estimated by frequency dependent charge pumping, as outlined in [32].

III. Results

The inversion capacitance and μ_{eff} were measured at both room temperature (RT) and at 200 °C (HT), as seen in Fig. 2. The $C - V$ curve shifts to lower voltages, indicating V_t shift of ∼3.7 V. The slope becomes steeper at HT, indicating lower amount of active traps. The estimated μ_{eff} increases with increasing field and increasing temperature, indicating Coulomb scattered limited mobility. The transistors have clear depletion/inversion behavior at both RT and HT, as seen in Fig. 2a) and 3a). The inversion capacitance corresponds to a capacitance equivalent thickness (CET) of ∼35 nm. This thickness is appropriate for 2 μm gate length devices [14], [33]. The estimated μ_{eff} at HT is relatively low, ≤1 cm^2/Vs. It is comparable to previous results with steam oxidation [12].

The NMOS transistors have normal long channel output behavior at HT, as seen in Fig. 3b). V_t median is 8.0 V and the sample standard deviation is 0.8 V, with the cumulative distribution function (CDF) shown in Fig. 3c).

The PMOS output characteristics, shown in Fig. 3b), show some non-linearity at low drain voltages. This makes it difficult to estimate the mobility since the drain conductance cannot be determined from such data. Compared to the NMOS devices the saturation is also less clear. Physical device simulations confirm that both an overetch for the channel recess, as well as a non-conformal gate oxide thickness at the source/drain sidewalls and recess corners result in degraded subthreshold slope (not shown), higher V_t and non-linear/saturating output characteristics. A challenge with this process is to optimize both the PMOS and NMOS at the same time, since the etch

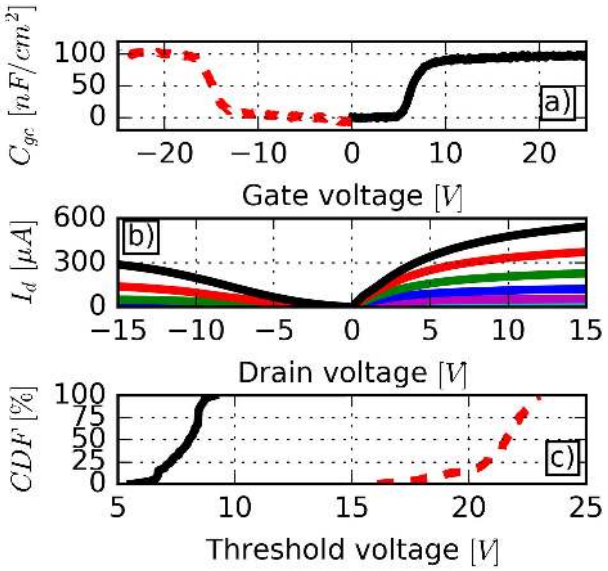

Fig. 3. PMOS and NMOS (100 × 2) transistors, measured at HT. a) $C_{gc} - V_g$ measured at 100 kHz, 30 mV (RMS). The PMOS (dashed) enters invertsion at −14.8 V, and the NMOS (solid) at 6 V. b) $I_d - V_d$. $|V_{gs}|$ from 15 V to 25 V in steps of 2 V. PMOS is on left-hand side, NMOS on right-hand side. The mismatched current is due to mismatched V_t. c) CDF of $|V_t|$, estimated by CC method ($|I_t| = 1$ nA). The NMOS $|V_t|$ (solid) has a median of 8.0 V and an interquartile range (IQR, range within 25–75 %) of 1.2 V. The PMOS $|V_t|$ (dashed) is higher than the NMOS, with an median of 21.6 V and a IQR of 1.4 V. The best PMOS (lowest $|V_t|$) is shown in a) and b).

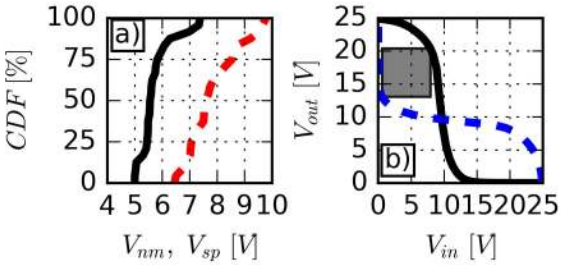

Fig. 4. Inverters measured at HT. a) CDF of V_{nm} (solid) and V_{sp} (dashed). b) Inverter transfer characteristics. V_{nm} is estimated by fitting the largest square inside the transfer curve (solid) and its transposed curve (dashed), with the length of the side of the square being the estimated V_{nm} [33, ch. 5].

variations accumulate for the last processed transistor. Even small etch variations can have significant impact for recessed channel SiC devices [25]. $|V_t|$ is very high, see 3c), with the median 21.6 V and the sample standard deviation is 1.6 V.

D_{IT} was measured by charge pumping at HT. The estimated median and sample standard deviation of D_{IT} is 2.4×10^{12} cm^{-2} eV^{-1} and 0.25×10^{12} cm^{-2} eV^{-1}, respectively. D_{IT} is high but not unreasonable for non-optimized SiC gate oxide process. The high D_{IT} contributes to Coulomb scattering and reduce the observed mobility [34]. This low temperature and short oxidation time with steam may give higher D_{IT} than high temperature and long oxidation time [35].

The inverters (PMOS to NMOS width ratio was 60 μm/40 μm, channel length 2 μm for both) were mapped across the wafer at HT. 25 out of the 52 (48%) inverters provided a voltage output swing ≥90% of the power supply (25 V). The distribution of estimated noise margin voltages (V_{nm}) and switching point voltage (V_{sp}) is shown in Fig. 4a).

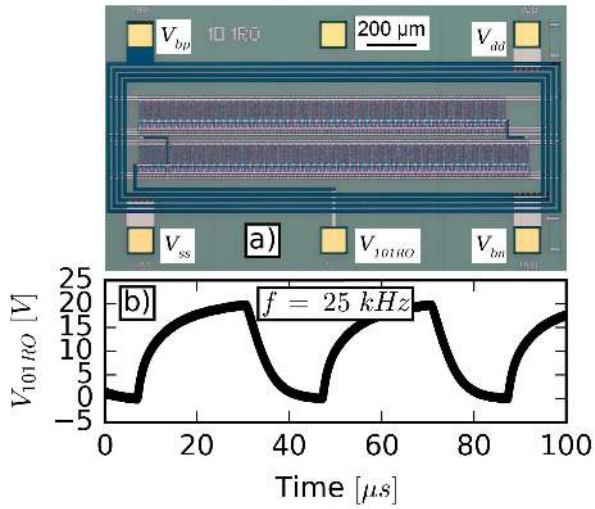

Fig. 5. Ring oscillator. a) Photograph of a 101-stage RO. It occupies an area of 0.95 mm × 1.7 mm (1.615 mm^2). The circuit was designed to use four power supplies (V_{bp}, V_{dd}, V_{ss}, V_{bn}) to allow adjustable V_t. This feature was not used in this measurement ($V_{bp} = V_{dd} = 25$ V, $V_{ss} = V_{bn} = 0$ V). b) Oscillation at HT of a 101-stage RO. The frequency (f) is 25 kHz.

The medians are 5.5 V and 7.5 V, respectively (22% and 30% of the power supply, respectively). V_{nm} and V_{sp} can be improved (closer to 50 %) by reducing the PMOS V_t to be closer to the NMOS V_t. The transfer curve itself of the best inverter found (highest V_{nm}) is shown in Fig. 4b).

101-stage ROs (PMOS to NMOS width ratio was 60 μm/10 μm, channel length 2 μm for both) were measured at HT to determine if the within-die yield was sufficiently high for circuit applications. A 101-stage RO is shown in Fig. 5a) and the oscillating signal is shown in Fig. 5b). While the pull-up was not strong enough to achieve full swing (25 V), the RO was oscillating, indicating that all 206 transistors (2 × 101 from the RO and 2 × 2 from the two-step output buffer) were operational.

The tested ROs oscillated for a few minutes before permanently breaking. It is likely that the power supply (25 V) is too high for reliable operation, since the maximum electric field of the gate dielectric exceeds >6 MV/cm [36]. Given previous results in the literature [14], [36], 10.5–14 V would provide adequate reliability. The PMOS transistors require targeted process improvement in order to reduce $|V_t|$ below 10.5 V.

IV. Conclusions

A recessed channel CMOS process in SiC technology has been demonstrated. This process does not require ion implantation, and the highest process temperature is 1050 °C (gate oxidation). Conformal gate oxide is strongly required to get recessed channel transistors with adequate performance, which prohibits the use of long time and high temperature gate oxidation processes and requires deposited SiO_2-film with post-deposition annealing. Inverters and ring oscillators have been demonstrated to be operational at 200 °C. The most important improvement required for this process is to reduce the PMOS V_t below 10 V for the intended gate oxide thickness (35 nm), as this would allow the CMOS circuits to operate at 10 V power supply in order to ensure long-term reliability.

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