High-throughput Low-complexity Mixed-radix FFT Processor using a Dual-path Shared Complex Constant Multiplier

Tram Thi Bao Nguyen and Hanho Lee

Abstract—This paper presents a high-throughput low-complexity 512-point eight-parallel mixed-radix multipath delay feedback (MDF) fast Fourier transform (FFT) processor architecture for orthogonal frequency division multiplexing (OFDM) applications. To decrease the number of twiddle factor (TF) multiplications, a mixed-radix $2^4/2^3$ FFT algorithm is adopted. Moreover, a dual-path shared canonical signed digit (CSD) complex constant multiplier using a multi-layer scheme is proposed for reducing the hardware complexity of the TF multiplication. The proposed FFT processor is implemented using TSMC 90-nm CMOS technology. The synthesis results demonstrate that the proposed FFT processor can lead to a 16% reduction in hardware complexity and higher throughput compared to conventional architectures.

Index Terms—Fast Fourier transform (FFT), mixed-radix, multipath delay feedback (MDF), dual-path, complex constant multiplier, orthogonal frequency division multiplexing (OFDM)

I. INTRODUCTION

The fast Fourier transform (FFT) algorithm is primarily a fast and efficient method to compute the discrete Fourier transform (DFT). FFT processors are among the most widely used components in various digital signal processing (DSP) applications and systems. Moreover, FFT processors gained intense research interest with the appearance of orthogonal frequency division multiplexing (OFDM) communication systems, not only in digital broadcasting systems and mobile telecommunications but also in power line communication (PLC) systems [1-3]. In particular, in recent years, with the increasing demand for multimedia applications using wireless transmissions over short distances, the millimeter wave (mmWave) 60 GHz wireless personal area network (WPAN) has been intensively researched for many years. Also, the IEEE 802.11 Task Group ad (IEEE 802.11ad) has been developed a standard for the mmWave wireless local area network (WLAN) and WPAN systems [4]. In the physical layer design of high-rate WPANs, OFDM modulation has been adopted, and the FFT processor has a high hardware complexity. One OFDM symbol in the IEEE 802.11ad standards consists of a length of 512 subcarriers. Therefore, FFT processor conducts the FFT computation with 512-point arithmetic. Because of its massive computational complexity, FFT processor architectures require high hardware complexity and power consumption. Thus, several FFT processor architectures have been proposed to reduce the hardware complexity and to provide higher throughput.

Among various FFT algorithms, the Cooley and Tukey algorithm [5] is highly popular because they first introduced the concept of FFT, which can reduce the computational complexity by making efficient use of the symmetry and periodicity properties of the twiddle

factors (TFs). To further reduce the computational complexity, several algorithms have been proposed, including radix-2^3 [6], radix-2^4 [7, 8], radix-2^5 [9], and mixed-radix [10]. In common, these higher-radix algorithms reduce the number of non-trivial multiplications in the radix-2 algorithm. Other studies have been done on parallel FFT architectures, which can achieve higher throughput with lower computation latency [6-8]. However, some critical problems still exist and need improvement for the speed, area, and power consumption considerations. Therefore, this paper focuses on the throughput and hardware complexity improvement for FFT processor architectures.

In this paper, we propose a high-throughput and low-complexity 512-point eight-parallel multipath delay feedback (MDF) architecture using an area-efficient mixed-radix $2^4/2^3$ FFT algorithm. In addition, we propose the architecture of a dual-path shared multi-layer canonical signed digit (CSD) complex constant multiplier (DPS-MLCCM) to reduce the hardware complexity for TF multiplication of parallel FFT processors. The proposed FFT processor provides better throughput and less hardware complexity compared to previous designs [9-11].

The rest of this paper is organized as follows. Section II describes the mixed-radix $2^4/2^3$ FFT algorithm. In Section III, the architecture of the proposed mixed-radix FFT processor and the DPS-MLCCM for TF multiplication is presented. Section IV presents the implementation results and performance comparison. Finally, conclusions are provided in Section V.

II. MIXED-RADIX $2^4/2^3$ FFT ALGORITHM

The DFT of length N is defined as

$$X(k) = \sum_{n=0}^{N-1} x(n) \cdot W_N^{nk}; \qquad 0 \le k \le N-1 \qquad (1)$$

where k is the frequency index and n is the time index; the TF is defined as

$$W_N^{nk} = e^{-j2\pi\frac{nk}{N}} \qquad (2)$$

The basic idea of FFT is based on the fundamental principle of decomposing the computation of the N-point DFT into successively smaller DFTs [5].

1. Radix-2^3 Algorithm

To derive the radix-2^3 algorithm, the first three steps in cascade decomposition are considered. The linear index mapping is transformed into four-dimensional linear index maps [6]:

$$
\begin{aligned}
n &= \left\langle \frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + n_4 \right\rangle_N \\
k &= \left\langle k_1 + 2k_2 + 4k_3 + 8k_4 \right\rangle_N
\end{aligned}
\qquad (3)
$$

Applying the four-dimensional linear index map to (1),

$$
\begin{aligned}
&X\left(k_1 + 2k_2 + 4k_3 + 8k_4\right) \\
&= \sum_{n_4=0}^{\frac{N}{8}-1}\sum_{n_3=0}^{1}\sum_{n_2=0}^{1}\sum_{n_1=0}^{1} x(\frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + n_4) \cdot W_N^{nk} \\
&= \sum_{n_4=0}^{\frac{N}{8}-1}\left[L_{\frac{N}{8}}(n_4,k_1,k_2,k_3) \cdot W_N^{n_4(k_1+2k_2+4k_3)} \right] \cdot W_{\frac{N}{8}}^{n_4 k_4}
\end{aligned}
\qquad (4)
$$

With the cascade decomposition, the TF can be expressed in the form of

$$
\begin{aligned}
&W_N^{(\frac{N}{2}n_1+\frac{N}{4}n_2+\frac{N}{8}n_3+n_4)(k_1+2k_2+4k_3+8k_4)} \\
&= \underbrace{(-1)^{n_1 k_1}}_{Stage1BF}\overbrace{(-j)^{n_2 k_1}}^{Stage1TF}\underbrace{(-1)^{n_2 k_2}}_{Stage2BF}\overbrace{W_8^{n_3(k_1+2k_2)}}^{Stage2TF} \\
&\quad \underbrace{(-1)^{n_3 k_3}}_{Stage3BF}\overbrace{W_N^{n_4(k_1+2k_2+4k_3)}}^{Stage3TF} W_{\frac{N}{8}}^{n_4 k_4}
\end{aligned}
\qquad (5)
$$

2. Radix-2^4 Algorithm

In [7], radix-2^4 algorithm is derived by considering the first four steps of decomposition. Applying a five-dimensional linear index map,

$$
\begin{aligned}
n &= \left\langle \frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + n_5 \right\rangle_N \\
k &= \left\langle k_1 + 2k_2 + 4k_3 + 8k_4 + 16k_5 \right\rangle_N
\end{aligned}
\qquad (6)
$$

The CFA takes the form of

$$X\left(k_1 + 2k_2 + 4k_3 + 8k_4\right)$$

$$= \sum_{n_5=0}^{\frac{N}{16}-1} \sum_{n_4=0}^{1} \sum_{n_3=0}^{1} \sum_{n_2=0}^{1} \sum_{n_1=0}^{1} x(\frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + n_5) \cdot W_N^{nk}$$

$$= \sum_{n_5=0}^{\frac{N}{16}-1}\left[G_{\frac{N}{16}}(n_5, k_1, k_2, k_3, k_4) \cdot W_N^{n_5(k_1+2k_2+4k_3+8k_4)} \right] \cdot W_{\frac{N}{16}}^{n_5 k_5} \qquad (7)$$

With the cascade decomposition, the TF can be expressed in the form of

$$W_N^{(\frac{N}{2}n_1 + \frac{N}{4}n_2 + \frac{N}{8}n_3 + \frac{N}{16}n_4 + n_5)(k_1+2k_2+4k_3+8k_4+16k_5)}$$

$$= \underbrace{(-1)^{n_1 k_1}}_{Stage1BF} \underbrace{\overbrace{(-j)^{n_2 k_1}}^{Stage1TF}}\ \underbrace{(-1)^{n_2 k_2}}_{Stage2BF} \overbrace{W_{16}^{(2n_3+n_4)(k_1+2k_2)}}^{Stage2TF}$$

$$\underbrace{(-1)^{n_3 k_3}}_{Stage3BF} \overbrace{(-j)^{n_4 k_3}}^{Stage3TF} \underbrace{(-1)^{n_4 k_4}}_{Stage4BF} \overbrace{W_N^{n_5(k_1+2k_2+4k_3+8k_4)}}^{Stage4TF}\ W_{\frac{N}{16}}^{n_5 k_5}$$

$$\qquad (8)$$

3. Mixed-radix $2^4/2^3$ Algorithm

Many conventional FFT algorithms are variations of the Cooley-Tukey algorithm. The FFT architecture, in which the radices of component butterflies are not all equal, is called the mixed-radix FFT. If the radix is properly chosen for different stages on the basis of the FFT specifications, the optimized design for speed and area can be obtained. Then, the proposed 512-point FFT processor adopts the mixed-radix $2^4/2^3$ FFT algorithm. Fig. 1 shows a signal flow graph for the 64-point mixed-radix $2^4/2^3$ algorithm.

The mixed-radix $2^4/2^3$ algorithm for 512-point FFT computation consists of nine stages in which the radix-2^4 is adopted in the first four stages and the radix-2^3 algorithm is used in the remaining stages. Table 1 presents the sequence of the 512-point FFT TF computation at each stage for the radix-2^k and mixed-radix algorithm. As can be observed, the mixed-radix $2^4/2^3$ algorithm can reduce the number of TF multiplications. Hence, the area and power consumption of the complex multipliers can be reduced accordingly.

III. PROPOSED FFT ARCHITECTURE

1. Proposed MDF Architecture

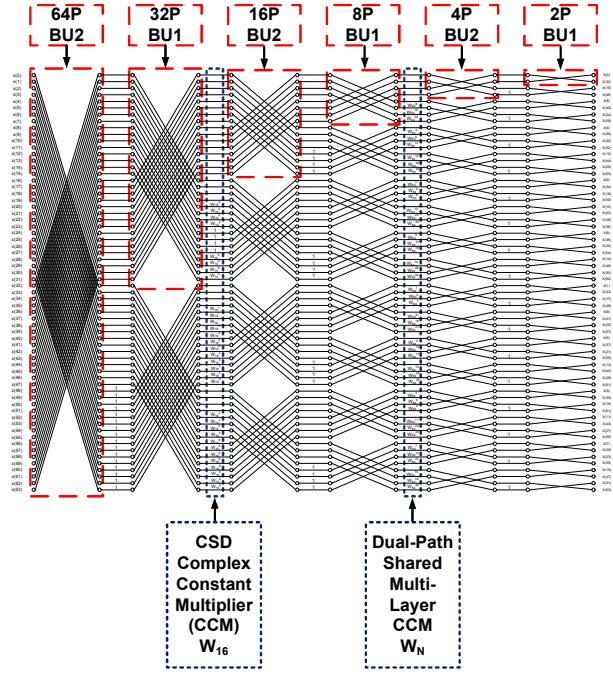Several pipeline architectures for FFT processor have

Fig. 1. Signal flow graph of the 64-point mixed-radix $2^4/2^3$ algorithm.

Table 1. Sequence of the 512-point FFT TF computation for radix-2^k and the mixed-radix algorithm

Algorithm	Stage							
	1	2	3	4	5	6	7	8
Radix-2^2	$-j$	W_{512}	$-j$	W_{128}	$-j$	W_{32}	$-j$	W_8
Radix-2^3	$-j$	W_8	W_{512}	$-j$	W_8	W_{64}	$-j$	W_8
Radix-2^4	$-j$	W_{16}	$-j$	W_{512}	$-j$	W_{16}	$-j$	W_{32}
Radix-2^5	$-j$	W_8	W_{32}	$-j$	W_{512}	$-j$	W_8	W_{32}
Mixed-Radix-$2^4/2^3$	$-j$	W_{16}	$-j$	W_{512}	$-j$	W_8	W_{32}	$-j$

been proposed over the past few decades [6]. In general, the multi-path delay commutator (MDC) scheme can achieve a higher throughput rate while the single-path delay feedback (SDF) scheme requires less memory and hardware complexity [12]. The proposed MDF architecture can provide high throughput rate with minimal hardware cost by incorporate the features of MDC and SDF [12-14].

The block diagram of the proposed eight-parallel 512-point mixed-radix $2^4/2^3$ MDF FFT processor architecture is presented in Fig. 2. The architecture contains nine stages with the following sub-blocks: the IFFT/FFT select unit, based on the duality between the IFFT and FFT characteristic; module 1, based on the radix-2^4 FFT algorithm for stage 1 to stage 4; module 2, which consists
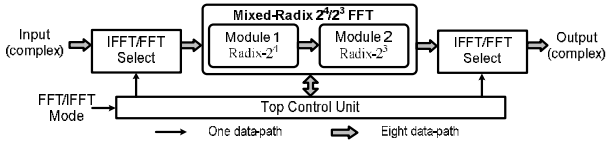
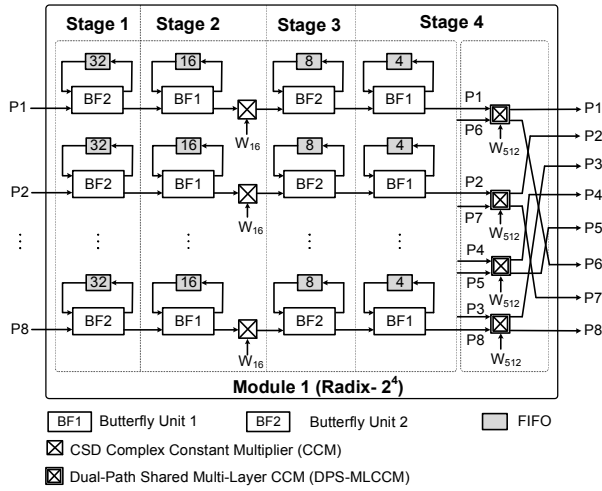**Fig. 2.** Block diagram of the proposed 512-point mixed-radix $2^4/2^3$ MDF FFT processor.

Fig. 3. Block diagram of Module 1.

Fig. 4. Block diagram of Module 2.

2. Proposed Dual-path Shared Multi-layer CSD Complex Constant Multiplier

A complex multiplier is a component that has a critical effect on the hardware complexity, the power consumption, and throughput of FFT processors. Even if a low-complexity FFT algorithm is adopted, the complex multiplier can be realized by various approaches to reduce hardware complexity. Generally, the CSD representation of a TF is able to reduce hardware complexity better than binary representation of a TF when the TF has only few coefficients. For a TF with many coefficients, the Booth multiplier has been widely used in existing research. However, its primary problem is that it requires high hardware complexity.

In this paper, a novel DPS-MLCCM architecture for TF W_{512} multiplication is presented. First, we consider the multiplications of the input x{Re,Im} with the TF $W_{512}^t = e^{(-j2\pi t/512)} = X_t + jY_t$ (where t is from 0 to 465), which can be divided into eight regions as illustrated in Fig. 5. From the symmetry property, the TFs in other regions can be obtained by mapping from region A. The value of t is mapped to t', i.e., $W_{512}^{t'} = X_{t'} + jY_{t'}$, where t' is from 0 to 64 in region A. Second, the TF $W_{512}^{t'}$ is decomposed so that the multiplication can be implemented by a multi-layer CCM. The decomposition is applied to reduce the number of CSD constant multipliers needed. The multiplication of the input x{Re,Im} with the TF $W_{512}^{t'} = X_{t'} + jY_{t'}$ is now derived as

of stage 5 to stage 9 relying on the radix-2^3 FFT algorithm; and the top control unit. The details of each module are discussed as follows.

Module 1 has a radix-2^4 structure as depicted in Fig. 3. The input data is processed in eight-parallel data-paths. Module 1 covers from stage 1 to stage 4 of the proposed FFT processor and consists of the first-in first-out (FIFO) registers, two types of butterfly unit (BF1 and BF2), the conventional CSD complex multiplier (CCM) using a common sub-expression sharing (CSS) technique for stage 2, and the proposed DPS-MLCCM using the CSS technique for TF W_{512} in stage 4. The BF1 only implements complex additions and subtractions while the BF2 includes TF W_4 multiplication utilizing the multiplexers and control signals [9].

Module 2 is realized by the radix-2^3 FFT algorithm as shown in Fig. 4. Most of the components of module 2 are similar to that of module 1: FIFO registers, butterfly units BF1 and BF2, the CCM using the CSS technique for stage 6, and a dual-path shared CCM (DPS-CCM) using the CSS technique for TF W_{32} in stage 7.
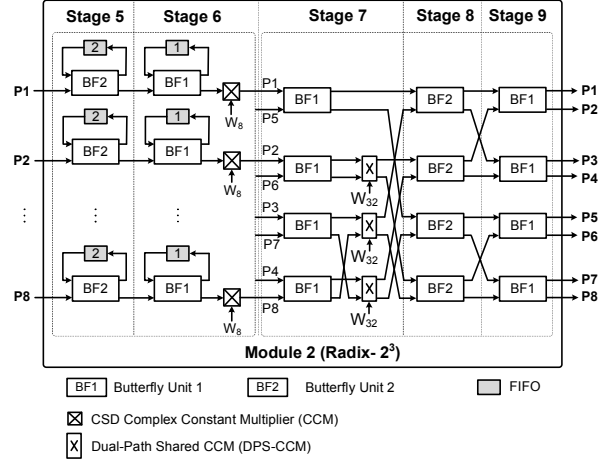
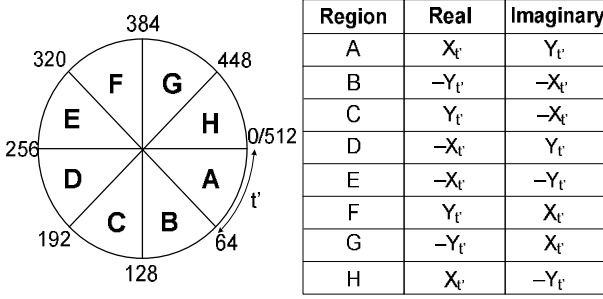| Region	Real	Imaginary
A	$X_{t'}$	$Y_{t'}$
B	$-Y_{t'}$	$-X_{t'}$
C	$Y_{t'}$	$-X_{t'}$
D	$-X_{t'}$	$Y_{t'}$
E	$-X_{t'}$	$-Y_{t'}$
F	$Y_{t'}$	$X_{t'}$
G	$-Y_{t'}$	$X_{t'}$
H	$X_{t'}$	$-Y_{t'}$

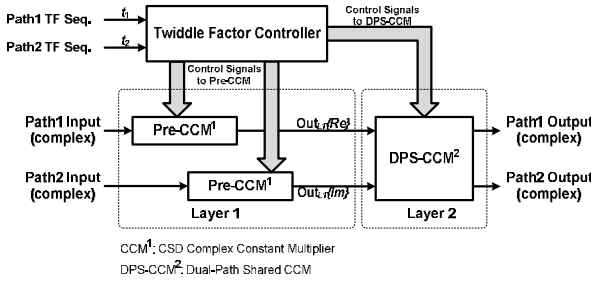**Fig. 5.** TFs with the corresponding mapping in eight regions of the unit circle for DPS-MLCCM.

Fig. 6. Block diagram of DPS-MLCCM for W_{512} TF multiplication.

$$x \times W_{512}^{t'}$$
$$= x \times W_{512}^{(8t_1+t_2)}$$
$$= x \times W_{512}^{8t_1} \times W_{512}^{t_2} \quad ; where \begin{cases} 0 \le t_1 \le 8 \\ 0 \le t_2 \le 7 \end{cases}$$
$$= \underbrace{[\text{Re}\{x\}+j\text{Im}\{x\}] \times W_{512}^{8t_1}}_{Layer1} \times W_{512}^{t_2}$$
$$= \underbrace{[\text{Re}\{Out_{Layer1}\}+j\text{Im}\{Out_{Layer1}\}] \times W_{512}^{t_2}}_{Layer2}$$

(9)

Through the TF mapping and decomposition process, the entire multiplication unit can be implemented using 15 different TFs in total. The number of TFs needed for layer 1 and layer 2 of the proposed DPS-MLCCM are eight and seven, respectively. Fig. 6 presents the block diagram of the proposed DPS-MLCCM for W_{512}TF multiplication.

The input data, together with the mapping TF coefficient and the regional selection data generated from the TF controller block, pass through two layers of the multiplier to generate the output result. On the basis of the characteristic of the scheduling of the TF in the DPS-MLCCM layer 2, the path sharing scheme can be applied in this layer for further hardware complexity reduction.

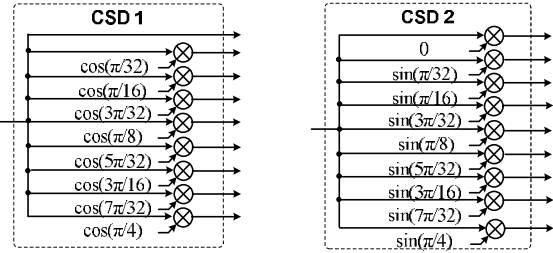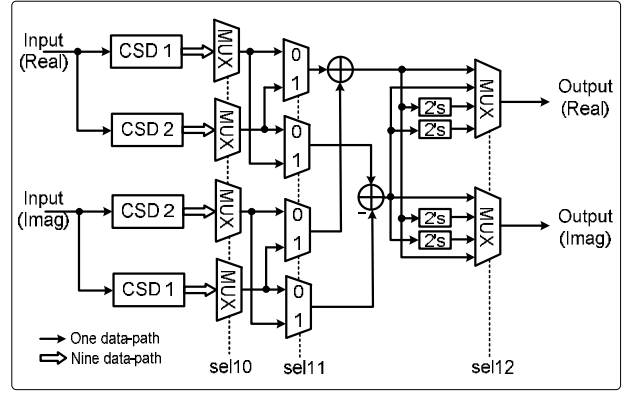Layer 1 of the multiplier is responsible for the

Fig. 7. Architecture of the pre-CCM in DPS-MLCCM layer 1 for W_{512} TF multiplication.

complex multiplication of input x with a TF $W_{512}^{8t_1}$, $0 \le t_1 \le 8$. Since the number of TFs is quite small, the multiplication in layer 1 can be exploited using the pre-CCM.

When the TF is equal to W_{512}^0, the pre-CCM is operated by a bypass operation without an additional CCM. Therefore, this layer consists of a CCM using only 16 coefficients. In addition, the CSS technique is applied to these coefficients, for minimizing hardware complexity. The detailed hardware architecture of the pre-CCM of the proposed DPS-MLCCM for W_{512} TF multiplication is shown in Fig. 7. This pre-CCM of layer 1 consists of the CCM using the CSS technique, the two's complement logic, and the multiplexers for proper control.

The output of layer 1 is then sent to the input of the DPS-CCM in layer 2 of the DPS-MLCCM for the remaining computations to be implemented. Layer 2 of the DPS-MLCCM is responsible for the multiplication of the input data set $Out_{L1}\{Re, Im\}$, which is the output from layer 1 of the multiplier with the TFs $W_{512}^{t_2}, 0 \le t_2 \le 7$. When the TF is equal to W_{512}^0, no multiplier is required for computation, as described in the previous section. Therefore, this layer consists of only seven complex
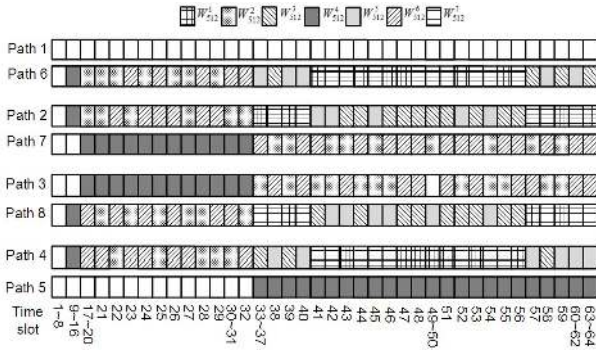
Fig. 8. Scheduling of the TF at each time slot.

Fig. 9. Architecture of DPS-CCM in DPS-MLCCM layer 2 for W_{512} TF multiplication.

multipliers. Similarly, the TF multiplication in layer 2 can be exploited using 14 CCMs.

On the basis of the characteristic of the scheduling of the TF in eight-parallel data-paths, the proposed dual-path sharing technique can be applied in layer 2 of the DPS-MLCCM to further reduce the hardware complexity. Fig. 8 shows the corresponding values of TF $W_{512}^{t_2}$ for eight data-paths at different time slots. According to the scheduling of the TFs at each time slot for eight data-paths in the proposed 512-point mixed-radix FFT processor, it can be observed that the same TF never occurs at the same time in each pair of these two parallel data-paths: path 1 and path 6, path 2 and path 7, path 3 and path 8, and path 4 and path 5. However, the CCM used for $t_2 = 4$ must be duplicated in order to avoid the conflict of DPS-CCM control. Consequently, a total of 16 CCMs are required in the DPS-CCM architecture.

The detailed DPS-CCM architecture of layer 2 of the proposed DPS-MLCCM for W_{512} TF multiplication is shown in Fig. 9. This layer consists of the CCM using the sharing technique, two's complement logic, and the multiplexers for appropriate control of regional remapping.

IV. IMPLEMENTATION RESULTS AND PERFORMANCE COMPARISON

Prior to the hardware implementation of the proposed FFT processor, an appropriate word length and a quantization error performance evaluation is determined by a fixed-point evaluation is determined by a fixed-point simulation using MATLAB. From the simulation results, a 12-bit word length is chosen for both the real and imaginary parts because the output signal to noise ratio (SNR) was saturated at a 12-bit word length.
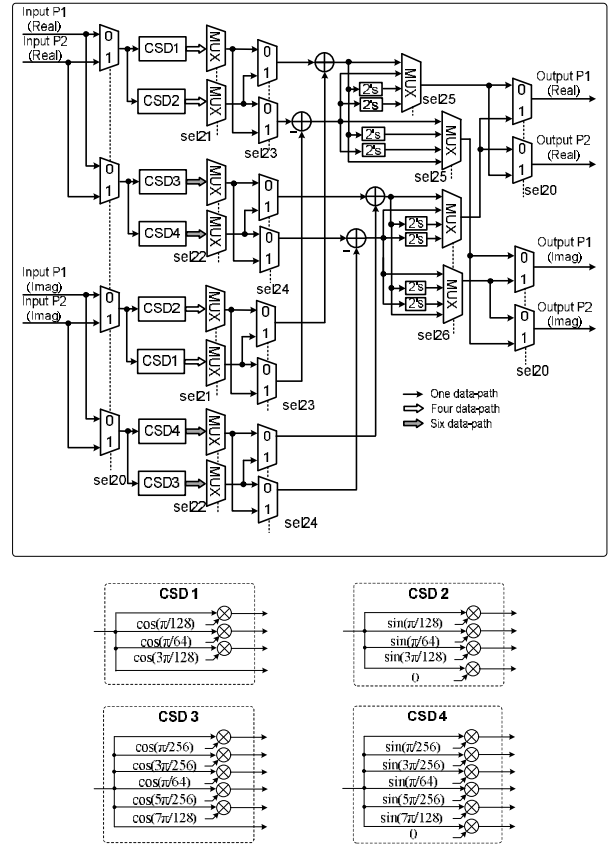
The determined word length not only keeps the quantization noise to the least value but also can minimize the hardware complexity. When the word length is set to 12 bits, the proposed FFT processor architecture yields a signal to quantization noise ratio (SQNR) of 41.2 dB without using a data scaling approach.

After a proper word length was determined, the proposed FFT architecture was designed in Register Transfer Level (RTL) using Verilog HDL and functionally verified using a commercial Verilog HDL simulator. In addition, the entire design was synthesized using a Synopsys design compiler with a TSMC 90-nm CMOS technology optimized for a 1.2-V supply voltage. The proposed processor has a 243,000 gate count, and the operating clock frequency is 385 MHz.

Table 2 presents a comparison of the hardware complexity between different 512-point FFT processor architectures. In order to compare the hardware complexity, the complex multipliers are synthesized and

Table 2. Hardware complexity comparison of different 512-point FFT processors

	[9]	[10]	[11]	Proposed
FFT size	512	512	512	512
No. of CR	504	504	640	504
No. of CA	120	120	112	120
No. of CBM $N.A^g = 1$	8	8× (0.76+0.57)	16×0.76	-
No. of CCM (W_8) $N.A^g = 0.12$	8	9	-	8
No. of CCM (W_{16}) $N.A^g = 0.28$	8	8	12	8
No. of CCM (W_{32}) $N.A^g = 0.46$	8	-	-	-
No. of DPS-CCM (W_{32}) $N.A = 0.43$	-	-	-	3
No. of DPS-MLCCM (W_{512}) $N.A = 1.9$	-	-	-	4
Total N.A of complex mult.	14.88	13.96	15.52	12.09
TF LUT size (bits)	10,240	-	-	-

CR denotes the complex registers.
CA denotes the complex adders.
CBM denotes the complex Booth multiplier.
CCM denotes the complex constant multiplier.
DPS-CCM denotes the dual-path shared CCM.
DPS-MLCCM denotes the dual-path shared multi-layer CCM.
N.A denotes the normalized area.

Table 3. Performance of the proposed FFT processor compared with previous implementations

	[9]	[10]	[11]	Proposed
Technology	90-nm	90-nm	90-nm	90-nm
Architecture	MDF	MDF	Memory-based	MDF
FFT Size	512	512	512	512
No. of data-paths	8	8	16	8
Algorithm	Modified Radix-2^5	Mixed-Radix $2^4/2^2/2^3$	Radix-16	Mixed-Radix $2^4/2^3$
Internal word length (bits)	12	14	12	12
SQNR (dB)	35	-	57	41.2
Measurement	Logic synthesis	Post-layout	Post-layout	Logic synthesis
Clock rate (MHz)	310	220	324	385
Throughput (GS/s)	2.5	1.76	2.59	3.08
Gate count	290K	-	-	243K

then the area of each multiplier was normalized. Compared with other architectures, the proposed architecture has the lowest total normalized area of the complex multipliers. In addition, there is no need to allocate memory to store the twiddle factor.

Table 3 shows the performance comparisons between the proposed 512-point eight-parallel mixed-radix $2^4/2^3$ MDF FFT/IFFT processor using CCM and several existing 512-point FFT processors [9-11]. The results show that the proposed FFT processor obtains much better SQNR performance than that of [9]. The design in [9] is also a pipelined eight-parallel MDF architecture for a 512-point FFT processor. However, it requires much more complex multipliers and memory than the proposed design. Therefore, the proposed architecture results in a low hardware complexity.

Moreover, the highest throughput of the proposed FFT processor can reach 3.08 GS/s at 385 MHz by employing eight-parallel data-paths. The throughput rate is the fastest among the presented algorithms in Table 3. Finally, it is quite evident from Table 3 that the proposed architecture has an advantage in terms of hardware complexity; the gate count for the overall FFT processor is reduced more than 16% compared to that of [9]. This hardware complexity reduction results from using the proposed multi-layer CSD complex multiplier architectures and the sharing technique.

V. CONCLUSIONS

This paper presents a 512-point eight-parallel MDF mixed-radix $2^4/2^3$ FFT processor using a novel DPS-MLCCM. In particular, a dual-path sharing technique and a multi-layer CCM architecture for TF multiplication is proposed to efficiently reduce the hardware complexity of the FFT processor based on parallel MDF architecture. From fixed-point simulation results, the SQNR performance is 41.2 dB with a 12-bit word-length implementation. Total estimated NAND gates are 243,000 from the synthesized results, and the throughput is 3.08 GS/s for the proposed FFT processor. The proposed FFT processor is the most area-efficient and high-throughput architecture for the eight-parallel 512-point MDF FFT processors. Therefore, the proposed FFT processor is a promising solution for OFDM systems that require high throughput and low complexity.

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