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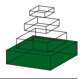

High-throughput multiple dies-to-wafer bonding technology and III/V-on-Si hybrid lasers for heterogeneous integration of optoelectronic integrated circuits

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Integrated optical light source on silicon is one of the key building blocks for optical interconnect technology. Great research efforts have been devoting worldwide to explore various approaches to integrate optical light source onto the silicon substrate. The achievements so far include the successful demonstration of III/V-on-Si hybrid lasers through III/V gain material to silicon wafer bonding technology. However, for potential large-scale integration, leveraging on mature silicon complementary metal oxide semiconductor (CMOS) fabrication technology and infrastructure, more effective bonding scheme with high bonding yield is in great demand considering manufacturing needs. In this paper, we propose and demonstrate a high-throughput multiple dies-to-wafer (D2W) bonding technology, which is then applied for the demonstration of hybrid silicon lasers. By temporarily bonding III/V dies to a handle silicon wafer for simultaneous batch processing, it is expected to bond unlimited III/V dies to silicon device wafer with high yield. As proof-of-concept, more than 100 III/V dies bonding to 200 mm silicon wafer is demonstrated. The high performance of the bonding interface is examined with various characterization techniques. Repeatable demonstrations of 16-III/V die bonding to pre-patterned 200 mm silicon wafers have been performed for various hybrid silicon lasers, in which device library including Fabry–Perot (FP) laser, lateral-coupled distributed-feedback laser with side wall grating, and mode-locked laser (MLL). From these results, the presented multiple D2W bonding technology can be a key enabler toward the large-scale heterogeneous integration of optoelectronic integrated circuits.

Keywords: silicon photonics, hybrid lasers, heterogeneous integration, die-to-wafer bonding, optoelectronic integrated circuits

INTRODUCTION

In the future generation of datacom and computercom, which demand ever higher bandwidth and lower power, the conventional electrical interconnection routing the electronic signals becomes bandwidth-limited along with prohibitively high power consumption (Beausoleil et al., 2008). One solution to the challenge is the optical interconnect technology (Goodman et al., 1984; Miller, 2000, 2009; Ohashi et al., 2009), in which high bandwidth optical signals are routed by low-loss optical fiber and waveguides. In contrast to the electrical interconnection (i.e., the copper wire), optical interconnect has many merits, e.g., high speed, low crosstalk, immunity to electromagnetic interference, low overall power consumption (Alduino and Paniccia, 2007). Most importantly, with the up scaling potential, optical interconnect is expected to provide much higher transmission capacity and longer signal transmission distance than the electrical interconnect.

Although it was proposed initially 30 years ago (Goodman et al., 1984), there was no significant development progress with solid demonstrations of optical interconnect for very-large-scale integration (VLSI). The situation has changed since the concept of silicon photonics (Pavesi and Lockwood, 2004; Reed and Knights, 2004; Lipson, 2005; Guillot and Pavesi, 2006; Jalali and Fathpour, 2006; Soref, 2006; Poon et al., 2009a,b; Vivien and Pavesi, 2013; Xu et al., 2014), which utilizes low-cost silicon material along with leveraging on the advancement of silicon complementary metal oxide semiconductor (CMOS) process, integration, and mature infrastructure. Envisioned by Soref and Lorenzo (1985), silicon photonics has emerged and progressed steadily. Especially in the past decade, we have been witnessing rapid growth in research and development activities along with product development efforts exploiting silicon photonics technology for the optical interconnect (Pavesi and Lockwood, 2004; Reed and Knights, 2004; Lipson, 2005; Guillot and Pavesi, 2006; Jalali and Fathpour, 2006; Soref, 2006; Fedeli et al., 2008; Poon et al., 2009a,b; Michel et al., 2010; Reed et al., 2010; Feng et al., 2012; Liow et al., 2013; Vivien and Pavesi, 2013; Dong et al., 2014a,b; Lim et al., 2014; Xu et al., 2014). For instance, to minimize the small core silicon waveguide propagation losses, considerable research work has been devoted to minimize the waveguide sidewall roughness by using the deep ultra-violet (DUV) photolithography and optimized patterning technique (Dumon et al., 2004; Bogaerts et al., 2005) and sidewall smoothing technique [e.g., double thermal oxidations (Sparacin

et al., 2005; Xia et al., 2006)]. Indeed, submicrometer-scale silicon wire waveguides have shown a propagation loss of 2 dB/cm and less (Xia et al., 2006). Furthermore, owing to the enabling CMOS fabrication technologies, we have seen the establishment and utilization of a myriad of essential silicon photonic passive and active components including optical filters (Xiao et al., 2007; Zhou and Poon, 2007; Guha et al., 2010; Fang et al., 2012), optical switches (Poon et al., 2009a,b; Van Campenhout et al., 2009; Luo et al., 2012; Song et al., 2013), low-power-consuming modulators with up to 50 Gb/s-speed operation (Dong et al., 2009; Reed et al., 2010; Tu et al., 2013, 2014), and Ge-on-Si photodetectors with bandwidth larger than 40 GHz (Michel et al., 2010; Liow et al., 2013). It is these demonstrated silicon photonic devices and technologies that make ultimate optical interconnection a viable solution to address the distance/bandwidth/cost and power-consumption challenges. To this end, silicon photonics provides nearly all key building blocks for optical interconnection. Furthermore, the CMOS-compatible fabrication processes make it possible to integrate both electronics and photonics either through monolithic or heterogeneous approach. Such significant progress has led the optical interconnect to become a much more practical technology.

However, silicon-based on-chip optical light source, which is one of the key components for the light generation for carrying information, has been the missing piece for optical interconnect. This is mainly because silicon is transparent in the telecommunication wavelengths (i.e., 1310 and 1550 nm wavelengths) due to the indirect bandgap, which prohibits efficient light emission from silicon. Thus, to solve the challenge, numerous research efforts have been devoted to explore various technologies for light source on silicon chips.

REVIEW ON RESEARCH FOR LASERS ON SILICON

Historically, researchers worldwide have devoted many research efforts by exploring various possibilities for the development of lasers on silicon, which mainly focused in the following directions:

(1) silicon material engineering by introducing emissive centers to assist the efficient light emission (Pavesi et al., 2000; Han et al., 2001; Rotem et al., 2007a,b; Shainline and Xu, 2007),
(2) strained Ge (Liu et al., 2007, 2009, 2010; Cheng et al., 2009; Sun et al., 2009b,c; Camacho-Aguilera et al., 2012),
(3) silicon Raman laser (Boyraz and Jalali, 2004, 2005; Rong et al., 2005a,b, 2007), and
(4) heterogeneous integration of III/V gain materials through packaging (Chu et al., 2009; Fujioka et al., 2010; Urino et al., 2011) or wafer bonding (Park et al., 2005; Fang et al., 2007a,b; Liang et al., 2009a,b, 2010; Stanković et al., 2010; Grenouillet et al., 2012).

Here, we will limit our review to the heterogeneous integrated silicon lasers. With regard to the silicon laser through heterogeneous integration of III/V gain materials on silicon, there are two major types of integration strategies, namely the packaging scheme and the bonding scheme. Research groups from Japan devoted many efforts for the development of silicon lasers using packaging methods. Chu et al. (2009) demonstrated the first wavelength-tunable-laser fabricated with silicon photonic technology, which comprised a semiconductor optical amplifier (SOA) chip and a silicon photonic chip, and were hybrid-integrated by using passive alignment technology. An SiON mode-size converter was adopted between the silicon waveguide and III/V SOA for low coupling loss. Later on, silicon photonic-based optical interconnects were also demonstrated by integrating lasers, silicon modulators, and Ge photodetectors on single silicon substrate (Urino et al., 2011). While such demonstrations have shown the advantage in principal of being capable to integrate various building blocks together for optical interconnection, the main issue is the complicated fabrication process. It typically requires precise alignment between the SOA and the silicon waveguide, even with assistance of the mode-size converter. Considering the III/V gain region of <200 nm in thickness, for instance, it became a difficult challenge for alignment with acceptable coupling loss. Such complicated fabrication process is a potential show stopper for future massive production demanding high yield, thus significantly increases the product cost.

Heterogeneous integration of III/V gain materials on silicon through wafer bonding technology is another major directional strategy for silicon lasers. UMR-CNRS and LETI initiated the research work of III/V laser on silicon wafers for photonic integration by using wafer bonding technology. In 2001, they demonstrated the first InP-based microdisk laser integrated on a silicon wafer through SiO_2–SiO_2 molecular bonding (Seassal et al., 2001). Although this work did not show complete integration of III/V optoelectronics with silicon photonics waveguide structures, it showed the potential of such wafer bonding technology for future heterogeneous integrated optoelectronic circuit. Following such demonstration, Hattori et al. (2006) demonstrated an integration scheme of III/V microdisk laser with silicon waveguide in 2006. By aligning the microdisk laser atop silicon waveguide, the laser emissions can be vertically coupled into the underneath silicon waveguide with 35% coupling efficiency. Such demonstration showed the capability of the hybrid photonic integration of III/V laser with silicon waveguide for photonic links application.

The so-called hybrid silicon laser was proposed and first demonstrated by Park et al. (2005) with optical injection. In this work, the III/V wafer with AlGaInAs quantum well structure is directly bonded to pre-patterned silicon wafer using low-temperature oxygen plasma-assisted wafer bonding. The laser cavity was defined by endface-polished silicon waveguide structure, while the III/V provides the optical gain. As the III/V optoelectronic structures are fabricated after the wafer bonding with best precise, only possibly achieved via lithographic process, alignment to the silicon device layer, thus there is no stringent alignment requirement to the bonding process, which significantly simplifies the fabrication process and makes the possibility of wafer-level-oriented manufacturing ability. Subsequently, Fang et al. (2006) demonstrated an electrically pumped AlGaInAs-silicon evanescent laser with continuous-wave (CW) operation in 2006. Subsequently, various hybrid lasers with different structures and also enhanced laser performances are demonstrated by various research groups using molecular wafer bonding technology, including Fabry–Pérot lasers (FP) (Ben Bakir et al., 2011; Dong et al., 2013), racetrack lasers (Fang et al., 2007a,b), distributed Bragg reflector (DBR) lasers (Fang et al., 2008a,b,c),

distributed-feedback (DFB) lasers (Fang et al., 2008a,b,c), microring lasers (Liang et al., 2009a,b, 2012), wavelength tunable lasers (Keyvaninia et al., 2013a,b,c), multiple-wavelength lasers (Van Campenhout et al., 2008; Kurczveil et al., 2011), and mode-locked lasers (MLL) (Fang et al., 2008a,b,c).

Besides such direct bonding method, wafer bonding can also be realized through an adhesive material as the bonding interlayer. Among all kinds of adhesive bonding materials, divinylsiloxane-bisbenzocyclobutene (DVS-BCB or BCB) is the most popular one for hybrid silicon lasers due to the merits such as the high bonding strength and the sustainability in the subsequent III/V process. IMEC has used BCB-assisted adhesive bonding method for heterogeneous integration (Roelkens et al., 2005). In 2006, Roelkens et al. (2006) demonstrated the first electrically injected InP/InGaAsP laser integrated on silicon waveguide circuit using BCB-assisted adhesive bonding technology. Similar to Seassal et al. (2001), the optical laser is purely made with III/V layer with the laser facets being defined by dry etching. With optimized mode-size converter, the optical light can be vertically coupled down to the underneath silicon waveguide with high efficiency. By designing hybrid mode waveguide comprising silicon waveguide and III/V gain medium, they also demonstrated a hybrid FP laser (Stanković et al., 2011) and a DFB laser (Stanković et al., 2012; Keyvaninia et al., 2013a,b,c), and multiple-wavelength laser (Keyvaninia et al., 2013a,b,c) using such adhesive bonding technology.

Apart from BCB, some kinds of metal can also be adopted as the bonding interlayer for adhesive bonding. AuGeNi is one of the most popular metals for metal bonding as it not only functions as a bonding media but can also be used for the Ohmic contact to the InGaAsP structure. Tanabe et al. (2010) demonstrated a InAs/GaAs quantum-dot laser on Si substrate by metal-assisted wafer bonding with room temperature operation at 1.3 μm wavelength. Meanwhile, Hong et al. (2010) also demonstrated an FP laser through selective-area metal bonding using AuGeNi. The silicon waveguide in such demonstration is with 5 μm and 800 nm thickness. The demonstrated FP laser is with threshold current density of 1.7 kA/cm and a maximum output power of 3 mW. However, the drawback of the AuGeNi-assisted bonding is the Au contamination. Thus, Tatsumi et al. (2012) further demonstrated an Au-free metal-assisted wafer bonding for lasers on silicon chip. Besides, Creazzo et al. (2013) also demonstrated another type of silicon laser by using metal-assisted bonding of III/V epitaxial material directly onto the silicon substrate. The demonstrated that silicon laser had a threshold of ~50 mA and maximum optical power of ~8 mW. The benefit of such metal-assisted bonding is the advantage of effective thermal dissipation, which shows a thermal resistant of only 21°C/W.

Beyond these two major heterogeneous integration schemes, there are also other methods for III/V-on-Si lasers, including direct III/V epitaxy on silicon substrate (Liu et al., 2011; Lee et al., 2012) and III/V epitaxial layer transfer-printing to silicon wafers (Justice et al., 2012; Yang et al., 2012). However, while the direct epitaxy method faces major challenges of high-density dislocations due to the lattice mismatch between III/V material and silicon after many years of research, the transfer-printing method for hybrid silicon laser needs further demonstrations to show the repeatability and reliability.

From these analyses, it shows that among various approaches, the hybrid silicon laser through wafer bonding technology can be considered as the most successful and promising one for silicon photonic heterogeneous integration circuits due to the ever-demonstrated advanced performances and the fabrication process compatibility with silicon photonics. **Table 1** summarizes some of the representative demonstrations of hybrid silicon lasers through wafer bonding technology.

WAFER BONDING TECHNOLOGIES FOR ON-CHIP SILICON LASERS

In general, there are two mainstreams of wafer bonding methods applying to heterogeneous integrated silicon photonics, namely the molecular bonding through interfacial bonds, and the adhesive bonding assisted with another adhesive material as bonding interface such as polymer or metal. Such wafer bonding technology is a mature process, which is widely applicable for SOI wafer fabrication, MEMS technology, and optoelectronic device fabrication. As a lot of review papers already exist (Lasky, 1986; Maszara, 1991; Tong and Goesele, 1999; Alexe and Gösele, 2004; Christiansen et al., 2006), we thus only focus the discussion on the application of hybrid silicon lasers. According to the existing demonstrations, we further summarize here the major bonding technologies as below:

(1) wafer-to-wafer (W2W) molecular bonding,
(2) die-to-wafer (D2W) molecular bonding,
(3) BCB-assisted D2W adhesive bonding, and
(4) metal-assisted adhesive bonding.

The W2W molecular bonding for hybrid silicon lasers is mainly driven by the UCSB group. Through such plasma-activated low-temperature W2W molecular bonding (Pasquariello and Hjort, 2002), they, together with their collaborators, have demonstrated various hybrid silicon lasers, starting from the first-hybrid FP laser (Fang et al., 2006), followed by racetrack-shaped laser (Fang et al., 2007a,b), DBR lasers (Fang et al., 2008a,b,c), DFB lasers (Fang et al., 2008a,b,c), MLL (Fang et al., 2008a,b,c), and multi-wavelength arbitrary waveform generation (AWG) laser (Kurczveil et al., 2011). However, for the conventional III/V-to-Si W2W bonding without thick oxide interlayer, the generated gas by-products of H_2 and H_2O are easily trapped inside the bonding interface and form the interfacial voids, which subsequently affect the bonding quality. In order to effectively remove such trapped gases, some proper outgas channels are designed, such as in-plane outgassing channels (IPOC) (Kissinger and Kissinger, 1993) or vertical outgassing channels (VOC) (Liang and Bowers, 2008). IPOS is formed by etching some lateral channels extended to the chip edges, so that the by-product gases can be directed to outside the bonding interface to the chip edge during post bonding annealing. However, for some close-loop structures, such as microrings, there is no way to design such IPOS. In order to solve such issue, VOC is proposed by etching some array of holes down to the BOX layer. The generated by-product gases can migrate to the closest VOC and are absorbed by SOI BOX. As both IPOS and VOC can be formed during the waveguide etching, there is no particular design requirement from the fabrication point of view. However, as the formation of such outgas channels affects the silicon layer

Table 1 | Representative demonstrations of hybrid silicon lasers through wafer bonding technology.

Laser types	Bonding type	Waveguide scheme	Performances						Reference
			λ (nm)	*T* (°C)	I_{th} (mA)	P_{out} (mW)	SE (mW/mA)	Z_t (°C/W)	
Fabry–Perot laser	Molecular bonding	Hybrid WG (75 vs. 3% mode confinement within Si WG and QW)	1577	CW @ 15	65	1.8	0.013[a]	40	Fang et al. (2006)
DBR laser	Molecular bonding	Hybrid waveguide with inverse taper (66 vs. 4.4% mode confinement within Si WG and QW)	1569	CW @ 15	65	11	0.088[a]	40	Fang et al. (2008a,b,c)
	D2W molecular bonding with oxide interlayer	Hybrid waveguide with adiabatic mode transformer	1570	Pulse @ 20	100	7.2	0.021[a]	–	Ben Bakir et al. (2011)
	W2W molecular bonding with oxide interlayer	Hybrid waveguide with inverse taper, thermal tunable microring for wavelength tuning	1553	CW @ 20	40	4	0.025[a]	–	Keyvaninia et al. (2013a,b,c)
	Metal-assisted D2W bonding	III/V gain material butt-coupling with Si waveguide through a waveguide coupler	1562	CW @ 20	41	8	0.038	21	Creazzo et al. (2013)
DFB laser	Molecular bonding	Hybrid waveguide with inverse taper (59.2 vs. 5.2% mode confinement within Si WG and QW)	1600	CW @ 10	25	5.4	0.072[a]	132	Fang et al. (2008a,b,c)
	D2D BCB adhesive bonding	Hybrid waveguide (70 vs. 3% mode confinement within Si WG and QW)	1308	CW @ 20	20	2.1	0.026	–	Stanković et al. (2011)
	Selective-area metal bonding	Hybrid WG (94% mode confinement within Si)	1554	Pulse @ RT	35	3	0.05	–	Hong et al. (2010)
Microdisk laser	D2W molecular bonding	InP microdisk laser light vertically coupling to Si WG	1590	CW @ 20	0.9	0.012	0.008	–	Van Campenhout et al. (2008)
Microring laser	Molecular bonding	Racetrack microring, hybrid waveguide	1590	CW @ 15	175	29	0.089	–	Fang et al. (2007a,b)
	Molecular bonding	Hybrid microring with side coupled Si WG	–	CW @ 10	7.5	2.5	0.2	–	Liang et al. (2011)

[a] *Data are extracted from the power–current curves.*

pattern density, which will finally affect the bonding strength, it is desirable to take into account the design tradeoff between the bonding strength and the gas removal effectiveness.

Alternatively, plasma-assisted D2W molecular bonding has also been investigated for hybrid silicon lasers mainly by LETI. For large-scale manufacturability for potential massive production, the key enabling capability is the multiple dies to wafer bonding with high yield. Kostrzewa et al. (2006) first demonstrated a molecular bonding of multiple InP dies to a 200 mm silicon CMOS wafer with only 1 mm × 1 mm die size (Kostrzewa et al., 2006). For strong hydrophilic molecular bonding, both InP and silicon wafers were covered with oxide layer. Pick-and-place technology was used in order to align the InP dies to specific spots in silicon wafer, as well as to supply mechanical force to the dies through pick-and-place head. Using such D2W bonding, they demonstrated electrically pumped microdisk lasers integrated with a silicon waveguide circuit (Van Campenhout et al., 2007). However, in such D2W bonding, as the cleaning of the dies is performed ahead of the pick-and-place process, the bonding surface could be contaminated, and subsequently affecting the bonding quality and bonding yield. Furthermore, with the consideration of the pick-and-place time of 30 s/die, it takes approximately an

hour for bonding 100 dies. Such long bonding time through pick-and-place process for individual die would cause the bonding surface deactivation for the molecular bonding with plasma activation.

BCB-assisted D2W adhesive bonding can address such issue with potential capability of bonding unlimited number of dies. Stanković et al. (2010) demonstrated such D2D adhesive bonding technology using BCB. The BCB is first spin-coated on silicon wafer with controlled thickness of <100 nm in order to ensure the vertical light coupling efficiency, followed with die attaching and subsequent curing at 240°C for 1 h in a nitrogen atmosphere at 1000 mbar. With the assistant of BCB adhesion, the stringent requirements of contamination-free and smooth bonding surfaces for molecular bonding are relieved significantly. Furthermore, there is, in principle, no limitation for multiple dies bonding by the assistance of BCB adhesive layer (Keyvaninia et al., 2012). Through such bonding method, various hybrid lasers, including FP laser (Stanković et al., 2011), DFB laser (Stanković et al., 2012), microring and AWG integrated multi-wavelength DBR lasers (Keyvaninia et al., 2013a,b,c), and microdisk laser (Mechet et al., 2013) have been demonstrated. However, although such adhesive bonding is with good robustness and bonding strength, the thermal dissipation could be a major problem due to the low thermal conductivity of the BCB layer. Besides, robust polymer coating process ensuring the controllable BCB thickness is also very important.

Apart from these three major bonding methods, metal-assisted adhesive bonding (Hong et al., 2010; Tanabe et al., 2010; Creazzo et al., 2013) is another one that can be used for hybrid laser integration. However, due to the potential metal contamination and the non-compatibility with the subsequent fabrication process, such as acid etching for substrate removal, the metal-assisted adhesive bonding method might not be an optimal choice for silicon heterogeneous optoelectronic integrated circuits.

In **Table 2**, we summarize and compare these four different bonding methods.

OUTLINE OF THE MANUSCRIPT

The rest of the submission is organized as follows. In the Section "III/V-to-Si Wafer-to-Wafer (W2W) Bonding Technology," we show a demonstration of the wafer-to-wafer bonding by using low-temperature plasma-activated molecular bonding method with oxide as the bonding interlayer. In the Section "High-Throughput Multiple Dies-to-Wafer Bonding Technology," we propose and show the demonstration of an alternative bonding technology that can perform high-throughput D2W bonding for potential massive production of silicon hybrid lasers, which is based on a batch process to simultaneously bonding all the dies to the silicon wafer. In the Section "Design of III/V-on-Si Lasers," we provide some design guidelines of hybrid silicon laser, including the design of III/V multiple quantum wells (MQW) structures, the silicon waveguide thickness selection for hybrid laser, and the design of the vertical coupling structures. The Section "Demonstration of III/V-on-Si Hybrid Lasers" shows some hybrid silicon laser demonstrations using the bonded wafers from the proposed high-throughput D2W bonding, including FP laser, lateral-coupled distributed-feedback (LC-DFB) laser with side wall grating, and MLL. The Section "Summary and Future Outlook" summarizes this paper and addresses some of the future challenges.

III/V-TO-Si WAFER-TO-WAFER BONDING TECHNOLOGY

We have started the development of wafer bonding technology for hybrid silicon photonics integration in 2011. Considering the complete integration with existing silicon photonic integrated circuit, which consisting various silicon passive waveguide devices, high-speed modulator, and photodetectors, and are normally

Table 2 | The major bonding technology for hybrid integration.

Bonding methods	Process description	Fabrication tolerance	Manufacturing scalability	Comments
W2W molecular bonding	O_2 plasma-assisted direct bonding with 12 h annealing at 300°C	Small tolerance of contamination-free, smooth, and flat bonding surfaces	Difficult due to wafer size mismatch	Low utilization of both III/V and silicon wafers Sensitive to the wafer bowing
D2W molecular bonding	O_2 plasma-assisted bonding with oxide interlayer and 3 h annealing at 250°C	Small tolerance of contamination-free and smooth bonding surfaces	Difficult due to contamination and surface deactivation during pick-and-place process for large number of dies bonding	Difficult to ensure high yield with large number of dies bonding
BCB-assisted D2W adhesive bonding	BCB adhesive bonding with post curing of 1 h at 240°C	Large tolerance with low requirement on the bonding surface. Yet it requires controllable polymer coating regarding the thickness and flatness	Easy to be scalable with multiple dies and large-sized wafers	Thermal dissipation problem due to the low thermal conductivity of the BCB layer
Metal-assisted adhesive bonding	Metal-assisted bonding with annealing	Large tolerance with low requirement on the bonding surface. However, potential metal contamination, and process incompatibility. Potential coupling problem due to the metal absorption	Easy to be scalable with multiple dies and large-sized wafers	Enhanced thermal resistant due to the metal utilization

with thick oxide cladding, we adopt the low-temperature plasma-activated molecular bonding method (Pasquariello and Hjort, 2002) with oxide as the bonding interlayer. Furthermore, such thick cladding oxide also serves as the diffusion and absorption medium for the bonding by-products gases, thus with enhanced bonding quality and bonding yield.

For the initial development, we deposit 1.1 μm PECVD oxide on top of silicon wafers, followed with chemical mechanic polishing (CMP) to remove 100 nm oxide in order to ensure the smooth bonding interface. For all the bonding process described hereafter, we will use the similar PECVD oxide as cladding followed with CMP to smooth the bonding surface. Thus, we characterize and compare the oxide properties in terms of wafer-level uniformity and surface roughness before and after CMP. **Figures 1A,B** show the wafer-level oxide thickness before and after CMP. The non-uniformity is only ~1% after CMP, which suggests a very flat surface. **Figures 1C,D** show the AFM results before and after CMP. As deposited, the surface is relatively rough, with RMS of ~2.5 nm, while after CMP, the surface roughness is reduced significantly with RMS of ~0.4 nm, which is more suitable for wafer molecular bonding (Christiansen et al., 2006).

The bonding process starts with the wafer cleaning, separately for silicon wafer and III/V wafer. First, standard SPM clean for 10 min is performed to the silicon wafer in order to remove any organic contaminants, followed with 5 min SC1 clean with megasonic to remove any particle on the surface. The III/V wafer is separately cleaned in the NH_4OH solution (NH_4OH:DI water = 1:15) for 1 min. Second, O_2 plasma activation in a RIE chamber is performed for both silicon wafer and III/V wafer, subsequently followed with DI water rinse. These two bonded wafers are then physically contacted with each other immediately after drying and placed inside to the EVG 520 bonder for pre-bonding under N_2 for 3 min with 1000 N mechanic force. After that, post bonding annealing at 300°C in vacuum is applied to the bonded pair for 12 h. **Figure 2A** shows the optical image of a 50 mm InP wafer bonding to a 200 mm silicon wafer before unloading from the bonder track.

The bonded wafers are first characterized by scanning acoustic microscope (SAM) using Sonix HS3000. **Figure 2B** shows the typical CSAM image for the bonded wafer. We observe that larger than 98% of the 50 mm InP area is bonded to the silicon wafer, with only limited voids, which are attributed to the particles remaining on bonding surface. Besides, the bonding quality in the wafer

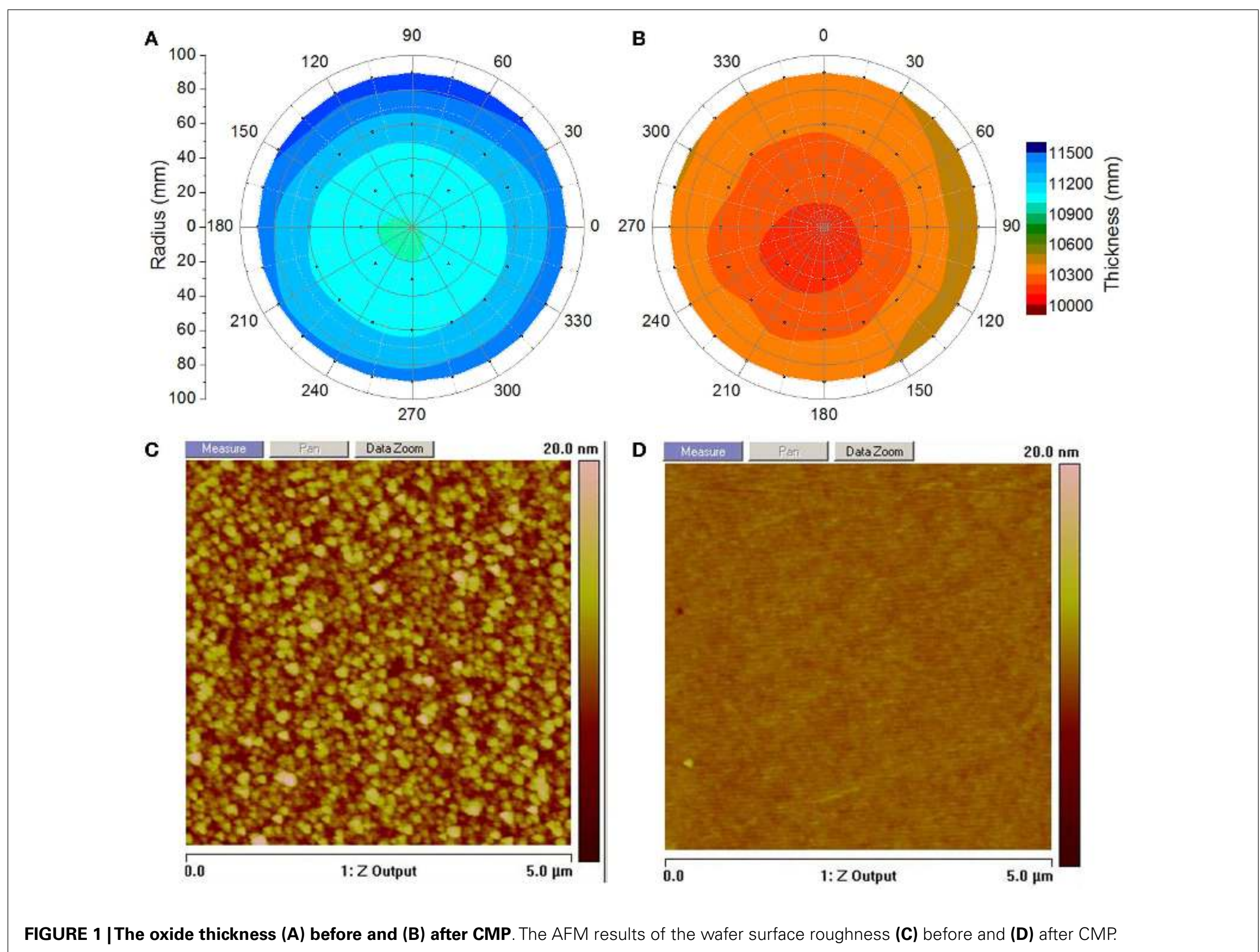

FIGURE 1 | The oxide thickness (A) before and (B) after CMP. The AFM results of the wafer surface roughness **(C)** before and **(D)** after CMP.

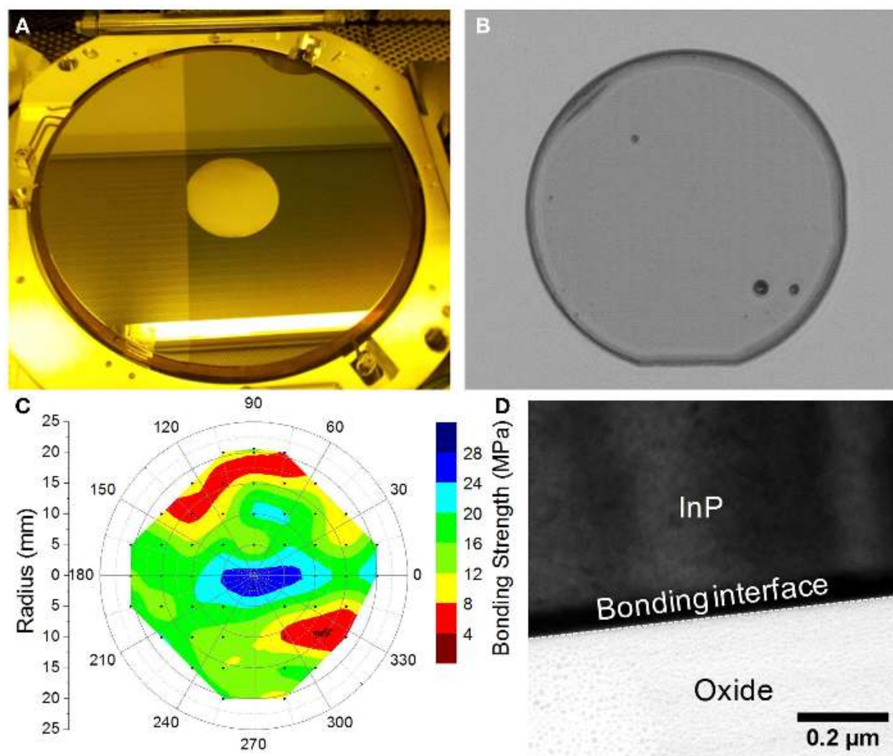

FIGURE 2 | (A) The bonded wafer before unloading from the EVG bonder. **(B)** The CSAM result. **(C)** The shear testing result. **(D)** The TEM results show the high-quality bonding interface.

periphery is also not good enough, which is due to the ring-shaped imperfection of the InP wafer.

The whole wafer is then diced into 5 mm × 5 mm dies for shear testing by using a Die Shear Tester (Dage Series 4000). **Figure 2C** shows the extracted bonding strength, with maximum bonding strength of ~30 MPa in the wafer center region, and the averaged value of 15 MPa. We believe such bonding strength is high enough for any of the post optoelectronic fabrication process. **Figure 2D** shows the TEM results of the bonded wafer, which indicate a very tight bonding between InP and oxide, again suggesting a high-quality bonding.

However, although such W2W bonding has been demonstrated with high quality, there are still existing big challenges, including:

(1) insufficient III/V wafer utilization,
(2) insufficient silicon wafer utilization due to wafer size mismatch,
(3) III/V wafer global stress-induced bonding voids.

First of all, for practical application of optical interconnection, only very small portion of the silicon waveguide area needs to be bonded with III/V material for optoelectronic fabrication to form optical lasers. With whole III/V wafer bonding, most of the III/V material will be subsequently etched away during post optoelectronic fabrication. Giving such precious III/V wafers, the insufficient utilization of the III/V material results in significantly increased device cost and waste, which in turn makes it ineffectual to use the silicon photonics though it is of low cost. Second, the main stream silicon photonics has already adopted 200 mm silicon wafers. However, due to the brittleness of the InP wafers, it is very difficult to make large-sized wafers to match with silicon wafers. Although the largest available III/V epitaxial wafer can go with 150 mm, the commercially available largest-sized III/V epitaxial wafer is only 75 mm. Thus, such wafer size mismatching definitely results in the insufficient utilization of the silicon device wafer, which in turn increased the cost. Furthermore, InP wafers with multiple quantum well structures are normally with high global stress, which induces the wafer bowing. Such stress-induced wafer bowing will easily trap the air between the bonding interfaces with remained voids, thus reducing the bonding quality.

HIGH-THROUGHPUT MULTIPLE DIES-TO-WAFER BONDING TECHNOLOGY

Based on the aforementioned W2W bonding method, we propose an alternative proprietary high-throughput multiple D2W bonding method, which is based on temporarily bonding III/V dies to a handle silicon wafer through pick-and-place process for simultaneous batch processing. Such high-throughput multiple D2W bonding method is the key enabling technique for potential manufacturability of large-scale hybrid optoelectronic integrated circuit (H-OEIC).

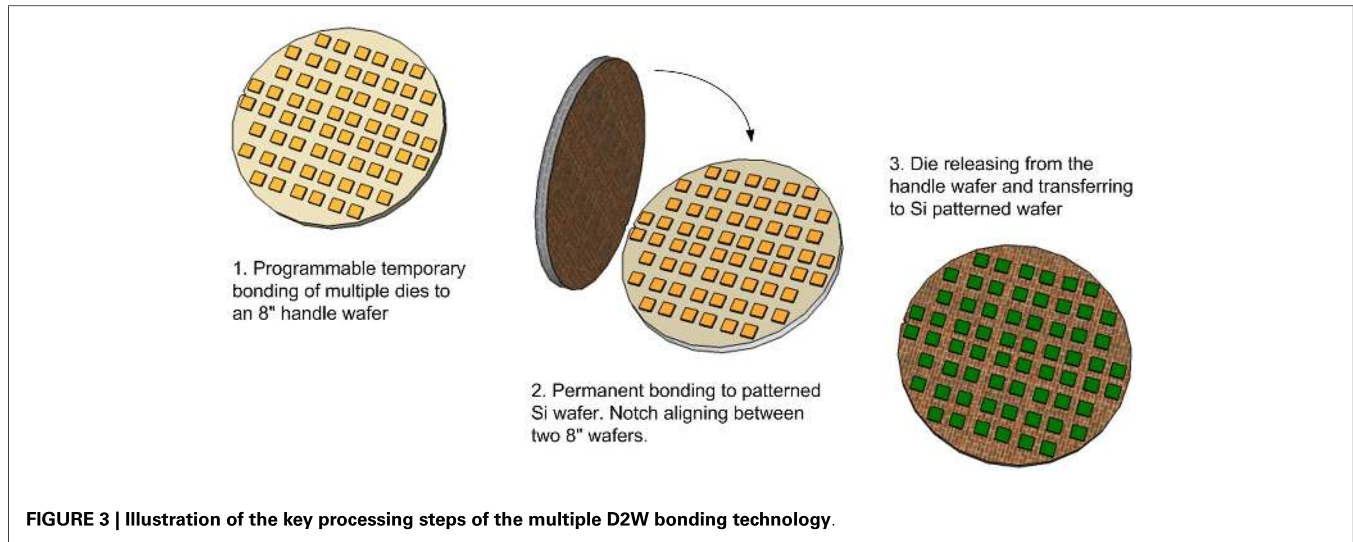

FIGURE 3 | Illustration of the key processing steps of the multiple D2W bonding technology.

Figure 3 shows the key process steps of the proposed multiple D2W bonding technology, which includes:

(a) the programmable reconfiguration of III/V dies onto a handle wafer via pick-and-place process,
(b) the D2W bonding through the notch alignment between the two 8″ wafers, after batch processing of wafer cleaning and plasma activation, and
(c) the dies releasing from the handle wafer and transferring to silicon device wafer.

The most critical step here is the choice of the adhesion layer for the temporary III/V dies bonding to the handle wafer, which includes the following two trade-off considerations.

(1) The adhesion should be strong enough to stick the III/V dies on the handle wafer without peeling off during the subsequent III/V dies batch processing, including InGaAs cap layer wet etching, pre-clean, wafer drying, and plasma activation, etc.
(2) The adhesion should not be excessively strong so that the III/V dies can be successfully released and transferred to the Si device wafer after pre-bonding.

The programmable reconfiguration of the dies onto the handle wafer is realized through pick-and-place process by predetermining the position coordinates of each die with considering the wafer-level silicon device die distribution. Unlike the pick-and-place process in flip-chip bonding, which directly bonds the dies to the actual wafer (Kostrzewa et al., 2006), the pick-and-place in our proposed method only helps to distribute the dies onto a handle wafer without flipping the chips. Thus, all the dies attached to the handle wafer can be simultaneously performed with different process steps for wafer bonding, such as InGaAs cap layer etching, wafer clean, and plasma activation.

The D2W bonding alignment accuracy is mainly determined by the notch alignment, which is performed manually and induces a relatively large misalignment of $\pm 500\,\mu m$, compared to the misalignment of only $\pm 5\,\mu m$ from the programmable reconfiguration by pick-and-place process. However, as the alignment of the III/V devices to the silicon waveguide device is determined through photolithography during optoelectronic fabrication process after wafer bonding, such misalignment can easily be compensated by adopting relatively large-sized III/V dies.

Figure 4 schematically illustrates the detailed bonding process flow starting from the preparations of silicon and III/V wafer. For either blanket silicon wafer or patterned silicon wafer with photonic devices, the wafers are cladded with PECVD oxide, followed with CMP process to smooth the bonding surface. As the hybrid laser performance is largely dependent on the vertical coupling efficiency, which is determined by the inter-layer oxide thickness, it is of very importance to control the oxide thickness by CMP process.

The preparation of the III/V dies includes the III/V wafer dicing into certain sized dies, the preparation of the adhesion layer to the handle wafer, and the programmable reconfiguration of the III/V dies temporary bonding to the handle wafer through pick-and-place process. Typically, the mechanical wafer dicing will result in edge roughness along the dicing lane, thus subsequently cause the low quality bonding near the die periphery. Besides, such dicing process may also introduce particles to the wafer surface cause contamination. Thus, a sacrificial InGaAs cap layer in order to protect the III/V bonding surface is designed in our demonstration. The applied mechanic force by the pick-and-place head also needs to be well controlled in order to ensure the successful die releasing from the handle wafer after pre-bonding. Due to the direct contact of the pick-and-place head, the die surface could be contaminated. However, owing to the sacrificial InGaAs layer, the bonding surface can be well protected without contamination or surface damage. We have checked and compared the surface condition of the III/V dies before and after the etching of the sacrificial InGaAs layer. We observe the particles on the chip surface after the wafer dicing and pick-and-place process, which is with relatively high RMS of 0.198 nm. In comparison, after the etching of InGaAs cap layer, the surface roughness is improved with reduced RMS of

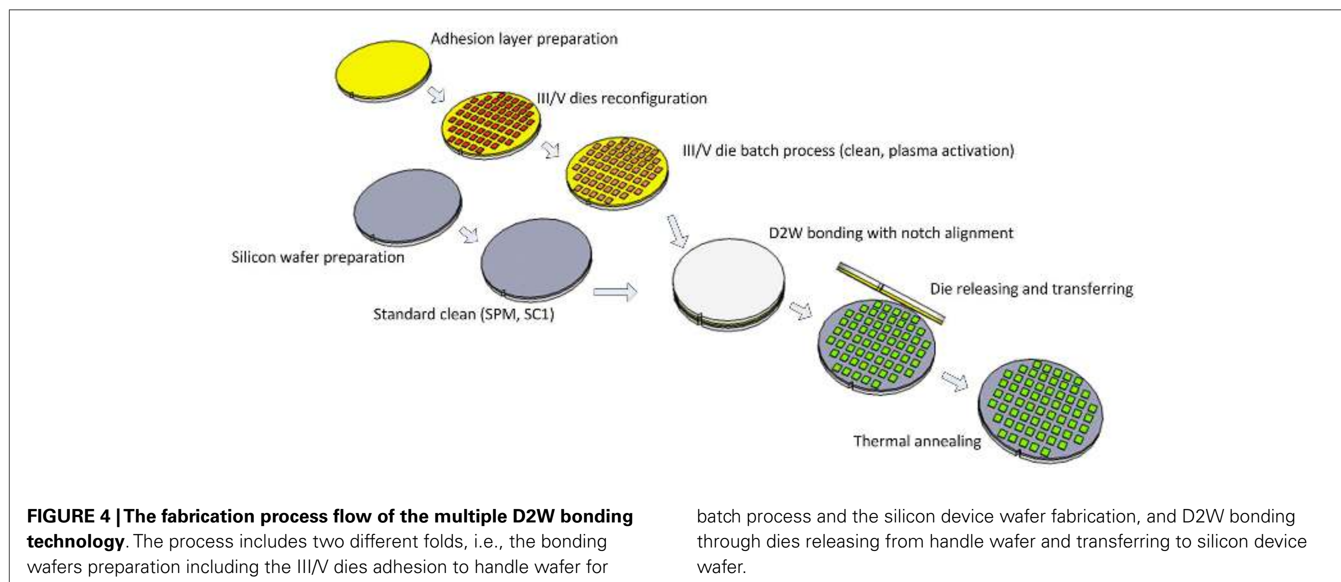

FIGURE 4 | The fabrication process flow of the multiple D2W bonding technology. The process includes two different folds, i.e., the bonding wafers preparation including the III/V dies adhesion to handle wafer for batch process and the silicon device wafer fabrication, and D2W bonding through dies releasing from handle wafer and transferring to silicon device wafer.

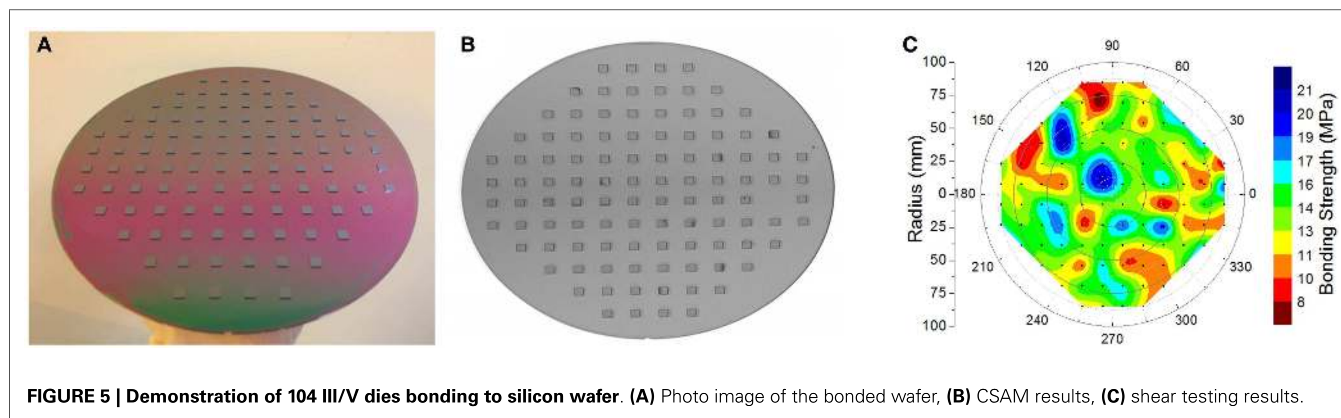

FIGURE 5 | Demonstration of 104 III/V dies bonding to silicon wafer. **(A)** Photo image of the bonded wafer, **(B)** CSAM results, **(C)** shear testing results.

0.182 nm, which is far below the required RMS of <1 nm for wafer direct bonding (Christiansen et al., 2006).

Prior the physical contact of the wafers for molecular bonding, the silicon wafer is performed with standard SPM clean for 10 min and SC1 clean with mega sonic for 5 min, while III/V die-attached handle wafer is first performed with sacrificial InGaAs cap layer etching in H_3PO4 solution for 1 min, followed with standard clean in NH_4OH solution for 2 min. After that, O_2 plasma activation is applied to both silicon wafer and III/V dies in a RIE chamber for 1 min, followed with DI water rinsing and wafer drying. The III/V dies and the silicon wafer are then physically contacted with each other by notch alignment between two 8″ wafers, followed with pre-bonding in the 200 mm EVG bonder for 2 min with 1000 N mechanical force applied. The III/V dies are released from the handle wafer after pre-bonding, and all III/V dies are now transferred to the silicon device wafer. Finally, the bonded pairs are placed back to the EVG bonder for post-bonding annealing at 300°C for 12 h.

As a proof-of-concept demonstration, we show here the bonding of 104 InP dies to an 8″ silicon wafer. The silicon wafer is covered with 1 μm PECVD oxide after CMP. The InP dies are diced into 5 mm × 5 mm in size. **Figure 5A** shows the photo image of the bonded wafers with nearly all InP dies are successfully bonded to the silicon wafer. The only missing piece is peeled off during pick-and-place process. The CSAM shown in **Figure 5B** suggests a successful bonding. The dark areas, which suggest less strong bonding, come from the dies located in the InP wafer edge. **Figure 5C** shows the sheer testing results. The maximum bonding strength is larger than 20 MPa, with an averaged bonding strength of ~13 MPa, which is comparable with that of W2W bonding under the same process.

All in all, we believe that there are at least two significant implications of the proposed multiple D2W bonding technology:

(1) The significantly increased bonding efficiency owing to the simultaneous batch process. Through the batch process of the III/V dies (pre-clean, plasma activation, etc.), it is possible to bond unlimited number of dies. It also helps to avoid potential contamination by performing the pick-and-place before cleaning process, and eliminates the time link constraint of the bonding surface deactivation. This is the most significant processing advantage comparing to the conventional pick-and-place method.

(2) The scalability to whatever-sized silicon wafers. Such multiple D2W bonding technology can easily be adopted for even larger-sized silicon wafers, such as 300 mm wafer. This is the most critical step toward the potential manufacturability of H-OEIC.

DESIGN OF III/V-on-Si LASERS

A hybrid III/V-on-silicon laser consists of a III/V epitaxial-layered structure and a silicon waveguide. It is a device that emits laser beams from silicon waveguides by electrical/optical injection to the III/V region. In this section, we will discuss the design of hybrid III/V-on-silicon lasers with regard to two fundamental laser elements, namely, optical gain medium and optical waveguide cavity.

DESIGN OF III/V MQW STRUCTURES

There are two main material systems for the fabrication of long-wavelength lasers emitting at 1.55 μm, which are InGaAsP/InP and InGaAlAs/InP systems. Both kinds of materials can be used to fabricate hybrid lasers. InGaAlAs MQWs exhibit a larger conduction band discontinuity ($E_c = 0.72E_g$), and smaller valence band discontinuity compared with InGaAsP MQW. This leads to an improved electron confinement, which can improve the temperature characteristics of semiconductor laser diodes. Thus, InGaAlAs/InP material system is more suitable for high speed and uncooled operation of semiconductor laser diode. In this study, we select this material system for the hybrid silicon lasers demonstration. The MQW region includes eight $Al_{0.055}Ga_{0.292}In_{0.653}As$ quantum wells separated by nine $Al_{0.055}Ga_{0.292}In_{0.653}As$ barriers. The gain spectrum of the MQW is calculated and the wavelength of peak gain is designed at 1550 nm when the carrier injection density increases from 5×10^{17} to $5 \times 10^{18}/cm^3$ as shown in **Figure 6A**. **Figure 6B** shows the measured photoluminescence (PL) spectrum for III/V epitaxial wafer at room temperature with the peak wavelength at about 1550 nm.

DESIGN OF HYBRID LASER VERTICAL WAVEGUIDE STRUCTURE

As mentioned, the optical gain comes from overlying III/V stack layer, which needs to be structured to efficiently inject electrons or holes into the MQW regions. A high overlap between the optical mode and the MQW benefits to achieve a high optical gain, which means that the optical mode needs to be well confined in the III/V waveguide. However, on the other hand, the light has to be confined sufficiently inside the silicon output waveguide for the efficient light extraction. In view of this, there are mainly two kinds of waveguide structures considering the optical power distribution for the hybrid laser with optical mode predominantly confined either in the silicon waveguide or in the III/V overlay. This leads to two different optical cavity designs. In the first design, the optical cavity comprises both III/V and silicon waveguides and the mode is mainly guided within the Si waveguide and evanescently coupled with the III/V waveguide. Such structure is also called as overlapped structure with hybrid mode (Fang et al., 2006, 2007a,b, 2008a,b,c, 2009). It has the advantage of making the coupling to a passive silicon waveguide straightforward and wavelength selective features can easily be defined in the silicon waveguide layer using CMOS fabrication techniques, which provides an accurate mechanism to control the emission wavelength of the laser. However, it requires a controllable thin bonding layer (<50 nm) for efficient optical coupling, which may increase the difficulty of bonding process. Furthermore, due to the weak interaction between the optical mode and gain material, it usually requires longer laser cavity, and thus resulting in high power consumption. In the second design, the mode in the hybrid section is mainly guided by the III/V waveguide, and the light is coupled from the III/V waveguide to the silicon waveguide through waveguide mode transformer, such as inverse tapers (Yariv and Sun, 2007; Sun et al., 2009a; Ben Bakir et al., 2011). In such design, the bonding interface can be relatively thick (typically from 30 to 150 nm) due to the released coupling constrain for the bonding interface. The advantage is that the optical mode experiences a high optical gain in the central region of the laser structure. However, the challenge of this structure is the fabrication of low-loss tapered waveguides. Hereafter, we name such design as adiabatic tapered coupling structure.

Silicon waveguide thickness selection

The selection of the silicon waveguide thickness depends on the detailed device dimensions/structures and the fabrication process. For indium phosphide (InP)-based gain waveguides, the effective refractive index is typically larger than 3.2 if the waveguide width and height are larger than 1 μm. In order to achieve this index for silicon waveguides for effective coupling with the InP-based gain

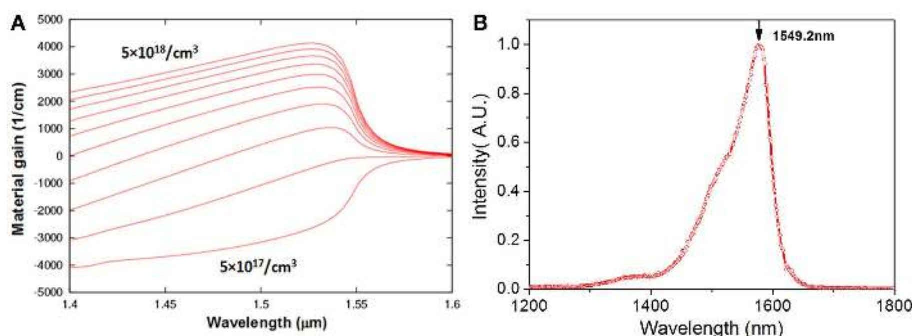

FIGURE 6 | (A) The calculated gain spectrum under different carrier injection concentration. **(B)** The measured photoluminescence (PL) spectrum for III/V epitaxial wafer.

region, the corresponding silicon waveguide thickness needs to be sufficiently large. **Figure 7** shows the calculated effective refractive index of the fundamental mode in silicon waveguide depending on the waveguide thickness. It indicates that the required silicon thickness needs to be larger than 450 nm to achieve an effective index of 3.2 for the waveguide with 2 μm in width. Such thick silicon layer does not match with the current mainstream silicon photonics. However, on the other hand, it is still possible to couple light from 220 nm silicon to InP waveguides by using very narrow InP waveguides (~200 nm) to push down the value of effective index, although the fabrication is difficult to form these narrow InP waveguides by conventional photolithography.

Overlapped structure with hybrid mode

As mentioned above, there is a tradeoff between the optical mode confinement in the III/V and silicon regions for the overlapped structure. The bonded III/V-Si structure forms the hybrid waveguide cavity. The effective refractive index of III/V active and Si regions are critical parameters for the hybrid waveguides, which, respectively, determine the light confinement factors in III/V and Si region. In our design, the confinement factors over the silicon and the quantum well regions are modified by altering the silicon waveguide thickness and the separate confinement heterostructure (SCH) thickness in order to ensure sufficiently low-threshold gain for lasing. While the thicker silicon waveguide pulls the optical mode into the silicon layer, the larger SCH thickness can drag back the optical mode into the III/V region.

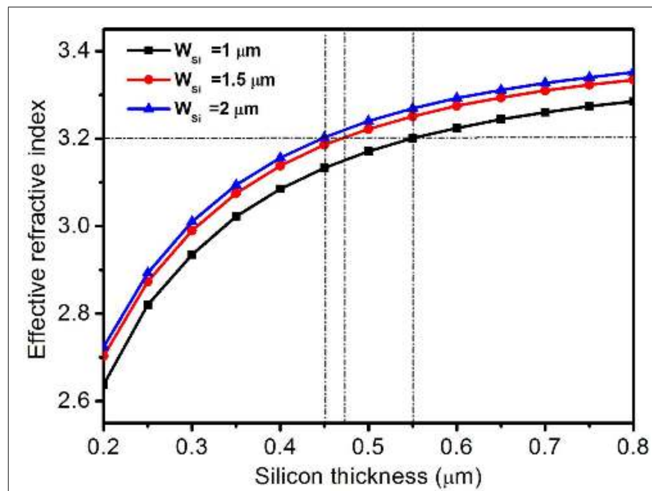

FIGURE 7 | Effective refractive index of the silicon waveguide fundamental mode as the function of silicon waveguide thicknesses. Both top and bottom claddings are oxide ($n = 1.45$) and silicon index is chosen as 3.48 at the wavelength of 1550 nm.

Figure 8A shows the calculated optical confinement factors in MQW and Si depending on the Si waveguide width under different Si thickness, with assuming the III/V ridge width and the SCH thickness of 6 μm and 250 nm, respectively. It shows that when the waveguide widths of III/V and Si are fixed, the optical confinement in Si waveguide can be increased by using a thick Si layer. With the silicon waveguide thickness of 700 nm, large confinement of up to 70% in silicon waveguide is achieved. However, the device performance is very sensitive to the bonding interface quality due to the overlapping of the optical mode with the bonding interface between the III/V and the silicon. Based on the analysis, we adopt silicon thickness of 500 nm for the demonstration of hybrid Si lasers.

Figure 8B shows the simulated optical confinement factor in MQW and in silicon waveguide with different SCH thickness, with the fixed III/V and Si waveguide widths of 4 and 2 μm, and Si waveguide thickness of 500 nm. As the SCH thickness increases, the optical mode confinement in III/V region increase, which in turn significantly decreases the optical mode confinement in silicon waveguide. Inserts in **Figure 8B** show the simulated field distributions with SCH thicknesses of 0.1 and 0.5 μm. It shows obviously that for the small SCH thicknesses, the optical mode lies primarily in the silicon region, while the optical mode is dragged into III/V region with increased SCH thickness. The ability to control the optical mode with the SCH thickness is a key feature of this platform. For hybrid lasers, higher optical confinement is needed to achieve lower threshold current. Thus, we choose an optimized SCH thickness of 0.18 μm for the hybrid lasers.

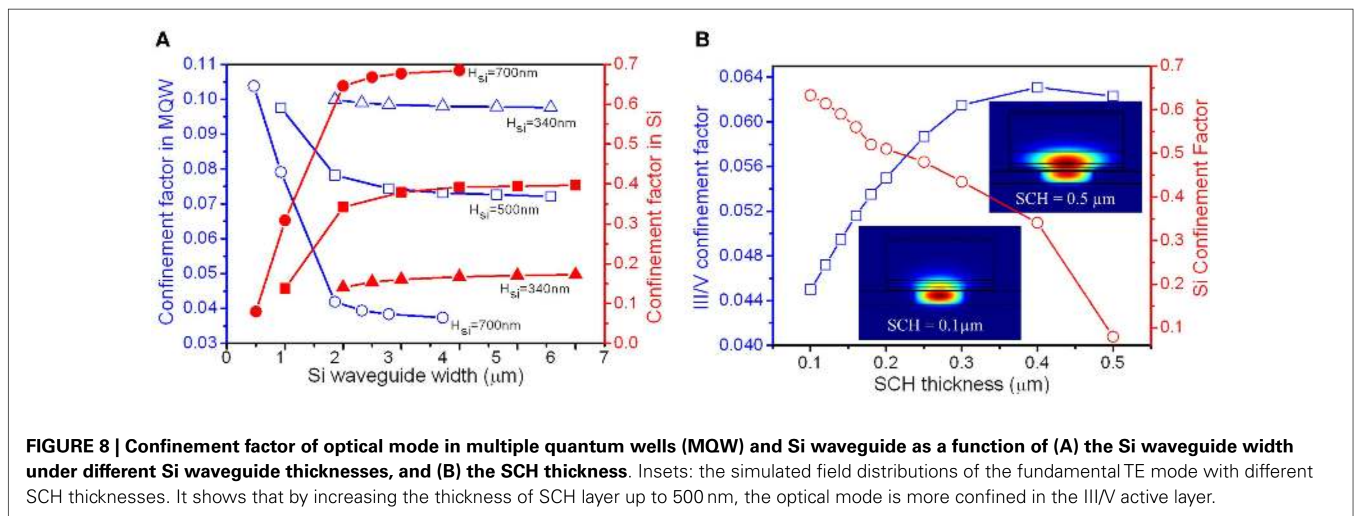

FIGURE 8 | Confinement factor of optical mode in multiple quantum wells (MQW) and Si waveguide as a function of (A) the Si waveguide width under different Si waveguide thicknesses, and (B) the SCH thickness. Insets: the simulated field distributions of the fundamental TE mode with different SCH thicknesses. It shows that by increasing the thickness of SCH layer up to 500 nm, the optical mode is more confined in the III/V active layer.

For such hybrid III/V-on-silicon lasers, another challenge arises from the control of the bonding layer thickness. Generally, a thin bonding layer (<50 nm) is needed for efficient optical coupling between III/V and silicon regions, while the thicker bonding layer benefits to the bonding quality of III/V layer and the bonding yield improvement. For direct bonding without oxide interlayer, it is easy to achieve such thin thickness, which is usually only the native oxide. However, this process is particularly sensitive to surface roughness and particles contamination, which would limit the bonding quality and bonding yield. DVS-BCB bonding can be used for the heterogeneous integration of III/V material on silicon to improve the yield. However, it is difficult to obtain a controllable thin bonding interlayer of <50 nm. In our case, we choose silicon oxide as interlayer between III/V and silicon, which is also compatible with the mainstream silicon phonics, in which all the devices are with oxide cladding.

Figure 9A shows the calculated optical confinement factor in MQW and silicon waveguide as the function of interlayer oxide thickness. In the simulation, we assume the fixed silicon thickness of 500 nm, the silicon waveguide width of 3 μm, and III/V ridge waveguide with of 6 μm. We observe from the results that the Si confinement factor largely decreases when the interlayer thickness increases from 10 to 100 nm. Only approximately 5% optical light is confined in the silicon waveguide when the interlayer thickness is 100 nm.

Additionally, the interlayer of oxide at the bonding interface also affects the characteristics temperature of hybrid III/V-on-silicon laser due to the poor thermal conductivity of as low as 1.3 W/m/K. The modal gain of laser is dependent on the temperature of the active region. As the temperature of active region increases, the modal gain decreases due to the increased carrier leakage out or not reaching the active region, and/or increased non-radiative recombination. The decrease of modal gain leads to high threshold current and low output optical power. In order to investigate the effect of interlayer on the thermal characteristics of the hybrid lasers, a two-dimensional model of the device structure is conducted using COMSOL by mapping out the heat dissipation of each layer. **Figure 9B** shows the simulation structure. In the simulation, the structure parameters are as follows: III/V ridge width, Si ridge width and thickness, and the laser cavity length are assumed to be 6 μm, 1 μm, 500 nm, and 1000 μm, respectively. Injection current is 500 mA and the corresponding voltage is 4 V. **Figure 9C** shows the calculated working temperatures in the III/V active region with different thicknesses of the oxide interlayer. The increase of temperature in the III/V active region versus interlayer thickness is about 0.02 K/nm. For illustration purpose, **Figure 9D** shows as an example the thermal distribution within the layered structure for the oxide interlayer thickness of 0 nm. The thermal distributions for the other thicknesses are similar. Actually, we can conclude from the study that the main hurdle for the heat dissipation is the SOI BOX layer, which can be seen from the results without oxide bonding interlayer (thickness = 0 nm). Thus, for enhanced thermal management, novel designs such as thermal shunt (Liang et al., 2012) are required to effectively remove the generated heat.

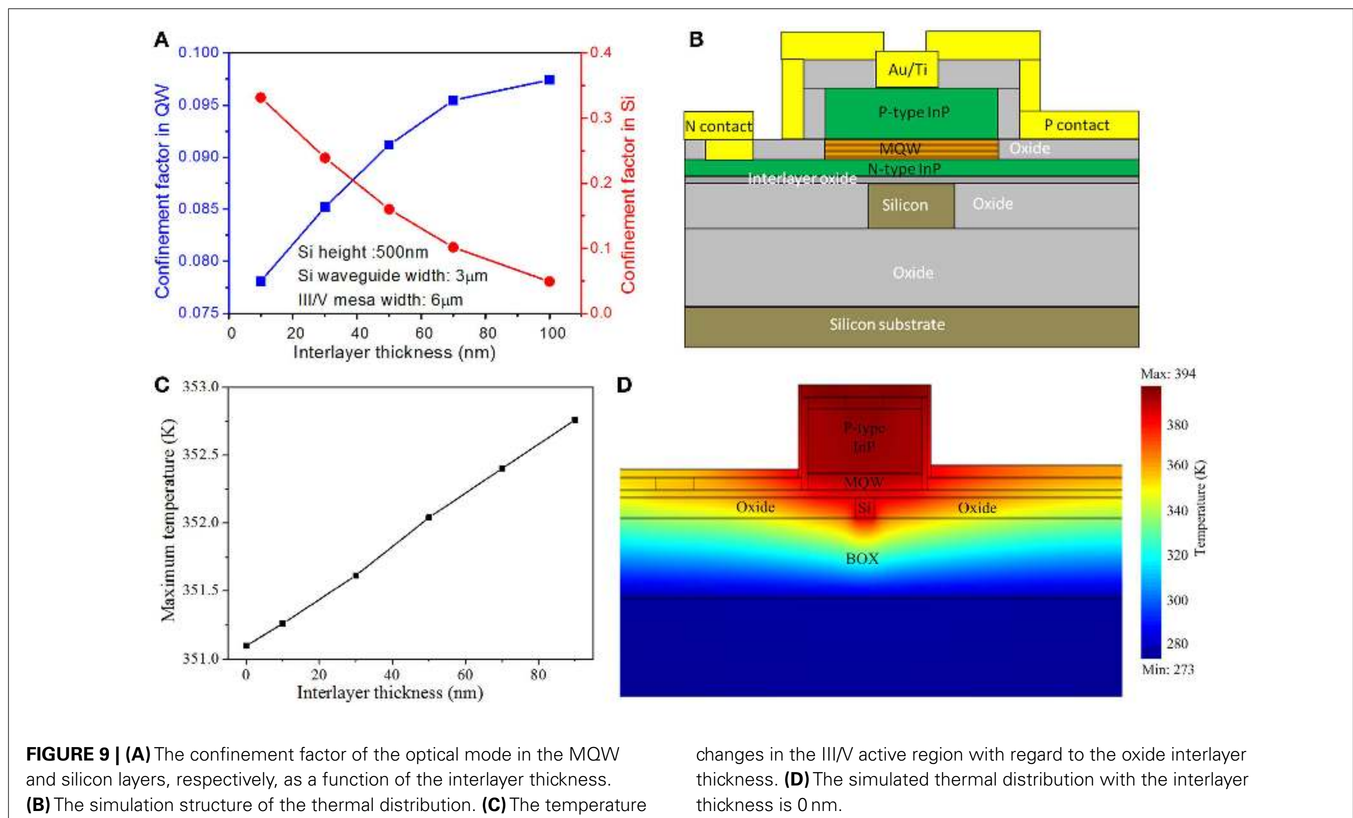

FIGURE 9 | (A) The confinement factor of the optical mode in the MQW and silicon layers, respectively, as a function of the interlayer thickness. **(B)** The simulation structure of the thermal distribution. **(C)** The temperature changes in the III/V active region with regard to the oxide interlayer thickness. **(D)** The simulated thermal distribution with the interlayer thickness is 0 nm.

Adiabatic tapered coupling structure

For the adiabatic tapered coupling structure, the mode in the hybrid section is mainly guided by the III/V waveguide, and the light is coupled from the III/V waveguide to the silicon waveguide through a tapered waveguide. It shows that a tapering length ~100 μm is required for a sufficient light coupling with minimized optical loss. By using such tapered coupling, it eliminates the tricky tradeoff between the modal gain and vertical coupling efficiency, which is inherent in the overlapped waveguide structures. Therefore, hybrid lasers with a short cavity as pure III/V laser are possible. Up to now, the hybrid lasers with the high performances are achieved using such tapered coupling scheme (Levaufre et al., 2014; Zhang et al., 2014).

In order to efficiently couple the light between the Si-III/V hybrid waveguide and the silicon waveguide, the III/V waveguide and silicon waveguides are tapered simultaneously in the same direction. Here, we adopt a three-dimensional approximated model based on beam propagation method (BPM) in order to optimize the tapering structure of the silicon waveguide and III/V waveguide for an efficient coupling. **Figure 10A** schematically illustrates the design of such waveguide tapering structure. The coupling efficiency largely depends on the tapering design, especially the III/V waveguide taper width and taper length. Here, we simulate such dependency by varying the taper width and taper length, while fixing the III/V waveguide width of 5 μm, the silicon waveguide width of 1 μm, and the silicon taper length of 100 μm.

Figures 10B,C, respectively, show the simulated coupling efficiency from III/V-Si hybrid waveguide to silicon waveguide as functions of the III/V waveguide taper width and tape length. It suggests that the coupling efficiency from III/V-Si hybrid waveguide to Si waveguide can be as high as 85% by using an 80-μm-long III/V waveguide taper and a 100-μm-long silicon waveguide

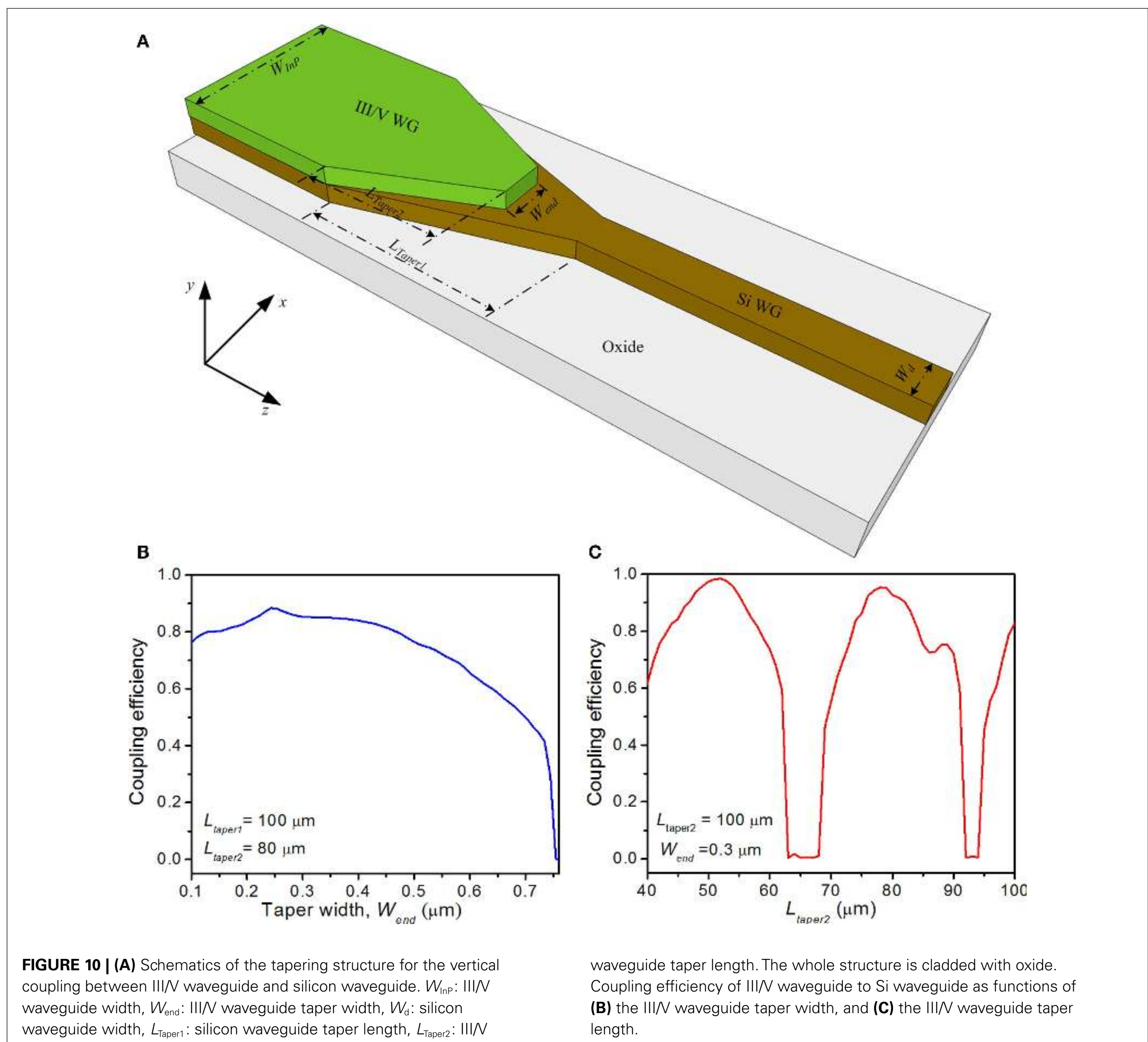

FIGURE 10 | (A) Schematics of the tapering structure for the vertical coupling between III/V waveguide and silicon waveguide. W_{InP}: III/V waveguide width, W_{end}: III/V waveguide taper width, W_d: silicon waveguide width, L_{Taper1}: silicon waveguide taper length, L_{Taper2}: III/V waveguide taper length. The whole structure is cladded with oxide. Coupling efficiency of III/V waveguide to Si waveguide as functions of **(B)** the III/V waveguide taper width, and **(C)** the III/V waveguide taper length.

tape. Through optimizing the III/V waveguide taper width and III/V waveguide taper length, the maximum coupling efficiency can be as high as 99%. However, due to the optoelectronic fabrication limitation, we are not able to demonstrate the hybrid laser using such adiabatic tapered coupling structure.

DEMONSTRATION OF III/V-on-Si HYBRID LASERS

Using the proposed multiple D2W bonding technology, we have demonstrated various hybrid silicon lasers, including FP lasers, DBR lasers, sidewall-grating lasers, racetrack-shaped microring lasers, and MLL. In this section, we will first introduce the hybrid silicon laser fabrication process, leveraging on IME's CMOS-compatible silicon photonic fabrication facilities and NTU's expertise in optoelectronics fabrication capability, followed with showing some hybrid silicon laser demonstrations as the examples.

III/V-on-Si HYBRID LASER FABRICATION PROCESS

The III/V-on-Si hybrid laser fabrication in our demonstrations includes two parts, namely silicon passive device fabrication using IME's CMOS line and multiple D2W bonding in IME's MEMS line, and III/V optoelectronics fabrication in NTU. **Figure 11** shows the fabrication process flow. We adopt commercially available SOI wafer with 340 nm silicon layer sitting on a 2 μm buried oxide (BOX) layer. The fabrication starts with the blanket silicon epitaxy to ~500 nm for refractive index matching between silicon waveguide device and InP gain medium. After the deposition of 70 nm oxide as the hard mask, the waveguide structures, including both grating coupler and inverse taper coupler are patterned by deep UV photolithography and transferred onto the silicon layer by using deep RIE etching. For the grating coupler, the silicon etching thickness is 377 nm. While for other waveguide devices, second silicon etch is applied down to the BOX layer by covering the surface grating coupler area with additional photo resist. Oxide cladding of 650 nm in thickness is deposited followed by a surface planarization step, which includes oxide etch-back with 500 nm in depth and CMP process. Such planarization steps with CMP also help to smooth the bonding surface with very small surface roughness for molecular bonding. The interlayer oxide thickness can be well controlled by the CMP process, with only ~50 nm oxide left atop the silicon waveguide in our demonstration. For enhanced flatness and uniformity of the bonding surface, we only etch away the silicon surrounding the devices, remaining most of the silicon areas forming silicon plateaus.

The multiple D2W bonding is then performed after the preparation of III/V dies, followed with the process described in Section "III/V-to-Si Wafer-to-Wafer (W2W) Bonding Technology." As the designed devices are all within an area of 8 mm × 8 mm, the InP dies are all diced with 9 mm × 9 mm with the consideration of bonding misalignment of ±500 μm for the notch alignment, thus ensuring the full covering of all the silicon photonic devices within the III/V die area. For a 50 mm InP wafer, there are only 16 full dies with 9 mm × 9 mm in size. Thus, for the purpose of hybrid silicon laser demonstration using such D2W bonding technology, we only perform 16-dies bonding to 200 mm silicon wafers, with some of the silicon photonics device area being wasted. **Figure 12A** shows the photo image of the 16-dies bonded silicon wafer. **Figure 12B** shows the CSAM results. Except some particle-induced bonding defects, all the dies are bonded very well. However, we clearly observe that some of the die edge periphery regions are not bonded well due to the wafer dicing induced damage. **Figures 12C,D**, respectively, show the TEM and cross-SEM of the bonding structures, both suggesting very reliable bonding quality.

The III/V optoelectronic fabrication starts from the InP substrate removal using HCl solution. After photolithography, the InP mesa structures are formed by using H_3PO_4, H_2O_2, and HCl mixed solution to etch the InGaAs contact layer and p-InP cladding layer. The SCH layer and QW layer are also etched using H_3PO_4:H_2O_2:H_2O solution, stopping on the n-InP cladding layer.

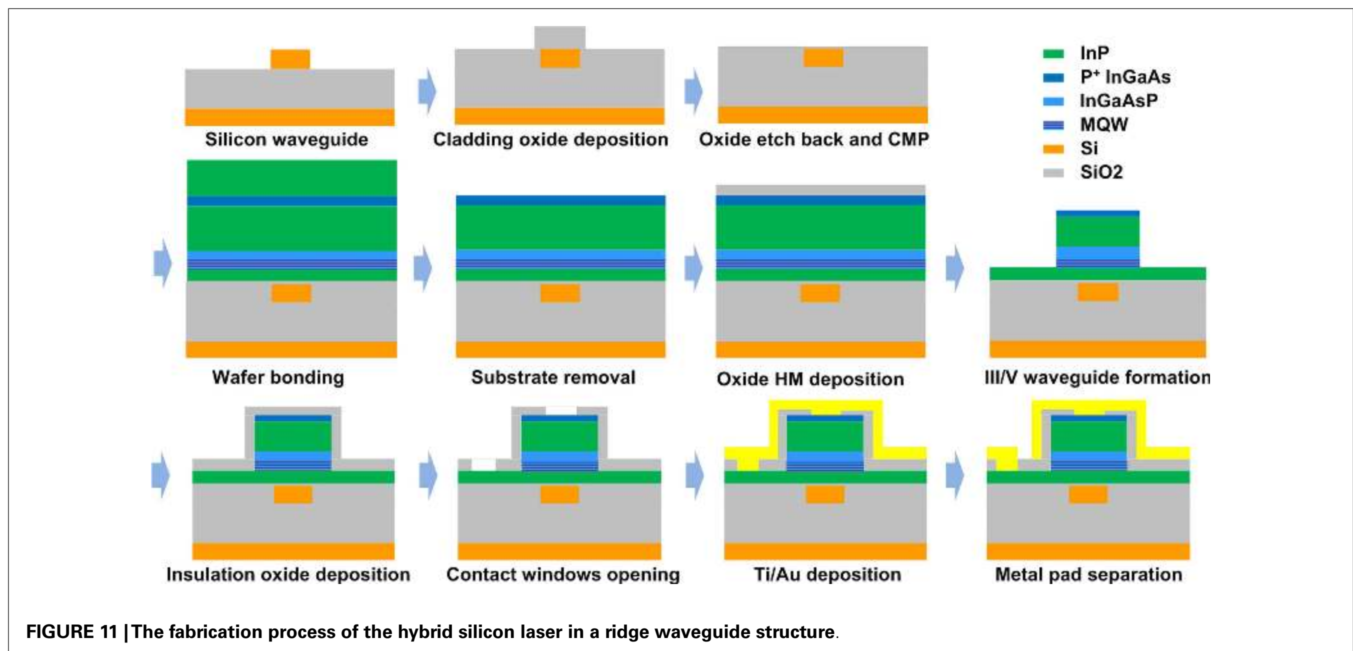

FIGURE 11 | The fabrication process of the hybrid silicon laser in a ridge waveguide structure.

Then, an SiO_2 insulator layer with the thickness of 300 nm is deposited, followed with the contact opening for p-type and n-type injection by one-time photolithography and the oxide is etched by HF solution. After that, Ti/Au metal contacts are formed by sputtering, with wet etching to form a Ti/Au slot between the n-type and p-type contacts using diluted HF and KI solution, respectively.

FABRY–PEROT LASERS

The CW operation of the optical laser requires good thermal management to remove the generated heat. In the case of FP lasers, another way is to design narrow ridge waveguide to generate less heat. In our demonstration, we design a FP laser with ridge waveguide width of 6 μm. The laser facets are formed by lapping down the Si substrate to around 60 μm, followed with mechanical cleaving. The length of the FP laser is ~720 μm. The demonstrated FP laser is able to work at room temperature with CW operation. **Figure 13A** shows the measured *P–I* curves under different temperatures. The threshold current at 264 K is ~45 mA, and increases significantly to ~100 mA at room temperature. We attribute such fast increase of the threshold to the thick oxide interlayer, which prohibits the heat dissipation efficiently. The measured output power from a single facet without any reflection coating is more than 1 mW. This includes the coupling loss due to the un-optimized testing setup for light collection, which is estimated only with ~20% light collection efficiency. The thermal dissipation is very important for CW lasing. **Figure 13B** shows the measured lasing spectra under different temperatures. The wavelength shift with temperature is about 0.75 nm/K.

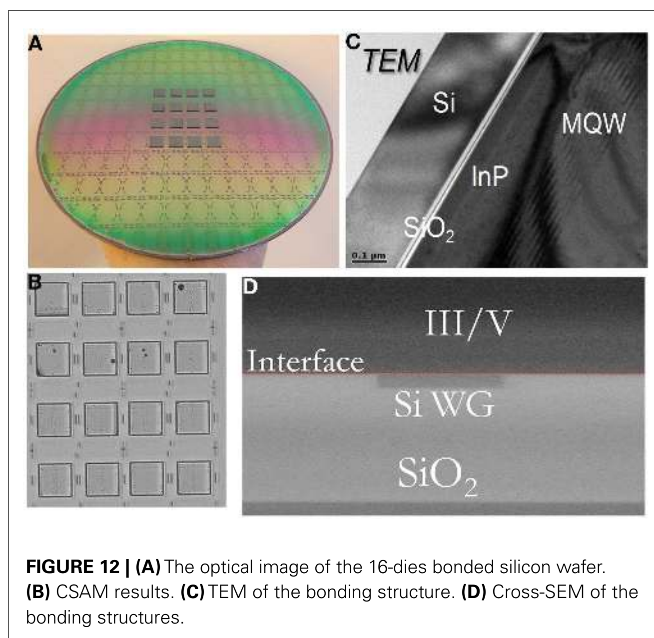

FIGURE 12 | (A) The optical image of the 16-dies bonded silicon wafer. **(B)** CSAM results. **(C)** TEM of the bonding structure. **(D)** Cross-SEM of the bonding structures.

LATERAL-COUPLED DISTRIBUTED-FEEDBACK LASERS WITH SIDE WALL GRATING

The FP laser is fabricated by lapping down the silicon substrate and mechanical cleaving to form the facets. From the optical communication and optical interconnect applications point of view, such FP lasers are not practical for photonic integration. Furthermore, how to achieve good facet is still a main challenge and a key limiting factor for high-performance hybrid lasers as reflection coating is always required in order to optimize the cavity transmission and reflection. In view of this, optical resonators, Bragg grating structures that form the cavities through fabrication are the good candidates for on-chip hybrid laser. We here show as an example of a hybrid laser using LC-DFB structure as the laser cavity.

Figure 14A schematically shows the perspective view of the LC-DFB hybrid laser with illustration of the key parameters, including the Bragg grating period Λ, the silicon ridge width *D*, and the grating teeth width, W_1. Considering the fabrication limitation, we design third-order later Bragg grating in order to achieve single-mode operation. With regard to the silicon thickness of 500 nm, the grating period Λ is 670 nm with filling factor of 0.5. The ridge width *D* and the teeth width W1 are, respectively, designed with 2 and 1 μm. The Bragg grating is centered beneath the III/V gain region, which is with the width of 12 μm. Both LC-DFB structure and III/V gain region are designed with the same lengths. In order to extract the output laser light for easy characterization, the vertical grating couplers are adopted. For the vertical grating coupler, the period is designed to be 640 nm with filling factor of 0.5, and the silicon etch depth is 377 nm. Such grating coupler design is purely based on theoretical calculation, without any process

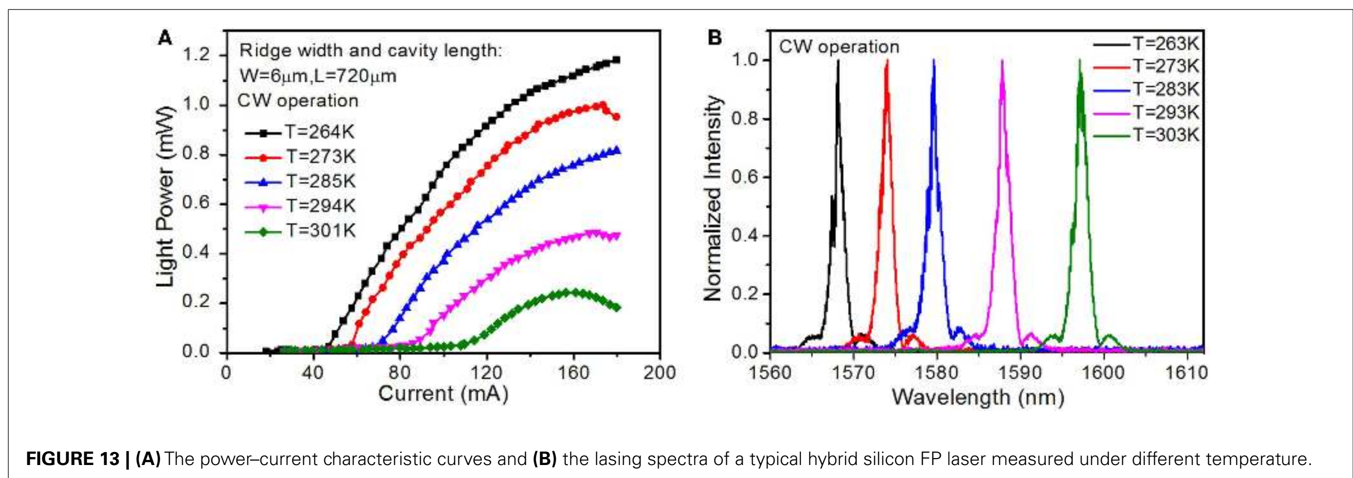

FIGURE 13 | (A) The power–current characteristic curves and **(B)** the lasing spectra of a typical hybrid silicon FP laser measured under different temperature.

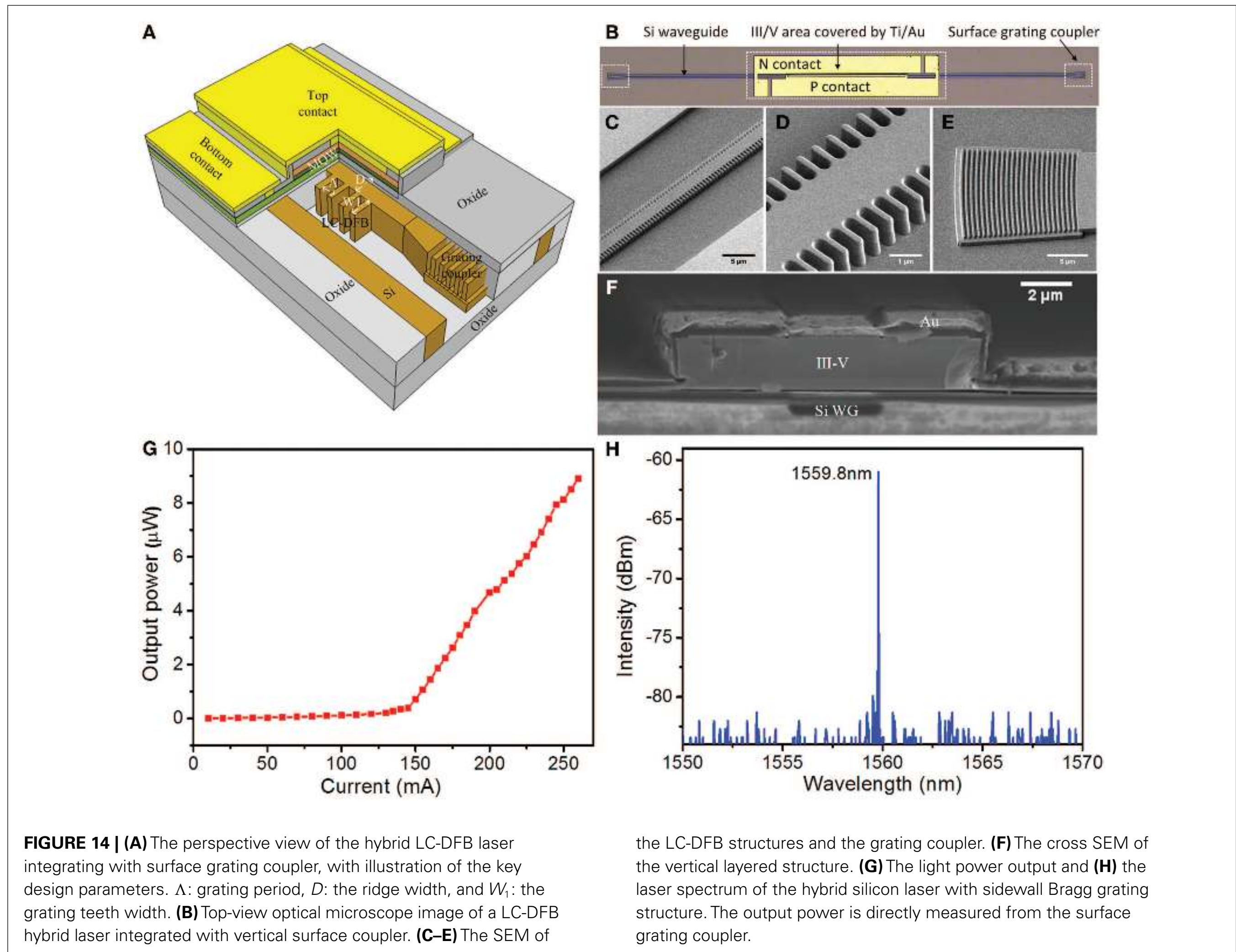

FIGURE 14 | (A) The perspective view of the hybrid LC-DFB laser integrating with surface grating coupler, with illustration of the key design parameters. Λ: grating period, *D*: the ridge width, and W_1: the grating teeth width. **(B)** Top-view optical microscope image of a LC-DFB hybrid laser integrated with vertical surface coupler. **(C–E)** The SEM of the LC-DFB structures and the grating coupler. **(F)** The cross SEM of the vertical layered structure. **(G)** The light power output and **(H)** the laser spectrum of the hybrid silicon laser with sidewall Bragg grating structure. The output power is directly measured from the surface grating coupler.

verification and optimization. For this demonstration, we did not design any mode transformer between III/V layer and silicon waveguide layer, thus expecting some transition loss. **Figure 14B** shows the optical microscope image of the fabricated hybrid LC-DFB laser with integrated vertical grating couplers. The LC-DFB structure and the III/V gain region are designed with same length of 700 μm, while the silicon device including two grating couplers is ~2750 μm. Due to the optoelectronic fabrication limitation, there is no designed taper between III/V waveguide and silicon waveguide, thus expecting relatively high transition loss. **Figures 14C–E** show the SEM images of the fabricated LC-DFB and vertical grating coupler, while **Figure 14F** shows the cross-sectional SEM of the vertical structures, illustrating the Si waveguide, the III/V layer, and the Ti/Au layer.

Figures 14G,H show the measured *P–I* curve and the spectrum of the LC-DFB hybrid laser under pulse operation. The threshold current is ~120 mA, corresponding to a threshold current density of ~1.42 kA/cm^2. From the spectrum, we see clearly single-mode operation with the peak wavelength at 1559.8 nm and a side-mode-suppression ratio (SMSR) larger than 20 dB. This is expected from the LC-DFB design. However, the maximum output power is only ~10 μW upon 250 mA current injection, which also can be observed from the spectrum measurement. We attribute the relatively low output power to the following two reasons, namely, the accumulated optical loss, and the inefficient vertical light coupling. First of all, the optical loss, which mainly includes the surface grating coupler coupling loss, the Bragg grating scattering loss, and the non-radiative recombination loss from the bonding interface, affects the light output significantly. From the reference measurement for the device only with passive silicon waveguide yet bonded III/V layer, the accumulated total loss is >40 dB, which is mainly due to the unoptimized surface grating coupler. Second, the oxide interlayer in our design, which might not be able to control precisely, will affect the light coupling efficiently from III/V layer to silicon waveguide. Furthermore, the polarization sensitivity of the surface grating coupler can also induce additional optical loss. Thus, the optimized grating coupler design for the light extraction from the silicon waveguide and the vertical light transition structure for light coupling from III/V layer to silicon waveguide can significantly increase the laser output power. Besides, by optimization of the Bragg grating period and silicon waveguide thickness, the SMSR can also be enhanced.

PASSIVELY MODE-LOCKED LASERS

Semiconductor MLLs are excellent candidates for generating stable ultra-short optical pulses, which have a corresponding wide optical spectrum of phase correlated modes and high repetition rate. Optical frequency combs emitted by MLLs can have high extinction ratios, low jitter, and low chirp, which can be utilized in a variety of applications including AWG, optical clock generation and recovery, coherent communications systems, high-speed analog-to-digital conversion (ADC), and optical time-division multiplexing (OTDM), etc. Integration of MLLs on silicon is very promising as it combines the low-loss and low-dispersion characteristics of silicon material with high gain III/V material, thus ensuring improved performance. Furthermore, it will be possible for semiconductor MLLs to generate ultra-short optical pulses with low repetition rate on the silicon platform owing to the long cavity length. Here, we show our preliminary demonstration of a passive MLL using the developed heterogeneous integration platform.

The optical cavity of the MLL is defined by a 1250-μm-long gain section, a saturable absorber (SA) with the length of 30-100μm, and cleaved facet at the waveguide end. The gain section and SA are separated by a 20 μm electrical isolation region with isolation resistance >1 kΩ. The SA is made up of the same active material as the gain section. The difference between the SA and gain section is that SA absorbs the light in the cavity upon applying a reverse bias, while the gain section amplifying light upon forward current injections.

The laser optical output is collected by a photodiode located in front of the cleaved facet. The typical threshold current with an unbiased 50-μm-long SA section is 88 mA. The device has a maximum single facet CW output power of 1 mW at room temperature when the injection current is 140 mA. The series resistance is about 8.5 Ω, while the slope efficiency is about 0.02 mW/mA. **Figure 15A** shows the measured optical spectra at different injection currents. It shows that the widest optical emission is centered at about 1605 nm with a full-width at half-maximum (FWHM) of 5.4 nm at the injection current of 110 mA measured by an optical spectrum analyzer (OSA). Assuming the generated optical pulse is chirp-free and the shape of the pulse is with a Sech-function, the width of the optical pulse is calculated to 0.5 ps.

Passive mode locking of the device is obtained by forward biasing the gain section (I_{gain}) and reverse biasing (V_{sa}) or un-biasing the SA section. The mode locking behavior of the device is characterized by measuring the radio frequency (RF) spectrum using the spectrum analyzer (Agilent E4448A). **Figure 15B** shows the measured RF spectrum of the III/V-on-Si MLL at the injection current to the gain section (I_{gain}) of 110 mA and reverse biasing the SA section at −0.9 V. The resolution bandwidth (RBW) during measurement is 1 MHz. The repetition frequency is about 30.0 GHz with signal-to-noise ratio above 30 dB. By changing I_{gain}, it can be tuned to more than 30 GHz, giving clear evidence of passively mode locking of light signal. The measured RF linewidth of the injection locked laser is about 7 MHz by Lorentzian fitting the RF spectrum.

SUMMARY AND FUTURE OUTLOOK

KEY ACHIEVEMENTS

In summary, we reviewed in this paper the recent demonstrations of optical light source in silicon for the application of H-OEIC, with major focus on hybrid silicon lasers through wafer bonding technology. Furthermore, we proposed a proprietary high-throughput multiple dies-to-wafer (D2W) bonding technology by temporarily bonding III/V dies to a handle silicon wafer through pick-and-place process for subsequent simultaneous batch processing. Such high-throughput multiple D2W bonding technology features the merits of high bonding yield with unlimited III/V dies and scalability to whatever-size silicon wafers, thus is the key enabling technique toward potential manufacturability of large-scale H-OEIC. As proof-of-concept demonstration, we showed the III/V dies to silicon wafer bonding with up to 104 dies. Repeatable demonstrations of 16-III/V dies bonding to pre-patterned 200 mm silicon wafers are performed for the fabrication of hybrid silicon lasers with various laser cavities, including FP lasers, LC-DFB laser with side wall grating, and MLL.

CHALLENGES AND FUTURE OUTLOOK

However, there are still many key issues need to be addressed before the hybrid silicon laser applied to optical interconnects system.

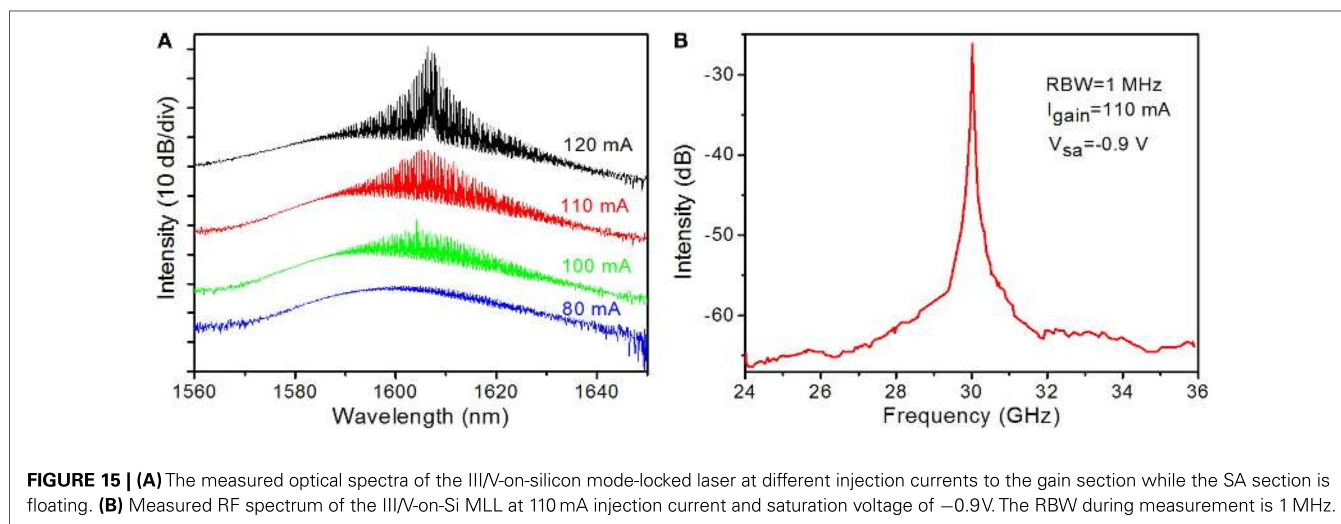

FIGURE 15 | (A) The measured optical spectra of the III/V-on-silicon mode-locked laser at different injection currents to the gain section while the SA section is floating. **(B)** Measured RF spectrum of the III/V-on-Si MLL at 110 mA injection current and saturation voltage of −0.9 V. The RBW during measurement is 1 MHz.

Here, we will only discuss three of the most important issues, including:

(1) the thermal management;
(2) the integration with other silicon photonic devices with full wafer processing capability; and
(3) the new platform beyond silicon for high-performance advanced hybrid lasers.

Thermal management is one of the major obstacles for achieving high-performance hybrid silicon lasers for practical applications (Sysak et al., 2011). Due to the poor thermal conductivity of the SOI BOX layer as well as the inter oxide layer between bonding surface, such layers would prevent the efficient heat dissipation to the silicon substrate, thus resulting in the poor laser performances, such as lower laser power. One of the simple ways to increase the thermal dissipation efficiency is to design the contact electrodes with thick and large area metal, serving as the top surface heat sink. Another efficient way for thermal dissipation is to remove the BOX layer in some areas and refill it with high thermal conductive materials such as polycrystalline silicon or metals, serving as thermal shunt (Liang et al., 2012). However, although such approach has been demonstrated with enhanced thermal management and increased laser performance, it still requires further development in order to further improve the performance.

The integration of such hybrid laser with the existing silicon photonics building blocks is another key issue before it is applied for H-OEIC. For most of the demonstrated hybrid silicon lasers, the silicon waveguide is normally with more than 500 nm thickness in order to ensure the optical index matching with III/V material for efficient light coupling to silicon waveguide. Such thick waveguide design is actually not compatible with the mainstream silicon photonics, with most of the key building blocks are demonstrated in 220 nm silicon wafers (Xu et al., 2014). Thus, novel designs taking care of both of these design considerations are required. Recently, Dong et al. (2014a,b) demonstrated novel integration scheme with associated transition structure via epitaxial growth of silicon in a pre-defined trench. Such epitaxial-grown silicon mesa also serves as the bonding interface with III/V gain material. Thus, the rest of the device area leaves with 220 nm silicon for other existing silicon photonic devices. Such novel demonstration sets a path toward the integration of hybrid silicon laser with existing silicon photonics building blocks. However, for practical integration with high-speed modulator and photodetector, which involves even complicated integration process with multiple oxide etch-back and CMP, it is still very challenging on how to ensure the flatness and smoothness of the bonding surface. More sophisticated design and further demonstration with integration of such are highly demanded.

The third issue is associated with current new demonstration trend that utilizes extremely low-loss SiN or SiON waveguide as the passive waveguide layer (Bovington et al., 2014; Luo et al., 2014). As we know, for some advanced type of hybrid lasers, such as the MLLs, extremely low optical loss is required for achieving high performances. The state-of-the-art demonstration of the silicon waveguide is still with propagation loss of ~2 dB/cm, which is higher comparing that of SiN waveguide of 0.1 dB/m (Bauters et al., 2011). Thus, III/V-SiN platform for hybrid lasers is another interest research area, which can address the loss issue. The integration between SiN waveguide and other SOI-based devices is also CMOS-compatible and ready for further application (Huang et al., 2014).

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