High-Value Tunable Pseudo-Resistors Design

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***Abstract*—Pseudo-resistor circuits are used to mimic large value resistors and base their success on the reduction of occupied area with respect to physical devices of equal value. This paper presents an optimized architecture of pseudo-resistor, made in standard CMOS $0.35\,\mu\mathrm{m}$ technology, to bias a low-noise Trans-Impedance Amplifier for high sensitivity applications in the frequency range $100\,\mathrm{kHz}$ - $10\,\mathrm{MHz}$. The architecture was selected after a critical review of the different topologies to implement high-value resistances with MOSFET transistors, considering their performance in terms of linearity of response, symmetric dynamic range, frequency behavior and simplicity of realization. The resulting circuit consumes an area of $0.017\,\mathrm{mm}^2$ and features a tunable resistance from $20\,\mathrm{M}\Omega$ to $20\,\mathrm{G}\Omega$, dynamic offset reduction thanks to a more than linear I-V curve and a high-frequency noise well below the one of a physical resistor of equal value. This latter aspect highlights the larger perspective of pseudo-resistors as building blocks in very low-noise applications in addition to the advantage in occupied area they provide.**

***Index Terms*—Pseudo-resistor, High-value resistor, Active resistor, Tunable resistor, CMOS.**

I. Introduction

HIGH value resistors are known to be difficult to be designed in standard CMOS integrated technology. This is because the minimum doping level of silicon and polysilicon structures, below which process reproducibility may be affected, gives typical values of sheet resistance in a range from few $\Omega/\square$ to few $\mathrm{k}\Omega/\square$. High values would therefore be reached only by designing long resistors, with multiple folds to keep the layout compact. In addition to size and related cost, long resistors made of hundreds of squares introduce large parasitic distributed capacitances that degrade their frequency response and cause higher noise as frequency increases.

All these disadvantages motivated the research of alternative solutions for the fabrication of high value resistors. They are based on circuital structures employing transistors, that exhibit a given V-I relationship with very high equivalent resistance while occupying a considerably smaller area than a physical resistor of equal value. This class of devices is called Pseudo-resistors because they act, from an electronic point of view, as resistors. They have demonstrated their effectiveness in specific circuits, such as Trans-Impedance Amplifiers for high sensitivity current measurements on nano-devices down to fA [1]–[4], filters showing very large time constants despite the use of small capacitors in the tens of fF range [5], [6], or ultra low noise CMOS current amplifiers [7], [8].

In this paper we target capacitive-feedback architectures, that require a resistive feedback path to bias the amplifier and to handle the DC leakage currents that could be present at its input. Capacitive-feedback architectures are indeed a very good option when a pA sensitivity in the current measurement is desired, together with high linearity response over a rail-to-rail output voltage and large operating frequency range, between $100\,\mathrm{kHz}$ and $10\,\mathrm{MHz}$, as it is the case for example in impedance sensing or impedance spectroscopy circuits. The DC-handling network should not impact those parameters and its value should be adapted to the level of DC leakage current produced by the connected sensor.

Given the large variety of proposed pseudo-resistors available in the literature, each having been optimized both in topology and in performance to different applications, this paper begins (Section II) by analyzing the simplest possible structures of active resistors made of a single-cell and extends (Section III) to pseudo-resistors with symmetric behavior, both with fixed and tunable value of resistance. In these two sections the devices performance are compared in terms of resistance value, linearity, frequency response and size. Furthermore, the effects of large signals on the resistance value are also considered in Section III-B, evaluating dynamic range and bipolar operation, and showing how the large-signal non-linearities can be exploited to obtain useful effects in different applications. Based on this analysis, a new architecture of tunable pseudo-resistor is introduced (Section IV) achieving symmetric behavior, resistance tunability, wide bandwidth, very low noise and dynamic offset reduction thanks to a super-linear behavior of the device I-V curve on large signals. All analyses have been supported and validated by simulations and experimental results (Section VI) on standard $0.35\,\mu\mathrm{m}$ CMOS technology by AMS. The paper also contains Section V, which describes how to design the floating voltage generators that are needed to properly bias the tunable pseudo-resistors to the desired working point.

II. Single-cell Pseudo-resistors

A. Non-Tunable

The simplest way to implement a high-value pseudo-resistor is by using a single MOSFET transistor connected in trans-diode configuration, like the pMOSFET shown in Fig. 1a [9]–[11]. To use this pseudo-resistor with relatively large bipolar signals, it is necessary to short-circuit the well and source terminals: the resulting device behaves as a MOSFET for $V_{AB} = V_A - V_B < 0$ and as a diode for $V_{AB} > 0$.

When operating around $V_{AB} = 0\,\mathrm{V}$ bias, the parasitic diode is OFF and the MOSFET operates in deep-subthreshold region. The small signal equivalent resistance can reach very high-values, exceeding tens of $\mathrm{T}\Omega$ as shown in the simulation results of Fig. 1c (inset), in agreement with the experimental

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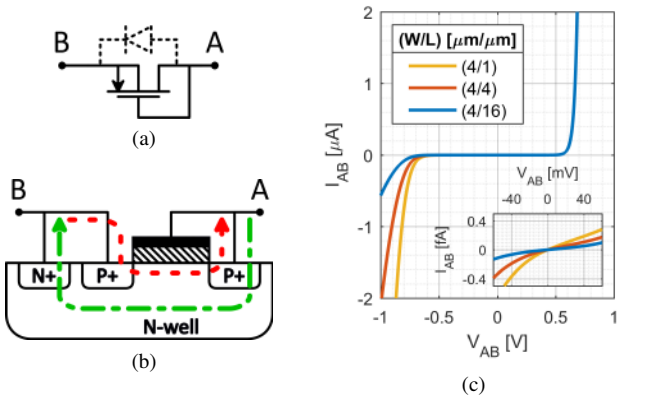


Fig. 1. pMOSFET connected with gate-drain short-circuited to be used as a high value pseudo-resistor. The characteristic curves (c) highlight the two different conduction regimes based on the sign of the bias voltage: drain-well p-n junction when $V_A > V_B$ (current shown as green line in (b)) or p-channel conduction when $V_A < V_B$ (current shown as red line in (b)). The inlet of (c) highlights the subthreshold current regime around $V_{AB} = 0V$. Equivalent resistances range from $200\,\mathrm{T\Omega}$ ($L = 1\,\mu\mathrm{m}$) to $1\,\mathrm{P\Omega}$ ($L = 16\,\mu\mathrm{m}$), with $V_T = 720\,\mathrm{mV}$

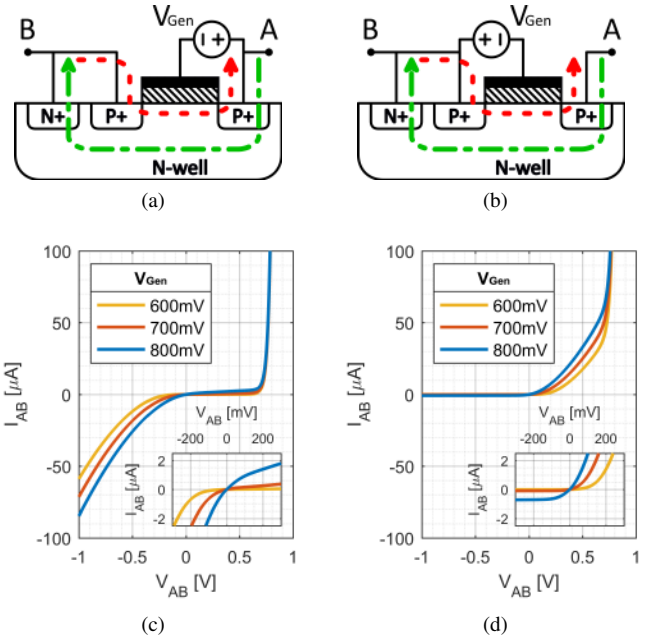


Fig. 2. Tunable pseudo-resistor cells with the floating voltage source placed at node A (left column) or at node B (right column). Characteristic curves refer to devices with $(W/L) = (4\,\mu\mathrm{m}/1\,\mu\mathrm{m})$ and $V_T = 720\,\mathrm{mV}$.

data reported in [12]. In this condition, the current is inversely proportional to the length of the transistor (Fig. 1c), indicating a current through the drain-well diode negligible compared to the current flowing through the channel [13]. Consequently, the equivalent resistance can be evaluated by using the equation for the sub-threshold current of the transistor:

$$I_{SD} = I_{SD0} \cdot \exp\left(\frac{V_{SG}}{nV_{th}}\right) \cdot \left[1 - \exp\left(-\frac{V_{SD}}{V_{th}}\right)\right] \qquad (1)$$

where

$$I_{SD0} = 2n\mu C'_{OX}\left(\frac{W}{L}\right) V_{th}^2 \cdot \exp\left(-\frac{|V_T|}{nV_{th}}\right) \qquad (2)$$

and where n is the sub-threshold slope, C'_{OX} is the gate oxide capacitance per unit area, μ is the mobility of the carriers, $V_{th} = kT/q$ is the thermal voltage, (W/L) is the aspect ratio of the transistor and V_T is its threshold voltage. The equivalent resistance of the pseudo-resistor around $V_{AB} = 0V$ is then

$$r_{eq0}|_{V_{AB}=0} = \left(\left.\frac{\partial I_{SD}}{\partial V_{SD}}\right|_{V_{SD},V_{SG}=0}\right)^{-1} = \frac{V_{th}}{I_{SD0}} \qquad (3)$$

No conceptual difference would be present in using a nMOSFET, provided that it is enclosed in its own floating p-well. Being the goal to reach high resistance values, pMOSFETs are usually preferred due to the lower mobility of holes compared to electrons.

This pseudo-resistor, made of a single transistor, is very compact but has an inherently asymmetric characteristic curve and shows a linear behavior only for very small signals, as can be noticed in the inset of Fig. 1c. However, this simple structure can be successfully used in ratiometric topologies, where the non-linear and asymmetric features are compensated with an identical cell with different aspect ratio, as used in [1], [6], [7] to implement a $\mathrm{fA/V}$ transconductor.

Moreover, the resistance value is very sensitive to process variations and cannot be regulated during operation as it is set by the technological parameters and by the geometry chosen in the design phase. Lower and more controllable equivalent resistances, in the MΩ to GΩ range, can be obtained by disconnecting the gate terminal of the transistor from the drain and connecting it to an external potential, which can be tuned during operation [10], [11], [14]–[16]. In this case the pseudo-resistor has become a tripole, with the disadvantage that its behavior depends now also on gate-drain (V_{GD}) and gate-source (V_{GS}) voltages. This means that the "common-mode" voltage of drain and source greatly affects the resistance of the device and makes this structure more difficult to be used where a simple high-resistance element is needed.

B. Tunable

The resistance of a bipole pseudo-resistor can be tuned independently of the absolute voltage of source and drain by means of a *floating voltage generator* placed either between gate and drain (Fig. 2a) or between gate and source-well (Fig. 2b). The value of V_{Gen} determines the working region of the transistor among weak, moderate and strong inversion. The presence of the floating voltage generator does not affect the behavior of the well diode, whose current is still negligible for small V_{AB} voltages applied to the pseudo-resistor.

The first variant (shown in Fig. 2a and 2c) has the voltage source placed between the gate and node A. When $V_{AB} > 0$, the current flows from A to B and the Source of the transistor is at node A. The pMOSFET works in the inversion region, with a set $V_{SG} = V_{Gen}$, starting from Ohmic regime for small voltage differences V_{AB} and reaching saturation when the voltage difference increases over a certain threshold: $V_{AB} > (V_{Gen} - V_T)$ for strong inversion, $V_{AB} > 4V_{th} \approx 100\,\mathrm{mV}$ for sub-threshold regime. When $V_{AB} < 0\,\mathrm{V}$, the current flows

from B to A and the source of the transistor is at node B. In this case, the gate-source voltage difference is set by V_{AB} and the current increases quadratically in the case of strong inversion or exponentially in the case of weak inversion. Note that the MOSFET reaches strong inversion for high V_{AB} even if it is initially biased in sub-threshold regime by the floating generator.

The second variant, represented in Fig. 2b and 2d, has the floating voltage source between the gate and node B [11], [14], [15]. The behavior of the MOSFET in this case is symmetrical to the one just explained. The difference between the two structures is how the current given by the diode (independent of V_{Gen}) is summed to the transistor current. In Fig. 2c, the diode dominates the saturating behavior of the transistor when V_{AB} is sufficiently positive. In Fig. 2d, the diode only dominates when V_{AB} is large enough to overcome the quadratic growth of the transistor. As a result, this circuital variant has really different behaviors for two opposite polarities of the differential voltage, giving a sharp non-linearity on large signal.

Another important difference between the two structures in Fig. 2 is given by the *body-effect*. In Fig. 2c, when $V_{AB} > 0\,\mathrm{V}$, the transistor operates in saturation regime with a source-well voltage equal to V_{AB} and the body-effect decreases the threshold voltage of the MOSFET. The resulting increase of the saturation current improves the linearity of the pseudo-resistor for small applied voltages as shown in the inset of Fig. 2c. On the contrary, in Fig. 2d, the saturation regime of the transistor ($V_{AB} < 0\,\mathrm{V}$) is obtained with the source and well at the same potential, i.e. no body-effect is present. The current is approximately insensitive to the applied voltage causing a I-V curve strongly asymmetric (Fig. 2d, inset).

C. Equivalent resistance

The floating voltage generator is crucial to allow the tunability of the resistance of the pseudo-resistor to the designer's need. For a device operating in sub-threshold regime (the most common case for high-value equivalent resistances) the small-signal resistance can be derived from (1) and (2), as in the case of the non-tunable pseudo-resistor, with $V_{SG} = V_{Gen}$:

$$r_{eq,T}|_{V_{AB}=0} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\bigg|_{V_{SD}=0} \right)^{-1} = \frac{V_{th}}{I_{SD0}} \cdot \exp\left(-\frac{V_{Gen}}{nV_{th}}\right) \tag{4}$$

Substituting I_{SD0} as given by (2), the complete mathematical expression linking $r_{eq,T}$ to design and process parameters is obtained:

$$r_{eq,T} = \frac{1}{4n\mu C'_{OX} V_{th}} \left(\frac{L}{W}\right) \cdot \exp\left(\frac{|V_T| - V_{Gen}}{nV_{th}}\right) \tag{5}$$

The resistance value of the pseudo-resistor therefore depends on the technology and can be tailored by properly sizing the transistors and by changing the bias voltage V_{Gen}.

III. Multi-cell Symmetric Pseudo-resistors

Both structures presented in Fig. 1 and in Fig. 2 are very asymmetric. A symmetric pseudo-resistor would be beneficial in many applications thanks to: i) the same response for both positive and negative currents, a desirable behavior for resistive bipoles; ii) the suppression of even-order harmonics when stimulated by a sinusoidal signal around the $V_{AB} = 0\,\mathrm{V}$ bias. The flow of a spurious continuous (DC) current, that is a component of the even-order harmonics, is also avoided.

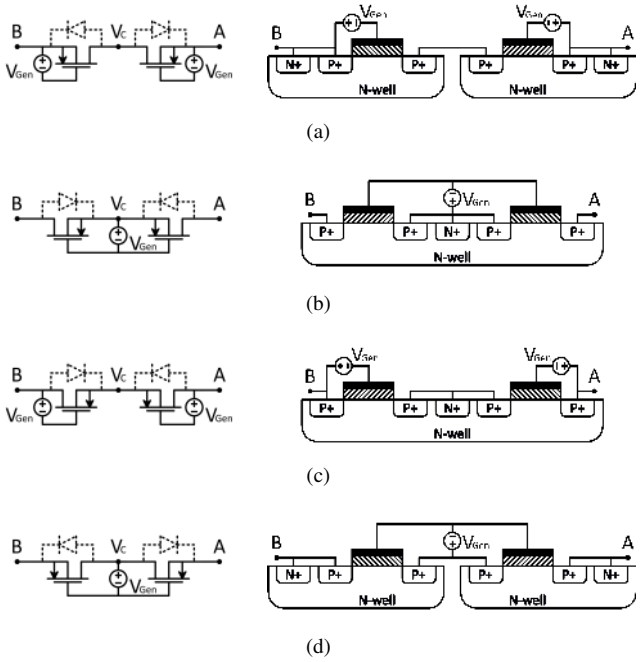


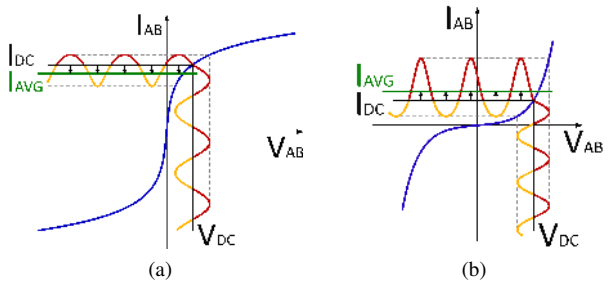
Fig. 3. Schematic and corresponding cross-section of symmetric series pseudo-resistors. Their non-tunable counterparts can be obtained by imposing $V_{Gen} = 0$.

A symmetric pseudo-resistor is obtained by mirroring the elementary building blocks of Section II in series or in parallel [17]. When they are connected in series, the current is set by the least conductive element; when they are connected in parallel, the current is the sum of each element in the structure. If non-tunable cells are used, extremely high resistance (up to tens of $\mathrm{T}\Omega$) are reached, yet fixed; if tunable cells are used, the full spectrum of values can be explored and used.

A. Series architectures

Fig. 3 summarizes the possible series combinations of elementary cells [10], [11], [15]. Only tunable pseudo-resistors are shown since their non-tunable counterparts can be obtained by imposing $V_{Gen} = 0$.

In the structures of Fig. 3b and Fig. 3c the n-type wells can be shared between the two MOSFETs, leading to a compact layout. As a drawback, the potential at the internal node modulates the voltage of the well. Consequently, the large capacitive coupling between the well and the substrate produces a path to ground unbalancing the currents at the terminals A and B and affecting the frequency behavior of the device and its symmetry, especially when large common mode signals are applied to it. Due to the high resistance involved, the spurious current flowing into the substrate is likely to limit the use of these structures to very low-frequency applications. Instead, in the structures of Fig. 3a and Fig. 3d,



(a) (b)

Fig. 4. Qualitative characteristic curves of (a) sub-linear and (b) super-linear pseudo-resistors, showing the effect of the two different non-linearities on the DC current of the devices.

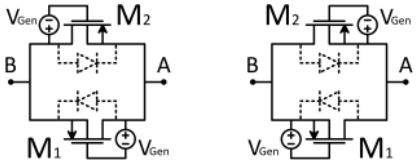
the two parasitic capacitances given by the wells toward the substrate can be voltage-driven directly by the nodes A and B, thus extending their operative frequency range with respect to the previous structures. However, the area occupation is higher because the two wells operate at different voltages and must be independent.

Similar considerations hold for the floating voltage generators. In the pseudo-resistors of Fig. 3b and Fig. 3d the voltage generator can be shared between the two cells, with an advantage in terms of complexity and size. As a drawback, the bias circuit loads the internal node of the pseudo-resistor and limits the frequency response of the device, just like the well capacitance. Nevertheless, the structure in Fig. 3d has been used in applications up to 100 kHz, confirming its simplicity in requiring only a single voltage generator [5], [18], [19]. The structures in Fig. 3a and Fig. 3c have the disadvantage of requiring two matched generators, but may be easier to design because they are referenced to the external pins and their parasitic capacitances do not load the internal nodes of the pseudo-resistor, leading to a wider frequency response.

B. Non linearity in symmetric structures

One important property that differentiates the four structures of Fig. 3 is the kind of non-linearity they show when large V_{AB} signals are applied. This is an important aspect when, for example, the pseudo-resistor is used as feedback element in a Trans-Impedance Amplifier, where the combined effect of bias (DC) and signal (AC) may produce significant distortions.

1) Sub-linear Topologies: In the devices of Fig. 3a and Fig. 3b the current is always limited in value by the saturation of one of the two transistors, causing the composite structure to globally show a symmetric and sub-linear behavior. When biased at $V_{AB} = 0\,\mathrm{V}$, the device has a small-signal resistance, $r_{eq} \approx 2r_{eq,T}$, that can be tuned by setting V_{Gen}. Instead, when a constant voltage bias V_{DC} is applied (Fig. 4a), the working point changes and enters the non-symmetric sub-linear region. Here, a sinusoidal voltage signal superimposed to the V_{DC} bias produces different current amplitudes on each half-wave, leading to an average current I_{AVG} different from I_{DC}, in this case lower than the one flowing without the signal. Thus, the DC accuracy of the device is affected by the presence of AC signals. However, this behavior can be advantageous if the application requires a device that automatically limits its own DC current, as both the on-bias and on-signal behaviors tend to reduce the DC current compared to a completely linear element.



(a) (b)

Fig. 5. Parallel combinations of the elementary tunable pseudo-resistor cells.

2) Super-linear Topologies: The two devices of Fig. 3c and Fig. 3d are instead super-linear. Their I-V characteristic curve (Fig. 4b) shows a symmetrical *more-than-linear* behavior.

When one of these devices is biased by a constant voltage V_{DC} in a working point away from $V_{AB} = 0\,\mathrm{V}$, applying a sinusoidal voltage results in an asymmetric current signal, with an average value I_{AVG} higher than I_{DC}. We have taken full advantage of this property in the feedback path of our transimpedance amplifier as described in Section IV-C to dynamically reduce the DC output voltage.

C. Parallel architectures

The two parallel structures shown in Fig. 5 do not improve the dynamic range and both require two separate wells and floating voltage generators, but are suitable for high frequency symmetric operation due to the absence of internal nodes. The parasitic capacitances may modify the effective resistance depending on the working frequency but they cannot produce any asymmetry in the behavior of the device nor induce a modification in the working point of the transistors.

The small-signal equivalent resistance of the cell, evaluated around $V_{AB} = 0$, is given by the parallel of the equivalent resistances of the two MOSFETs:

$$r_{eq} = r_{M1} \parallel r_{M2} = \frac{r_{eq,T}}{2} \tag{6}$$

where we have assumed two identical transistors with an equivalent resistance given by (4).

Both Fig. 5a and Fig. 5b have the two well diodes in parallel with opposite orientation. Therefore, their exponential (super-linear) behavior becomes dominant when the differential voltage $|V_{AB}|$ is high enough to turn on the diodes. When the diodes are not dominant ($|V_{AB}| \ll 0.7\,\mathrm{V}$), both structures have a super-linear quadratic behavior, given by the turn-on of the MOS transistors. In this operating region the pseudo-resistor of Fig. 5b is affected by the *body-effect*: on both polarities of the signal the MOSFET that is turning-on has its drain acting as source and V_{DB} is changing with V_{DG}. As a consequence this pseudo-resistor turns-on faster than the one in Fig. 5a, which is not affected by this effect and is therefore more linear. In the following only the structure of Fig. 5a is considered and analyzed.

The tunability with V_{Gen} and the symmetric behavior of this pseudo-resistor can be appreciated in Fig. 6, showing a circuital simulation of the structure.

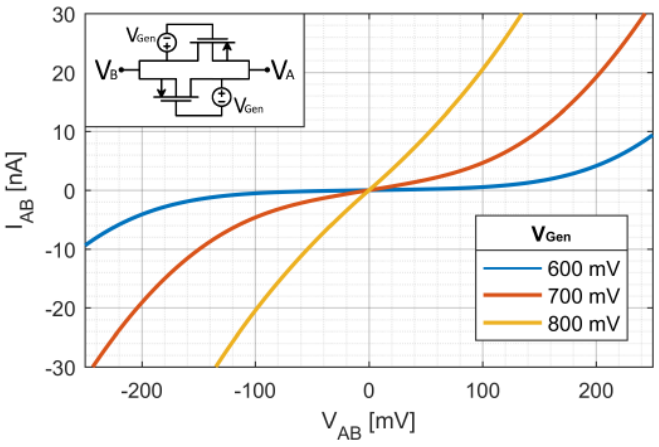


Fig. 6. Simulated I-V curve of the pseudo-resistor cell in the inlet for three different values of the generator voltage V_{Gen}. Characteristic curves refer to devices with $(W/L) = (1\,\mu\text{m}/30\,\mu\text{m})$ and $V_T = 770\,\text{mV}$.

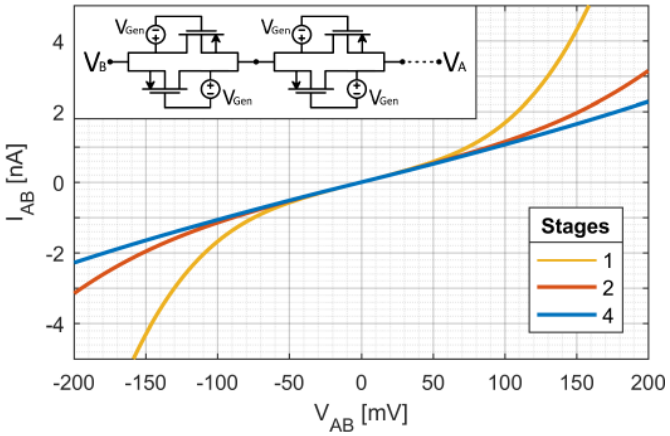


Fig. 7. Extension of the linear range of the device by cascading multiple pseudo-resistor cells in series: sample structure and simulated I-V curves as a function of the number of cells. Characteristic curves refer to devices with $(W/L) = (1\,\mu\text{m}/30\,\mu\text{m})$ and $V_T = 770\,\text{mV}$. V_{Gen} was selected in each experiment to obtain the same small signal resistance around $V_{AB} = 0\,\text{V}$ for every structure: $V_{Gen} = 650\,\text{mV}, 680\,\text{mV}, 713\,\text{mV}$ for $N = 1, 2, 4$ stages.

The linearity of the pseudo-resistor can be extended over the few tens of mV shown in Fig. 6 by adding more cells in series [15]. Fig. 7 shows how four stages already extend the dynamic range of the linear response to hundreds of mV.

IV. Tunable Pseudo-Resistor for Low-Noise Wide-Band Trans-Impedance Amplifiers

The pseudo-resistors reviewed so far can be used in different combinations to adapt to many specific desired application. In this section we present our original design of a pseudo-resistor used to bias a high-performance capacitive-feedback *Trans-Impedance Amplifier* in standard CMOS $0.35\,\mu\text{m}$ technology (Fig. 8).

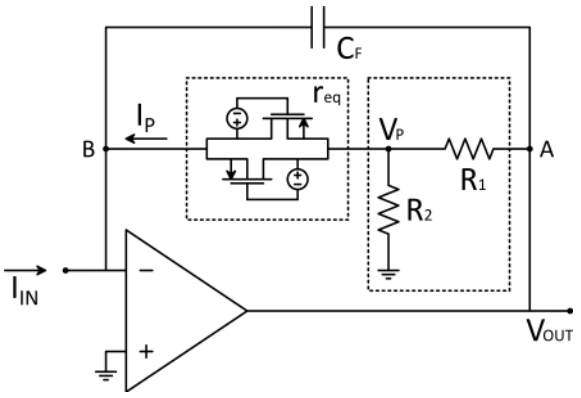


Fig. 8. Capacitive-feedback Trans-impedance Amplifier with the proposed pseudo-resistor as DC-handling network. The linear range of the pseudo-resistor is extended by means of a resistive voltage divider.

A. Selection of the best Pseudo-Resistor topology for DC-handling

TIA are widely used as first preamplifier stage to convert tiny currents coming from sensors in a useful voltage signal [20]–[23]. Capacitive-feedback architectures are the best option to target a pA sensitivity in the current measurement, very low noise and a high linearity response over a rail-to-rail output voltage span, together with a large operating frequency range, between $100\,\text{kHz}$ and $10\,\text{MHz}$. A resistive feedback path is required to bias the amplifier and to handle small DC leakage currents that could be present at the input of the TIA. This DC-handling network should not impact the response of the circuit in the frequency range of the AC signal and must therefore have high linearity and a high enough equivalent resistance to create a pole at a much lower frequency than the desired signal bandwidth [8], [21], [22].

The symmetric and tunable pseudo-resistor topology shown in Fig. 5a has been selected among the other possibilities for its symmetric behavior, tunability range of its resistance value, wide frequency range due to the absence of internal nodes, and dynamic offset reduction thanks to the super-linear I-V curve (Section IV-C). The pseudo-resistor series topologies shown in Section III-B2, while adequate for low-frequency resistive-feedback TIAs [3], were excluded because incompatible with the high frequency operation reachable by a capacitive-feedback TIA. Although the detrimental effect of the well capacitances discussed in Section III-A can be reduced using a CMOS SOI technology [2], [3] allowing an operation up to few hundreds of kHz, here the goal is to extend the frequency in the MHz range maintaining a standard CMOS process.

B. Linearity over an extended range

To extend the linearity range of the pseudo-resistor, it could be implemented using multiple cells in series as showed in Fig. 7. Nevertheless for applications where the pseudo-resistor is used as a voltage-driven current generator, as in the feedback of the TIA, a more compact option is the one shown in Fig. 8.

It uses only one pseudo-resistor cell and a resistive voltage divider to provide an equivalent resistance R_{eq} given by:

$$R_{eq} = \frac{V_{out}}{I_P} = \left(1 + \frac{R_1}{R_2}\right) \cdot r_{eq} + R_1 \tag{7}$$

By considering $R_1 \ll r_{eq}$ and by defining $N = 1 + R_1/R_2$, the equivalent resistance of the pseudo-resistor is

$$R_{eq} \cong N \cdot r_{eq} \tag{8}$$

This structure is equivalent to having N stages in series, because it reduces the effective voltage applied across the pseudo-resistor cell, with an enormous advantage in terms of complexity and occupied area (minimum number of transistors and voltage sources). Furthermore, the implementation with a series of N elementary cells would require a floating voltage generator referred to the output node of the OTA (V_A), thus introducing a limitation on the output voltage swing to maintain the generated voltage $V_A + V_{Gen}$ within the power supply range.

Factor N is selected to obtain the required THD in the signal bandwidth (100 kHz to 10 MHz) at the output of the TIA. At these frequencies the gain is set by the feedback capacitor, but a too high non-linearity of the pseudo-resistor could anyway impair the overall linearity of the amplifier. For example: in a TIA biased with a single pseudo-resistor cell having $(W/L)_{M_1,M_2} = (1\,\mu m/30\,\mu m)$ and $V_{Gen} = 610\,mV$, a 2 V peak-to-peak 1 MHz output signal has a 6.82 % THD. In the same conditions, $N = 4$ (with $V_{Gen} = 665\,mV$ to get the same R_{eq} of 280 MΩ) is sufficient to reduce the THD to 0.24 %, both using the implementation with 4 cells in series and using the one with a factor 4 voltage divider. If the pseudo-resistor was to be used as gain-setting element, $N = 4$ would not be sufficient: at frequencies lower than the pole of the amplifier ($f < 1$ kHz), where the pseudo-resistor is dominant over the feedback capacitance, the simulated THD becomes higher than 20 %.

A peculiarity of the structure with the voltage divider is that only the equivalent differential resistance V_{AB}/I_P is increased, while the single ended resistance from A to ground is considerably reduced to $\approx (R_1 + R_2)$, 80 kΩ in our case. It is therefore compatible with the TIA architecture while its not tailored to other applications where a floating bipole is required, as in the case of a RC filter. In the latter case, the best method to extend the linear range remains the use of multiple cells in series.

C. Dynamic offset reduction

The residual non-linearity of the pseudo-resistor reflects on the output offset of the stage if $V_{AB} \neq 0$ V due to a leakage current, and has been selected to provide a beneficial effect of dynamic offset reduction when the AC signal is applied to the stage. As explained in Section III-B, the average current flowing in the pseudo-resistor changes depending on its non-linearity, when a sinusoidal signal is superimposed to the DC bias. In particular, a super-linear topology would increase the average current in the feedback path as effect of the AC signal. However, the total DC current is set at the input of the TIA and consequently the circuit reacts by *reducing* the DC output voltage to recover the correct current value I_{DC}. The reduction of output offset increases with the amplitude of the AC signal and restores the full output dynamic range of the amplifier. Instead, if a sub-linear topology had been selected, the feedback of the TIA would have reacted by further *increasing* its output DC voltage to keep the original value of DC current. Fig. 9 compares the effects of a linear resistor, a sub-linear pseudo-resistor and a super-linear pseudo-resistor on the *Total Harmonic Distortion (THD)* at the output of the TIA, clearly showing that a super-linear pseudo-resistor can handle much higher DC input leakage currents than a linear resistor of the same value.

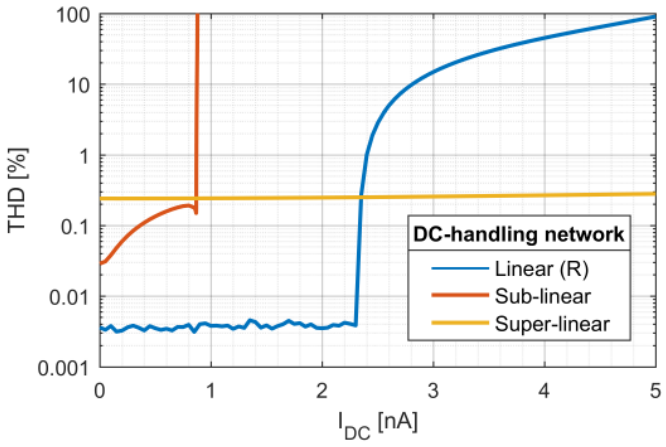


Fig. 9. Comparison of the THD measured at the output of three TIAs having different DC handling networks: an ideal resistor (blue), a sub-linear pseudo-resistor (red) and a super-linear pseudo-resistor (yellow). The TIAs have an output dynamic range of 3.3 V, a feedback capacitor of 500 fF, and an equivalent feedback resistance of 280 MΩ. The sub-linear and super-linear pseudo-resistors are the ones of Fig. 3b and Fig. 5a, both with a factor 4 linearity improvement (voltage divider of Section IV-B). The simulation was performed with a peak-to-peak AC output signal of 2 V at 1 MHz, for increasing values of DC input leakage current I_{DC}. The TIAs with a linear resistor or a sub-linear pseudo-resistor show a steep degradation of the THD when I_{DC} becomes too high, due to the AC output voltage exceeding the output range of the amplifier. Instead, the TIA with a super-linear pseudo-resistor, while having a slightly higher distortion, never shows output saturation due to I_{DC}.

D. Noise behavior

For the noise analysis of the pseudo-resistor, the two transistors can be modeled as the parallel of an ideal noise-free resistance with value r_{eq} and a current generator with noise power spectral density $S_{i,eq}$, as shown in Fig. 10. The equivalent input-referred noise of the pseudo-resistor in the frequency range where the loop gain of the TIA is much higher than 1 is:

$$S_{input} \cong S_{i,eq} + \frac{4kTR_1}{R_{eq}^2} + \frac{4kT}{R_2}\left(\frac{R_1}{R_{eq}}\right)^2 \tag{9}$$

When $I_{IN} = 0$ A, $V_{DS} \approx 0$ V and the noise of transistors is given by the thermal noise of their small-signal resistance ($4kT/r_{eq}$). For increasing input currents, the transistors enter saturation regime and the noise becomes shot-limited

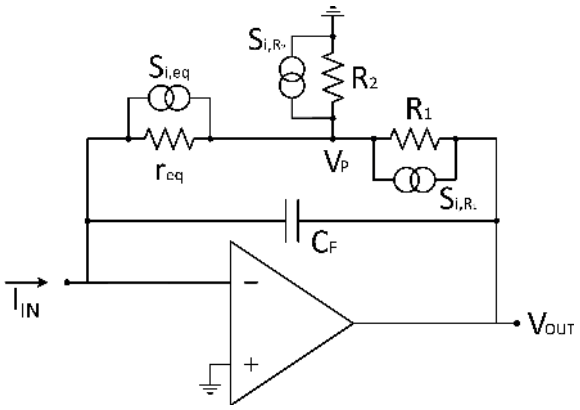


Fig. 10. Capacitive TIA topology with the current noise sources of the pseudo-resistor in Fig. 8.

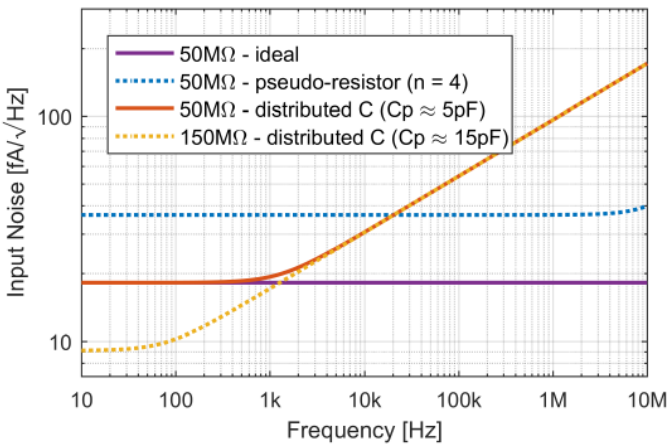


Fig. 11. Simulated spectral density of the input-referred current noise of a TIA due to the feedback resistance: comparison between an ideal resistor (purple), our pseudo-resistor (dotted blue) and two different resistors with a distributed-capacitance model (orange and dotted yellow). Real resistors were sized at the minimum available width ($W_R = 0.8\,\mu\text{m}$), giving a resistance (r) and a capacitance (c) per unit length of $2\,\text{k}\Omega/\mu\text{m}$ and $0.2\,\text{fF}/\mu\text{m}$, respectively. The pseudo-resistor was sized with $(W/L) = (1\,\mu\text{m}/4\,\mu\text{m})$, $V_{Gen} = 740\,\text{mV}$ and $N = 4$ ($R_1 = 60\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$).

$(2qI_{IN})$ [24]. For even higher input currents, the transistors begin to operate in strong inversion and the noise is again limited by the thermal noise of the channel. Since $R_1, R_2 \ll R_{eq}$, the thermal noise of the resistors R_1 and R_2 is always negligible with respect to the contribution of the transistors.

1) Voltage divider effects: When thermal noise limited, the noise can be evaluated as a function of the equivalent resistance R_{eq} of the pseudo-resistor reported in (8):

$$S_{i,input} \cong \frac{4kT}{R_{eq}} \cdot N \tag{10}$$

This indicates that the use of the voltage divider to improve linearity indeed causes an amplification of the thermal noise spectral density of the same factor N with respect to an ideal resistor with the value R_{eq}. This effect is not present when multiple cells in series are used to extend the linearity of the pseudo-resistor.

When shot noise limited, the noise does not depend on the equivalent resistance R_{eq} and the input noise is simply:

$$S_{i,input} \cong 2qI_{IN} \tag{11}$$

Differently from thermal noise, the shot noise of the pseudo-resistor is not affected by the presence of the voltage divider. Again, this behavior differs from multiple-cell pseudo-resistors, where the shot noise decreases for an increasing number of cells [3].

2) Advantages of a pseudo-resistor over a physical resistor: Despite the increase in thermal noise given by the voltage divider, if we compare the noise of the pseudo-resistor with the one introduced by an integrated resistor of the same value R_{eq}, the advantages come into sight. This is due to the distributed parasitic capacitance that a real resistor exhibits toward the substrate. Since high-value integrated resistors, in the $10\,\text{M}\Omega$ range, would be very long (several mm), they behave as a distributed RC line starting from a low frequency approximately given by $\pi/8RC_p$, where C_p is the total parasitic capacitance of the resistor [25]. The high-frequency impedance of the resistor $Z_R(f)$ becomes frequency-dependent and decreases proportionally to the square root of the frequency [26]. The thermal current noise of a resistor is given by the real part of its admittance [27], therefore it increases at high frequency as:

$$S_{R,HF} = 4kT \cdot Re\left[\frac{1}{Z_R(f)}\right] \cong 4kT \cdot \sqrt{\frac{c \cdot \pi f}{r}} \tag{12}$$

where r and c are the resistance and capacitance per unit length. Fig. 11 compares the noise spectral density of three different devices with equal DC small-signal resistance ($50\,\text{M}\Omega$):

- An ideal, parasitic-free resistor.
- A real integrated resistor with $C_p \approx 5\,\text{pF}$.
- High-linearity pseudo-resistor with linearity improvement factor $N = 4$.

It is clear that for high frequency, where the TIA with a capacitive feedback is operated, there is a considerable advantage in using a pseudo-resistor, which does not suffer from the parasitic-induced noise degradation. Note that using an higher value physical resistor would not lead to a noise performance improvement, because for a given technology r and c are fixed and the high-frequency noise limitation is the same for every resistor value.

V. Floating Voltage Generator Design

The floating voltage generator is crucial to allow the tunability of the resistance (r_{eq}) of the pseudo-resistor, as it affects the MOSFET behavior by changing its channel conductivity. The exponential relationship between the bias voltage V_{Gen} and the equivalent resistance (see equation (4)) imposes a special care for a precise setting of the r_{eq} value. A useful guideline is obtained by observing that the saturation current $I_{SD,sat}$ of a transistor operated in sub-threshold regime is

$$I_{SD,sat} = I_{SD0} \cdot \exp\left(\frac{V_{SG}}{nV_{th}}\right) \tag{13}$$

that is obtained by (1) with $V_{SD} \gg V_{th}$. By setting $V_{SG} = V_{Gen}$ the (4) can then be rewritten as:

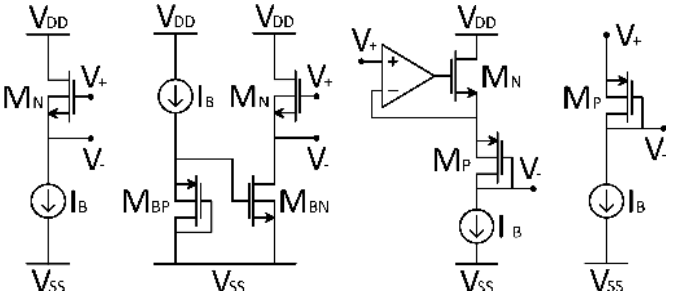


Fig. 12. Topologies to implement a floating voltage generator of value $V_{Gen} = V_+ - V_-$: (a) Source-Follower, (b) Improved Source-Follower, (c) Buffered-Input Trans-diode, (d) Trans-diode.

$$r_{eq,T} = \frac{V_{th}}{I_{SD,sat}} \tag{14}$$

Thus, it may be convenient to have a mirrored architecture where the bias voltage V_{Gen} is generated by forcing a given bias current I_B to an auxiliary transistor operating in saturation regime and sub-threshold. The V_{SG} of the auxiliary transistor is then applied to the actual pseudo-resistor in order to obtain an equivalent resistance of $r_{eq} \approx V_{th}/I_B$. Many variations of floating generators based on this principle are found in the literature [2], [3], [5], [14], [18], [19], [28].

A. Process-stability and CMOS Technology Requirements

The main objectives that guided our design of the pseudo-resistor bias network are: (i) compatibility with single-well CMOS $0.35\,\mu\text{m}$ technology; (ii) stability of the pseudo-resistor value on process and mismatch variations.

The simplest topology is the source-follower stage of Fig. 12a, made by a transistor of the opposite type of the pseudo-resistor MOSFET, as presented in [18]. Although very simple to integrate, this basic structure does not meet our objectives, having two important disadvantages:

1) The CMOS technology must offer both p-wells and n-wells. The body effect in the follower (transistor M_N) must be avoided, because it would make V_{GS} dependent on the absolute potential of the V_+ and V_- voltages. Therefore, both the pseudo-resistor and the source-follower need an isolated body-source connection, and both types of wells are required.
2) The value of the resistance is highly affected by the technological process variation. Given a fixed bias current, V_{GS} depends on the process and temperature variations of the threshold voltage of the nMOSFET transistor. At the same time, the equivalent resistance of the pseudo-resistor depends on the threshold voltage variations of the pMOSFET transistors. The two effects combine and lead to a very large variability in the resistance of the device.

An improved source-follower topology (Fig. 12b) has been proposed in [19]. Threshold voltage changes of all transistors are compensated by the topology and therefore the equivalent resistance of the device is ideally equal to V_{th}/I_B with a limited effect of the process variations [19]. If I_B is generated by a PTAT current generator the pseudo-resistor bias is also independent of the temperature fluctuations [3]. However, this topology is not suitable for our application since it requires both type of wells to avoid the body effect (through isolated body source connections), which would otherwise ruin the matching between the pairs of transistors (M_N-M_{BN} and M_{BP} with the pseudo-resistor).

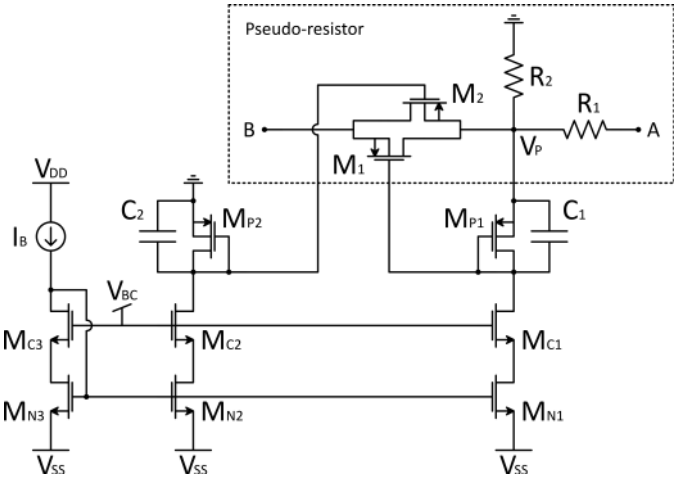


Fig. 13. Matched floating voltage generators to bias the parallel pseudo-resistor cell of Fig. 8.

A trans-diode topology can be exploited to use the same type of transistor for both the bias circuit and the pseudo-resistor, thus cancelling the threshold voltage process variations. In [5], an operational amplifier is used to buffer the voltage V_+ (Fig. 12c), but we chose against this topology, as the increase in area occupation and power consumption can become relevant, particularly for high frequency operation or for rail-to-rail applications. In [28], the trans-diode is left hanging and is directly connected to the signal line of the pseudo-resistor (Fig. 12d), avoiding the Op-Amp entirely. However, the use of this configuration should be evaluated carefully: if the bias current I_B flowed into the pseudo-resistor, the transconductance and the noise of the pseudo-resistor would dramatically increase [14].

B. Trans-diode bias voltage generators

We propose here an improved version of the Trans-diode showed in Fig. 12d. The complete schematic of the two matched voltage generators is shown in Fig. 13, detailing the connections to our high-linearity pseudo-resistor.

Two identical pMOSFET trans-diodes, each in its own n-well, are used to bias our p-type pseudo-resistor, allowing only one type of well to be used. The bias currents are provided by two matched branches ($M_{N1} - M_{C1}$ and $M_{N2} - M_{C2}$) of a cascode current mirror from a single branch ($M_{N3} - M_{C3}$) with current I_B. The transistors M_{N1}, M_{N2} and M_{N3} are designed with a considerable area ($W_N = 32\,\mu\text{m}$, $L_N = 4\,\mu\text{m}$) to improve the matching of the mirrored currents against statistical variations. The cascode transistors, instead, do not

affect the matching and can be designed with minimal size ($W_C = 1\,\mu\text{m}$, $L_C = 3\,\mu\text{m}$) to reduce the parasitic capacitances (towards ground) at the pseudo-resistor nodes by a factor $W_N/W_C = 32$, allowing for a better frequency behavior. Moreover, two $2\,\text{pF}$ capacitors C_1 and C_2 have been placed in parallel to the trans-diodes to stabilize the generated voltage at high-frequency and to filter out the noise of the bias circuit at the frequencies of interest, which becomes negligible with respect to the noise of the pseudo-resistor itself.

The gate voltage of M_2 has to be referred to the potential of the virtual ground (node B in Fig. 8 and Fig. 13). In this condition, M_{P2} would inject its current into the virtual ground of the operational amplifier, severely impairing the correct operation of the circuit. However, being the voltage of the virtual ground fixed by the circuit topology, the source of M_{P2} can be directly connected to ground instead of the virtual ground, avoiding the current injection.

The transistor M_1 requires a true floating voltage generator forcing the connection of the M_{P1} source at the pseudo-resistor node V_P. Thanks to the effect of the feedback loop, the bias current of M_{P1} flows in the resistor R_1 giving a voltage offset at the output of the TIA equal to $R_1 \cdot I_B$. High value pseudo-resistors require bias current in the nA range producing a negligible output voltage offset.

The transistors M_{P1} and M_{P2} are operated in saturation regime and in sub-threshold for a precise setting of the pseudo-resistor value using the bias current I_B. By recalling the equations (14) and (8), the equivalent resistance can be written as:

$$R_{eq} = \frac{V_{th}}{2I_B} \cdot \frac{W_B}{W} \cdot N \tag{15}$$

where W_B is the width of the transistors M_{P1} and M_{P2}, W the width of M_1 and M_2 and all transistors are considered with the same length. This expression directly links the equivalent resistance of the pseudo-resistor to the geometrical dimensions of the transistors, the multiplication factor n and the bias current, that can be externally changed to fine-tune the resistance of the device.

Fig. 14 shows the results of a 600-points Monte Carlo simulation to evaluate the effects of process variations on the equivalent resistance R_{eq}. The plot compares our bias topology with the simple source-follower, the two architectures that do not require double-well CMOS technology and avoid the use of an additional operational amplifier. Since the process variations of the threshold voltage V_T affect R_{eq} exponentially, as shown in (13), the results of the Monte Carlo simulations are better shown on a logarithmic horizontal axis. Therefore, $R_{eq} = 10^{\alpha} = 10^{\mu_\alpha \pm 3\sigma_\alpha} = \mu \cdot 10^{\pm 3\sigma_\alpha}$. To present a fair comparison, the transistors biasing the pseudo-resistor have been designed of the same area and the nominal resistance R_{eq} has been tuned to about $280\,\text{M}\Omega$ with both circuits.

The R_{eq} of the pseudo-resistor biased by the source-follower spans about 3 decades from about $10\,\text{M}\Omega$ to more than $50\,\text{G}\Omega$, having an average value $\mu = 360\,\text{M}\Omega$ and a standard deviation of the exponent $\sigma_\alpha = 0.790$. Our bias topology shows $\mu = 289\,\text{M}\Omega$ and $\sigma_\alpha = 0.107$, leading to a minimum value of about $200\,\text{M}\Omega$ and a maximum of $500\,\text{M}\Omega$.

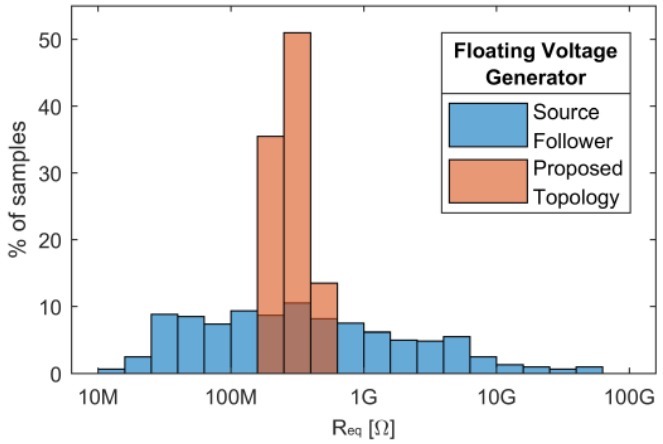


Fig. 14. Results of a 600-points Monte Carlo simulation comparing the effects of process variations on the equivalent resistance ($R_{eq} = 10^{\alpha}$) of a pseudo-resistor biased with a source-follower (blue) or the proposed topology (orange). The nominal value of the R_{eq} has been set to about $280\,\text{M}\Omega$ in both scenarios. The source-follower has an average value $\mu = 10^{\mu_\alpha} = 360\,\text{M}\Omega$ and a standard deviation σ_α of the exponent of 0.790. Our bias topology shows $\mu = 289\,\text{M}\Omega$ and $\sigma_\alpha = 0.107$.

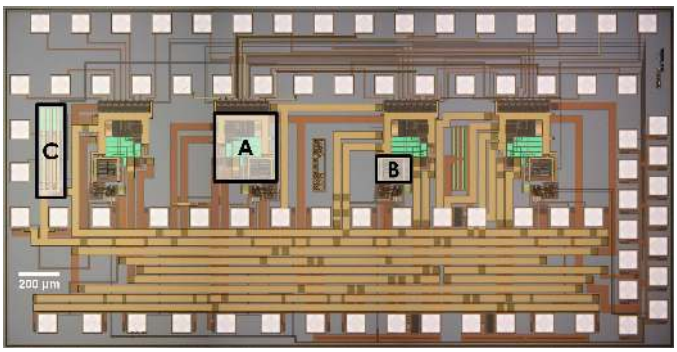


Fig. 15. Micro-photograph of the four channel fabricated chip highlighting the proposed devices: (A) TIA and (B) Pseudo-resistor (one per channel). (C) Chip-level bias circuit.

Mismatch Monte Carlo simulations show a much smaller and approximately linear effect on R_{eq}, similar in both topologies, with μ equal to the nominal value and sigma of the exponent $\sigma_\alpha = 0.028$. Finally, we simulated in our topology the effect of temperature variations on the resistance nominal value: at $0\,^\circ\text{C}$ R_{eq} increases to $282\,\text{M}\Omega$ and decreases to $275\,\text{M}\Omega$ at $85\,^\circ\text{C}$.

VI. Experimental results

The proposed TIA, complete with the custom pseudo-resistor and the floating voltage generators, has been designed, fabricated and tested in AMS CMOS $0.35\,\mu\text{m}$ technology as high-bandwidth low-noise front-end for the readout of CLIPP detectors [29] in a Silicon Photonic application (Fig. 15). The operational amplifier, described in [21], has a gain-bandwidth product of $400\,\text{MHz}$, allowing an operation of the TIA up to few tens of MHz. In this test chip, the feedback capacitance C_F has a value of $500\,\text{fF}$, while the pseudo-resistor has been sized as follows: $(W/L)_{M_1,M_2} = (1\,\mu\text{m}/30\,\mu\text{m})$, $(W/L)_{P_1,P_2} = (2.8\,\mu\text{m}/30\,\mu\text{m})$, $R_1 = 60\,\text{k}\Omega$, $R_2 = 20\,\text{k}\Omega$.

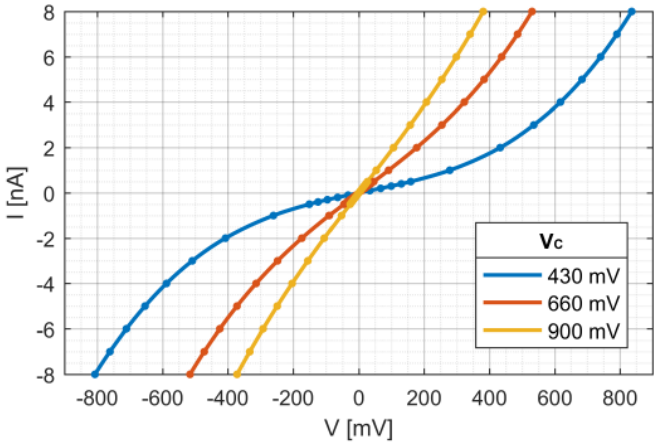


Fig. 16. Measured V-I curves of the pseudo-resistor for three different values of the external control voltage V_C.

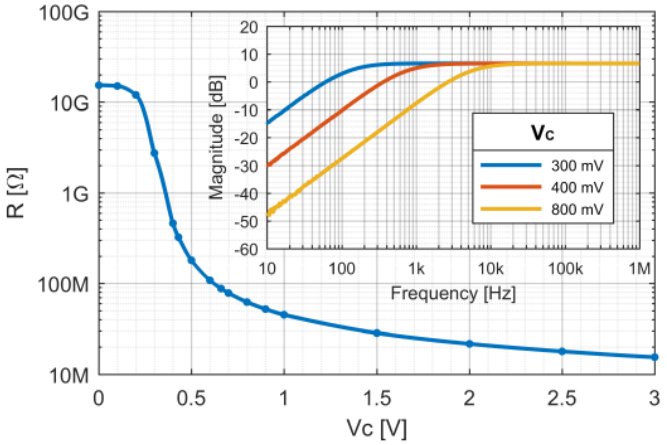


Fig. 17. Indirectly measured resistance of the pseudo-resistor as a function of the control voltage V_C. Resistance values were computed from the position of the low-frequency pole of the transfer function of the TIA (inset). Transfer functions were measured by applying a voltage signal to a 1 pF capacitor connected to the virtual ground node of the amplifier.

The pseudo-resistor occupies an area of $154\,\mu\text{m} \times 115\,\mu\text{m}$ and requires a bias current I_B of 2 nA to obtain an equivalent resistance of about 300 MΩ.

The bias current I_B of the pseudo-resistor is generated at chip-level (Fig. 15(C)) by applying an external control voltage V_C on an integrated resistance of 50 kΩ and reducing the current with a cascade of current mirror reducers of factors $\frac{1}{9}$, $\frac{1}{9}$, $\frac{1}{3}$, $\frac{1}{10}$:

$$I_B = \frac{V_C - V_{GS,M}}{50\,\text{k}\Omega} \cdot \frac{1}{2430} \tag{16}$$

where $V_{GS,M}$ is the gate-source voltage of the input branch of the mirror used to read the current (made of nMOS transistors with $V_T \approx 500\,\text{mV}$).

The characteristic curve of the device, due to its connection in the feedback path of the TIA, has been measured by setting the DC input current and by measuring the output voltage. The obtained curve is shown in Fig. 16 with the voltage on the x-axis to be consistent with the analyses of the previous sections. The measure proves the symmetric behavior of the pseudo-resistor and the tunability offered by the external control voltage V_C.

The tunability range of the resistance has been evaluated through an indirect measure from the transfer function of the TIA (inset of Fig. 17). In particular, knowing the value of the feedback capacitance of the TIA, it is possible to compute the equivalent resistance of the pseudo-resistor from the low-frequency pole of the transfer function. Fig. 17 shows the resistance for values of V_C from 0 V to 3 V. The device is capable of synthesizing a tunable resistance from 20 MΩ to 20 GΩ.

Fig. 18 shows the effect of the dynamic output offset reduction. A DC current of −1 nA has been injected into the TIA to simulate a leakage current for three different values of the pseudo-resistor external control voltage V_C. At the same time, an additional sinusoidal current signal at 1 MHz, with amplitude from 0 to 3.8 µA, has been applied to the TIA, leading to an oscillation of the output voltage in the range of 0 V to 1.2 V. The plot clearly shows the reduction of the output offset due to the leakage current for increasing amplitudes of

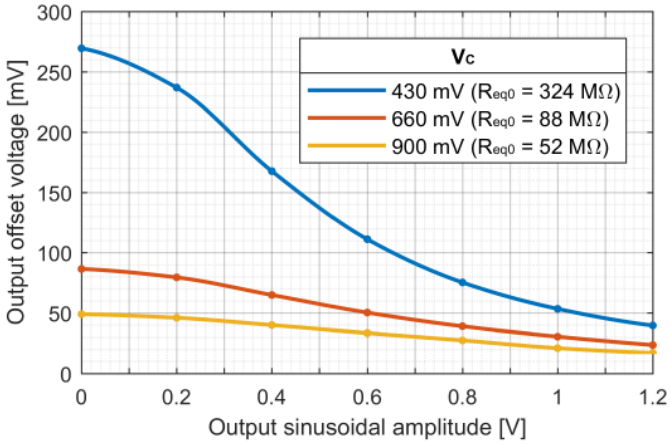


Fig. 18. Measured dynamic offset reduction as a function of the output signal amplitude, in presence of a constant leakage current of −1 nA, for three different values of the external control voltage V_C.

the sinusoidal signal, thanks to the super-linear behavior of the pseudo-resistor.

The linearity of the designed TIA has been evaluated by setting the pseudo-resistor equivalent resistance to 280 MΩ ($V_C = 430\,\text{mV}$) and applying a 1 MHz sinusoidal input current giving a peak-to-peak output signal of 2 V. The measured THD is 0.33 % when no DC input current is injected and 0.36 % when $I_{DC} = 5\,\text{nA}$. These results confirm the expected THD level and the ability of the designed pseudo-resistor to handle DC leakage currents without a linearity degradation.

The noise of the system has been measured at the output of the TIA and referred back to the input of the amplifier by dividing for its transfer function. The results for different values of the external control voltage V_C are shown in Fig. 19. At low frequency the noise is the one predicted in Section IV-D, given by the thermal noise of the equivalent resistance of the pseudo-resistor and worsened by the linearity improvement factor N. At high frequency the noise of the OTA, dependent on the capacitive impedance at the virtual ground node and

TABLE I
PERFORMANCE COMPARISON WITH OTHER DESIGNS

Reference	**[3]**	**[5]**	**This Work**
Resistance Range	$1\,\mathrm{M\Omega} - 1\,\mathrm{G\Omega}$	$500\,\mathrm{M\Omega} - 70\,\mathrm{G\Omega}$	$20\,\mathrm{M\Omega} - 20\,\mathrm{G\Omega}$
Frequency Range	$0\,\mathrm{Hz} - 2\,\mathrm{MHz}$	$0\,\mathrm{Hz} - 8\,\mathrm{kHz}$	$100\,\mathrm{kHz} - 10\,\mathrm{MHz}$
Process σ/μ	0.043	0.3	0.255
Mismatch σ/μ	0.043	0.13	0.067
THD	$< 1\%$ ($V_{out} = 1\,\mathrm{V_{pp}}$)	$< 1\%$ ($V_{out} = 2.4\,\mathrm{V_{pp}}$)	0.33% ($V_{out} = 2\,\mathrm{V_{pp}}$)
Area	$16\,000\,\mathrm{um}^2$	$54\,000\,\mathrm{um}^2$	$17\,700\,\mathrm{um}^2$
Power	$0.2\,\mathrm{mW@1.8\,V}$	$2\,\mathrm{uW@3.3\,V}$	$0.1\,\mathrm{uW@3.3\,V}$
Technology	SOI $0.18\,\mathrm{um}$	CMOS $0.35\,\mathrm{um}$	CMOS $0.35\,\mathrm{um}$

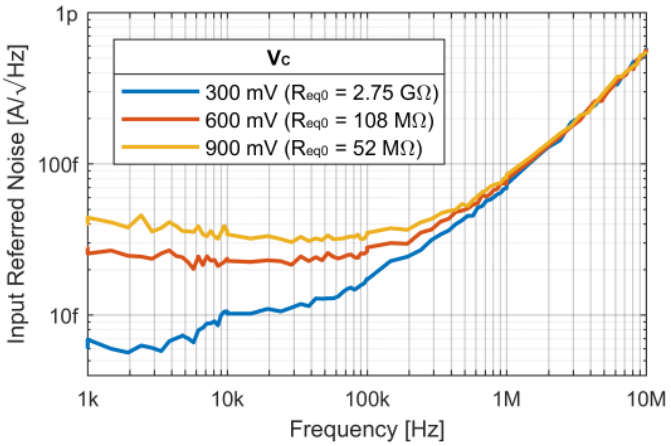


Fig. 19. Measured input referred noise of the system around $I_{DC} = 0\,\mathrm{nA}$ bias, for three different values of the external control voltage V_C.

proportional to the frequency, becomes dominant.

VII. CONCLUSION

This paper has presented an optimized architecture of pseudo-resistor, made in standard CMOS $0.35\,\mu\mathrm{m}$ technology, to bias a low-noise Trans-Impedance Amplifier for high sensitivity applications in the frequency range $100\,\mathrm{kHz}$ - $10\,\mathrm{MHz}$.

Multiple pseudo-resistor architectures have been critically reviewed in terms of resistance value, linearity of response, frequency behavior, simplicity of realization, and size.

The selected pseudo-resistor topology consumes an area of $0.017\,\mathrm{mm}^2$ and features a tunable resistance from $20\,\mathrm{M\Omega}$ to $20\,\mathrm{G\Omega}$, dynamic offset reduction thanks to a more than linear I-V curve and a high-frequency noise well below the one of a physical resistor of equal value. The pseudo-resistor bias network, implemented through floating voltage generators, has also been improved with respect to topologies found in the literature, compatible to the technology used and suitable for our application. Table I provides a comparison of our work with other state of art implementations, highlighting its strenghts in terms of frequency range, THD, area occupation, power consumption and stability against process variations.

The performance of the pseudo-resistor has been shown to be very competitive with respect to a physical resistor of the same value over a wide range of values so that pseudo-resistors are expected to be widely used in IC designs at a greater pace than have been so far.

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