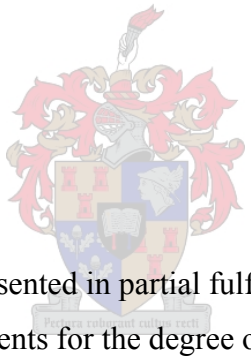
High voltage DC-DC converter using a series stacked topology

P.D. van Rhyn



Thesis presented in partial fulfilment of the requirements for the degree of Master of Engineering at the University of Stellenbosch

Supervisor: Prof. H. du Toit Mouton

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DECLARATION

I, the undersigned, hereby declare that the work contained in the thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

Signature: _____

Date: _____/_____/_____

SUMMARY

This thesis presents the design and implementation of a high voltage DC-DC converter using a series stacked topology. The converter's specifications were set by Spoornet and the converter forms part of a DC-AC inverter to be installed in Spoornet substations. Different converter topologies will be considered. A high frequency, high power coaxially wound transformer will be analysed, designed and manufactured for this specific converter application. A thermal analysis of the transformer will be carried out. The merits of different control schemes, leading to the choice of an average current mode controller, will be discussed. This controller will be designed and implemented to control the converter. The converter is then simulated to test and verify the controller functionality. A two-level series stacked converter is built and tested to verify the converter design and to test the functionality of the coaxially wound transformer. Finally, the results obtained will be discussed.

OPSOMMING

Hierdie tesis handel oor die ontwerp en implimentering van ‘n hoë-spanning GS-GS omsetter deur gebruik te maak van serie-gekoppelde topologie. Die omsetter se spesifikasies is vasgestel deur Spoornet en die omsetter vorm deel van ‘n GS-WS omsetter wat binne Spoornet sub-stasies geinstalleer gaan word. Verskillende omsetter-topologië sal oorweeg word. ‘n Hoë-frekwensie, hoë drywing, koaksiaal gewinde transformator sal geanaliseer, ontwerp en vervaardig word. ‘n Termiese analiese sal op die transformator uitgevoer word. Verskillende beheermetodes sal oorweeg word wat lei tot die keuse van ‘n gemiddelde stroom beheerder. Dié beheer metode sal in die omsetter geimplimenteer word. Die omsetter sal gesimuleer word om die werking van die beheerder te toets. ‘n Twee-vlak omsetter is gebou om die werking van die omsetter en die werking van die kaoksiaal gewinde transformator te toets. Laastens word die resultate verkry deur die praktiese opstelling bespreek.

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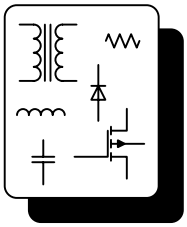
GLOSSARY

EPLD	Erasable Programmable Logic Device
VHDL	Very fast Hardware Description Language
RMS (rms)	Root Mean Square
emf.	Electromotive force
mmf.	Magnetomotive force
DC	Direct current
AC	Alternating current
ch	Channel
(Ex-y)	Equation y in chapter x



Chapter 1

PROJECT BACKGROUND

1.1 INTRODUCTION

This thesis covers the development of a high power DC-DC converter as part of the development of a high power DC-AC inverter. In this chapter the need for this new development is discussed and the specification outlining the development is stated. At the end of this chapter the thesis structure will be presented.

1.2 BACKGROUND

Some Spoornet substations are connected to the 11kV/6.6kV distribution supply system, from ESKOM, to operate their signal control systems. The Spoornet substations not connected to the ESKOM grid make use of a static thyristor inverter system to invert the available 3kV DC voltage of the railway lines to single-phase 220V AC (see Figure 1-1). These inverter systems are old and make use of potential dividers, indicated by R_V and D_1 to D_n in Figure 1-1, to drop the input voltage to the thyristor inverter to between 198V and 268V. The sum of the on-state forward voltage drop across each diode $(D_1$ to $D_n)$ is used to regulate the voltage at the input of the inverter while the resistor R_V limits the current from the 3kV power line through the diodes. This circuit configuration is not very efficient, but was the only option available since thyristor switches at that time were not able to withstand higher voltages. To get an idea of the current inverter's efficiency the following should be considered:

- All the current flowing into the thyristor inverter and the diodes $(D_1$ to $D_n)$ has to pass through R_V.
- Diodes $(D_1$ to $D_n)$ are permanently switched on to regulate the input voltage of the thyristor inverter. The diodes' conduction losses will contribute to the total power loss of the system.

It can be shown that the current potential divider setup will result in a system efficiency of less that 10%. With the recent advances in technology, such as the improvement in switch power ratings, a more efficient solution is possible (efficiency > 90%) and is required by Spoornet. Figure 1-1 shows a block diagram of the existing substation inverter setup.

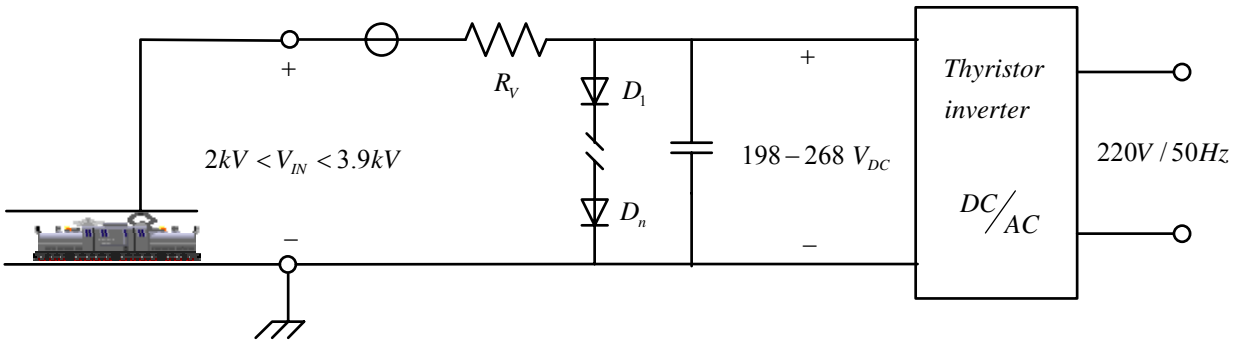


Figure 1-1 Block diagram of existing Spoornet-inverter arrangement

The new system required by Spoornet will consist of two main components, viz. A DC-DC converter to convert the varying 2kV-3.9kV Spoornet railway line voltage to a lower DC voltage level and a DC-AC converter to invert the lower DC voltage into 3 phase, $400V_{LL}$, AC voltage. A block diagram of the system new proposed system is shown in Figure 1-2. The existing Spoornet system implements a 50Hz isolation transformer inside the thyristor inverter. Since the inverter has a large power rating of 50kVA, this transformer will be bulky. The proposed system will implement a high frequency transformer inside DC-DC, converter which will greatly reduce the size of the transformer.

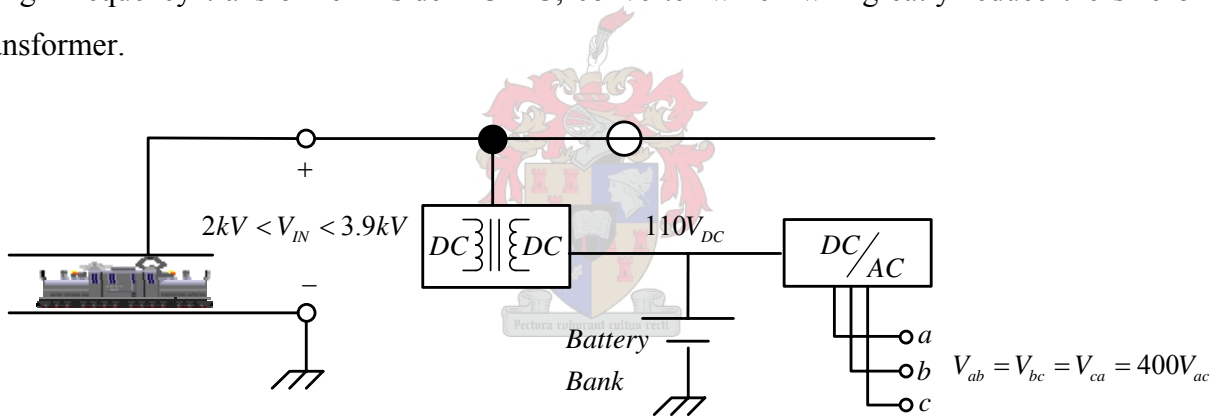


Figure 1-2 Block diagram of proposed Spoornet-inverter arrangement

Also indicated in Figure 1-2 is a battery bank which will be used as a backup supply. This will allow the DC-AC converter to continue operating even if a power outage occurs. As mentioned previously, the scope of this thesis is to design, simulate and implement the DC-DC converter part of the system.

1.3 SYSTEM REQUIREMENTS

The system specifications are stated in detail in [1]. Some of these specifications are discussed in the following section and all the specifications are summarized at the end of the section.

Figure 1-2 shows a battery bank at the output of the DC-DC converter and input to the DC-AC inverter. This battery bank serves as a backup and is standard equipment in every Spoornet

substation. This implies that the DC-DC converter will have to operate as a battery charger while supplying power to the load (DC-AC inverter).

The battery banks installed in the Spoornet substations are lead acid batteries. Lead acid batteries are usually charged according to their state of charge. If the battery terminal voltage is below a specified value, the battery is charged with a constant current. If the specified terminal voltage is reached the battery's terminal voltage is kept constant [2, 3]. This implies that the DC-DC converter will have to operate in such a manner that it is able to supply a constant current to the battery bank (and load) or keep the battery bank voltage constant.

The 3kV DC line voltage is not fixed and may vary between 2kV and 3.9kV. This variation in voltage is caused by the braking of an oncoming train. The frequency of the change in voltage should be considered when designing the control system for the converter.

Furthermore, this DC line voltage is generated by rectifying a 3-phase ESKOM supply by means of a full wave bridge rectifier. This method causes harmonics on the DC voltage and these harmonics lies in the range of 300Hz to 1200Hz. In converter topologies using bulk capacitors at the input of the converter, these harmonics may cause a large ripple current through these bulk capacitors. The capacitors should be designed to minimize this ripple current and to withstand whatever the magnitude of the ripple current may be after being minimized. The control circuit of the converter should also have good line regulation to avoid the ripple voltage at the input to filter through to the output.

According to the specifications, the power switches of the converter should be electrically isolated (withstanding 10.5kV) from the small signal electronics. This implies that a high frequency transformer will have to be used in the converter.

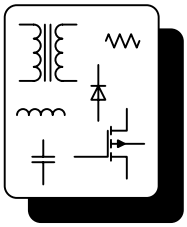
Table 1-1 gives a summary of the DC-DC converter specifications.

Table 1-1 DC-DC converter specifications	
Power rating	$50kVA$
Input voltage	$2kV < V_{IN} < 3.9kV\ (DC)$
Output current	$454.5A\ (DC)$
Output voltage	$110V\ (DC)$
Electrical Isolation	$10.5kV$
Operating temperature	$-10^{\circ}C$ to $50^{\circ}C$

1.4 THESIS OVERVIEW

The thesis is structured in the same manner as a systematic approach to designing a converter would be structured. The chapters of the thesis are in the following order:

- In chapter two, different DC-DC converter topologies are considered and potential topologies for implementation are identified. After analysing the advantages and disadvantage of the identified topologies, one topology is chosen.
- Chapter three covers the design of a high frequency transformer to be implemented in the converter. The transformer design forms a major part of the total converter design. An equivalent circuit is derived for this transformer and a thermal analysis is carried out.
- Chapter four covers the controller design for the converter. Different control options are discussed and the most suitable control scheme is chosen. A control circuit is then designed specifically for the application. Simulations are done to test the control scheme.
- Chapter five covers the hardware design of the converter. This includes the design of the bulk capacitors, power switches, filter components, driver circuits, protection circuits and controller board. Detailed circuit operation and loss calculations will be done.
- Chapter six shows the results obtained from the implemented converter system.
- Chapter seven will draw conclusions and discuss future work.



Chapter 2

HIGH POWER DC-DC CONVERTERS

2.1 INTRODUCTION

The aim of this chapter is to discuss all the converter topologies, existing or possibly new, that could be implemented in this specific DC-DC application. Potential topologies include basic DC-DC choppers such as the buck or buck derived topologies, multilevel topologies, and series stacked topology.

Note that the detailed circuit operation will not be discussed. The basic operating principles of each converter topology will be looked at instead in an attempt to identify one suitable topology for this specific DC-DC converter application.

2.2 DC-DC CHOPPERS

Since 3kV DC needs to be converted to 110V DC it is clear that a buck-type converter topology or buck derived converter topology will have to be implemented as converter topology. Figure 2-1 shows a simple buck converter [4]. For a buck converter the output voltage V_o is simply the duty cycle d times the input voltage V_i.

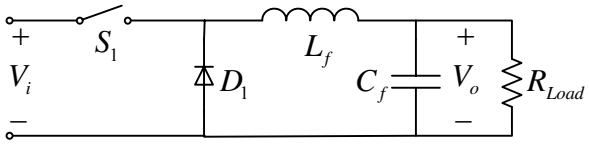


Figure 2-1 Buck converter

This buck topology would theoretically be the simplest topology to realise the required DC-DC converter. It is also easy to implement current mode control in the simple buck converter. The problem with this simple buck converter is that due to the converter's high power rating, 50kVA to be exact, the required switch (S_1) and filter components $(C_f$ and $L_f)$ will have to have high power ratings. The switch would have to block voltages in excess of 3.9kV. This eliminates the possibility of using a single MOSFET as a switch. If it were possible to find an IGBT capable of withstanding such high voltages the switching frequency would be limited to around 5kHz, implying that the filter components would be bulky and difficult to design and manufacture. The average current

through the switch will be large, 454A (50kVA/110V) at full load, which makes it even more difficult to find a suitable switch for this topology in this specific application.

It is possible to connect switches in series and parallel to reduce the voltage and current stresses in the switches [5 (pp 589-590), 6]. Figure 2-2 shows a buck converter with switches connected in series. This would reduce the required blocking voltage of each switch to $V_i/(\#\text{ of switches})$ where V_i is the input voltage of the converter.

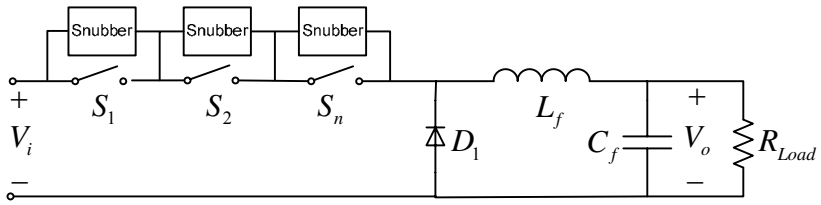


Figure 2-2 Buck converter with series connected switches

The main problem with connecting switches in series is that the dynamic voltage balance over the switches is not maintained due to turn-off delay time differences among the switches [4]. This could result in switch failure. This problem may be addressed by implementing accurate firing circuits and by using snubber circuits to force the voltage to divide evenly among the switches. However, these snubber circuits are difficult to design and cause additional power dissipation which reduces the converter efficiency. At higher switching frequencies (> 50kHz) snubber circuits becomes even more difficult to design and require a very fast snubber diode. This also increases the cost of the converter system.

Lastly, the simple buck converter does not implement a transformer. This implies that there is no electrical isolation between the input and output of the converter. Buck derived topologies such as the half-bridge and full-bridge [5] topologies provide the option of implementing a transformer which will provide electrical isolation between the primary and secondary sides of the converter. In the above-mentioned topologies the maximum switch blocking voltage is the DC bus voltage. In this high power application switches would have to be connected in series and parallel to handle the voltage and current stresses imposed on them. This could lead to a large number of required switches, dissipative snubber circuits, an accurate firing circuit, high current rectifying diodes and bulky filter components.

2.3 MULTILEVEL CONVERTERS

The multilevel converter topology is well known for its high bus voltage capabilities and harmonic-reduction properties [6, 7, 8]. There are three main multilevel topologies viz. the Flying capacitor (capacitor clamped) topology, the diode clamped (neutral point clamped) topology and the

cascaded multilevel converter topologies. The P2 cell multilevel topology was introduced in [9] and is a generalisation of the multilevel topologies. The flying capacitor and the diode clamped topologies can be derived from the general P2 cell multilevel topology [9]. Figure 2-3 (a) shows a M-level P2 cell multilevel converter, Figure 2-3 (b) a 5-level flying capacitor multilevel converter and Figure 2-3 (c) a 5-level diode clamped multilevel converter.

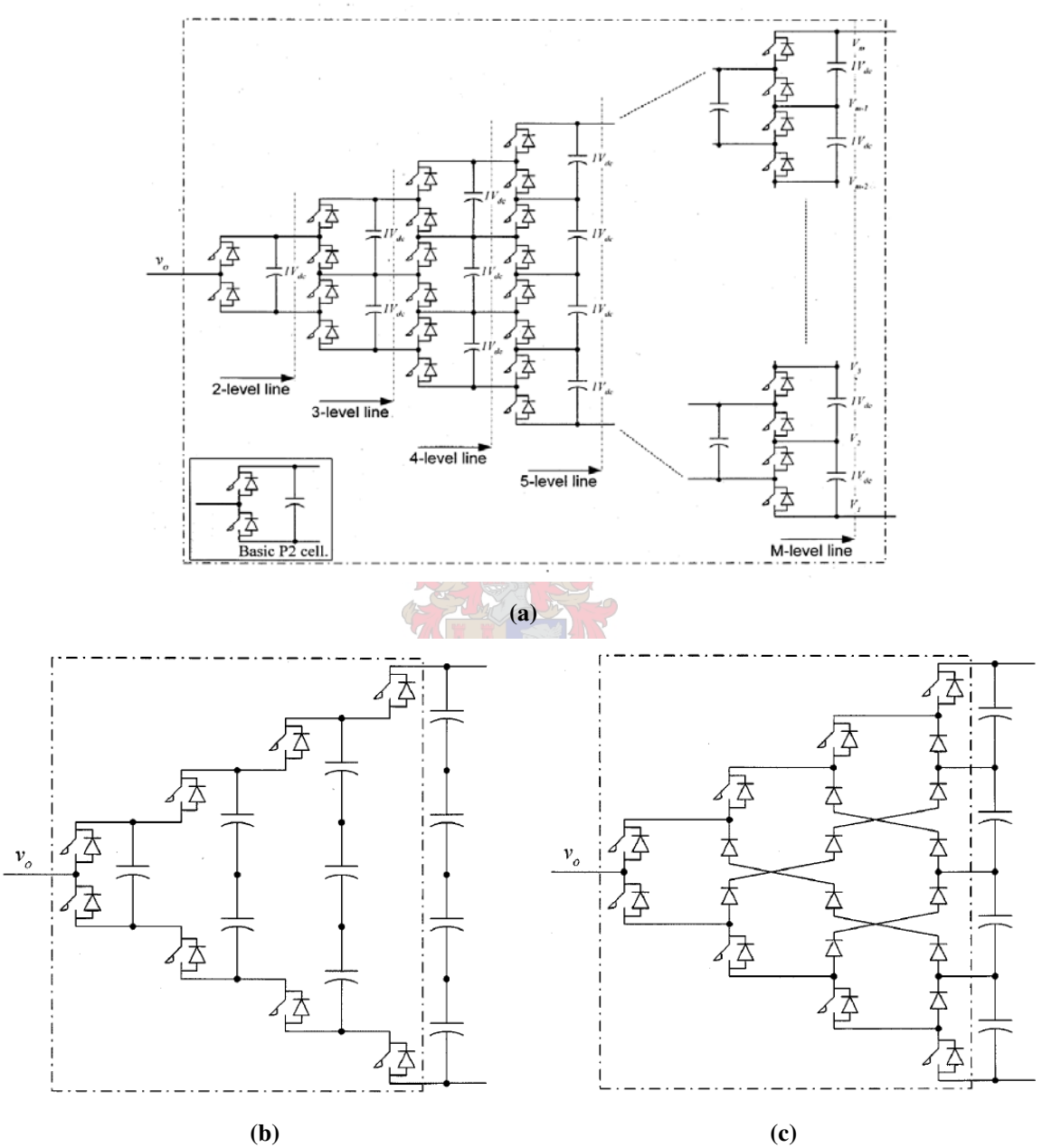


Figure 2-3 Multilevel converters (a) M-level P2 cell multilevel converter (b) 5-level flying capacitor multilevel converter (c) 5-level diode clamped multilevel converter [9]

The number of switches S_n used by the M-level P2 cell topology is $S_n = M \cdot (M-1)$. It can be seen that the number of switches required for such a converter quickly becomes large and impractical when the number of required levels is high. Both the flying capacitor and diode clamped topologies are simplifications of the P2 cell topology and require fewer switches to operate at the same voltage

level as the equivalent level P2 cell topology. In general, when the objective is to minimise cost, the flying capacitor and diode clamped topologies are preferred.

Figure 2-4 shows a standard three level (2 cell) flying capacitor multilevel inverter. The inverter is controlled by generating a carrier wave for every switch pair (S_1 and S_2 is one pair, S_3 and S_4 is another pair and so on) and comparing the carrier wave with a reference waveform. The reference waveform is normally sinusoidal and of a much lower frequency than the carrier waveform. Figure 2-5 shows an example of generating gate signals for one pair of switches. A switch pair is switched complementarily (if S_1 is on then S_2 is off). To improve the output voltage, waveform interleaved switching may be implemented to reduce the ripple on the output waveform [12]. This is done by phase shifting the carrier waveform of each switching pair with respect to each other. Figure 2-6 shows the output voltage of a two cell flying capacitor multilevel converter with the carrier waveforms' phases shifted by 180 degrees with respect to each other.

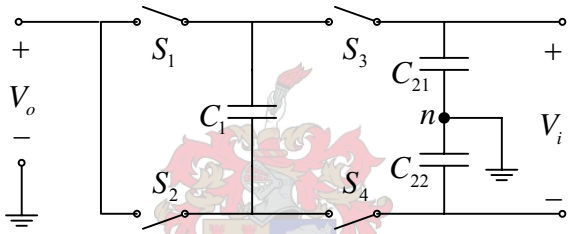


Figure 2-4 Three level flying capacitor converter

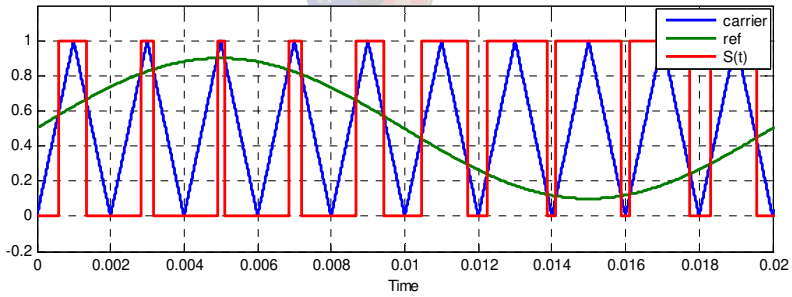


Figure 2-5 Carrier, reference and gate signal of one switch pair

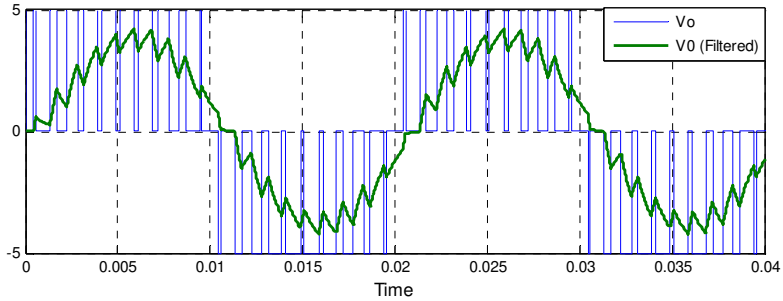


Figure 2-6 Filtered and unfiltered of V_o generated by a two cell flying capacitor multilevel converter with interleaved switching

To change the above discussed DC-AC inverter to a DC-DC converter the output voltage may be rectified and filtered. Figure 2-7 shows the circuit arrangement.

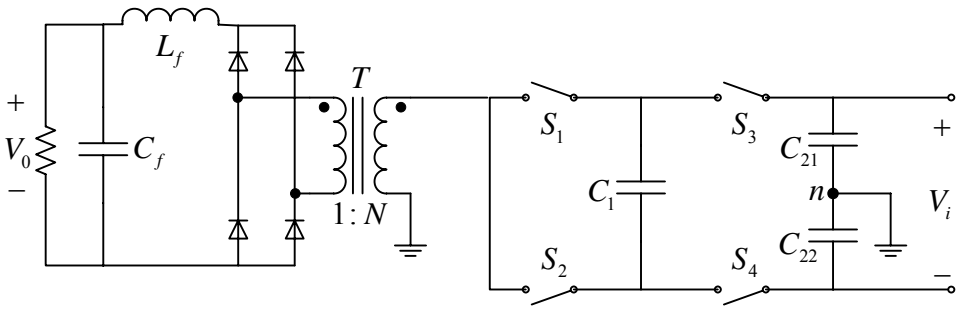


Figure 2-7 DC-DC converter arrangement derived from flying capacitor topology

The number of cells in the converter can be increased to satisfy maximum switch voltage requirements while the transformer increases the output voltage possibilities by changing the winding ratio. The output voltage is controlled by adjusting the amplitude of the reference waveform. This PWM method is not optimal since the voltage waveform across the transformer primary contains the frequency of the carrier waveform, which is a lot lower than the switching frequency. This would increase the size of the transformer significantly. The frequency of the carrier wave could be increased but this leads to a faster and more expensive controller.

To increase the frequency of the voltage waveform "seen" by the primary of the transformer, the PWM gate signals presented in [10] are used. [10] presents a three level (2 cell) capacitor clamped converter for DC-DC applications. In this discussion, the converter presented in [10] will be extended to a 4 level (3 cell) capacitor clamped converter. The configuration is shown in Figure 2-8.

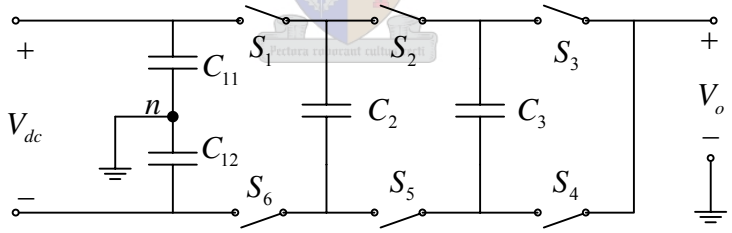


Figure 2-8 4 level (3 cell) Flying capacitor multilevel converter

Switches are grouped into pairs and phase shifted by $360^\circ/3$ because there are 3 cells used. Figure 2-9 shows the gating signals used to switch the converter. If it is assumed that the capacitors balance, the voltage across each capacitor may be calculated using the formula presented in [8]. In this specific case the voltages will be $C_{11} = C_{12} = V_{dc}/2$, $C_2 = 2V_{dc}/3$, and $C_3 = V_{dc}/3$. The output voltage V_o for each state is calculated in Table 2-1 and the output voltage waveform is shown in Figure 2-9.

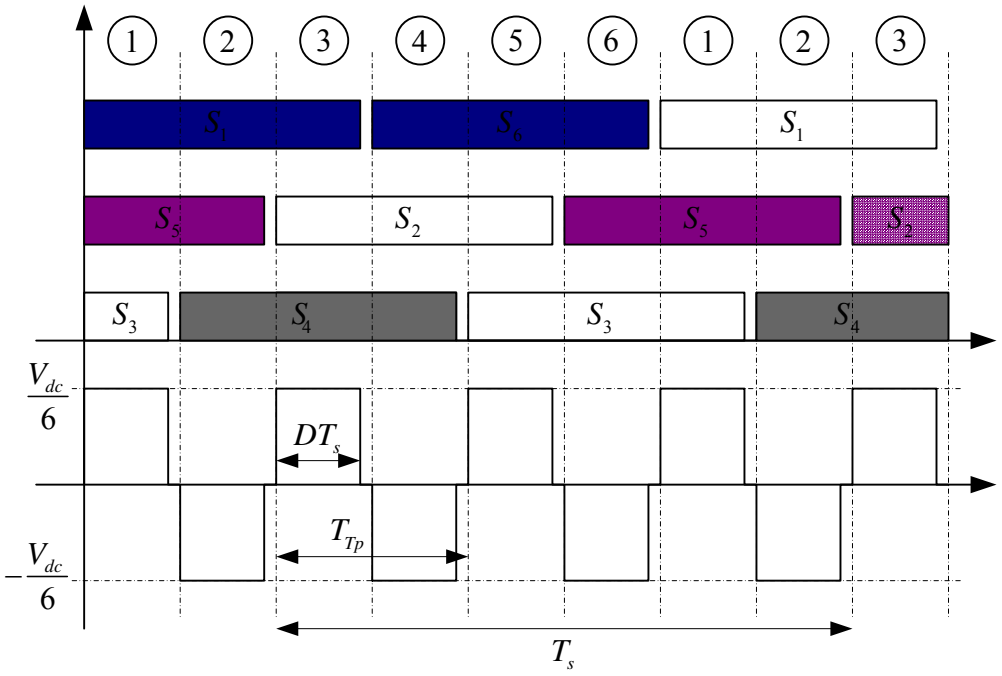
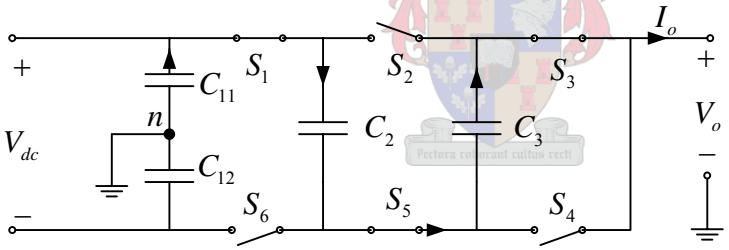
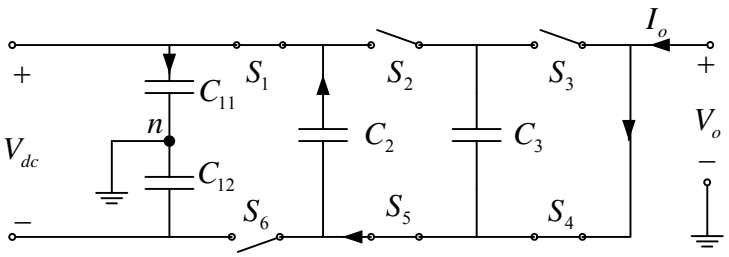
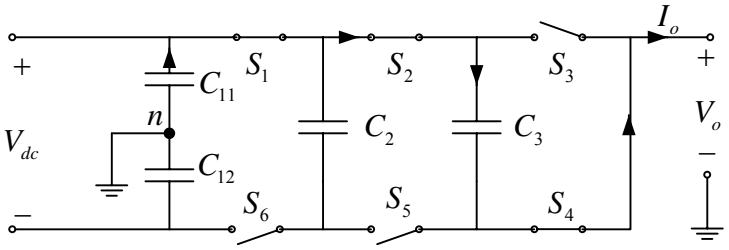
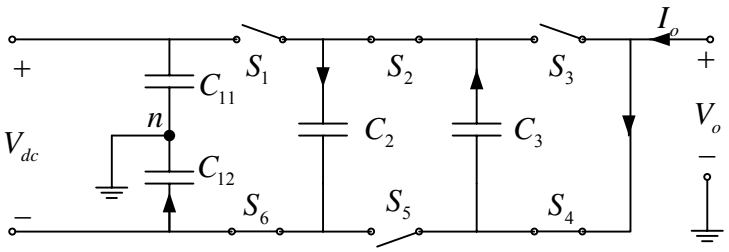
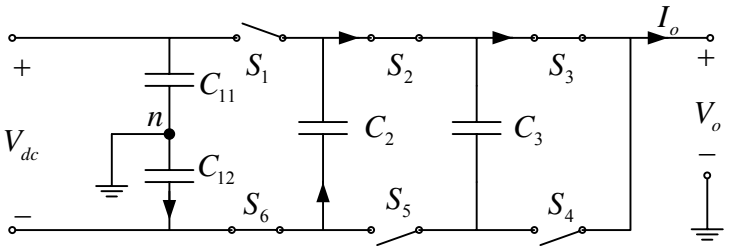
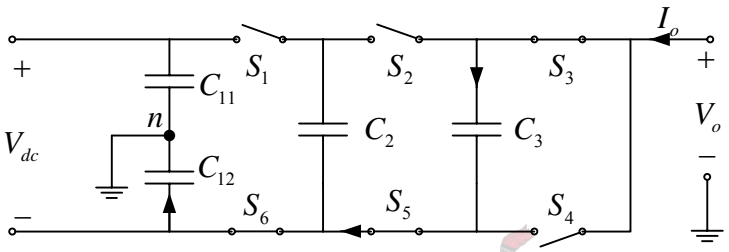


Figure 2-9 Phase shifted gate signals and output voltage waveform of 4 level (3 cell) flying capacitor multilevel converter

Table 2-1 Circuit diagram and output voltage of switching states for dc-dc operation

State	Circuit diagram of switching state	Output voltage
1		$-V_o+\frac{1}{2}V_{dc}-\frac{2}{3}V_{dc}+\frac{1}{3}V_{dc}=0$ $\Rightarrow V_o=\frac{1}{6}V_{dc}$
2		$-V_o+\frac{1}{2}V_{dc}-\frac{2}{3}V_{dc}=0$ $\Rightarrow V_o=-\frac{1}{6}V_{dc}$
3		$-V_o+\frac{1}{2}V_{dc}-\frac{2}{3}V_{dc}=0$ $\Rightarrow V_o=\frac{1}{6}V_{dc}$

4		$-V_o - \frac{1}{2}V_{dc} + \frac{2}{3}V_{dc} - \frac{1}{3}V_{dc} = 0$ $\Rightarrow V_o = -\frac{1}{6}V_{dc}$
5		$-V_o - \frac{1}{2}V_{dc} + \frac{2}{3}V_{dc} = 0$ $\Rightarrow V_o = \frac{1}{6}V_{dc}$
6		$-V_o - \frac{1}{2}V_{dc} + \frac{1}{3}V_{dc} = 0$ $\Rightarrow V_o = -\frac{1}{6}V_{dc}$

It can be seen from Figure 2-9 that the voltage frequency seen by the transformer primary is one third of the switching frequency. Assuming that the frequency at the primary of the transformer is fixed this may lead to reduced switching losses, since the required switching frequency is less than in other cases, e.g. the series stacked converter topology that will be discussed in the following chapter.

The switching strategy discussed may be extended to higher levels of the capacitor clamped topology. A disadvantage of this switching strategy is that not all possible switching levels are utilised. In the specific example only three of the possible four levels are used. This implies that a smaller than possible voltage will be applied to the primary of the transformer and this leads to higher currents flowing in the primary side of the converter.

Another concern about the flying capacitor topology is the large rms ripple current flowing through the clamping capacitors. Using this topology also means that one transformer will have to be implemented having a high power rating of 50kVA.

The diode clamped converter topology could also be implemented as a DC-DC converter. Switching schemes similar to these discussed above can be used to control the converter. A problem associated with the diode clamped topology is the difficulty in balancing the bulk capacitors for

converters having more than three levels. Ensuring equal voltage division among the clamping diodes also holds many design challenges [10].

2.4 SERIES OR PARALLEL CONNECTION OF CONVERTERS

Paralleling of converters to improve power ratings is commonly used [4, 11, 12, 13]. An example of two paralleled buck converters is shown in Figure 2-10.

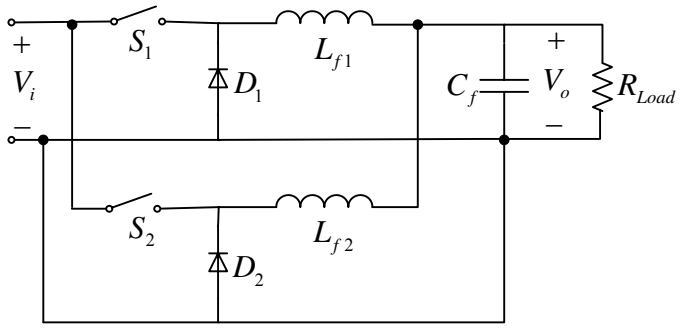


Figure 2-10 Two parallel connected buck converters

The main idea is to connect the converter inputs and outputs in parallel. This reduces the maximum current rating of each converter to one half for two converters in parallel and one third for three converters in parallel and so on. Control schemes have been developed to force equal current shearing among the converters. Also, interleaved switching has been implemented in some of these converters to reduce output current ripple [4].

Although the parallel connection of converters improves the power rating of a parallel connected converter system, it only reduces the maximum current rating of each converter. No reduction in the maximum voltage rating is possible since the inputs of the converters are all connected in parallel.

The most obvious way to reduce the switch voltage rating of a converter is to connect the input of the individual converters in series, creating one series stacked converter. An example of a series stacked converter is shown in Figure 2-11.

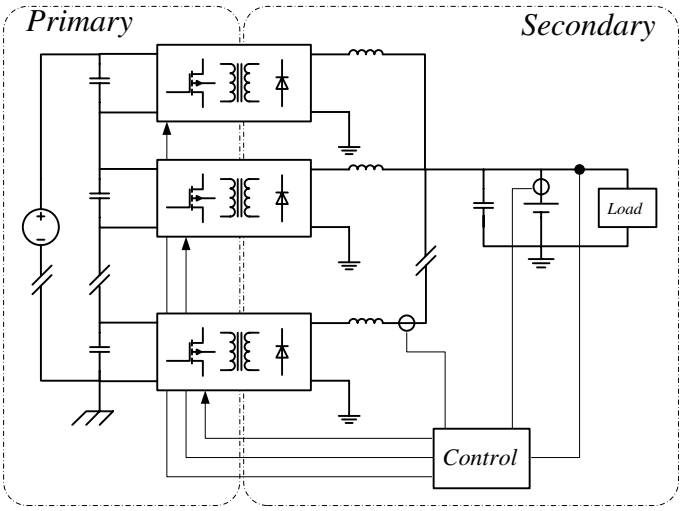


Figure 2-11 Series stacked converter –Input series, output parallel configuration

This idea of connecting the inputs of the individual converters in series and the outputs in parallel originated from [13]. In [13] two converters were stacked in series and there outputs were paralleled to reduce the voltage stress on the switches. The converters were successfully forced to share current by implementing an active charge control scheme.

Because there is only one source voltage, capacitors are used to divide the voltage at the inputs of all the converters in the stack. It is essential that these capacitors balance (have equal voltages across them) and stay balanced under all operating conditions. If the voltages across the capacitors are not equal some converters in the stack will have a larger voltage stress to handle. This could lead to system failure.

It is possible to stack half-bridge topology converters in series [5], but the full-bridge topology is preferred for the following reasons:

- In the full-bridge topology the output voltage waveform is twice the amplitude of the half-bridge equivalent. This implies that for equal converter power rating and maximum switch voltage, the switches of the full-bridge converter will carry half the current of their half-bridge converter equivalents. Since the voltage that will be seen by the transformer in the full-bridge topology is double that of the half-bridge equivalent, the transformer turn ratio from primary to secondary sides will have to be higher. As will be seen in chapter 3 this leads to a larger magnetisation inductance and less magnetisation current.
- There is some concern about the rms ripple current through the bulk capacitors of the half-bridge topology.

2.5 CHOOSING A TOPOLOGY

From the discussion in section 2.4.1 to section 2.4.3, three attractive topologies were identified as possible solutions to this specific high power converter application. These topologies are the flying capacitor topology and the diode clamped topology, using phase shifted control signals, and the series stacked full-bridge topology. To finally choose the most suitable topology a component cost analysis will be done. The major components contributing to total system cost are the type of controller and the number of high power components. A good indication of the most economical converter is obtained if the controller to be used and the number of power components are identified for each of the three converter topologies. For this analysis the following assumptions are made:

- The transformer winding ratio for each converter topology is fixed.
- The power switches, capacitors and clamping diodes to be used is the same for all three topologies.

2.5.1 FLYING CAPACITOR TOPOLOGY

From Figure 2-3 (b) it can be seen that the number of switches n_s used in a p-level flying capacitor converter is given by

$$n_s = 2(p-1)$$

The number of flying capacitors n_C is given by

$$n_C = \sum_{i=1}^{p-1} i$$

The number of levels to be used is determined by the maximum DC-bus voltage (3.9kV) divided by the maximum allowed switch voltage $V_{\max}$. For this specific case $V_{\max} = 650V$.

The control circuit required for the flying capacitor topology will be relatively expensive since there are no standard controllers for multilevel converters (flying capacitor or diode clamped topology) available on the market. A custom-made controller is needed and would consist of at least one expensive FPGA.

2.5.2 DIODE CLAMPED TOPOLOGIY

From Figure 2-3 (c) it can be seen that the number of switches n_s used in a p-level diode clamped converter is given by

$$n_s = 2(p-1)$$

The number of DC-bus capacitors n_C required is equal to $p-1$ and the number of clamping diodes n_D required is

$$n_D = 2\sum_{i=1}^{p-2} i$$

As mentioned in the previous section the diode clamped topology will require a relatively expensive control circuit.

2.5.3 SERIES STACKED FULL-BRIDGE TOPOLOGY

The number of switches n_s used in a stack of p full-bridge converters is given by

$$n_s = 4p$$

The number of required DC-bus capacitors n_C is given by

$$n_C = p$$

The free-wheeling diodes required in the full-bride topology in anti-parallel to each switch will not be counted separately because most IGBT and MOSFET packages have anti-parallel diodes implemented inside the package. The total cost will thus not be directly affected if one of the packages is used.

The controller circuit for the series stacked converter will be relatively inexpensive since many of full-bridge controller ICs are available on the market. A small EPLD may be used to interleave the switching signals for the individual converters in the stack.

The number of components required for each converter topology is listed in Table 2-2 and was calculated using the equations given in sections 2.5.1, 2.5.2 and 2.5.3.

Table 2-2 Number of components required for each converter topology

	Flying capacitor	**Diode clamped**	**Series stacked (Full-bridge)**
p	7	7	6
n_s	12 x 2	12 x 2	24
n_C	21	6	6
n_D	0	30	0
# of Transformers	1 (50kVA)	1 (50kVA)	6 (8.33kVA)
Controller cost	Expensive	Expensive	Inexpensive

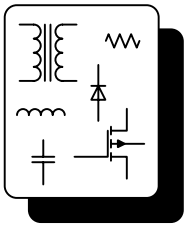
It is clear from Table 2-2 that the total number of components required by the series stack of full-bridge converters is a lot less than the total number of components required by the flying capacitor and diode clamped topologies. It is for this reason the series stack of full-bridge converters will be

used as converter topology. The series stack of full-bridge converters also requires a less expensive control circuit and makes use of six separate transformers, each with one sixth of the converter's total power rating. The use of six separate transformers will also simplify the transformer design with respect to thermal issues.

Lastly, one big advantage of the series stacked topology is that it is modular. Each converter in the stack serves as one module. The maximum power rating of the whole converter system may be increased or decreased simply by changing the number of modules in the stack.

2.6 SUMMARY

The aim of this chapter was to discuss all the converter topologies, existing or possibly new, that could be implemented in this specific DC-DC application. The diode clamped, flying capacitor and series stacked topologies were identified as the three most promising topologies for the specific application. The series stacked topology was selected as the best suited topology as it has many advantages, such as the lowest component count and inexpensive control circuitry, as well as being a modular converter.



Chapter 3

HIGH FREQUENCY, COAXIALLY WOUND TRANSFORMER

3.1 INTRODUCTION

The introduction of the first integrated circuit (IC) made a drastic improvement in the size, cost and performance of electronic equipment such as computers and telecommunication systems. Unfortunately, this was not the ultimate solution to the bulkiness of electronic equipment. All electronic devices need some sort of power supply. The first computer power supplies used 50/60Hz transformers to convert the available line voltage into the required voltage. The transformer was followed by a rectifier and linear regulators, to realise the required output voltage. This method was not very efficient.

In the 1950's the new silicon switches became available which enabled the development of multi-kHz switching frequency converters. These converters had smaller power transformers and filter components than the previous 50/60Hz transformers. At first, DC-DC regulators replaced the linear regulators on the secondary side of the 50/60Hz transformers. This greatly improved the system efficiency but did not eliminate the bulky line frequency transformer. Soon after this, with the introduction of 0.5kV to 1kV power transistors, the line voltage was rectified directly. This unregulated voltage was filtered by a large electrolytic capacitor and chopped, creating a higher frequency (square wave) voltage. This high frequency voltage resulted in a much smaller power transformer and finally power supplies became much smaller and more efficient.

The operating frequency of power supplies increased from line frequency into the kilohertz range. Today operating frequencies of up to 50MHz have been investigated. Transformers operating at these higher frequencies have been analysed in great detail and it has been shown that certain characteristics of the transformer influence the efficiency of the transformer itself and the efficiency of the system in which the transformer is implemented. These characteristics include leakage inductance, stray capacitance and eddy currents due to the skin effect and the proximity effect. The material used to construct the transformer and the structure of the transformer itself play a big part in the magnitude of these characteristics. This fact gave rise to the development of the coaxial transformer structure in an effort to increase the transformer efficiency.

The objectives of this chapter are to:

- Review the basic transformer theory.
- Compare the conventional transformer structure to the coaxially wound transformer structure.
- Analyse the coaxially wound transformer structure with special focus on leakage inductance, magnetisation inductance, dielectric breakdown and heat transfer.
- Design a special coaxially wound transformer for the high voltage DC-DC converter which is the main focus of this thesis.
- Practical implementation of the transformer in a DC-DC converter.
- Draw conclusions based on the results obtained from the practical implementation.

3.2 CONVENTIONAL TRANSFORMER

3.2.1 OPERATING PRINCIPLE

The easiest way to explain the operating principle of a transformer is to "invent" the transformer from scratch. Using a core with mean path length l, cross section area A and relative permeability μ. (see Figure 3-1 (a))

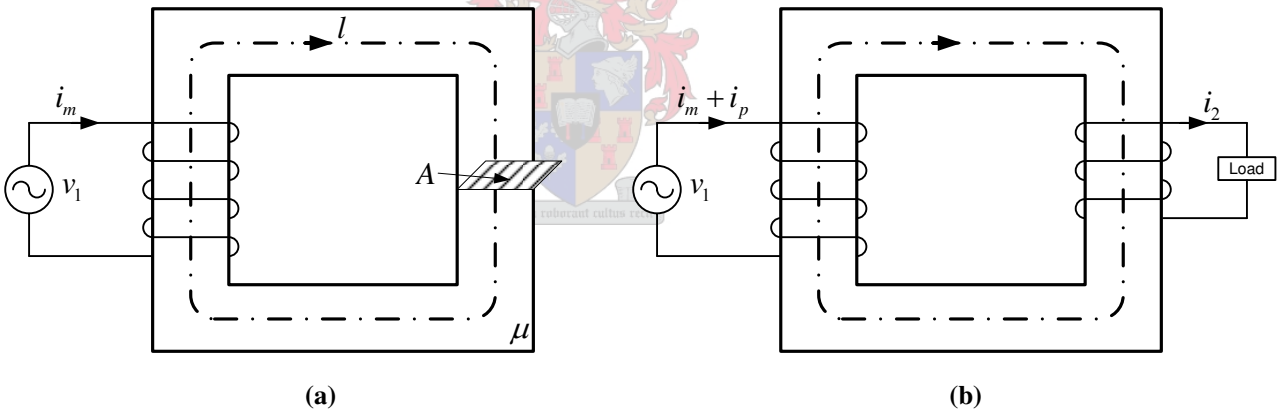


Figure 3-1 Transformer core plus coils

On the core there is a coil with an alternating voltage v_1 applied to it. An alternating current i_m will start to flow as a result of the applied voltage. Ampere's law tells us that the alternating current in the coil will produce an alternating flux ϕ in the core. Faraday's induction law tells us that the alternating flux will produce an emf. (a voltage) in any coil threaded by it, even if it is the coil producing the flux. If the induced emf. does not match the applied voltage, the current will increase or decrease so that the induced emf. matches the applied voltage exactly. Thus the dynamic balance is maintained.

Figure 3-1 (b) shows another coil added to the transformer with a load connected to it. The current flowing in this coil will contribute to the flux in the core. This causes the emf. in the primary core to be disturbed. A new component of current, i_p, starts to flow in the primary coil to restore the emf. in the primary winding.

3.2.2 EQUIVALENT CIRCUIT ANALYSIS

Transformers are implemented in electrical circuits. An equivalent electrical circuit for the transformer would help us in designing circuits and systems which include transformers. The derivation of the transformer equivalent circuit is well documented in many textbooks [5 (p 54)] and some theses [15] and it will not be repeated in detail here. It is however appropriate, with the aim of a later discussion on the coaxially wound transformer, to highlight some aspects of the basic transformer equivalent circuit and structure.

Figure 3-2 shows the derived wide bandwidth, high frequency transformer equivalent circuit [15]. It consists of the induced voltages $(e_1 \text{ and } e_2)$ on either side of an ideal transformer with a winding ratio as indicated. R_{c1} and R_{c2} represent the copper loss of the primary and secondary windings, while L_{l1} and L_{l2} represent the leakage inductance of the primary and secondary respectively. C_1 and C_2 are inter-winding capacitances and C_{12} represent the capacitive coupling between the primary and secondary. The magnetisation inductance is given by L_m.

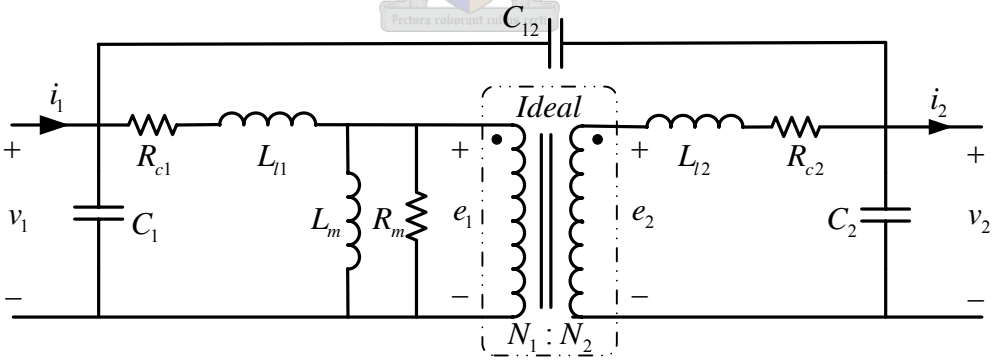


Figure 3-2 Wide bandwidth, high frequency transformer equivalent circuit

The equations for v_1 and v_2 are

$$v_1 = R_{C1} i_1 + L_{l1} \frac{di_1}{dt} + L_m \frac{di_m}{dt} = R_{C1} i_1 + L_{l1} \frac{di_1}{dt} + e_1 \qquad \text{(E3-1)}$$

$$v_2 = -R_{C2} i_2 - L_{l2} \frac{di_2}{dt} + \frac{N_2}{N_1} e_1 = -R_{C2} i_2 - L_{l2} \frac{di_2}{dt} + e_2 \qquad \text{(E3-2)}$$

Figure 3-3 shows the basic transformer arrangement similar to Figure 3-2 (b). Indicated in Figure 3-3 are the leakage flux components ϕ_{l1} and ϕ_{l2}. It is this leakage flux, which does not completely link the primary and secondary windings, which causes the leakage inductance components shown in Figure 3-2. The leakage flux is not necessarily an "unwanted" component. In some converter applications the primary leakage flux has been utilised and used to implement zero voltage switching [27]. If it is not in the designer's interest to utilise the leakage inductance for zero voltage switching, it is important to minimise this component to avoid undesirable circuit oscillations. Different transformer structures have been introduced to combat the leakage inductance problem. These include the E-core transformer with different winding structures presented in [17] and also the coaxially wound transformer discussed in section 3.3 of this chapter.

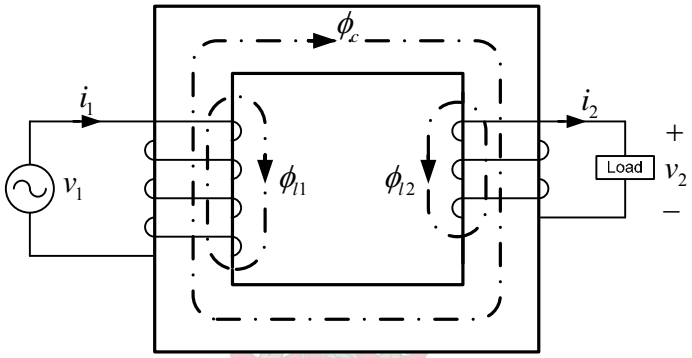


Figure 3-3 Transformer core with primary and secondary coils and associated leakage flux

3.3 COAXIALLY WOUND TRANSFORMER

It has been shown that the coaxially wound transformer structure is an excellent choice for realising high power, high frequency transformers [21]. Not only is the leakage inductance small, it is also very controllable as will be shown in the following section. It will also be shown that the leakage inductance is zero on the side of the transformer corresponding to the inner winding. For these reasons the coaxially wound transformer will be implemented in the high power DC-DC converter.

3.3.1 OPERATING PRINCIPLE

The coaxially wound transformer takes the form of coaxial cable as used in many high frequency applications. It is shown in Figure 3-4. It consists of an outer winding (tube or hollow conductor) and inner windings which could also be hollow conductors or litz wire. The transformer core consists of toroidal (or rectangular [16]) cores, placed around the outer conductor. Figure 3-4 shows the coaxial transformer arrangement. One disadvantage of this specific arrangement is that the winding ratio is restricted to n:1 or 1:n (n a chosen integer) because the outer conductor is a single winding. Other winding ratios are possible [15, 20] but they are difficult to construct and analyse. Some of these configurations are shown in Figure 3-5.

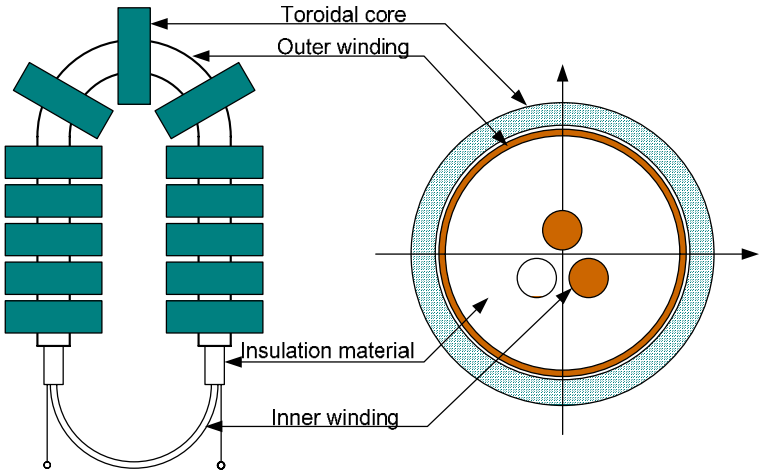


Figure 3-4 Coaxial transformer arrangement

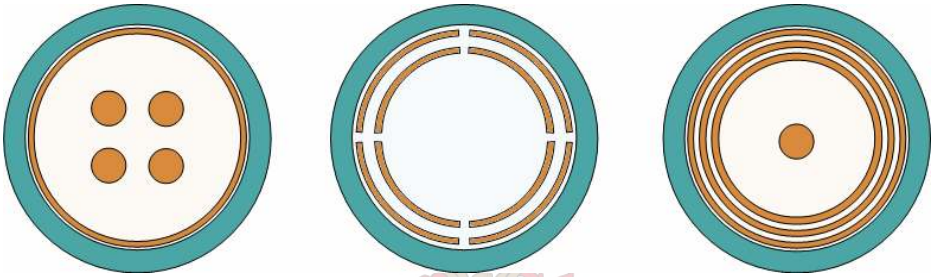
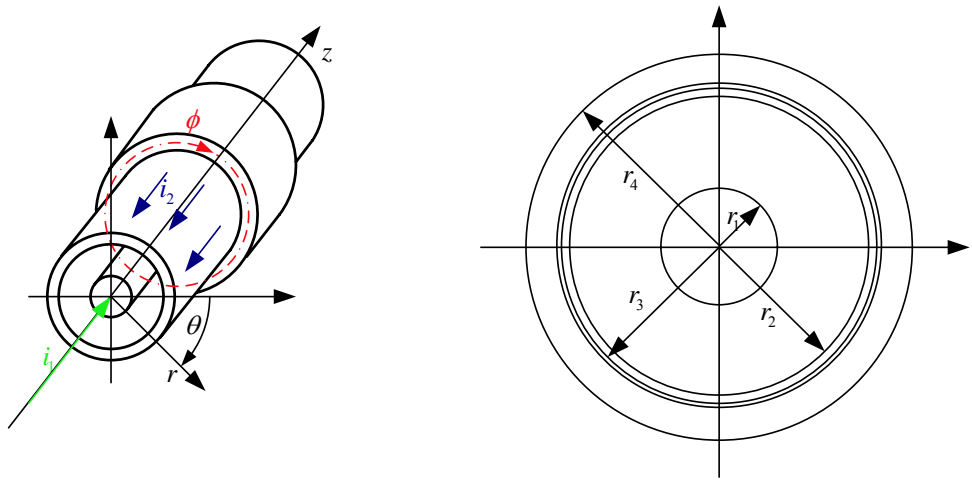


Figure 3-5 Different winding structures for coaxially wound transformer

The operating principle of the coaxially wound transformer is the same as presented in section 2 of this chapter. The transformer consists of an inner winding(s) and an outer winding(s) with the inner winding(s) chosen as the primary. If an alternating voltage v_1 is applied to this winding, it will result in an alternating current i_m through the primary conductor. According to Ampere's law a magnetic H-field will be formed around the current carrying conductor. This will result in a circulating flux in the core. Because the current in the conductor varies with time, the flux in the core will also vary with time. Faraday's induction law states that this time varying flux will induce emf. (a voltage) across all the windings threaded by it. Because of the U-shape of the transformer, the inner and outer windings are threaded around the core. This implies that an emf. will occur across both the windings. The same situation exists as in the conventional transformer. Figure 3-6 (a) shows one arm of the coaxially wound transformer with a primary and secondary current $(i_1$ and $i_2)$ as indicated. The circulating flux (ϕ) is also indicated. To determine the polarity of the induced voltages Lenz's law [5 (p 51)] is used.



(a) View of one "arm" **(b) Front-on view**

Figure 3-6 Coaxially wound transformer with one inner and one outer conductor.

3.3.2 EQUIVALENT CIRCUIT ANALYSIS

In order to use the coaxially wound transformer successfully in practical circuits an equivalent circuit model should be derived. This equivalent circuit model is similar to the one shown in Figure 3-2. The following sections of this chapter are devoted to calculating the values of the components in the equivalent circuit.

3.3.2.1 LEAKAGE INDUCTANCE AND MAGNETISATION INDUCTANCE

The theory, discussing the calculation of the leakage inductance for the coaxially wound transformer was first presented in [16]. To assist in the derivation of the transformer's leakage inductance and magnetisation inductance it is important to choose a coordinate system. A cylindrical system will be used to analyse the transformer system with unit vectors defined in Figure 3-7.

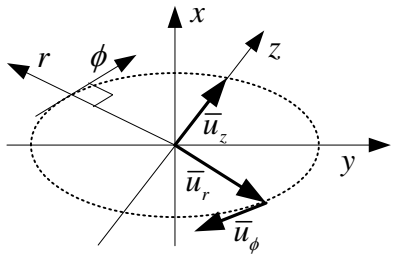


Figure 3-7 Unit vector definition

In order to find the leakage inductance and magnetisation inductance the H-field resulting from the current flowing in the inner conductor will have to be calculated. According to Ampere's law the line integral of this magnetic field intensity H equals the total enclosed current I_{enc}.

$$\oint_c \bar{H} \cdot d\bar{s} = \int_s \bar{J} \cdot d\bar{a} = I_{enc} \qquad \text{(E3-3)}$$

Because the enclosed current is not the same throughout the transformer, the transformer is divided into three regions (see Figure 3-6 (b)): inside the inner conductor $\left(0 < r < r_1\right)$, between the inner conductor and the outer conductor $\left(r_1 < r < r_2\right)$ and between the inner and outer radius of the outer conductor $\left(r_2 < r < r_3\right)$.

Start with the H-field inside the inner conductor. It is assumed that the current flowing inside the inner and outer conductors is uniformly spread. The uniform current density J is given by

$$J = \frac{i_1}{A} \text{ and } A = \pi r_1^2 \tag{E3-4}$$

where A is the cross section area of the inner conductor and i_1 the current flowing inside the inner conductor. It is found that

$$I_{enc} = \int_s \bar{J} \cdot d\bar{a} = \int_0^r \int_0^{2\pi} \frac{i_1}{\pi r_1^2} \left(r d\theta dr\right) = i_1 \frac{r^2}{r_1^2} \text{ for } \left(0 < r < r_1\right) \tag{E3-5}$$

Note that $\bar{J} = \left(J\right)\bar{u}_z$ and $d\bar{a} = \left(r dr d\theta\right)\bar{u}_z$. The left hand side of (E3-3) is now evaluated with $\bar{H} = \left(H\right)\bar{u}_\theta$ and $d\bar{s} = \left(r d\theta\right)\bar{u}_\theta$. It is found that

$$\oint_c \bar{H} \cdot d\bar{s} = \int_0^{2\pi} H r d\theta = 2\pi r H \tag{E3-6}$$

Setting (E3-5) equal to (E3-6), H is calculated as a function of r and in the θ direction.

$$2\pi r H = i_1 \frac{r^2}{r_1^2} \Rightarrow H_\theta\left(r\right) = \frac{i_1 r}{2\pi r_1^2} \text{ for } \left(0 < r < r_1\right) \tag{E3-7}$$

For the H-field in the region $r_1 < r < r_2$, it if found that the enclosed current is constant throughout the region. Thus,

$$I_{enc} = \int_s \bar{J} \cdot d\bar{a} = i_1 \tag{E3-8}$$

The left hand side of (E3-3) is the same for $r_1 < r < r_2$ and $r < r_1$. Thus,

$$2\pi r H = i_1 \Rightarrow H_\theta\left(r\right) = \frac{i_1}{2\pi r} \text{ for } \left(r_1 < r < r_2\right) \tag{E3-9}$$

For the region $r_2 < r < r_3$ the uniform current density is given by

$$J = \frac{i_2}{A} \text{ and } A = \pi\left(r_3^2 - r_2^2\right) \tag{E3-10}$$

The enclosed current is given by

$$I_{enc} = \int_s \bar{J} \cdot d\bar{a} = i_1 - \int_{r_2}^r \int_0^{2\pi} \frac{i_2}{\pi\left(r_3^2 - r_2^2\right)} \left(r d\theta dr\right) = i_1 - i_2 \left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right) \text{ for } \left(r_2 < r < r_3\right) \tag{E3-11}$$

It is clear from (E3-11) that if $r = r_3$ and an ideal transformer is assumed, with $i_1 = i_2$, the enclosed current equals zero. The left hand side of (E3-3) is the same for $r_2 < r < r_3$ and $r < r_1$. Thus,

$$2\pi r H = i_1 - i_2\left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right) \Rightarrow H_\theta(r) = \frac{1}{2\pi r}\left[i_1 - i_2\left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right)\right] \text{ for } (r_2 < r < r_3) \quad \text{(E3-12)}$$

It is now known that the H-field in various parts of the transformer. The relation between H-field and flux density is given by $B = \mu H$. The flux ϕ in various parts of the transformer may now be calculated by using

$$\bar{\phi} = \int_s \bar{B} \cdot d\bar{s} \quad \text{(E3-13)}$$

Start with the region where $0 < r < r_1$ and where it is known that $H_\theta(r) = i_1 r / 2\pi r_1^2$. The circulating flux is given by (E3-14). μ is the permeability of the medium under consideration.

$$\bar{\phi} = \int_s \mu \bar{H} \cdot d\bar{s} \quad \text{(E3-14)}$$

Note that internal flux linkage occurs inside the inner conductor. The flux linkage $\bar{\phi}_l$, which will eventually result in the internal inductance of the inner conductor [22], is calculated on a differential basis and integrated over the interior of the conductor. The differential flux linkage $d\phi_l$ is the differential flux $d\phi$ times the total current that is actually enclosed. The flux, per unit length, is calculated by $\phi = \int_0^{r_1} \mu H dr$ and the differential flux is given by $d\phi = \mu H dr$. Figure 3-8 shows a cross section view of the inner conductor with radius r_1.

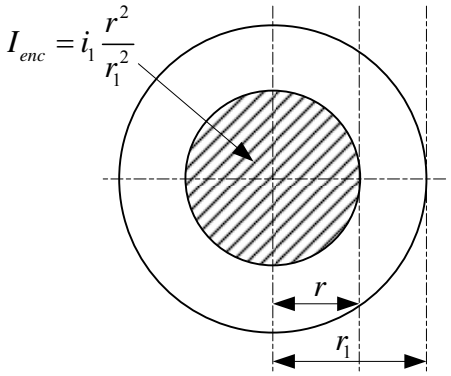


Figure 3-8 Cross section area of inner conductor with indicated enclosed current

The enclosed current I_{enc} is the current inside radius r and is a fraction of the total current i_1. The enclosed current is given by (E3-5) and is repeated for convenience.

$$I_{enc} = i_1 \frac{r^2}{r_1^2}$$

As a result the differential flux linkage or flux linkage for the ring is

$$d\phi_{l1} = \frac{I_{enc}}{i_1} d\phi = \left(\frac{r^2}{r_1^2}\right) \mu H dr = \left(\frac{r^2}{r_1^2}\right)\left(\frac{\mu i_1 r dr}{2\pi r_1^2}\right) \tag{E3-15}$$

The total flux linkage, per unit length, is now calculated by integrating the differential flux over the cross section area of the inner conductor:

$$\begin{aligned} \bar{\phi}_{l1} &= \int_0^{r_1} \left(\frac{r^2}{r_1^2}\right)\left(\frac{\mu i_1 r}{2\pi r_1^2}\right) dr \\ &= \frac{\mu i_1}{8\pi} \end{aligned} \tag{E3-16}$$

Finding the flux linkage $\bar{\phi}_{l2}$, per unit length, for the region $r_1 < r < r_2$ is much simpler because the enclosed current i_1 is constant. With $H_\theta = i_1/2\pi r$, it is found that

$$\bar{\phi}_{l2} = \int_s \mu \bar{H} \cdot d\bar{s} = \frac{\mu i_1}{2\pi} \ln\left(\frac{r_2}{r_1}\right) \text{ for } \left(r_1 < r < r_2\right) \tag{E3-17}$$

For the region $r_2 < r < r_3$ it was shown that $H_\theta(r) = \dfrac{1}{2\pi r}\left[i_1 - i_2\left(\dfrac{r^2 - r_2^2}{r_3^2 - r_2^2}\right)\right]$. Using the same method as that used in deriving (E3-16) the total flux linkage $\bar{\phi}_{l3}$, per unit length, is calculated as

$$\begin{aligned} \bar{\phi}_{l3} &= \int_{r_2}^{r_3} \left(\frac{I_{enc}}{i_1}\right) \mu \bar{H} dr \\ &= \int_{r_2}^{r_3} \left[\frac{i_1}{i_1} - \frac{i_2}{i_1}\left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right)\right] \frac{\mu}{2\pi r}\left[i_1 - i_2\left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right)\right] dr \end{aligned} \tag{E3-18}$$

Assuming an ideal transformer with a 1:1 turn ratio $(i_1 = i_2)$ it is found that

$$\begin{aligned} \bar{\phi}_{l3} &= \frac{\mu}{2\pi} \int_{r_2}^{r_3} \left[1 - \left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right)\right] \frac{i_1}{r} \left[1 - \left(\frac{r^2 - r_2^2}{r_3^2 - r_2^2}\right)\right] dr \\ &= \left(\frac{\mu}{2\pi} i_1\right) \left\{ \frac{r_3^4}{\left(r_3^2 - r_2^2\right)^2} \ln\left(\frac{r_3}{r_2}\right) - \frac{r_3^2}{\left(r_3^2 - r_2^2\right)} + \frac{1}{4} \frac{\left(r_3^2 + r_2^2\right)^2}{\left(r_3^2 - r_2^2\right)^2} \right\} \end{aligned} \tag{E3-19}$$

Finally the definition of inductance $\left(L = N\phi_l / i_1\right)$ is used to calculate the inductance for all the regions. Note that for N inner windings, $i_1 = N i_1$ in all the equations for ϕ_l and l is the length of the conductor. It is found that

$$L = \frac{N^2 \mu l}{8\pi} \text{ for } \left(0 < r < r_1\right) \tag{E3-20}$$

$$L = \frac{N^2 \mu l}{2\pi} \ln\left(\frac{r_2}{r_1}\right) \text{ for } \left(r_1 < r < r_2\right) \tag{E3-21}$$

$$L = \left(\frac{N^2 l \mu}{2\pi}\right)\left[\frac{r_3^4}{\left(r_3^2 - r_2^2\right)^2}\ln\left(\frac{r_3}{r_2}\right) - \frac{r_3^2}{\left(r_3^2 - r_2^2\right)} + \frac{1}{4}\frac{\left(r_3^2 + r_2^2\right)^2}{\left(r_3^2 - r_2^2\right)^2}\right] \text{ for } \left(r_2 < r < r_3\right) \qquad \text{(E3-22)}$$

It is now possible to calculate the leakage inductance L_{leak} since the leakage inductance is defined by the circulating flux not contributing to or opposing the current flowing in the opposite winding of the transformer. In the case of the coaxially wound transformer, this would be the inductance calculated for regions $0 < r < r_1$ and $r_1 < r < r_2$. Summing these inductances it is found that

$$L_{leak} = \frac{N^2 \mu l}{8\pi}\left[1 + 4\ln\left(\frac{r_2}{r_1}\right)\right] \qquad \text{(E3-23)}$$

It is important to remember that in this calculation uniform current distribution throughout the inner and outer windings and a winding ratio of 1:1 were assumed. For high frequency operation, the skin effect will force current to concentrate more closely to to the surface of the conductors. This will affect the result found in (E3-23). If multiple inner windings are used, the current distribution becomes even more complex and might influence the result even further. However, (E3-23) is widely used by designers and has been accepted as a good approximation for calculating leakage inductance on the inner winding side of the coaxially wound transformer. If the effect of skin depth has to be taken into account, a better approximation would be to assume that the current is uniformly spread up to one skin depth from the surface of the conductor. At very high frequencies, where the skin depth is very small in comparison with the radii of the inner and outer conductors, it can be assumed that the current is only flowing on the surfaces of the conductors.

The flux circulating inside the core $\left(r_3 < r < r_4\right)$ contributes to the magnetising inductance L_m. In this calculation it is assumed that no current is flowing inside the outer winding. This is done because, as discussed in section 3.2.1, flux needs to circulate inside the core before a voltage is induced and current starts to flow inside the outer conductor. The calculation is exactly the same as for calculating the inductance for the region $r_1 < r < r_2$. Replacing r_1 by r_3 and r_2 by r_4 it is found that.

$$L_m = \frac{N^2 \mu l}{2\pi}\ln\left(\frac{r_4}{r_3}\right) \qquad \text{(E3-24)}$$

3.3.2.2 CAPACITIVE COUPLING AND ELECTRIC FIELD STRENGTH

One important part of the transformer design is the isolation between the primary and secondary windings. In fact, this could well be the reason for implementing the transformer in a system in the first place. To find the maximum allowable potential difference between the inner and

outer windings the electric field strength between the inner and outer windings has to be looked at. The material or gas between the primary and secondary windings should then be analysed to see if a "breakthrough" situation may occur.

The equation for calculating the field strength E_r between the inner and outer conductor of the coaxial system has been derived in many textbooks [22, 23]. It is done using Gauss' law [18] and is given by

$$E_r = \frac{\Delta V}{r \ln\left(r_2 / r_1\right)} \tag{E3-25}$$

ΔV is the voltage difference between the inner and outer conductor, r is the radius, r_1 is the outer radius of the inner conductor and r_2 is the inner radius of the outer conductor (see Figure 3-6). It is clear from this equation that the field strength will be the strongest at the surface of the inner conductor. Thus, $r = r_1$. This result is used to ensure that the material used to separate the inner and outer conductor is sufficient enough to avoid breakthrough.

The capacitance C between the inner and outer conductor is also calculated in [23] and is given by

$$C = \frac{2\pi l \varepsilon}{\ln\left(r_2 / r_1\right)} \tag{E3-26}$$

l is the length of the conductors and ε the dielectric constant specific to the material used to separate the inner and outer conductors. In coaxial wound structure this capacitance could become significant and special care needs to be taken in selecting an insulation material to minimise the capacitance. Large values of this capacitance could cause unwanted currents to flow at switch turn on and turn off, causing EMI problems.

3.4 POWER LOSS

As in conventional transformers, two factors contribute to losses in the coaxially wound transformer. The first is core losses in the transformer core due to hysteresis loss and eddy currents flowing in the core. The second is copper losses caused by resistance of the copper windings. AC resistance arises from eddy current flowing in the copper windings due to the skin and proximity effects [17, 5 (p 771)].

3.4.1.1 CORE LOSS

A widely used formula to calculate core loss is found in [5 (p 745), 19]. The time average power loss per unit volume $\left(\overline{P_c(t)}\right)$ is given by.

$$\overline{P_c(t)} = kf^{\alpha}\hat{B}^{\beta} \tag{E3-27}$$

f is the frequency of operation, $\hat{B}$ is the peak flux density, and k, α and β are constants. These constants can be found in the manufacturer's datasheet by means of curve fitting. Normally a plot of core loss against flux density at a specific frequency is given on a log-log scale. This plot should be used to extract the constants k, α and β. (E3-27) is often referred to as the Steinmetz equation. The Steinmetz equation assumes the following:

- The excitation waveform is sinusoidal
- The flux density is uniform throughout the core
- The core does not saturate

To overcome the problem of non-uniform flux distribution in the coaxially wound transformer, the flux density is given a radial dependency [17]. Thus replace the $\hat{B}$ by $\hat{B}/r$ and integrating (E3-27) over the core volume would give the power loss of the core with non-uniform flux distribution taken into account. It turns out that the power loss caused by non-uniform flux distribution is less than the power loss caused by uniform flux distribution [17]. The difference in power loss is not significant.

A method of calculating the power loss for uniformly distributed flux with non-sinusoidal excitation is presented in [19]. In [19] it is identified that in piecewise linear flux waveforms, minor B-H loops exists where the waveform ceases to be monotonic. Two equations, containing the constants $(k,\ \alpha \text{ and } \beta)$ from the Steinmetz equation, are derived to calculate the power loss $\overline{P_c}$ in terms of the winding voltages V_j, assumed constant over each time period j of length Δt_j.

$$\overline{P_c} = \frac{k_i(\Delta B)^{\beta-\alpha}}{T}\sum_j \left|\frac{V_j}{NA_c}\right|^{\alpha}(\Delta t_j) \tag{E3-28}$$

Where

$$k_i = \frac{k}{2^{\beta+1}\pi^{\alpha-1}\left(0.276+\frac{1.7061}{\alpha+1.354}\right)} \tag{E3-29}$$

ΔB is the peak-to-peak flux of the loop under consideration, N the number of turns, A_c the core cross-section area and T the period of the waveform.

Since the method of calculating core loss by taking non-uniformly distributed flux into account does not differ significantly from the uniformly distributed flux calculation, the method of PWL waveform will be used to calculate core loss.

Note that core saturation is not considered because the design will ensure that the core does not saturate.

3.4.1.2 WINDING LOSS

Winding losses contribute a great deal to the total losses in the coaxially wound transformer. The high frequencies influence the current distribution in the windings and this increases the resistance of the windings. Winding power loss, P_{ave}, is calculated using $P_{ave} = R_{ac} I_{rms}^2$, where R_{ac} is the AC resistance of the winding conductor and I_{rms} is the rms value of current flowing through the winding conductors.

3.4.1.2.1 DC RESISTANCE

The dc resistance R_{dc} of a conductor with length l and cross section area A is given by

$$R_{dc} = \frac{\rho_c l}{A} \left[\frac{\Omega}{m}\right] \qquad \text{(E3-30)}$$

ρ_c is the resistivity of the material of the conductor. Note that the resistivity of a material changes with temperature.

3.4.1.2.2 AC RESISTANCE (SKIN EFFECT AND PROXIMITY EFFECT)

AC resistance is defined as $R_{ac} = R_{dc} + R_{ec}$. R_{ec} is the increase in resistance caused by eddy currents. This equation is normally expressed as $R_{ac} = F_R R_{dc}$. F_R is termed the resistance factor and

$$F_R = 1 + \frac{R_{ec}}{R_{dc}}.$$

Assuming cylindrical symmetry as in [17] and sinusoidal excitation current flowing in the outer transformer windings, the current distribution (J) is described by

$$\frac{d^2 J}{dr^2} + \frac{1}{r}\frac{dJ}{dr} - j\frac{\omega \mu_0}{\rho} J = 0 \qquad \text{(E3-31)}$$

r is the radial distance from the centre of the conductor and ω is the frequency of operation in radians per second. The solution (derived in appendix B) to this differential equation is found to be a linear combination of modified Bessel functions I_0 and K_0. For the inner winding it is found that

$$R_{ac(inner)} = \mathrm{Re}\left[\left(j\frac{f\mu_0}{a_i}\right)\left(\frac{I_0(a_i)K_1(b_i)+I_1(b_i)K_0(a_i)}{I_1(a_i)K_1(b_i)-I_1(b_i)K_1(a_i)}\right)\right] \quad \text{(E3-32)}$$

Where

$$a_i = \frac{\sqrt{2}r_{io}}{\delta}e^{\frac{j\pi}{4}} \quad \text{and} \quad \mathrm{b}_i = \frac{\sqrt{2}r_{ii}}{\delta}e^{\frac{j\pi}{4}}$$

For the outer winding it is found that

$$R_{ac(outer)} = \mathrm{Re}\left[\left(j\frac{f\mu}{b_0}\right)\left(\frac{I_0(b_o)K_1(a_o)+I_1(a_o)K_0(b_o)}{I_1(a_o)K_1(b_o)-I_1(b_0)K_1(a_0)}\right)\right] \quad \text{(E3-33)}$$

Where

$$a_o = \frac{\sqrt{2}r_{oo}}{\delta}e^{\frac{j\pi}{4}} \quad \text{and} \quad \mathrm{b}_o = \frac{\sqrt{2}r_{oi}}{\delta}e^{\frac{j\pi}{4}}$$

In most dc-dc converter applications, the current waveform will not be sinusoidal but triangular instead. In the case of non-sinusoidal excitation, the current waveform should be expressed in a Fourier series representation in conjunction with the ac resistance at each harmonic to calculate the total power loss.

It can be shown that the most effective tube thickness for the inner and outer windings is 1.55 times the skin depth (δ) [17]. This value is unfortunately not practical. A quick calculation of skin depth in a copper conductor with a current waveform frequency of 50kHz shows that the skin depth would be 0.29mm. An outer conductor of $1.55\delta = 1.55(0.29) = 0.449mm$ would be needed to satisfy this minimum ac resistance constraint. A tube with this wall thickness could possibly be mechanically unstable. The current density would also be very high when the current flowing through the conductor becomes large. To decrease the current density, the radius of the tube should be increased to enlarge the cross section area of the conductor. This could cause the conductor size to become impractical. With an increase in frequency the above mentioned problems become even more significant. In most application a tube thickness of around 2 to 9 times the skin depth is used.

When multiple windings are used to form the inner winding there is no longer coaxial symmetry between the inner and outer windings and the proximity effect needs to looked at for precise power loss calculations [5 (p 771), 15, 20]. However, the proximity effect is minimised by using litz wire and good results can be obtained by ignoring the fact that the windings are not centred.

3.4.2 THERMAL ANALYSIS

A thermal analysis of the coaxially wound transformer could not be found in the literature. It is however important to ensure that the transformer does not overheat under any operating condition. Overheating could cause the copper windings of the transformer to evaporate. It could also cause the core temperature to rise above the maximum rated temperature. This would decrease the permeability of the core and will result in unwanted core saturation. Doing a thorough thermal analysis would be complex and unnecessary for the purpose of simply protecting the transformer from overheating in any given section. Instead a "worst case" analysis will be done by constructing a thermal equivalent circuit of the transformer, using the basics of thermal resistance [5 (p 731), 24]. An approximate maximum temperature in various parts of the transformer will be calculated to ensure that the maximum rated temperature is not exceeded.

3.4.2.1 BASICS OF THERMAL RESISTANCE

Heat is transferred in three different ways, viz. conduction, convection and radiation [25]. The thermal resistances representing these three ways of conduction are $R_{\theta(cond)}$, $R_{\theta(conv)}$ and $R_{\theta(rad)}$ respectively. The thermal resistance for a heat conducting material with length l and cross section area A is given by

$$R_{\theta(cond)} = \frac{l}{KA}\left[\frac{^oC}{W}\right] \qquad \text{(E3-34)}$$

K is specific to different material and is called the thermal conductivity. This equation is similar to the electrical resistance R_{elec} of a current carrying material with length l and cross-section area A.

$$R_{elec} = \frac{l}{\sigma A}\ [\Omega] \qquad \text{(E3-35)}$$

σ represents the electrical conductivity of the material.

If conduction takes place in a radial direction, the electrical resistance of a hollow cylinder with length l, inner radius b and outer radius a is given by [18]

$$\mathrm{R}_{elec} = \frac{\ln(a/b)}{2\pi\sigma A}\ [\Omega] \qquad \text{(E3-36)}$$

Using this result and the analogue between thermal resistance and electrical resistance it is found

$$\mathrm{R}_{\theta(cond)} = \frac{\ln(a/b)}{2\pi KA}\left[\frac{^oC}{W}\right] \qquad \text{(E3-37)}$$

Equation (E3-37) can also be found by solving the heat transfer differential equation in cylindrical coordinates and using the appropriate boundary conditions [25].

The second method through which heat is transferred is convection. The thermal resistance due to convection may be calculated using

$$\mathrm{R}_{\theta(conv)} = \frac{T}{q} = \frac{\Delta T}{h_c A_s \Delta T_s} \quad \left[\frac{^oC}{W}\right] \tag{E3-38}$$

h_c is the convection heat transfer coefficient, A_s is the gradient (difference in temperature) from the surface to the ambient in the near vicinity of the surface and ΔT_s is the difference in temperature between the surface of the body and the surrounding area. Convection is more complicated than conduction because the convection heat transfer coefficient is a nonlinear function of ΔT. There are also separate convection coefficients for vertical and horizontal, and top and bottom surfaces. For most electronic components in still air, h_c may be approximated by the value of $0.47\left(mW\right)/\left(cm^2\right)\left(^\circ C\right)$. The thermal resistance may be calculated using

$$\mathrm{R}_{\theta(conv)} = \frac{1}{h_c A_s} \quad \left[\frac{^oC}{W}\right] \tag{E3-39}$$

Heat transfer via radiation is given by the Stefan – Boltzmann law:

$$P_{rad} = 5.7\times10^{-8} EA\left(T_s^4 - T_a^4\right) \tag{E3-40}$$

P_{rad} is the radiated power, E is the emissivity of the surface, A is the outer surface area, T_s the surface temperature in K and T_a the ambient temperature in K. The thermal resistance associated with this radiated power is given by

$$R_{\theta(rad)} = \frac{\Delta T}{P_{rad}} = \frac{\Delta T}{5.7\times10^{-8} EA\left(T_s^4 - T_a^4\right)} \tag{E3-41}$$

3.4.2.2 APPLYING HEAT TRANSFER BASICS TO TRANSFORMER STRUCTURE

The thermal analysis is started by looking at the physical structure (see Figure 3-9) of the coaxially wound transformer. The aim is to identify areas where the three ways of the transfer (discussed in previous section) are applicable. To reduce the complexity of the thermal equivalent circuit and keeping in mind that a worst case analysis will be done, the following assumptions are made:

- There is an electrically insulating material between the inner conductors and outer conductor with inner radius r_1 and outer radius r_2.
- The electrically isolating material and the outer conductor are separated by an air gap.
- The contact between the outer conductor and core and the inner conductors and electrically isolating material is perfect. This implies that there is a thermal resistance equal to zero between the aforementioned surfaces.

- The heat generated by the power dissipated inside the core is concentrated at the inside surfaces of the core. In the real situation, power is dissipated throughout the core resulting in heat generated evenly throughout the core.
- The heat generated by the power dissipated in the inner conductors and outer conductor is concentrated at the outside surfaces, but is distributed evenly throughout the length of these conductors.
- Heat transferred via radiation was not considered because temperature gradient between the surface of the transformer and the ambient are not big enough for radiation to play a significant role.

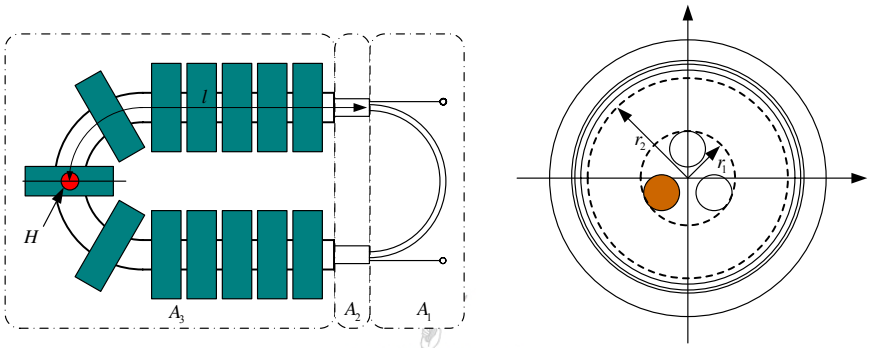


Figure 3-9 Coaxially wound transformer structure with identified heat transfer areas.

Three areas $(A_1, A_2$ and $A_3)$ with different ways of heat transfer were identified and shown in Figure 3-9.

- Area A_1: The exposed area of the inner conductor. Heat will be transferred via convection to the ambient.
- Area A_2: The exposed area of the inner conductor covered only by the electrically insulating material. Heat will be transferred in a radial direction through the electrically insulating material where convection will take place and transfer heat to the ambient.
- Area A_3: The main part of the transformer. Heat will be conducted in a radial direction by conduction through the inner conductor, electrically insulating material, air gap(s), outer conductor and core. Convection will cause heat to be transferred from the surface of the core to the ambient.

Note that heat will also be transferred through the length of the transformer. This will cause the transformer to cool down more quickly and it may ignored when a worst case analysis is done. Later in the section the effect of this heat flow on the temperature of the inner conductor will be looked at. Figure 3-10 shows the thermal resistance equivalent circuit of the transformer.

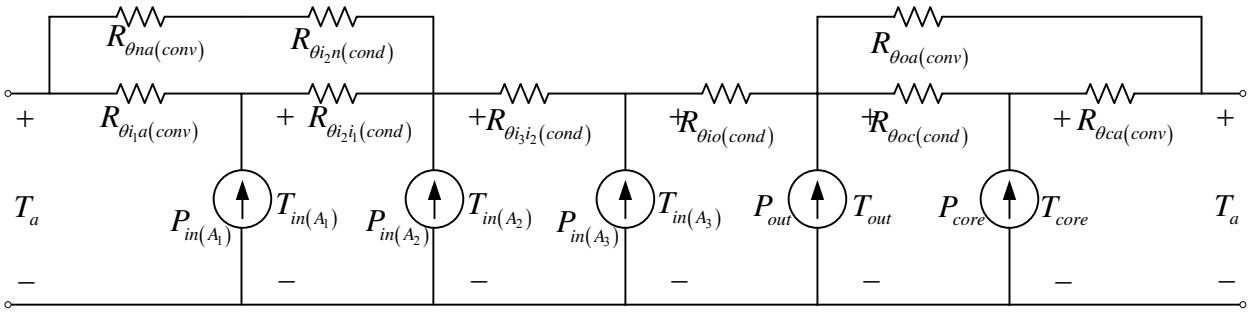


Figure 3-10 Thermal resistances equivalent circuit for transformer

Sources $P_{in(A_2)}$, $P_{in(A_3)}$, P_{out} and P_{core} represent the power dissipated in the inner conductors, outer conductors and core respectively and may be calculated using (E3-28), (E3-29), (E3-32) and (E3-33) The power dissipated in the inner conductor is divided into three parts, each representing a fraction of the power dissipated in the inner conductor. The fractions are determined by taking the length of the inner conductor falling in a specific area and dividing it by the total length of the inner conductor.

T_a, T_{out} and T_{core} represent the ambient, outer conductor and core temperatures respectively. $T_{in(A_1)}$, $T_{in(A_2)}$ and $T_{in(A_3)}$ represent the temperatures of the three parts of the inner conductor.

$R_{\theta i_1 a(conv)}$ is the thermal resistance opposing heat being transferred from the exposed inner conductor surface (A_1) to the ambient and is calculated using (E3-39). It is assumed that the heat generated inside the inner conductor, concentrates toward the outer surface of this conductor. This is valid because the inner conductor is thin and made of copper, which has a very high thermal conductivity. The skin effect also causes the current to flow on the outside surface of the inner conductor, which means that power dissipation largely takes place on the outside surface of the inner conductors.

$R_{\theta i_2 n(cond)}$ is the thermal resistance opposing heat being transferred, in a radial direction, from the inner conductor covered by the electrically isolating material (A_2), to the surface of this material. $R_{\theta i_2 n(cond)}$ is calculated using (E3-37).

$R_{\theta na(conv)}$ is the thermal resistance opposing heat being transferred from the surface of the electrically isolating material to the ambient and is calculated using (E3-39).

$R_{\theta io(cond)}$ is the thermal resistance opposing heat being transferred, in a radial direction, from the inner conductor (A_3) to the surface of the electrically isolating material and is calculated using (E3-37).

$R_{\theta oc(cond)}$ is the thermal resistance opposing heat being transferred from the inside of the outer conductor, in a radial direction, to the surface of the core and is calculated using (E3-37). The outer conductor is simplified and assumed to be an infinitely thin element at the inside of the core. This is valid because the wall of the outer conductor is very thin and it also has a very high thermal conductivity. It is also assumed that all the heat generated inside the core is generated at the inside surface of the core and not throughout the core volume. This will simplify the analysis and is valid in this worst case analysis.

$R_{\theta ca(conv)}$ is the thermal resistance opposing heat being transferred from the surface of the core to the ambient and is calculated using (E3-39).

Note that a part of the outer conductor is exposed to the ambient and heat will be transferred via convection and is represented by $R_{\theta oa(conv)}$ and calculated by using (E3-39).

$R_{\theta i_2 i_1(cond)}$ and $R_{\theta i_3 i_2(cond)}$ are the thermal resistances opposing heat being transferred from the covered part of the inner conductor $(A_1$ and $A_2)$, through the length of the transformer, to the exposed area of the inner conductor. From Figure 3-9 it can be seen that this resistance would be the largest looking from point H. It is assumed that the heat generated throughout A_3 is uniformly distributed. It is clear that point H is the "hot spot" of this specific transformer arrangement. The temperature gradient between the hot spot and the exposed area of the inner conductor may be calculated as follows:

Because it was assumed that the power dissipated inside the inner conductor is uniformly distributed, the inner conductor may be divided into n sections as shown in Figure 3-11. The thermal resistance between each section is equal to R_θ / n where R_θ is the total thermal resistance from the hot spot to the exposed are of the inner conductor. R_θ is calculated using (E3-34). The power dissipated in each section is calculated by dividing the total power dissipated inside the inner conductor by n. Thus, $P = P/n$

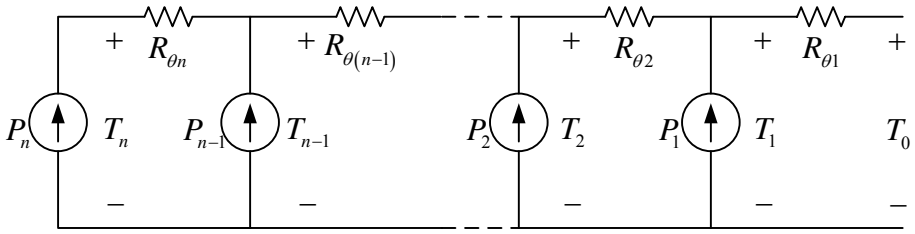


Figure 3-11 Model for calculating temperature gradient between the hot spot and exposed area of the inner conductor.

Using the analogue between electrical and thermal equivalent circuits and $\Delta T = PR_\theta$, the temperatures $\left(T_1, T_2, T_{n-1} \text{ and } T_n\right)$ for each section are calculated as follows.

$$T_1 = \frac{1}{n^2}\left(P_1 + P_2 + \ldots + P_{n-1} + P_n\right)R_{\theta 1} + T_0 \tag{E3-42}$$

$$T_1 = \frac{1}{n^2}\left(P_1 + P_2 + \ldots + P_{n-1} + P_n\right)R_{\theta 1} + T_0 \tag{E3-43}$$

$$T_{n-1} = \frac{1}{n^2}\left(P_{n-1} + P_n\right)R_{\theta(n-1)} + T_{n-2} \tag{E3-44}$$

$$T_n = \frac{1}{n^2}\left(P_n\right)R_{\theta n} + T_{n-1} \tag{E3-45}$$

Substituting (E3-42) into (E3-43), then (E3-43) into (E3-44) and then (E3-44) into (E3-45) it is found that

$$\begin{aligned} T_n &= \frac{1}{n^2}\left(\left(P_n\right)R_{\theta n} + \left(P_{n-1} + P_n\right)R_{\theta(n-1)} + \ldots + \left(P_2 + \ldots + P_{n-1} + P_n\right)R_{\theta 2} + \left(P_1 + P_2 + \ldots + P_{n-1} + P_n\right)R_{\theta 1}\right) + T_0 \\ &= \frac{1}{n^2}\sum_{j=1}^{n} R_{\theta j}\sum_{k=j}^{n} P_k + T_0 \end{aligned} \tag{E3-46}$$

Where j and k are integers. Simplifying (E3-46) it is found that

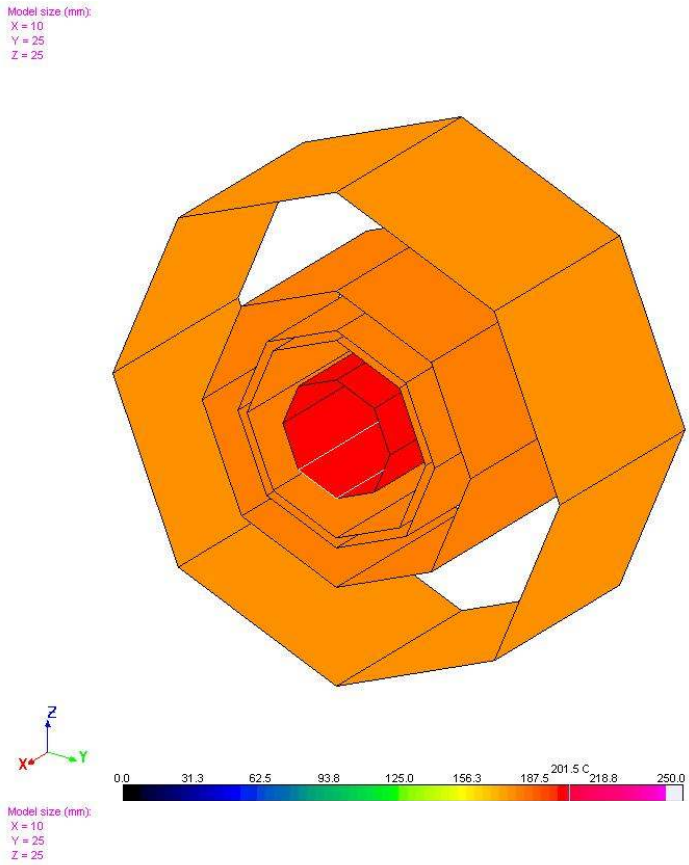
$$T_n = \frac{R_\theta P}{n^2}\sum_{j=1}^{n} j + T_0 \tag{E3-47}$$

Taking an infinite number of elements, thus $n \to \infty$, the summation turns into an integration from zero to infinity. It is found that

$$\begin{aligned} T_n &= \frac{R_\theta P}{n^2}\int_1^n j\,dj + T_0 \\ &= \frac{R_\theta P}{2} - \frac{1}{2}\frac{R_\theta P}{n^2} + T_0 \\ &= \frac{R_\theta P}{2} + T_0 \quad \text{for} \quad n = \infty \end{aligned} \tag{E3-48}$$

This result can easily be verified using the similarities between electrical and thermal equivalent circuits and by implementing Figure 3-10 in a simple spice simulation.

All the parameters shown in Figure 3-10 are now known and it is possible to find the temperatures of all the components in the transformer structure. To check if Figure 3-10 is a valid equivalent circuit representation WinTherm, a thermal analysis simulation package, was used. The simulation package is unfortunately limited and the number of elements used in the simulation was restricted. It was, however, possible to simulate heat transferred in a radial direction. Heat transferred through the length of the transformer was not considered and the transformer will thus be thermally insulated at the sides. Two simulations were done, each with different surface conditions of the outer conductor. For the first simulation the transformer was put in a box with no forced convection $\left(h_c = 4.7\left[W/m^2K\right]\right)$ and an ambient temperature of 50°C. The second simulation involved forced convection $\left(h_c = 170\left[W/m^2K\right]\right)$ with the same ambient temperature. The results of the simulations are shown in Figure 3-12.



(a) $h_c = 4.7\left[W/m^2K\right]$ **(b)** $h_c = 170\left[W/m^2K\right]$

Figure 3-12 Cross section view of simulated transformer temperature

As expected, the whole transformer structure is warmer in the case where the surface of the core is not exposed to forced convection. The simulated steady-state temperature of the inner conductor in the simulation involving no forced convection is 201.5ºC, and 105.4 ºC in the simulation involving

forced convection. It is clear that operating the transformer without forced convection at the surface of the outer conductor could damage the copper inner winding. If heat transferred in through the length of the transformer was taken into account, the simulated steady-state temperatures would be lower.

3.5 DESIGN PROCESS

This section will cover the actual design of the coaxially wound transformer. Starting off by listing the specific design inputs, and then using the theory discussed in the previous section to design the actual coaxially wound transformer that will be implemented in the dc-dc converter.

3.5.1 DESIGN INPUTS

As mentioned, six coaxially wound transformers will be implemented in a six level series stacked multilevel converter. Every converter has a power rating of 8.33 kW. The switching frequency will be 50 kHz. The winding ratio needs to be 2:1. Since it is easier to construct a coaxially wound transformer with one outer winding and multiple inner windings, the inner windings will be used as the primary of the converter. The secondary will be formed by a pipe with a large cross-sectional area and is perfect for the specific application since a large, high frequency current will flow in the secondary side of the transformer. The isolation between the primary and secondary is specified as 10kV. The operating ambient temperature is 50ºC. The primary voltage and current are shown in Figure 3-13.

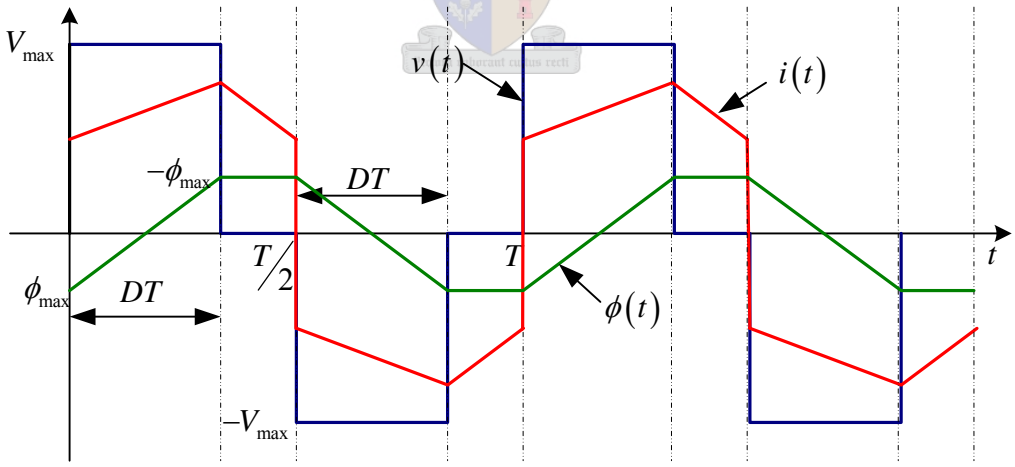


Figure 3-13 Voltage, current and flux waveforms at transformer primary

3.5.2 CORE CROSS-SECTIONAL AREA

Unlike in the theoretical world, an unlimited range (shapes and sizes) of copper tubes and toroidal cores are not available. Available for use are Philips toroidal cores (3E25 material) with an inner radius of 7.5mm, an outer radius of 12.5mm and width of 10mm. Also available to us is a copper tube with an outer radius of 14.5mm and an inner radius of 11mm.

A good starting point is to look at how many of these toroidal cores will be needed to ensure that the transformer core does not saturate. The voltage at the primary is given by

$$v(t) = N\frac{d\phi}{dt} \tag{E3-49}$$

N is number of primary windings. Using Figure 3-13 it is found that

$$dt = DT = \frac{D}{f} \tag{E3-50}$$

and

$$d\phi = \phi_{\max} - (-\phi_{\max}) = 2\phi_{\max} = 2B_{\max}A_c \tag{E3-51}$$

A_c is the cross section area of the core, $B_{\max}$ the maximum flux density, D the duty cycle and f the switching frequency. Substituting (E3-50) and (E3-51) into (E3-49) it is found that

$$V_{\max} = \frac{2NB_{\max}A_c f}{D} \text{ or } A_c = \frac{DV_{\max}}{2NB_{\max}f} \tag{E3-52}$$

The duty cycle when the input voltage is equal to $V_{\max}$ is 0.165. According to the Philips datasheet the core saturates at a flux density $(B_{\max})$ of $220mT$ at 100^oC. For temperatures lower than 100^oC the saturation point increases and is not of concern. The cross-sectional core area needed to avoid saturation can now be calculated using (E3-52).

$$A_c \geq \frac{DV_{\max}}{2NB_{\max}f} = \frac{0.165(667)}{2(2)(0.22)(50000)} = 25cm^2$$

The area of one toroid is also found on the datasheet an is equal to $48mm^2$. The number of toroids needed to avoid saturation may now be calculated as

$$\text{Number of toroids } = \frac{25}{0.48} = 52$$

Another factor that influence the number of toroids needed is the magnetisation current (i_m). i_m is calculated by using the magnetisation inductance of the transformer and looking the voltage-current relationship of an inductor where

$$v(t) = L\frac{di}{dt} \tag{E3-53}$$

For the coaxially wound transformer, it was found in section 3.3.2.1 that

$$L = L_m = \frac{N^2\mu l}{2\pi}\ln\left(\frac{r_{outer}}{r_{inner}}\right) = \frac{2^2\left(4\pi\cdot10^{-7}\cdot6000\right)(0.52)}{2\pi}\ln\left(\frac{12.5}{7.5}\right) = 1.28mH$$

μ is the permeability of the toroidal cores $\left(\mu = \mu_0\mu_r = \left(4\pi\cdot10^{-7}\right)\left(6000\right)\right)$, N the number of primary turns, l the length of the total core and r_{outer} and r_{inner} the outer and inner radii of a toroid respectively. From Figure 3-13 it can also be seen that

$$dt = \frac{D}{f} \tag{E3-54}$$

di may now be calculated by using (E3-53) and (E3-54)

$$di = \frac{DV_{\max}}{L_m f} = \frac{0.165\left(667\right)}{1.28\cdot10^{-3}\left(50000\right)} = 1.73A$$

This value of magnetisation current is relatively small compared to the peak-to-peak current ripple of the filter inductor (chapter 5). The number of toroids used will ensure that the magnetisation current remains within a reasonable range.

The leakage inductance is calculated using (E3-23).

$$L_{leak} = \frac{N^2\mu l}{8\pi}\left[1 + 4\ln\left(\frac{r_2}{r_1}\right)\right] = \frac{2^2\left(4\pi\times10^{-7}\right)\left(0.52\right)}{8\pi}\left[1 + 4\ln\left(\frac{0.055}{0.003}\right)\right] = 356nH$$

3.5.3 POWER LOSS

The power loss in the copper tube needs to be calculated to ensure that the heat generated will not become too much for the transformer to cool itself successfully. The outer conductor will be used as the secondary side of the transformer. The power P dissipated are given by

$$P = R_{ac}I_{rms}^2$$

The rms value of current I_{rms} on the secondary side of the transformer needs to be calculated, as well as the ac resistance R_{ac}, using the principles given in section 3.4.1.2.2 The Fourier series representation of the primary and secondary current $i_F\left(t\right)$ is given by

$$i_F\left(t\right) = a_k\cos\left(k\omega_0 t\right) + b_k\sin\left(k\omega_0 t\right) \quad \text{for} \quad k = 1,\ 3,\ 5...$$

Where

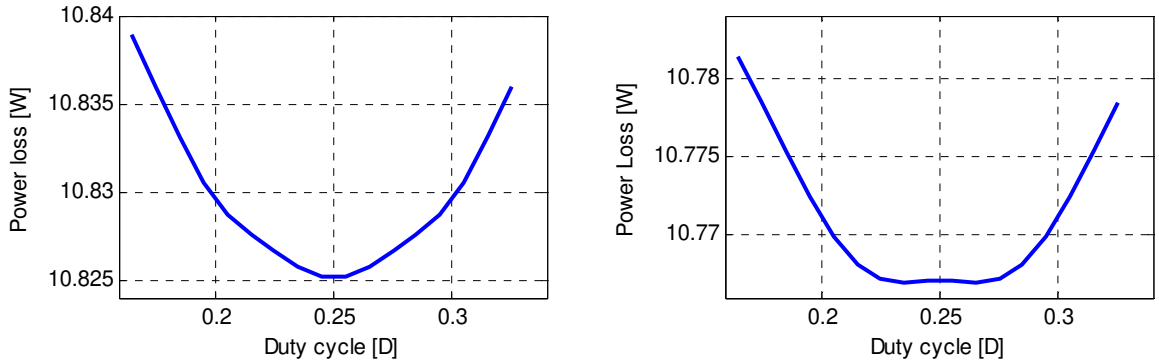
$$a_k = \frac{Tk_1}{\left(k\pi\right)^2}\left[\cos\left(k2\pi D\right) + 2k\pi D\sin\left(k2\pi D\right) - 1\right] + \frac{Tk_3}{\left(k\pi\right)^2}\left[\cos\left(k2\pi D\right) + 2k\pi D\sin\left(k2\pi D\right) + 1\right] + \frac{2\left(k_2 - k_4\right)}{k\pi}\left[\sin\left(k2\pi D\right)\right]$$

$$b_k = \frac{Tk_1}{\left(k\pi\right)^2}\left[\sin\left(k2\pi D\right) - 2k\pi D\cos\left(k2\pi D\right)\right] - \frac{Tk_3}{\left(k\pi\right)^2}\left[k\pi - \sin\left(k2\pi D\right) + 2k\pi D\cos\left(k2\pi D\right)\right] + \frac{2k_2}{k\pi}\left[1 - \cos\left(k2\pi D\right)\right] + \frac{2k_4}{k\pi}\left[1 + \cos\left(k2\pi D\right)\right]$$

Appendix A shows the complete derivation of the Fourier series. D is the duty cycle and T is the period of the waveform. k_1, k_2, k_3, and k_4 are constants describing the PWL waveform of the

primary or secondary current and can by found in appendix A. A MATLAB program was used to verify the solution.

The Fourier coefficients can be used to calculate the rms value of each harmonic of the waveform. Using (E3-32) and the ac resistance for each harmonic it is possible to calculate the power loss in the inner and outer conductors. Figure 3-14 (a) shows the power loss for the inner and outer conductors with $0.165 < D < 0.33$ and a primary current as presented in Figure 3-14 (b).



(a) Primary **(b) Secondary**

Figure 3-14 Calculated power loss in primary and secondary windings

Next the core loss in the transformer is calculated. Knowing the cross-sectional area, (E3-28) and (E3-29) is used, to calculate the power loss in the core resulting from the PWL flux waveform as shown in Figure 3-13. From the flux density against core loss plot on the toroidal core datasheet the parameters k, α and β is extracted. It is found that

$$k = 6.76\times10^{-6}$$
$$\alpha = 1.386$$
$$\beta = 2.74$$

Using (E3-29) it is found that

$$k_i = \frac{6.76\times10^{-6}}{2^{\beta+1}\pi^{\alpha-1}\left(0.276+\frac{1.7061}{\alpha+1.354}\right)} = \frac{6.76\times10^{-6}}{2^{2.74+1}\pi^{1.386-1}\left(0.276+\frac{1.7061}{1.386+1.354}\right)} = 361\times10^{-9}$$

Substituting k_i into (E3-28) it is found that

$$\begin{aligned}\overline{P_c} &= \frac{k_i(\Delta B)^{\beta-\alpha}}{T}\sum_j\left|\frac{V_j}{NA_c}\right|^{\alpha}(\Delta t_j)\\ &= \frac{361\times10^{-9}(440)^{1.354}}{20\times10^{-6}}\left[\left(3.3\times10^{-6}\right)\left|\frac{667}{2\cdot25\times10^{-4}}\right|^{1.386}+\left(3.3\times10^{-6}\right)\left|\frac{667}{2\cdot25\times10^{-4}}\right|^{1.386}\right]\\ &= 0.742\left[\frac{W}{cm^3}\right]\end{aligned}$$

The volume of the core is $157cm^3$. The core loss is calculated by multiplying the core volume by the power loss per cubic centimetre. Thus

$$P_{core} = 157 \times 0.742 = 116W$$

The maximum total loss of the specific coaxially wound transformer resulting from ac resistance and core loss are given by 116 + 10.77 + 10.83 = 113.3W. This is a 8.33kW transformer and will thus have a theoretically calculated efficiency of 98.4%.

3.5.4 ISOLATION

Lastly we have to ensure that the isolation between the primary and secondary side of the transformer is enough to prevent breakthrough. (E3-25) is used

$$E_r(r_1) = \frac{\Delta V}{r_1 \ln(r_2/r_1)} = \frac{10 \cdot 10^3}{(0.003)\ln(0.0055/0.003)} = 5.50\,MV/m$$

A material with breakdown voltage of more than $5.50\,MV/m$ is needed to prevent breakthrough. Table 3-1 lists a few possible usable materials with their breakdown voltages and relative dielectric constants ε_r.

Table 3-1 Materials with there relative dielectric constants and breakthrough voltages

Material	ε_r	Breakdown voltage $[MV/m]$
Air	1.0059	3
Myler polyester film	3.2	-
Rubber	2.8 - 3	12
Mika	5.4	-

From Table 3-1 it is clear that an air gap alone between the primary and secondary side of the transformer will not prevent breakthrough if the applied voltage is more than 10kV. The normal insulating coat covering the wire that will be used as inner winding is usually rated to be about 1kV. If the inner conductor is not exactly centred inside the outer conductor there is no guarantee that the transformer will not break through if the specified 10kV is applied to it. A possible solution is to use a rubber tube to insulate the primary and secondary windings. This would also help to centre the inner conductor which would result in more accurate leakage inductance calculation. Although rubber would probably serve well as an insulating material, no datasheet is available and manufacturing defaults are very likely in a normal rubber pipe manufacturing process. It was decided to use heat shrink as an insulating material, which has a rated breakthrough voltage of 30kV and will be able to withstand the high temperatures which will occur inside the transformer during operation.

The capacitance between the inner and outer windings may be calculated by using (E3-25). The dielectric constant of the heat shrink material used is not known. The capacitance was measured by measuring the time constant of a simple RC circuit. With R known, C could easily be calculated and was found to be $16\,pF$.

3.6 PRACTICAL RESULTS

Figure 3-15 shows a photo of a 8.33kW, 50kHz prototype coaxially wound transformer built in the laboratory. This transformer has a winding ration of 2:1. The transformer's primary and secondary terminals are indicated in Figure 3-15.

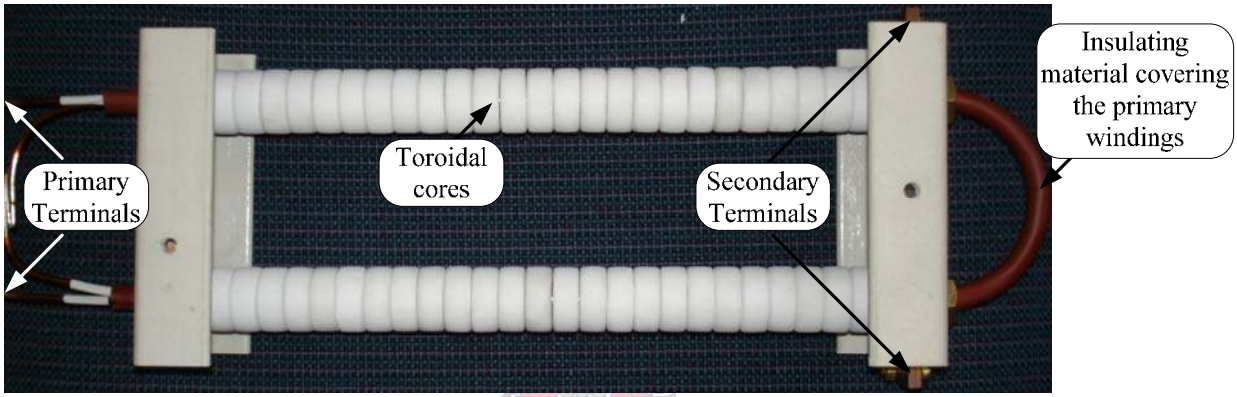


Figure 3-15 Photo of a prototype coaxially wound transformer build in PEG laboratory

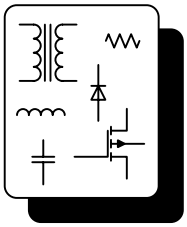
Due to manufacturing constraints, the outer winding (pipe) of the transformer could not be bent in order to fit toroidal cores all the way around the as shown in Figure 3-9. This will unfortunately increase the leakage inductance (see Table 3-2) of the transformer since flux will circulate around the exposed conductor (i.e. the part of the primary winding not covered by cores) and not contribute to flux circulating in the core. An advantage of building the coaxially wound transformer this way is that the "hot spot" discussed in section 3.4.2.2 will now be exposed to air and will result in a cooler steady state operating temperature than previously calculated. The prototype transformer's equivalent circuit parameters are summarised in Table 3-2.

Table 3-2 Prototype transformer's equivalent circuit parameters

	Theoretical	Practical
L_m	$1.28mH$	$1.33mH$
L_{leak}	$356nH$	$1.9uH$
C_{12}	$61pF$	$16\,pF$

3.7 SUMMARY

In this chapter, the basic transformer's theory was briefly reviewed and its structure was then compared to the structure of the coaxially wound transformer. The coaxially wound transformer was analysed with special focus on the leakage inductance, magnetisation inductance dielectric breakdown (between primary and secondary windings) and heat transfer. A prototype transformer was designed and built in the laboratory. The equivalent circuit parameters of the prototype transformer correlate well with the theoretically calculated parameters.

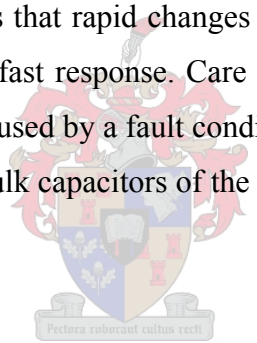


Chapter 4

CONTROL OF THE CONVERTER

4.1 INTRODUCTION

The controller of any converter forms an important part in the successful operation of the system. The controller of the converter under discussion has to incorporate two main functionalities. Firstly, the controller has to control the battery current while the converter is in the bulk charging state and secondly, the controller has to control the battery voltage while the converter is in the float charge state. Since the converter will be subjected to changes in load current and line voltage, the controller also has to ensure good load regulation and line regulation, respectively. The system's response time to a change in the battery voltage could be relatively slow because the battery will act as a large voltage source. This implies that rapid changes in the battery voltage will not occur and for this reason there is no need for a fast response. Care should be taken to avoid in-rush current through the inductor, which may be caused by a fault condition on the load side of the inductor. The controller also has to ensure that the bulk capacitors of the stack balance and stay balanced under all operating conditions.



The objectives of this chapter are to:

- Discuss different control schemes for DC-DC converter applications.
- Identify a control scheme that will satisfy the specific system requirements.
- Design a control system for this application.
- Simulate the control system to ensure proper functioning.

4.2 DC-DC CONTROL SCHEMES

Different control schemes have been developed to control DC-DC converters. The three most popular schemes are voltage mode control, peak current mode control and average current mode control [28, 29]. Another interesting control scheme, named charge control, was presented in [30]. In order to identify the most suitable control scheme, these four control schemes will briefly be discussed.

4.2.1 VOLTAGE MODE CONTROL

In voltage mode control [5 (pp 332-337), 28, 29], the output voltage of a converter is fed back to the PWM controller and the duty cycle is adjusted accordingly. Figure 4-1 shows a converter implementing voltage mode control.

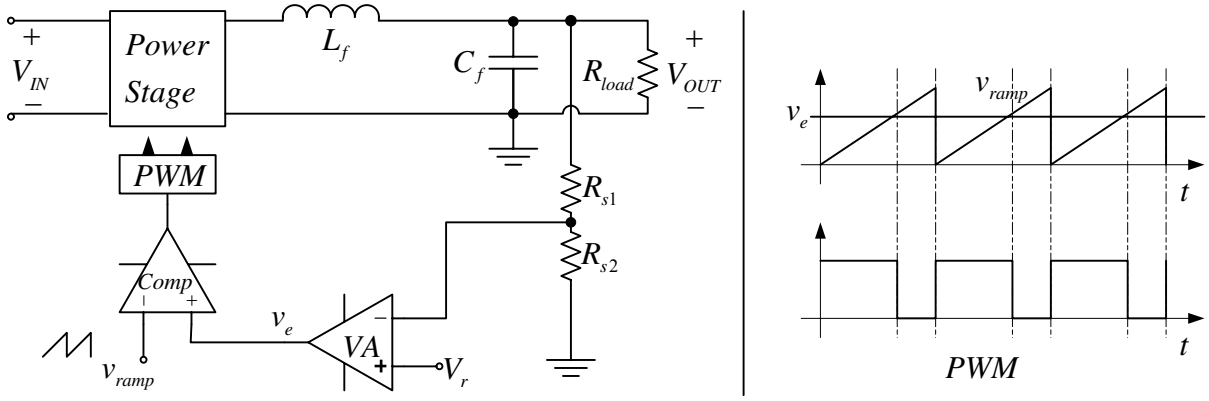


Figure 4-1 Block diagram of voltage mode controller

Voltage mode control has only one control loop, normally referred to as the voltage control loop. To design a stable control loop, the small-signal transfer functions of the converter power stage, voltage measurement and gain of the PWM comparator need to be taken into account [5 (pp 332-337), 29]. The control loop is stabilised by adding a compensation network around *VA* as shown in Figure 4-1.

The advantages and disadvantages of voltage mode control are listed below.

Advantages:

- It is easy to analyse the one feedback loop, thus simplifying the compensator design.
- The large amplitude ramp waveform (generated in the PWM comparator IC) ensures good noise immunity.

Disadvantages:

- The control loop is relatively slow in responding to changes in the line voltage and load current. This is because these changes are indirectly sensed as a change in output voltage.
- The input voltage range is reduced because of the fact that the input voltage occurs in the small signal transfer function of the converter power stage.

Voltage mode control could not used as control scheme for this application because of the bad line regulation characteristic and the fact that voltage mode control does not allow the control of current anywhere in the system.

4.2.2 PEAK CURRENT MODE CONTROL

In peak current mode control [28, 29, 31], the switch or inductor current is measured and compared to a reference value. This reference value is the output of a voltage error amplifier v_e. The switch (or switches, depending on the converter topology) is turned on while the measured current is less than the reference value and then turned off as it reaches the reference value. Normally a clock pulse will then turn the switch on again and the cycle repeats itself. Figure 4-2 shows a block diagram of peak current mode control and is self-explanatory.

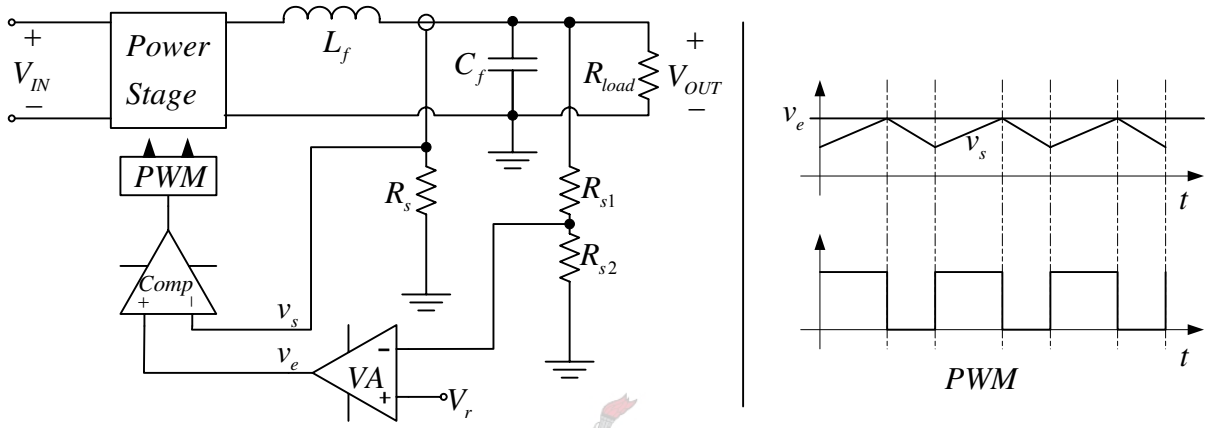


Figure 4-2 Block diagram of peak current mode controller

The advantages and disadvantages of peak current mode control are listed below.

Advantages:

- Since the inductor current rises with a slope determined by $(V_{IN} - V_{OUT})/L_f$, (input voltage minus output voltage divided by filter inductance [29]) the change in line voltage will reflect in the measured inductor current waveform. Thus, the converter will respond instantaneously to changes in line voltage. The delayed response due to a change in line voltage, and that is associated with voltage mode control, is eliminated in peak current mode control.
- The use of an error amplifier to control a current rather than a voltage minimises the effect of the output filter inductor and reduces the transfer function of the output filter to a single pole. This simplifies the compensation design.
- It allows inherent pulse-by-pulse current limiting by the converter.
- It allows load current to be shared if multiple converters are used.

Disadvantages:

- There are two feedback loops, making the circuit analysis more complex.
- Slope compensation is needed for duty cycles above 50% [28, 29, 31].

- Noise at the edges of the sensored current reduces the noise immunity of the system and requires additional filters which could influence current-loop design.
- Resonance in the power stage could insert noise into the control loop.
- Because the peak current is measured, there will be a peak to average current error. This error may be improved by slope compensation [31, 32].
- To accurately measure the high frequency inductor current waveform, required for this control scheme, will require a high bandwidth current measurement. This will be difficult to achieve since the inductor current to be measured will be large.

Peak current mode control is a more attractive control scheme for the specific application because it offers a way of directly controlling the inductor current.

4.2.3 AVERAGE CURRENT MODE CONTROL

The deficiencies of peak current mode control basically relate to the low internal loop gain. Average current mode control eliminates this problem by adding a current error amplifier into the current control loop (see Figure 4-3). Actually, average current mode control, when optimised, functions in exactly the same way as peak current mode control, together with all the positive attributes such as the same cross-over frequency and the same instantaneous response to a current overload. At frequencies below the cut-off frequency where the gain of a peak current loop flattens out to around 5 to 10, the average current control loop keeps rising until it reaches around 1000. This much higher gain at lower frequencies eliminates the peak-to-average current error and enables the average current mode control loop to function well under a light load when the inductor current becomes discontinuous.

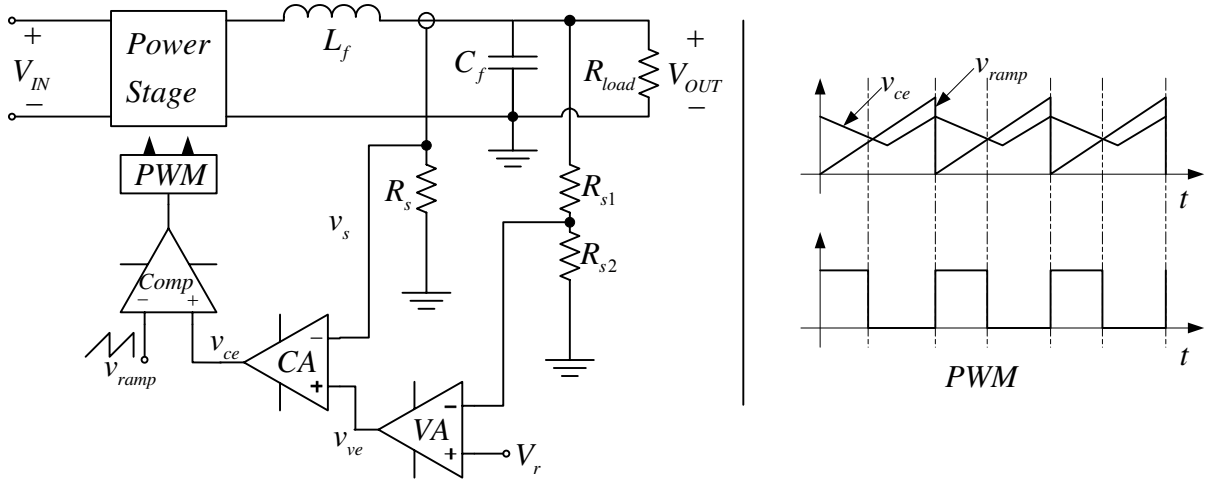


Figure 4-3 Block diagram of average current mode controller

In average current mode control, the switch or inductor current is measured and compared to a reference value through the current error amplifier CA. The reference value is given by the output of a voltage error amplifier v_{ve}. The output of current error amplifier (v_{ce}) is then compared to a fixed reference value, which is a pre-generated saw-tooth waveform. The switch is turned on while the output of the current error amplifier is greater than the saw-tooth reference and is turned off while the output of the current error amplifier is less than the saw-tooth reference.

Average current mode control is an attractive control method for the specific application. It allows accurate control of the average output current and functions well under discontinuous inductor current operation. The current measurement problem associated with peak current mode control is eliminated by average current mode control because the exact peak of the measured current is not required.

4.2.4 CHARGE CONTROL

Charge control [30] has the ability to control the charge per cycle of the switch current of a PWM converter. This control scheme is illustrated in Figure 4-4. The active switch in the power stage is turned on at the beginning of each cycle and the switch current is integrated to obtain its total charge. When the voltage across C_T reaches the control voltage v_e, the power switch is turned off and the switch across C_T is turned on, totally discharging C_T before the start of the next cycle. The total charge of the switch current in one cycle is proportional to the average current through the switch. This implies that the average switch current is controlled.

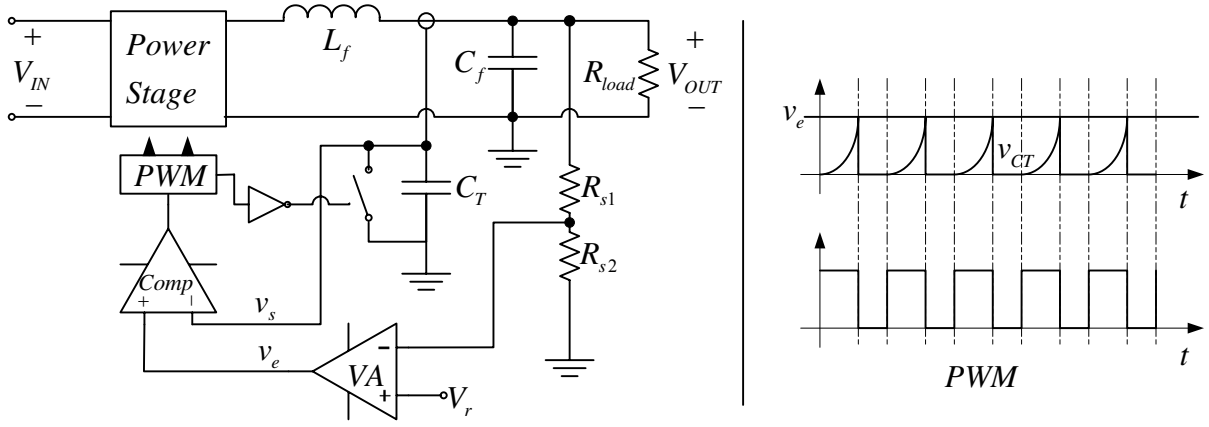


Figure 4-4 Block diagram of "charge" controller

Charge control offers a way of indirectly controlling the average switch current or inductor current. However, concern about sub-harmonic oscillations at certain duty cycles and light loads is pointed out in [30] and discourages the use of charge control in the specific application.

From the discussion of the four control schemes it is clear that average current mode control is the most attractive control scheme and will therefore be used to control the converter.

4.3 CONTROLLER IMPLEMENTATION

Many battery charge ICs are based on average current mode control. [34] covers the design of an "off-line lead acid battery charger" based on the UC3909 battery charge IC. A block diagram of the controller used in [34] is shown in Figure 4-5.

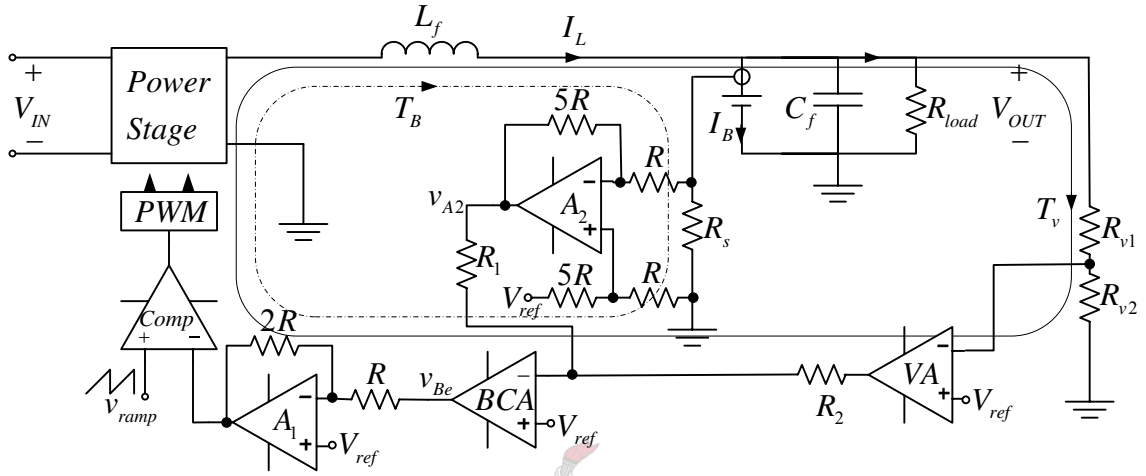


Figure 4-5 Block diagram of a lead acid battery charger's control scheme

In the above control scheme, the battery current I_B is measured through resistor R_s and amplified through A_2. The nature of the current sense amplifier is such that its output voltage v_{A2} is given by

$$v_{A2} = V_{ref} - 5R_s I_B \qquad \text{(E4-1)}$$

When the battery voltage is low and charged with constant current the output of the voltage error amplifier (VA) is high (equal to 5V). For the current error amplifier (BCA) to be in compliance, its inverting input must be equal to V_{ref}. The values of R_1 and R_2 may be calculated by summing the currents at the inverting input of BCA. Thus,

$$\frac{5 - V_{ref}}{R_2} = \frac{v_{A2}}{R_1} \quad or \quad R_1 = \frac{v_{A2}(R_2)}{5 - V_{ref}} \qquad \text{(E4-2)}$$

Knowing the value of both the reference voltage and battery current at which needs to be regulated, and choosing v_{A2} $(v_{A2} < 2.5V)$ the value of the current sense resistor may be calculated using (E4-1). R_1 and R_2 are then calculated using (E4-2).

R_{v1} and R_{v2} form a potential divider to feed back the output voltage to the VA. Amplifier A_1 is implemented to invert the output of the current error amplifier and ensure the right polarity for the PWM comparator. Compensation is added to the battery current control loop T_B by adding the

appropriate compensation networks around BCA and compensation is added to the battery voltage loop T_v by adding by adding the appropriate compensation network to VA.

The control scheme, discussed above, functions well for battery charging purposes. The shortcoming of the scheme is that only the battery current is sensed and the controller does not have any information on the inductor current (which includes information on the load current). If a load is connected, the battery will still be charged with the required current and current will be supplied to the load as long as the power stage is able to handle the sum of the currents. When a large step in load current is applied to the system (or a fault occurs in the load) the in-rush current through the inductor will not be controlled and this could damage the system. For this reason the control scheme discussed above could not directly be used in the specific application. Another control loop is added to measure the inductor current and avoid the risk of in-rush current damaging the system. The new control scheme is shown in Figure 4-6.

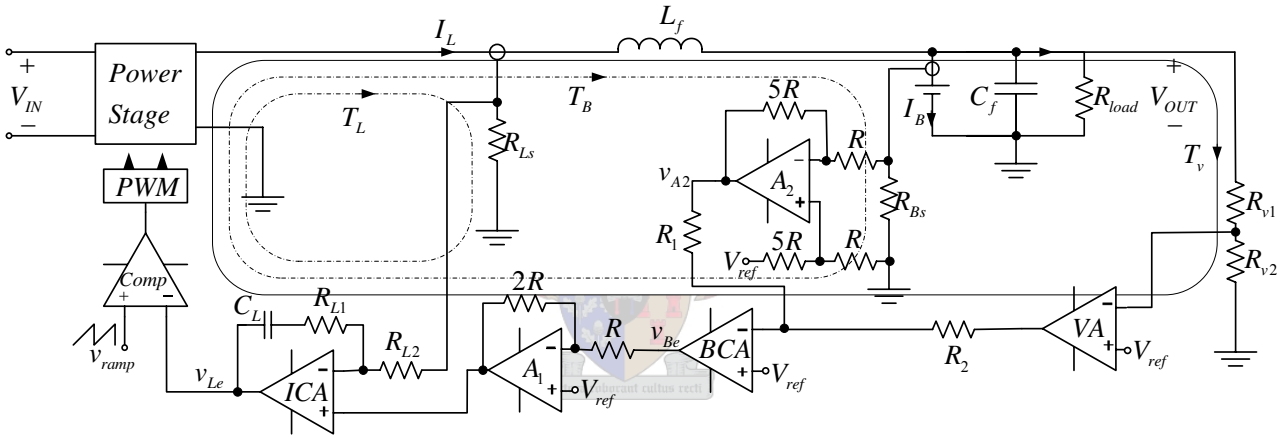


Figure 4-6 Control scheme to charge lead acid battery with added inductor current loop

Indicated in Figure 4-6 is the added inductor current loop T_L with its error amplifier ICA and compensation network consisting of C_L, R_{L1} and R_{L2}. R_{Ls} is the current sense resistor used to sense the inductor current. This control circuit functions in exactly the same way as conventional average current mode control. The only difference is the presence of two "outer control loops", the battery current and battery voltage loops, instead of the conventional single output voltage control loop. By proper design of the outer control loops, the battery current or battery voltage may be controlled depending on the state of charge of the battery.

Figure 4-7 shows a block diagram of the control system. Indicated in Figure 4-7 are all the transfer functions present in the system.

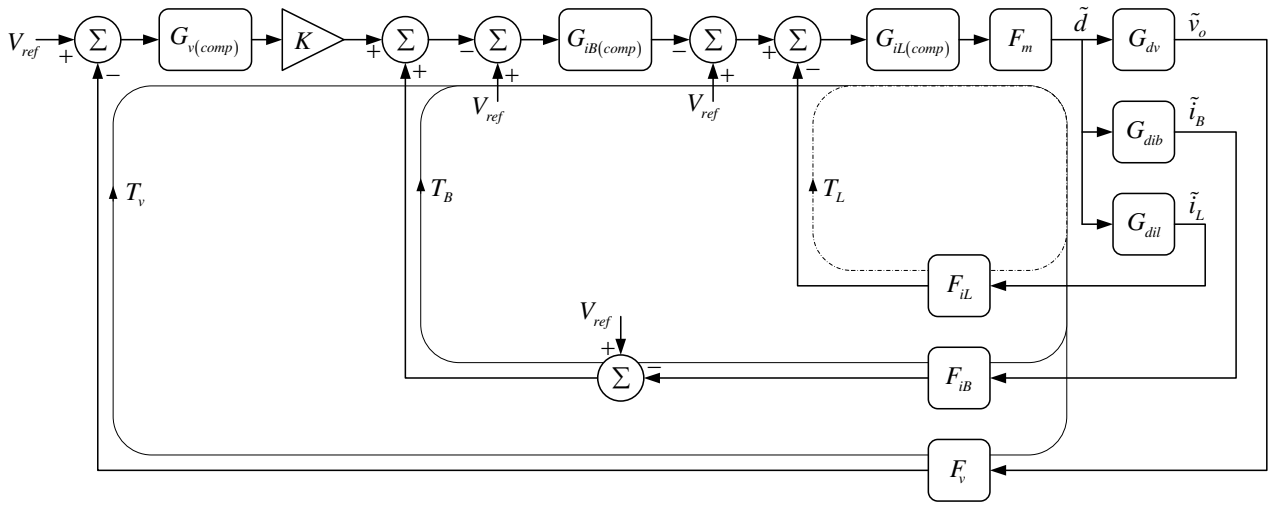


Figure 4-7 Block diagram of three loop control scheme

G_{dv}, G_{dib} and G_{dil} are the power stage transfer functions and represent the duty cycle to output voltage, duty cycle to battery current and duty cycle to inductor current respectively. F_m represents the PWM transfer function while F_v, F_{iB} and F_{iL} represent the output voltage measurement, battery current measurement and inductor current measurement respectively. $G_{v(comp)}$, $G_{iB(comp)}$ and $G_{iL(comp)}$ represent the compensation networks added to each control loop. K is a constant and is equal to the ratio R_1/R_2 (see Figure 4-6).

Each of the transfer functions will now be calculated in order to find the open loop gains of all three the control loops. The open loop gains will be used to help in designing the compensation networks for each loop.

4.3.1 LINNEARISATION OF THE POWER STAGE OF THE FULL-BRIDGE CONVERTER TOPOLOGY

The full-bridge converter topology is derived from the simple buck converter topology. To derive a linear model for the buck converter power stage the circuit (Figure 4-8) must first be averaged by combining the open and closed conditions of the power switch [5 (pp 332-337), 29]. The relationship between these two switch conditions is the duty cycle of the switch and its effect is accounted for through the use of a hypothetical DC-DC transformer. The output voltage can now be expressed as the product of the input voltage and the duty cycle $\left(V_o = dV_i\right)$. The input current can be expressed as the duty cycle times the output (inductor) current $\left(I_i = dI_o\right)$. The turn ratio of the hypothetical DC-DC transformer is equal to the duty cycle. The system is now continuous but is nonlinear because the duty cycle is not constant. The circuit is linearised by defining small signal parameters based on a large signal operating point. The process is well documented in [5 (pp 332-

337)] and will not be repeated here. Figure 4-8 shows the circuit diagram of the averaging and linnearisation processes.

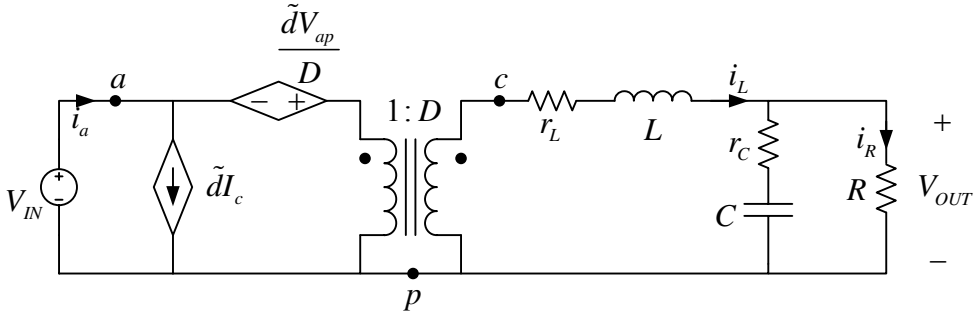


Figure 4-8 Averaging and linnearisation circuit for buck converter

4.3.2 DUTY CYCLE TO OUTPUT VOLTAGE TRANSFER FUNCTION $G_{dv}(s)$

Using the linearised model presented in the previous section, the duty cycle $\tilde{d}(s)$ to output voltage $\tilde{v}_o(s)$ transfer function may be calculated. The input voltage, shown in Figure 4-8, is multiplied by the winding ratio of the coaxially wound transformer implemented in the full-bridge topology. The filter components are the same as in Figure 4-8 with the addition of the battery, which will be modelled as a constant voltage source in series with a resistor. Figure 4-9 shows the new arrangement with the impedances transformed to the s-domain. Note that the constant voltage source in the battery model is shorted in the dynamic analysis.

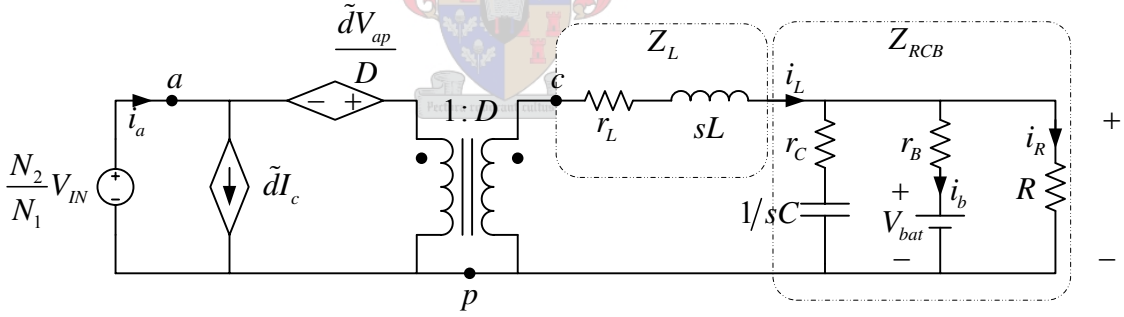


Figure 4-9 Linearised full-bridge converter with filter components

For the circuit in Figure 4-9 the following impedances are defined:

- Z_L, the impedance of the filter inductor with its DC resistance r_L
- Z_{RCB}, the impedance of the parallel combination of the filter capacitor with its ESR (represented by r_C), the batteries' series resistance r_B and the load resistance R.
- Z_{RC}, the same impedance as Z_{RCB} but excluding the series resistance of the batteries.

Using the voltage dividing rule it is found that

$$\frac{\tilde{v}_o(s)}{\tilde{v}_{cp}(s)} = \frac{Z_{RCB}}{Z_{RCB} + Z_L} \tag{E4-3}$$

Note that R is the parallel combination of the batteries' series resistance and the load resistance, r_C is the equivalent series resistance of the filter capacitor and r_L is the DC resistance of the inductor. Using Figure 4-9 and summing the voltages on the primary side of the DC-DC transformer it is found that

$$-\frac{V_{ap}}{D}\tilde{d} + \frac{\tilde{v}_{cp}}{D} = 0 \quad or \quad \tilde{v}_{cp} = \tilde{d}V_{ap} \tag{E4-4}$$

But $V_{ap} = V_{IN}N_2/N_1$ and it is calculated that

$$\frac{\tilde{v}_{cp}}{\tilde{d}} = V_{IN}N_2/N_1 \tag{E4-5}$$

Multiplying (E4-3) and (E4-5) it is found that

$$\begin{aligned} G_{dv}(s) &= \frac{\tilde{v}_o(s)}{\tilde{v}_{cp}(s)} \cdot \frac{\tilde{v}_{cp}(s)}{\tilde{d}(s)} \\ &= \frac{\tilde{v}_o(s)}{\tilde{d}(s)} \\ &= \left(\frac{V_{IN}N_2}{N_1}\right)\frac{Z_{RCB}}{Z_{RCB} + Z_L} \end{aligned} \tag{E4-6}$$

4.3.3 DUTY CYCLE TO INDUCTOR CURRENT TRANSFER FUNCTION $G_{dil}(s)$

To find the duty cycle $\tilde{d}$ to inductor current $\tilde{i}_L$ transfer function Figure 4-9 is used. $\tilde{i}_L$ is given by the voltage at the secondary of the DC-DC transformer $\tilde{v}_{cp}$, minus the output voltage $\tilde{v}_o$ divided by the impedance Z_L. Thus,

$$\tilde{i}_L = \frac{\tilde{v}_{cp} - \tilde{v}_o}{Z_L} \tag{E4-7}$$

Substituting (E4-3) into (E4-7) it is found that

$$\begin{aligned} \tilde{i}_L &= \frac{\tilde{v}_{cp} - \tilde{v}_o}{Z_L} \\ &= \frac{\tilde{v}_{cp}\left(1 - Z_{RCB}/\left(Z_{RCB} + Z_L\right)\right)}{Z_L} \\ &= \frac{\tilde{v}_{cp}}{\left(Z_{RCB} + Z_L\right)} \end{aligned} \tag{E4-8}$$

By substituting (E4-5) into (E4-8) the duty cycle to inductor current transfer function is calculated.

$$G_{dil}(s)=\frac{\tilde{i}_L}{\tilde{d}}=\left(\frac{V_{IN}N_2}{N_1}\right)\frac{1}{(Z_{RCB}+Z_L)} \tag{E4-9}$$

4.3.4 DUTY CYCLE TO BATTERY CURRENT TRANSFER FUNCTION $G_{dib}(s)$

The current flowing into the battery is the inductor current minus the sum of the load current and the current flowing into the capacitor. The inductor current is given in (E4-8) and the current flowing into the capacitor and load is calculated as is simply the output voltage $\tilde{v}_o$ divided by Z_{RC}. Thus,

$$\begin{aligned}\tilde{i}_B&=\tilde{i}_L-(\tilde{i}_C+\tilde{i}_B)\\&=\left(\frac{V_{IN}N_2}{N_1}\right)\frac{\tilde{d}}{(Z_{RCB}+Z_L)}-\frac{\tilde{d}}{Z_{RC}}\left(\frac{V_{IN}N_2}{N_1}\right)\frac{Z_{RCB}}{Z_{RCB}+Z_L}\end{aligned} \tag{E4-10}$$

The duty cycle to battery current transfer function may now be derived from (E4-10).

$$\begin{aligned}\frac{\tilde{i}_B}{\tilde{d}}&=\left(\frac{V_{IN}N_2}{N_1}\right)\frac{1}{(Z_{RCB}+Z_L)}-\frac{1}{Z_{RC}}\left(\frac{V_{IN}N_2}{N_1}\right)\frac{Z_{RCB}}{Z_{RCB}+Z_L}\\&=\left(\frac{V_{IN}N_2}{N_1}\right)\frac{(Z_{RC}-Z_{RCB})}{Z_{RC}(Z_{RCB}+Z_L)}\end{aligned} \tag{E4-11}$$

4.3.5 PULSE WIDTH MODULATOR TRANSFER FUNCTION $F_m(s)$

The pulse width modulator transfer function may be thought of as how the small signal duty cycle $\tilde{d}$ will change with small perturbation in error voltage $\tilde{v}_e$. This PWM transfer function depends on the type of control being used [28]. In average current mode control the output of the current error amplifier v_{CA} is compared with a saw tooth waveform, with amplitude equal to V_s, as shown in Figure 4-10. The slope of the ramp waveform m is equal to $2V_s/T_s$.

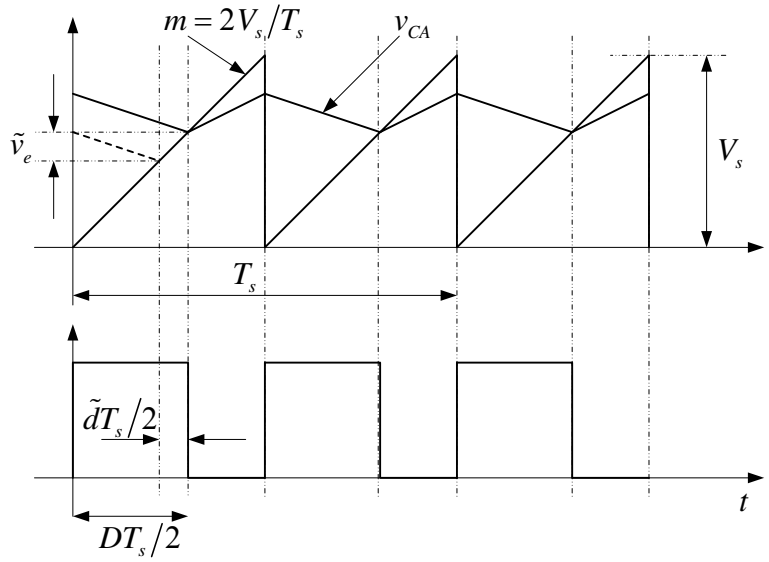


Figure 4-10 Modulator gain and duty cycle in average current mode control

Using Figure 4-10, the amplitude of a small perturbation on v_{CA} may be calculated by multiplying the change in duty cycle by the slope of the ramp waveform. It is found that

$$\begin{aligned} \tilde{v}_e &= \left(\tilde{d}T_s/2\right)\left(2V_s/T_s\right) = \tilde{d}V_s \\ \Rightarrow F_m(s) &= \frac{\tilde{d}}{\tilde{v}_e} = \frac{1}{V_s} \end{aligned} \tag{E4-12}$$

This formula for calculating the gain of the PWM is valid if the amplitude of the current amplifier waveform is small in comparison with the ramp waveform. If the gain of the current error amplifier is high, a similar amplitude perturbation in inductor current as shown in Figure 4-10 would result in a much smaller change in duty cycle. This is clearly illustrated in Figure 4-11.

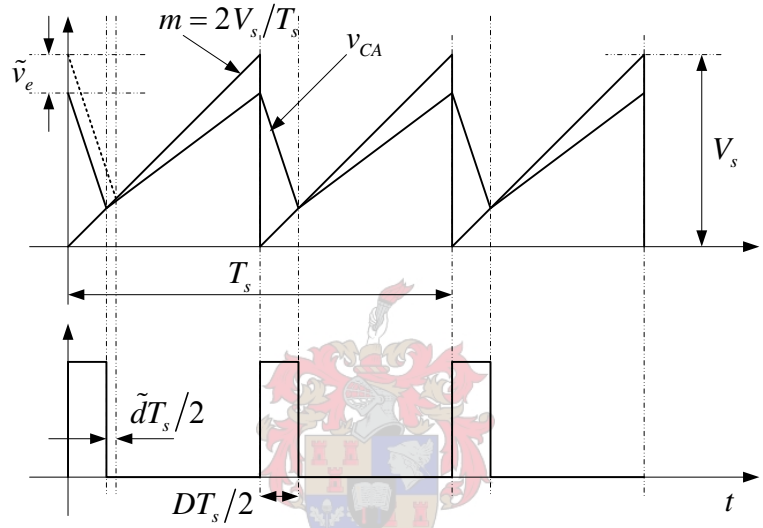


Figure 4-11 Modulator gain and duty cycle in average current mode control with large CA gain

By inspection, it can be seen that the PWM gain is a function of the duty cycle and (E4-12) becomes

$$F_m(s) = \frac{D}{V_s} \tag{E4-13}$$

4.3.6 CURRENT MEASUREMENT TRANSFER FUNCTION

The inductor and battery current will be measured using current transformer (1:1000 winding ratio) and a current sense resistor R_s which will convert the sensed current $\tilde{i}$ into a voltage $\tilde{v}$. This voltage representation of the current is the fed to the control circuitry. The transfer function conversion is given by

$$\frac{\tilde{v}}{\tilde{i}} = \frac{R_s}{1000} \tag{E4-14}$$

4.4 COMPENSATION DESIGN

When designing a compensator for each of the control loops in the converter system, the following should be kept in mind:

- The crossover frequency of the inner control loop (inductor current loop) should be the highest of the three loops to maintain the advantages of current mode control.
- The crossover frequency of the outer control loop (battery voltage loop) should be kept low to avoid interference with the other control loops. This may be done because changes in the battery voltage will be slow and a fast response to these changes in battery voltage is not required.
- The crossover frequency of the battery current control loop is set between the crossover frequencies of the outer control loop and the inner control current loop to allow a relatively fast response to changes in battery current, without interfering with the inner control loop.

4.4.1 INDUCTOR CURRENT CONTROL LOOP

From Figure 4-7 the inductor current control loop is obtained and is shown in Figure 4-12. To design a compensation network for this loop, the open loop gain is calculated. Bode plots of the open loop gain are then drawn for light load and full load cases, using MATLAB. Note that a light load condition occurs when the inductor current is on the boundary between being continuous and discontinuous [5 (pp 332-337)]. A full load condition occurs when the inductor current is equal to the maximum rated output current of a modul. These bode plots are then analysed to determine the crossover frequency and phase margin of the control loop for these two cases. Compensation is then added accordingly.

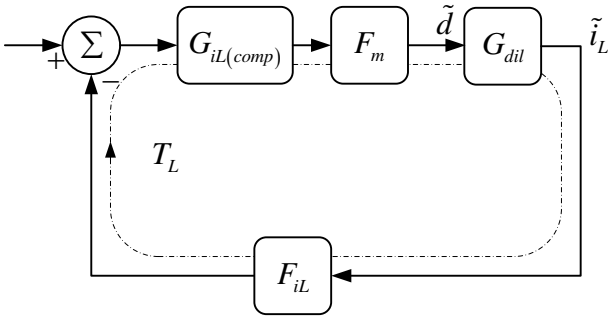


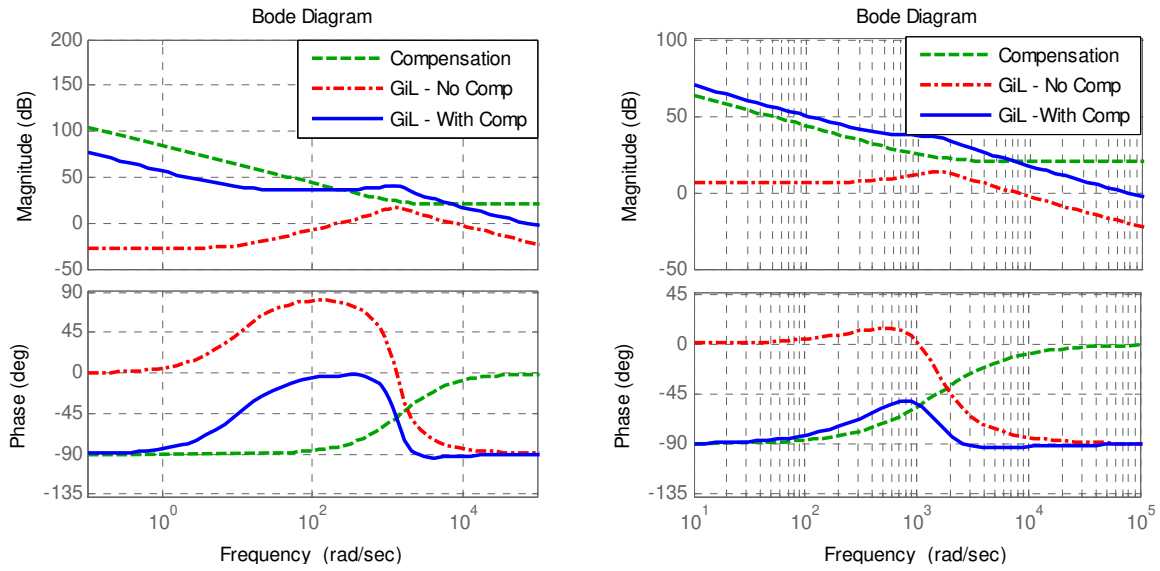
Figure 4-12 Inductor current control loop

The open loop gain of the inductor current loop $G_{iL(OL)}$ is given by

$$G_{iL(OL)} = F_m \times G_{dil} \times F_{iL} \qquad \text{(E4-15)}$$

Bode plots of $G_{iL(OL)}$ are shown in Figure 4-13 for the light load and full load cases. Because the inductor current loop is being analysed, the value of the amount of current drawn by the battery

and/or load is not required. It is only the value of inductor current that plays a part in the gain of the inner control loop.



(a) **(b)**

Figure 4-13 Bode plot of inductor current loop gain (a) Light load (b) Full load

As shown in Figure 4-13 (a), the inductor current control loop has a very small DC gain at light loads. Compensation was added to increase the DC gain of this control loop. The circuit used to implement the compensation network in the simulation and practical system is shown in Figure 4-14.

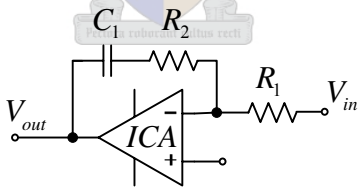


Figure 4-14 Circuit diagram of inductor current loop compensator

The transfer function $G_{iL(comp)}$ of this inductor current control loop compensator is given by

$$G_{iL(comp)} = \frac{V_{out}}{V_{in}} = \frac{(R_2C_1)s+1}{(R_1C_1)s} \qquad \text{(E4-16)}$$

By choosing the appropriate values of R_1, R_2 and C_1, it was possible to add a compensator to the inductor current control loop with a bode plot as shown in Figure 4-13. After compensation, the inner control loop has a crossover frequency of 11 kHz and a phase margin of more than 80 degrees in both the light load and full load cases (see Figure 4-13).

4.4.2 BATTERY CURRENT CONTROL LOOP

From Figure 4-7 the battery current control loop is obtained and is shown in Figure 4-15. The inductor current control loop is minimised by calculating the closed loop transfer function of the inductor current control loop and by placing this new transfer function in the battery current control loop, as on transfer function (see Figure 4-15). The closed loop gain $G_{iL(CL)}$ of the inductor current control loop is calculated by using (E4-17).

$$G_{iL(CL)} = \frac{G_{iL(OL)}}{1 + G_{iL(OL)}} \tag{E4-17}$$

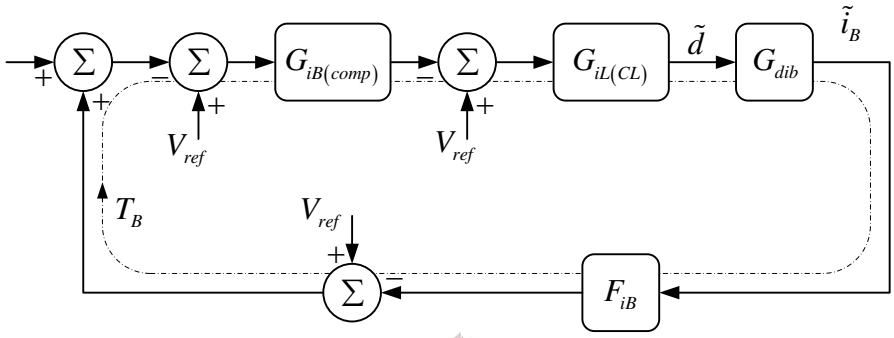


Figure 4-15 Battery current control loop

The open loop gain of the battery current control loop may now be calculated as

$$G_{iB(OL)} = F_{iB} \times G_{dib} \times G_{iL(CL)} \tag{E4-18}$$

Figure 4-16 shows four different bode plots of the open loop gains of $G_{iB(OL)}$. Each of the four bode plots represent one of the following cases:

- The converter operates at full load and the battery current is equal to the load current.
- The converter operates at full load with all the current drawn by the battery.
- The converter operates at full load with all the current drawn by the load.
- The converter operates at light load and the battery current is equal to the load current.

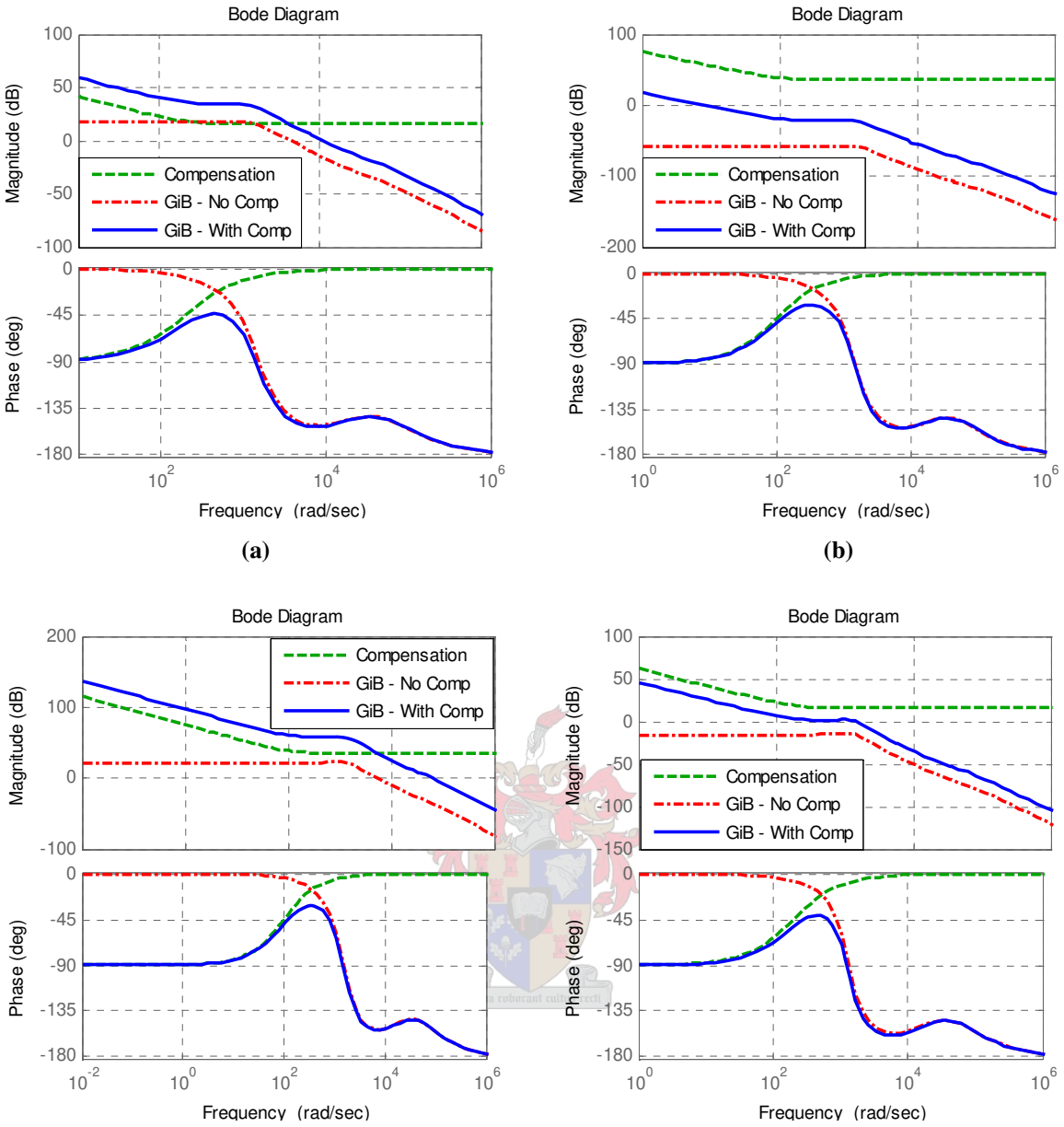


Figure 4-16 Bode plots of the battery current control loop's open loop gain
(a) Full load - Battery current = Inductor current **(b) Full load – Battery current >> Inductor current**
(c) Full load - Battery current << Inductor current **(d) Light load – Battery current = Inductor current**

It is clear from these bode plots that the uncompensated battery current control loop has a very low DC gain in all four cases and compensation is required to increase the loop gain. The phase margin is greater 30 degrees in all cases and no compensation is required to increase the phase margin. The circuit used to implement the compensator is exactly the same as the one used for the inductor current control loop (see Figure 4-16). By choosing the appropriate values of R_1, R_2 and C_1 it is possible to add a compensator to the battery current loop with a bode plot as shown in Figure 4-16.

The bode plots and the compensated battery current control loop are shown in Figure 4-16.

4.4.3 OUTPUT VOLTAGE CONTROL LOOP

From Figure 4-7 the battery voltage control loop is obtained and is shown in Figure 4-17. The battery current control loop is minimised by calculating the closed loop transfer function of the battery current control loop and placing this new transfer function in the battery current loop as one transfer function (see Figure 4-17). The closed loop gain $G_{iB(CL)}$ of the battery current control loop is calculated as in (E4-19).

$$G_{iB(CL)} = \frac{G_{iB(OL)}}{1 + G_{iB(OL)}} \tag{E4-19}$$

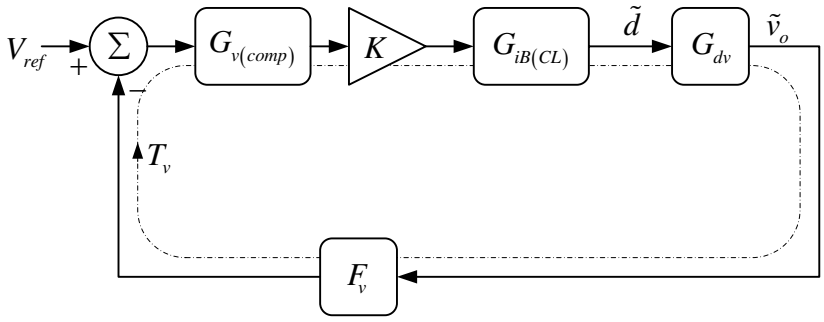
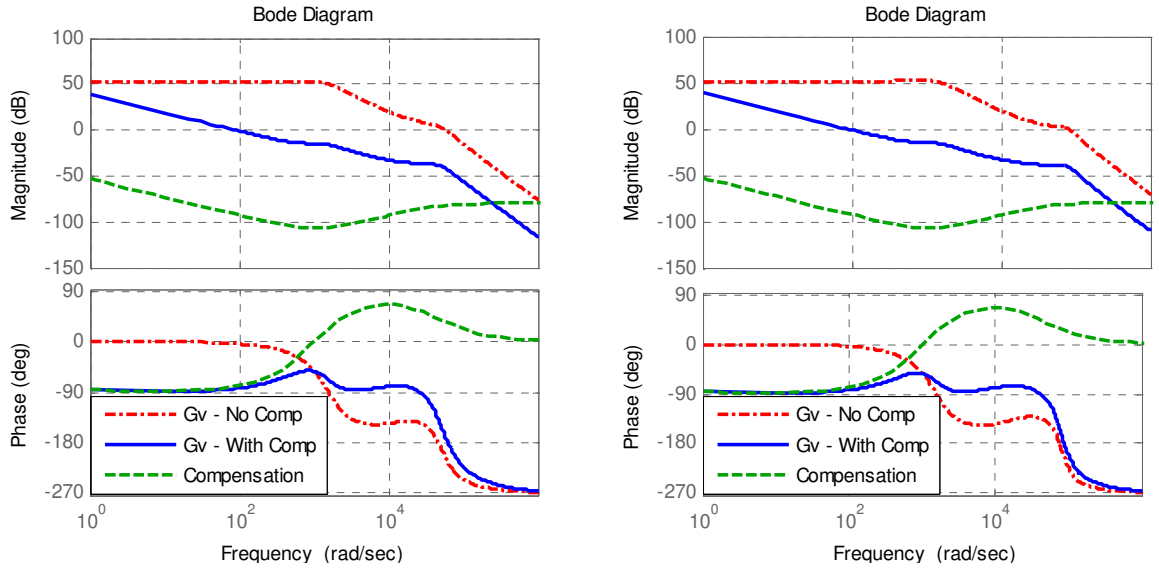


Figure 4-17 Battery voltage control loop

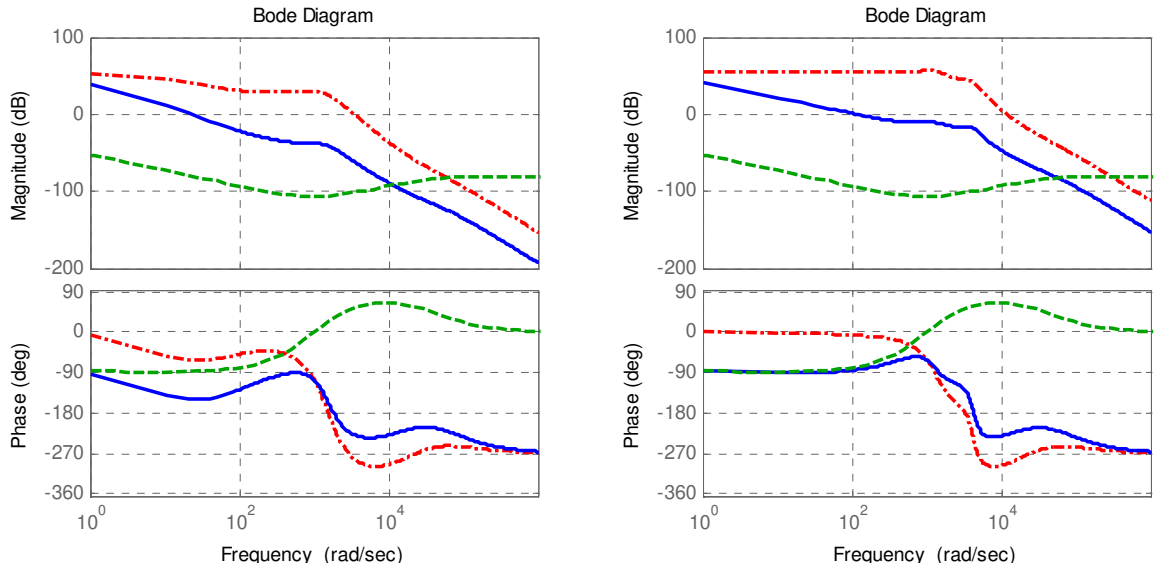
The open loop gain of the battery voltage control loop may now be calculated as

$$G_{v(OL)} = K \times F_v \times G_{dv} \times G_{iB(CL)} \tag{E4-20}$$

As for the battery current control loop, there are four bode plots that need to be analysed for loop stability. The bode plots of the open loop gain $G_{v(OL)}$ are shown Figure 4-18.



(a) **(b)**



(c) **(d)**

Figure 4-18 Bode plots of the batter voltage control loop's open loop gain
(a) Full load - Battery current = Inductor current (b) Full load – Battery current >> Inductor current
(c) Full load - Battery current << Inductor current (d) Light load – Battery current = Inductor current

It can be seen from the bode plots that the battery voltage control loop is unstable for certain loads because the phase goes below -180 degrees at the crossover frequency. A compensation network is required in all four cases to reduce the battery voltage loop gain and to ensure a phase margin of greater than 45 degrees. A lead and lag compensator was designed and implemented in the control system. The circuit diagrams of the lead and lag compensator are shown in Figure 4-19.

(a) **(b)**

Figure 4-19 Battery voltage control loop compensators (a) Lead compensator (b) Lag compensator

The transfer functions of the lead and lag compensators are given in (E4-21) and (E4-22).

$$G_{lead}(s) = \frac{V_{out}}{V_{in}} = \frac{\left(\frac{R_4}{R_3 + R_4}\right)(R_3 C_2 s + 1)}{\left(\frac{R_3 R_4 C_2}{R_3 + R_4}\right)s + 1} \quad \text{(E4-21)}$$

$$G_{lag}(s) = \frac{V_{out}}{V_{in}} = \frac{R_6 C_3 s + 1}{C_3 (R_5 + R_6) s + 1} \quad \text{(E4-22)}$$

By choosing the appropriate values for R_3, R_4, R_5, R_6, C_2 and C_3 it is possible to add a compensator to the battery current control loop with a bode plot as shown in Figure 4-18.

The bode plot of the compensated battery voltage control loop is shown in Figure 4-18.

4.5 CONTROLLER INPLEMENTATION –DIGITAL VS ANALOGUE

The commonly listed advantages and disadvantages of digital and analogue control for average current mode control are given in [33]. The main advantages and disadvantages are summarised in Table 4-1.

Table 4-1 Digital vs. Analogue control

	Advantages	Disadvantages
Digital	• Programmable • No component aging or drift • Large noise margin • More intelligent control possible	• Time consuming software • Expensive • Sampling and quantization lead to degraded performance
Analogue	• Design relatively simple • Low cost • High bandwidth	• Component aging and drift • Susceptible to noise

Analogue average current mode control is superior to its digital counterpart in terms of the two important considerations of speed and cost. To keep the total cost of the system as low as possible, it was decided to use an analogue average current mode control scheme for this application.

4.6 SIMULATION

The main aims of simulating the converter are to test if the converter's proposed controller meets the design specifications and to ensure that the converter's response to changes in line voltage and load current proves to be satisfactory. Simplorer was used for the simulations. Simplorer enables the user to use VHDL code in a simulation, which helps in the development and debugging of the VHDL code implemented in the EPLD of the controller board. The EPLD is used to generate the interleaved gate signals from the PWM controller (see chapter 5).

For a meaningful simulation of the VHDL code, a clock signal of 30MHz has to be generated, which puts an upper limit on the maximum step size of the simulation. If it is set to 10% of this clock signal, the maximum step size will be less than 4ns. If multiple converters are to be simulated, the simulation will take a very long time before any meaningful results can be obtained. For this reason, not all the simulations were done using a stack of converters. Simulating a stack (consisting of only one converter) will not change the response of the converter to line and load changes, since

only one converter's inductor current is measured in a multi-converter system. Each converter in the stack will have the maximum ratings and filter component values listed in Table 4-2

Table 4-2 Converter ratings rating and filter component values	
Power rating	$50\times10^{3}/6=8.33kW$
Input voltage	$334V<V_{IN}<650V$
Output current (inductor current)	$75A$
Output voltage (battery voltage)	$110V$
Filter capacitor	$470uF$
Filter inductor	$600uH$
Battery charge current	$20A$

Figure 4-20 shows a circuit diagram of the output of the simulated converter. The filter inductor L (with it's resistance R_L), filter capacitor (with ESR of R_C), battery bank (with ESR of R_B) and load (simulated as a resistor R_{load}) are connected as shown in Figure 4-20 and the positive current flow is indicated in Figure 4-20.

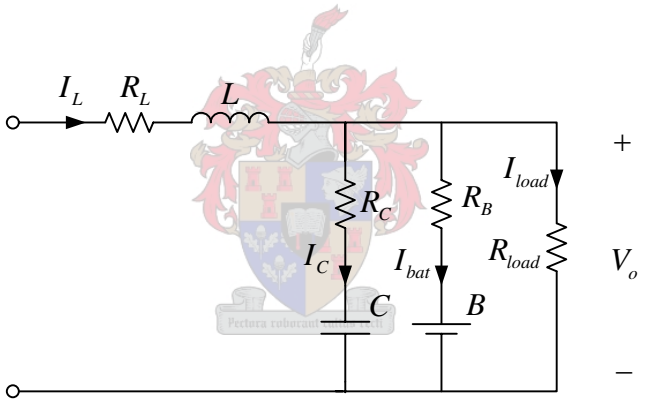


Figure 4-20 Simulated converter output with positive current flow indicated

Simulations were done for the converter operating in constant current mode (bulk charge mode) and constant voltage mode (float charge mode). For each of these two modes, line regulation and load regulation was simulated using one converter in the stack. Simulations were also done to check the converter's response to a short circuit condition and to verify that the bulk capacitors balance in a multi-converter system.

Figure 4-21 shows a tree diagram of the simulation carried out. Each of this simulation will be discussed in the following subsection.

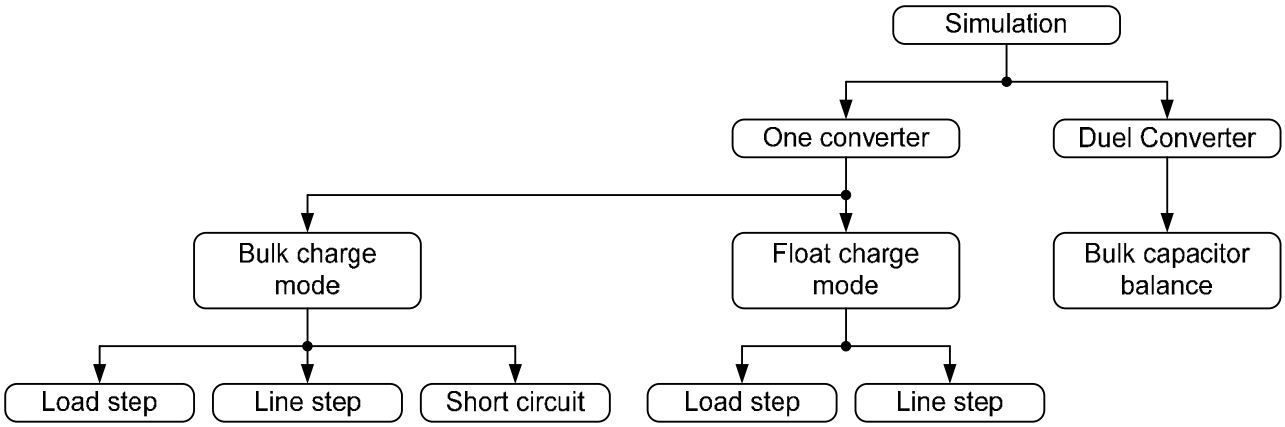
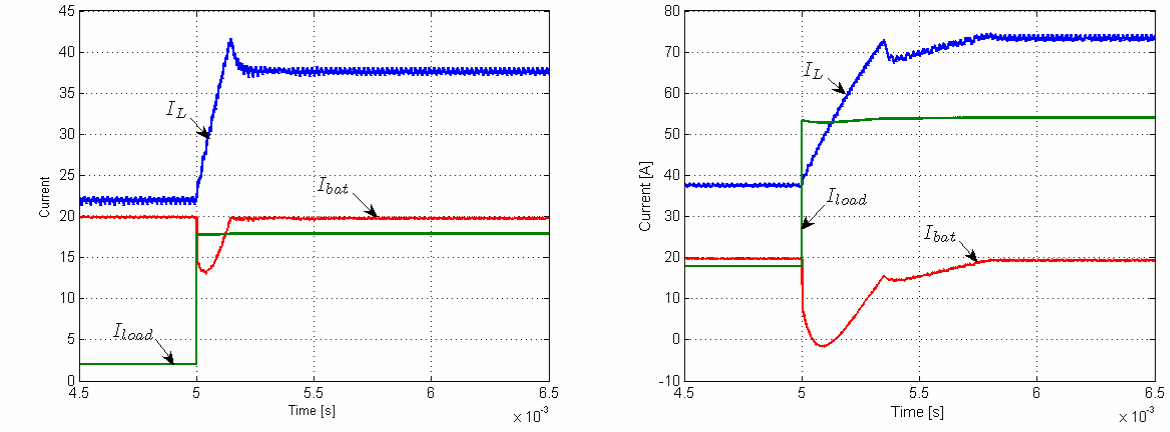


Figure 4-21 Tree diagram of simulations carried out

4.6.1 BULK CHARGE MODE

All the results given in this section are for the converter operating in bulk charge mode. The battery current is regulated at 20A.

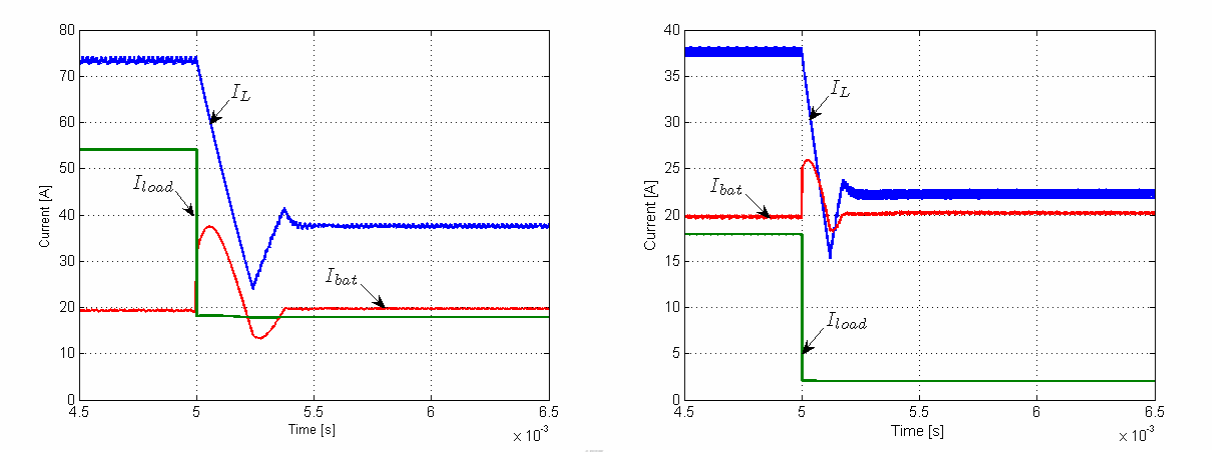
Figure 4-22 (a) shows the converter's response when a 16A (from 2A to 18A) step in load current is applied after 5ms. As expected, the battery current decreases while the controller adjusts the duty cycle to increase the inductor current. The drop in battery current is around 6A, which is exeptable for such a large step in load current. Figure 4-22 (b) shows the converter's response to a 37A (from 18A to 55A) step in load current. As expected, the battery current decreases while the controller adjusts the duty cycle to increase the inductor current. The drop in battery voltage is more than 20A, which indicates that for a short period of time the battery supplies current to the load. However, the inductor current increases until the converter is able to supply 20A to the battery and the required 55A to the load. Remember that the controller limits the inductor current to 75A. If the load requires more than 55A the battery current will start decreasing. This is illustrated in section 4.6.3 when a simulation is done to test the converter's response to a short circuit at the load.



(a) **(b)**

Figure 4-22 Inductor, battery and load current for bulk charge simulation. (a) 16A step in load current (b) 25A step in load current

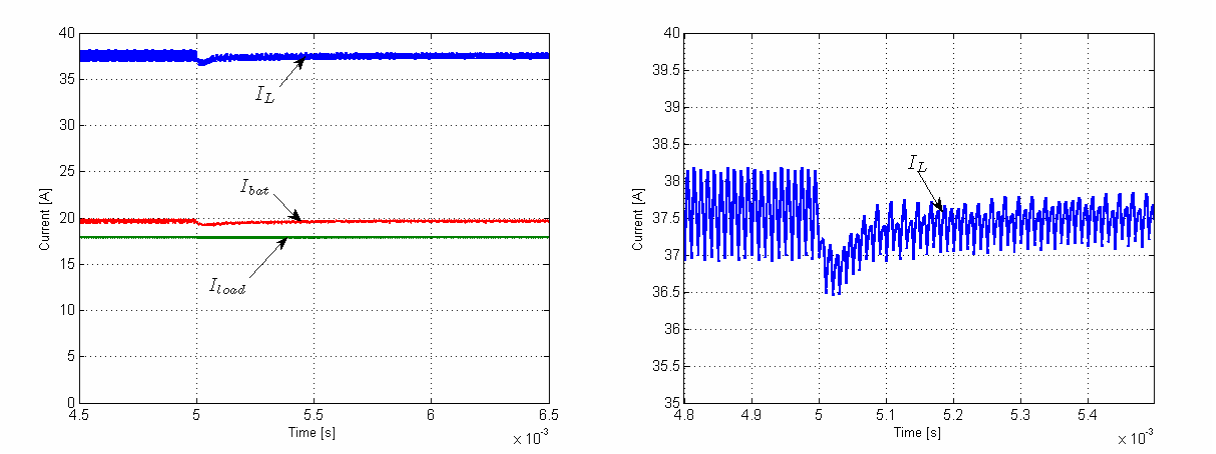
Figure 4-23 (a) shows the converter's response when a 25A (from 55A to 18A) drop in load current is applied after 5ms. As expected, the battery current increases while the controller adjusts the duty cycle to decrease the inductor current. The increase in battery current is large, almost twice the bulk charge value (20A), but the lead acid batteries should easily be able to withstand this current for a short period of time. Figure 4-23 (b) shows the converter's response when a 16A (from 18A to 2A) drop in load current is applied after 5ms. The result is similar to the previous simulation (25A drop in load voltage). The increase in battery current is smaller due to a smaller drop in load current.



(a) **(b)**

Figure 4-23 Inductor, battery and load current for bulk charge simulation. (a) 25A drop in load current (b) 16A drop in load current

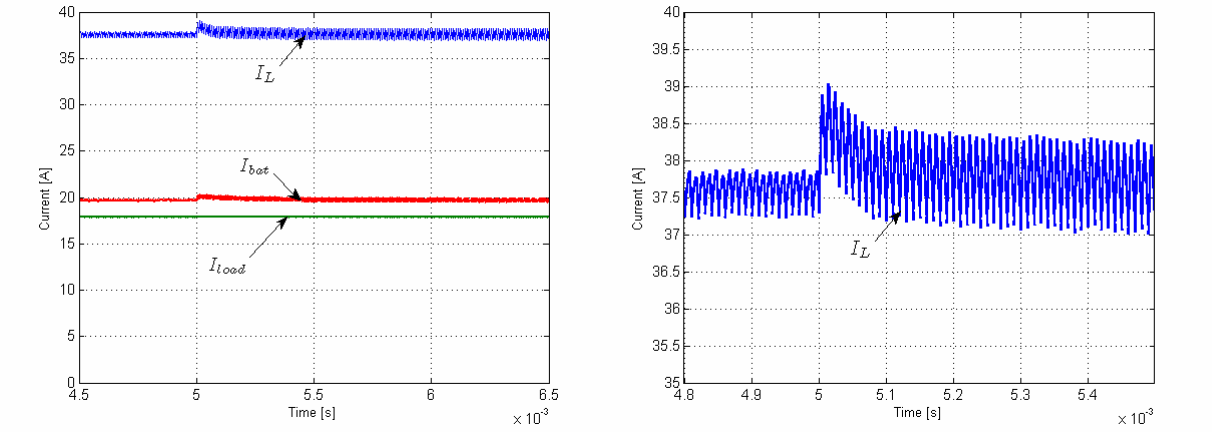
Figure 4-24 (a) and (b) show the converter's response to a drop in line voltage (from 650V to 334V). As shown in Figure 4-24 (a), a small error (deviation) in battery and load currents is visible but is quickly reduced by the controller. From the simulation results, it is clear that the line regulation of the converter is much better than the load regulation. This is because of the feed-forward property of current mode control. Figure 4-24 (b) shows a closer view of the inductor current. It can be seen that the current ripple decreases after the drop in line voltage. This is because the positive slope of the inductor current is given by $\left(NV_{IN} - V_o\right)/L$. Thus the inductor current ripple decreases when the input voltage decreases.



(a) **(b)**

Figure 4-24 Inductor, battery and load current for bulk charge simulation. (a) Drop in line voltage (b) Close-up view of inductor current during drop in line voltage

Figure 4-25 (a) and (b) show the converter's response to a step in line voltage (from 334V to 650V). Again, a small error in battery and inductor currents is visible but is quickly reduced by the controller. The inductor current ripple increases as the input voltage increases from 334V to 650V.



(a) **(b)**

Figure 4-25 Inductor, battery and load current for bulk charge simulation. (a) Step in line voltage (b) Close-up view of inductor current during step in line voltage

4.6.2 FLOAT CHARGE MODE

All the results given in this section are for the converter operating in float charge mode. The battery voltage is regulated at 110V.

Figure 4-26 (a), (b) and Figure 4-27 show the converter's response to a 18A drop in load current after 60ms. Figure 4-26 (a) shows the inductor, load and battery currents (I_L, I_{load} and I_{bat} respectively) and Figure 4-27 shows the battery voltage (V_{bat}). Two observations are made from this simulation. Firstly, the response time of the battery voltage is a lot slower in the float charge simulation than in the bulk charge simulation. This is to be expected since the battery voltage loop

is designed to be slower than the battery current loop. Secondly, there is an "initial response" visible on the waveforms under discussion. This "initial response" is better visible in Figure 4-26 (b), which is a magnification of Figure 4-26 (a). The "initial response" arises from the fact that during a load step, the battery draws or supplies (depending on a load step or load drop) current to the load. This current flowing in or out of the battery is picked up by the current sensor measuring the current flowing in or out of the battery. The battery current loop, which is a lot faster than the battery voltage loop, responds to this measured change in battery current. It is this response that is visible on the waveforms shown in Figure 4-26 (a), (b) and (c). The "initial response" is visible on all the load step simulations for the converter operating in float charge mode.

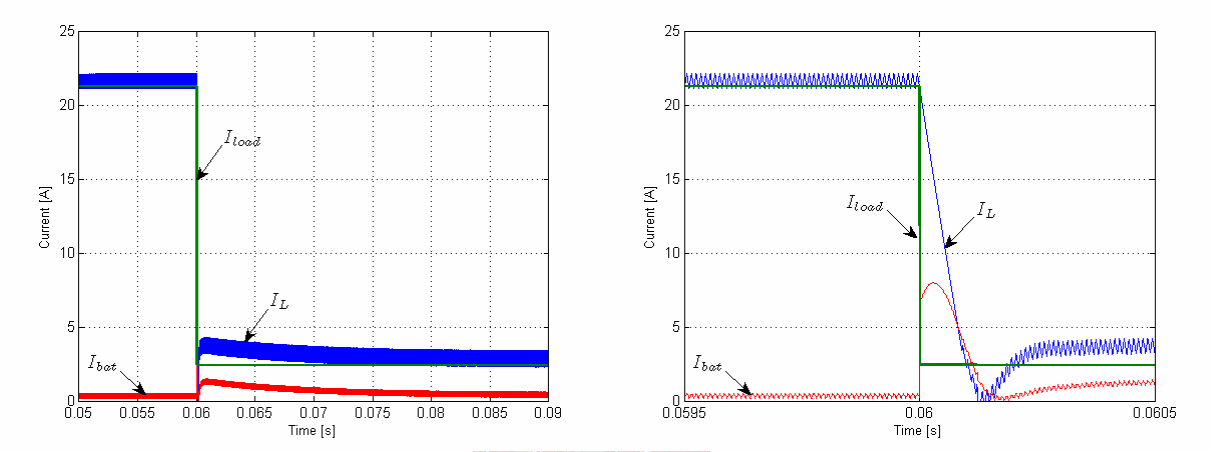


Figure 4-26 Inductor, battery and load current for float charge simulation. (a) 20A drop in load current (b) Close-up view of 20A drop in load current

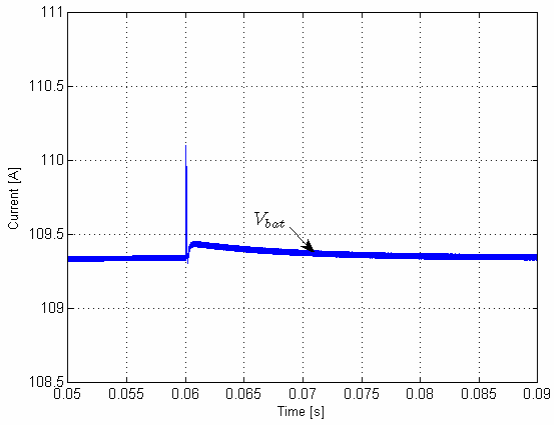


Figure 4-27 Battery voltage for float charge simulation. – 20A drop in load current

Figure 4-28 (a) and (b) show the converter's response to a 30A drop in load current, applied after 60ms.

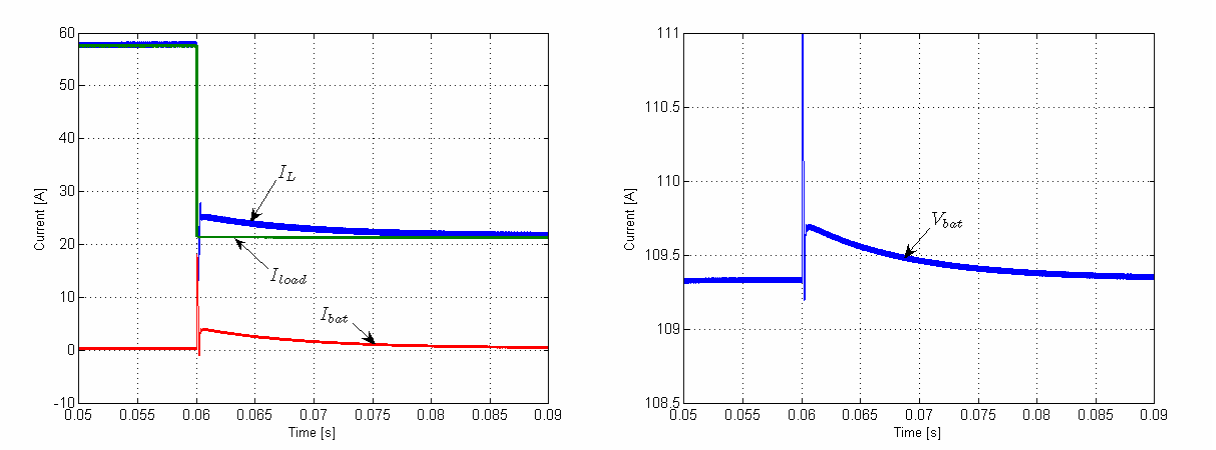
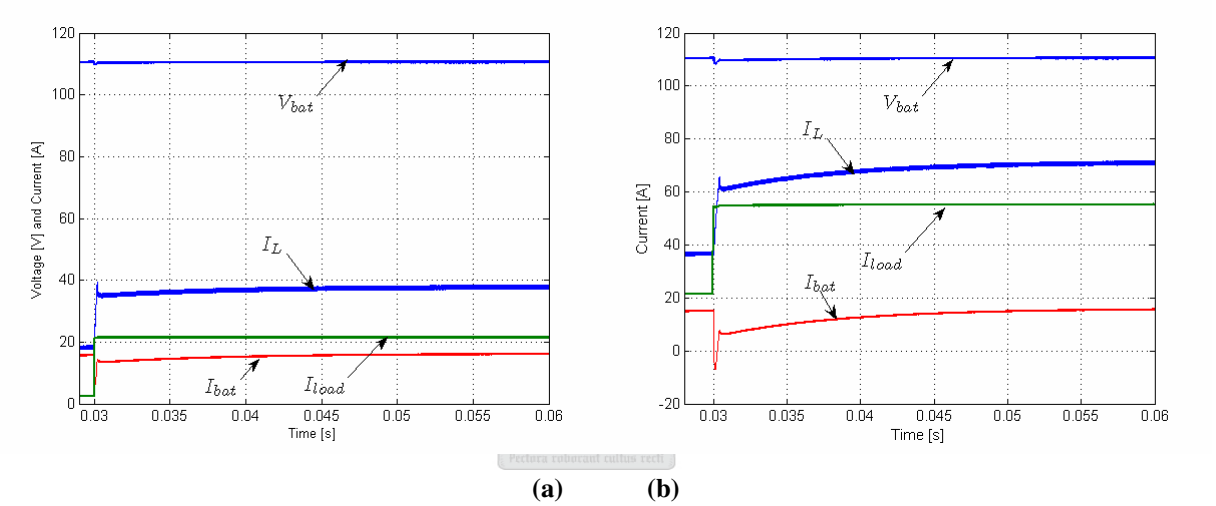


Figure 4-28 Inductor, battery and load current for float charge simulation. - 30A drop in load current

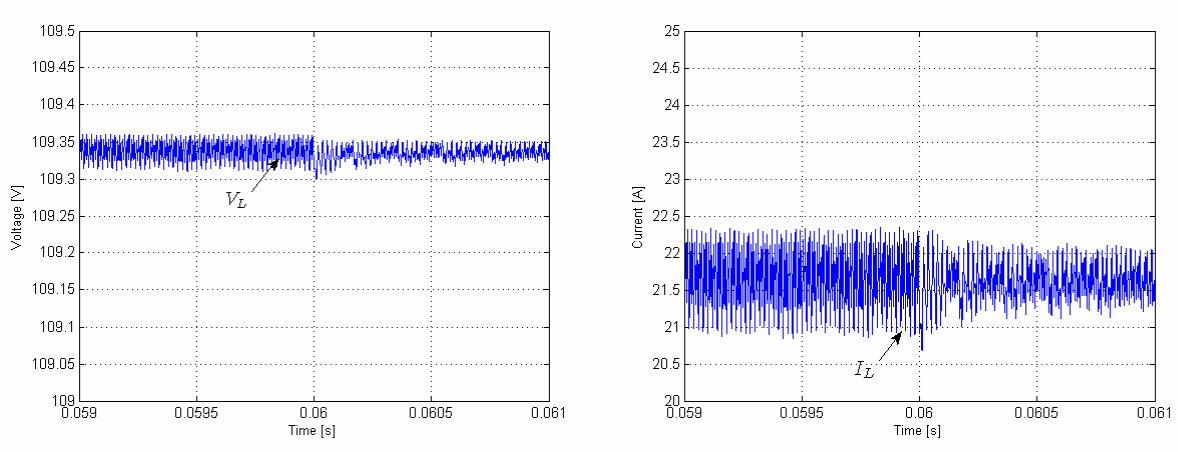
Figure 4-29 (a) and Figure 4-29 (b) show the converter's response to a 20A and a 30A step in load current respectively, which was applied after 30ms.



(a) **(b)**

Figure 4-29 Inductor, battery and load current for float charge simulation

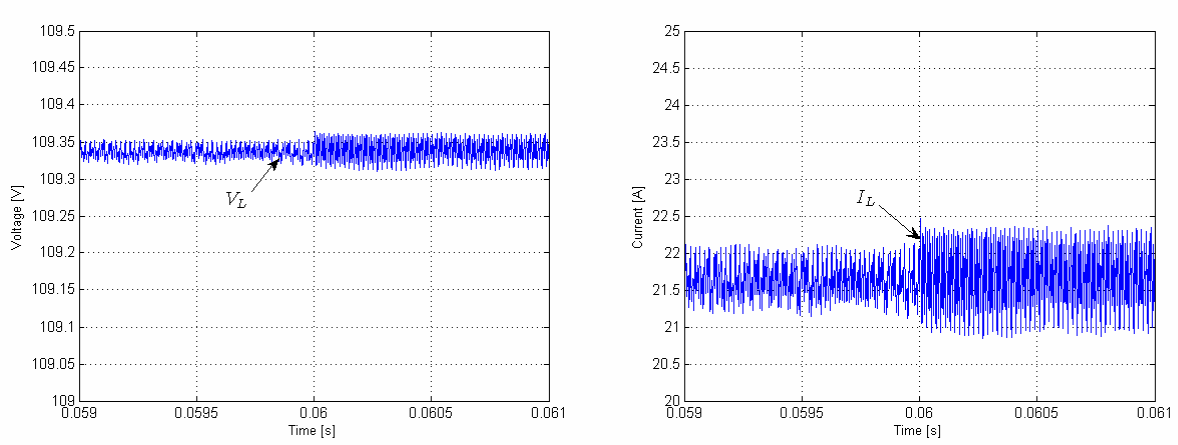
Figure 4-30 (a) and (b) shows the converter's response to a drop in line voltage (from 650V to 334V), applied after 60ms. Figure 4-30 (a) shows the output voltage of the converter and Figure 4-30 (b) shows the inductor current. A deviation in output voltage and inductor current is barely visible. Again, this can be related to the excellent line regulation property of current mode control.



(a) **(b)**

Figure 4-30 Converter's response to drop in line voltage (a) Battery voltage response (b) Inductor current response

Figure 4-31 (a) and (b) show the converter's response to a step in line voltage (from 334V to 650V), applied after 60ms. Figure 4-31 (a) shows the output voltage of the converter and Figure 4-31 (b) shows the inductor current. The results are exactly the same as for the previous simulation where a drop in line voltage was applied to the converter. The only difference is that the ripples on the output voltage and inductor current increase instead of decrease because the input voltage increases.



(a) **(b)**

Figure 4-31 Converter's response to drop in line voltage (a) Battery voltage response (b) Inductor current response

4.6.3 SHORT CIRCUIT SIMULATION

A short circuit simulation was done to ensure that the inductor current does not become too large during this situation. For this simulation the load was shorted after 5ms. Figure 4-32 shows the inductor current response to the shorted load. The current should be limited to 75A to stay within the design constraints. It can be seen that the inductor current has some overshoot and reaches a peak value of 90A. The inductor current response is relatively fast and will not cause damage to the passive components (such as the inductor, transformer and copper cables). The main concern is that the semiconductor devices (MOSFETs and rectifying diodes) will not be able to

withstand the current pulse. According to the datasheet of the rectifying diodes, 3 paralleled diodes will be able to withstand a pulse current of 36 x 3 = 108A for 10ms. The over current condition lasts around 1ms and the maximum current during this period is 90A. Thus, according to the datasheet, the diodes will be able to withstand the over current condition. Similarly, it can be shown from the MOSFET datasheet that over current condition will also not damage the MOSFETs.

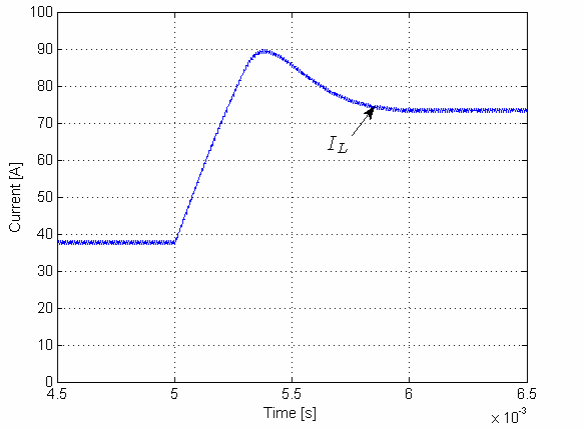


Figure 4-32 Inductor current response to short circuit at the load

Note that when a short circuit occurs at the load, the inductor current is limited by the controller. There is no limit to the battery current, which will be a large negative current, and this negative current will not be picked up by the controller. It is advisable to place a DC-breaker in the current path from the battery to the load to break this large current and protect the battery bank.

4.6.4 MULTIPLE CONVERTER SIMULATION

The multiple converter simulation was done to ensure that the bulk capacitors in a multi-converter system balance and that the output current is shared among the converters. The multiple converter simulation is also used to ensure that the VHDL code, used to generate the interleaved gate signals, functions correctly. A stack of only two converters was simulated to shorten simulation time. In this simulation the input voltage was dropped from 1200V to 700V after 25ms. The bulk capacitors' values are 10uF.

Figure 4-33 shows the bulk capacitors' voltages $(V_{C1}$ and $V_{C2})$. Focusing on the part of Figure 4-33 before the drop in line voltage (< 25ms), it can be seen that the capacitors balance, but the voltages across the two capacitors are not equal $(V_{C1} \approx 620\text{V}$ and $V_{C2} \approx 580V)$. If the capacitors were perfectly balanced, a voltage of 600V (1200/2) would have been measured across each capacitor. Capacitor C_1 is thus over-charged by 3.34%. If it is assumed that the percentage of overcharge during steady state operation remains the same for all input voltages, it is concluded that the MOSFETs' maximum voltage ratings of 800V will not be exceeded. However, it might be possible

that the voltage across a capacitor exceeds 800V during a large step/drop in load current or a large step/drop in line voltage. A Schmitt trigger was implemented in each converter in the stack to eliminate the possibility of a switch over-voltage.

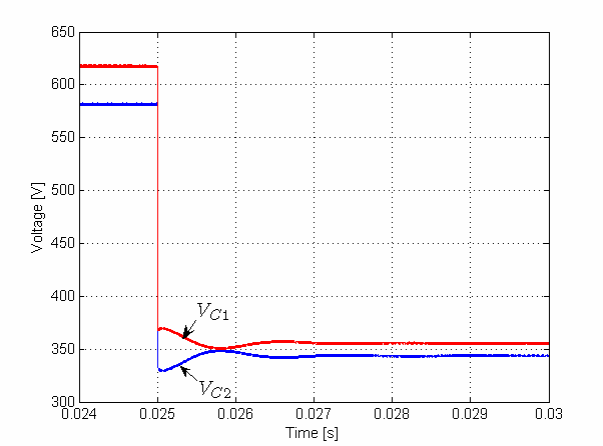
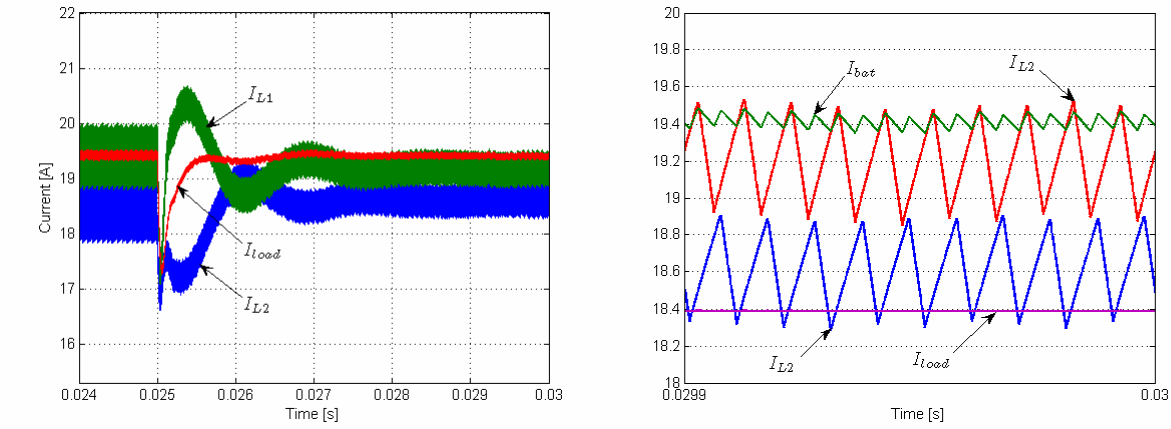


Figure 4-33 Capacitor voltages for a drop in line voltage during a dual-converter simulation

Figure 4-33 also shows that the capacitors' voltages balance after the voltage drop occurred (> 25ms). It takes around 4ms for the capacitors' voltages to completely return to their balanced state. The time it takes for the capacitors to return to their balanced state is determined by their value of capacitance. If large bulk capacitors are used it will take longer for the capacitors to return to a balanced state after a load/line step/drop. Figure 4-34 (a) shows the inductor current of the two converters as well as the battery current. These waveforms correspond to the bulk capacitors' voltages shown in Figure 4-33.



(a) **(b)**

Figure 4-34 Inductor currents, load current and battery currents for a drop in line voltage during a dual-converter simulation. (a) Normal view (b) Close-up view

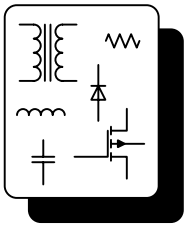
Figure 4-33 (b) shows a close-up view of the two inductors' currents, the load current and the battery current. From Figure 4-33 it is observed that the effect of the interleaved switching on the battery current. The amplitude of the ripple on the battery current is a lot smaller than the amplitude

of the ripple on the inductor current. The frequency of the ripple on the battery current is also twice the frequency of the ripple on the inductors' currents. These observations are as expected and illustrate the advantages of interleaved switching (i.e. reduced current ripple means that smaller filter inductors can be used).

The simulations performed in this chapter prove that the proposed controller provides the converter with the ability to operate in bulk charge mode and float charge mode. The converter's response is good, considering that the simulations were done for extreme cases. The simulations also show that the bulk capacitors of a multi-converter system do balance for steady state operation. Although the bulk capacitors' voltages are not exactly equal during steady state operation, it is not of major concern. Losses in a practical system, such as those caused by cable resistance, tend to boost the voltage balancing process and are not included in the simulations. Therefore, in a practical system the bulk capacitors will reach a balanced state more quickly and the voltages across then will be even closer together than for the preceding simulation.

4.7 SUMMARY

In this chapter, different control schemes for DC-DC converters were discussed. A multi-loop control scheme was designed which enables the converter to operate in bulk charge mode and float charge mode, depending on the state of charge (output voltage level) of the battery bank. The converter was simulated for various line and load conditions to test the control scheme. As expected, the converter had good response to changes in line voltage and relatively slow response to changes in load current. The simulations also showed that the bulk capacitors do balance in a multi-converter system. The positive characteristics of interleaved switching were also highlighted by the simulations.



Chapter 5

HARDWARE DESIGN

5.1 INTRODUCTION

The idea behind the converter under consideration is to connect a number of full-bridge topology converters in series at their inputs and in parallel at their outputs (see Figure 5-1). The output voltage, the battery current and one of the converter's inductor current is measured and fed back to the control unit. The control unit uses average current mode control to determine the required duty cycle. Control signals are generated for one converter and this signal is interleaved (phase shifted) for the rest of the converters. The control signals are then sent to the individual converters via fibre-optic cables to provide electrical isolation between the primary and secondary side of the converter. Figure 5-1 shows an overview of the system with a clear indication of the primary and secondary sides of the converter.

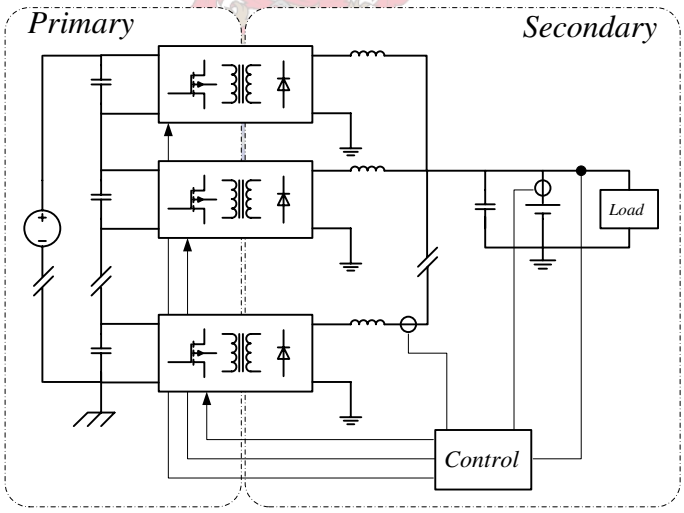


Figure 5-1 Converter overview

The aim of this chapter is to take a closer look at essential components in the converter and design them according to their specific operating condition. These components include:

- The DC bus capacitors
- The main switches and rectifying diodes
- The driver circuit for the switches
- The filter components
- The controller board circuit

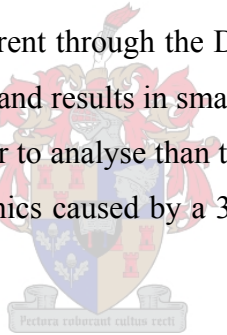
The full-bridge topology is well-known, therefore detailed circuit operation and all the circuit waveforms will not be discussed if they do not play a part in the design of essential components.

5.2 DESIGN OF THE DC-BUS CAPACITORS

One of the main concerns in designing the converter is that the rms current flowing through the DC-bus capacitors will exceed the maximum rms current rating of the capacitor. Two factors contribute to the rms current flowing through the DC-bus capacitors. The first contributor is the low frequency (300Hz) ripple on the Spoornet DC supply line. The second contributor is the high frequency (100kHz) current drawn from the capacitors in the DC-bus by the switching of the converters in the stack. These two components of the rms current through the DC-bus are separately calculated in the following two subsections.

5.2.1 DC-BUS CAPACITOR - RMS CURRENT CAUSED BY VOLTAGE RIPPLE

The DC-bus is connected to the 3kV (nominal) Spoornet railway line. This 3kV DC voltage is obtained by rectifying an ESKOM supply, using a six pulse rectifier. The rectifying process results in harmonics on the Spoornet power line that lie in the range of 300-1200Hz [1]. It is these harmonics that contribute to the rms current through the DC-bus capacitors. A six pulse rectifier is an improvement on the 3-phase rectifier and results in smaller amplitude harmonics on the Spoornet power line. The 3-phase rectifier is easier to analyse than the 6-pulse rectifier, and because a "worst case" analysis is being done, the harmonics caused by a 3-phase rectifier may be used to calculate the maximum rms current.



The output voltage V_d (rectified voltage) of a 3-phase rectifier is given in [5 (pp 103-105)] and this is the voltage across the DC-bus v_{C-bus}. It is found that

$$\begin{aligned} v_{C-bus}(t) &= V_d(t) \\ &= \sqrt{2}V_{LL}\cos(\omega t) \quad \text{for} \quad \left(-\frac{\pi}{6} < \omega t < \frac{\pi}{6}\right) \end{aligned} \tag{E5-1}$$

V_{LL} is the rms value of the line-to-line voltages and ω is the angular frequency of the line to line voltage (50Hz). The voltage waveforms are shown in Figure 5-2.

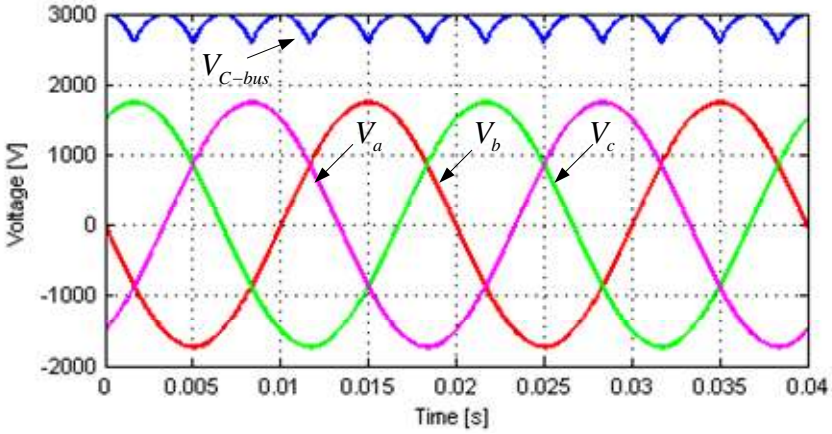


Figure 5-2 Rectified voltage of 3-phase full-bridge rectifier

The current flowing through the DC-bus i_{C-bus} capacitors is calculated by using the fact that the current through a capacitor is the derivative of the voltage with respect to time, multiplied by the capacitance. Thus,

$$\begin{aligned} i_{C-bus} &= C\frac{d}{dt}\left[v_{C-bus}(t)\right] \\ &= C\frac{d}{dt}\left[\sqrt{2}V_{LL}\cos(\omega t)\right] \\ &= -C\omega\sqrt{2}V_{LL}\sin(\omega t) \quad \text{for} \quad \left(-\frac{\pi}{6} < \omega t < \frac{\pi}{6}\right) \end{aligned} \tag{E5-2}$$

C is the total capacitance of the DC-bus. The current waveform is shown in Figure 5-3

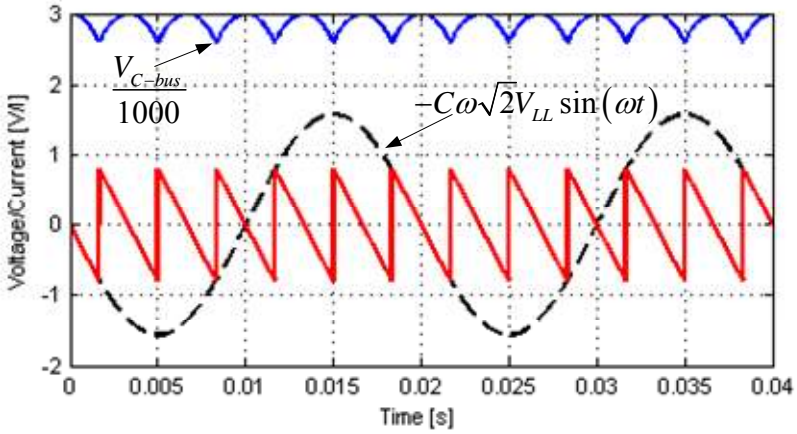


Figure 5-3 Current through DC-bus capacitors

The rms value of the current may now be calculated by using the standard equation for calculating rms values

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T \left[i(t)\right]^2 dt} \tag{E5-3}$$

Substituting (E5-2) into (E5-3) it is found that

$$
\begin{aligned}
i_{C-bus(rms)}^2 &= \frac{3}{\pi}\int_{-\pi/6}^{\pi/6}\left[-C\omega\sqrt{2}V_{LL}\sin(\omega t)\right]^2 d(\omega t) \\
&= \frac{3}{\pi}\left(C\omega\sqrt{2}V_{LL}\right)^2\left[\frac{\omega t}{2}-\frac{\sin(\omega t)\cos(\omega t)}{2}\right]_{-\pi/6\omega}^{\pi/6\omega} \\
&= \frac{3}{\pi}\left(C\omega\sqrt{2}V_{LL}\right)^2\left[\frac{\pi/6}{2}-\frac{\sin(\pi/6)\cos(\pi/6)}{2}+\frac{\pi/6}{2}-\frac{\sin(\pi/6)\cos(\pi/6)}{2}\right] \\
&= \frac{3}{\pi}\left(C\omega\sqrt{2}V_{LL}\right)^2\left[\frac{\pi}{6}-\sin(\pi/6)\cos(\pi/6)\right] \\
i_{C-bus(rms)} &= 0.4159C\omega V_{LL}
\end{aligned}
\qquad \text{(E5-4)}
$$

5.2.2 DC-BUS CAPACITOR - RMS CURRENT CAUSED BY CONVERTER SWITCHING

The current drawn from the DC-bus capacitors when the converter is switching is dependant on the type of source connected to the DC-bus. If a "stiff source" is connected to the DC-bus, implying that the inductance of the Spoornet power line is equal to zero, the rms current drawn from the DC bus capacitors will be the smallest. This is because the small or zero inductance allows high frequency current to pass through and contribute to the AC current drawn by the converters in the stack. If the line inductance is high only the DC component of current drawn by the converters in the stack is supplied by the source while the AC component is supplied by (or drawn from) the capacitors in the DC-bus.

The DC and AC components of the current drawn by each converter in the stack are shown in Figure 5-4.

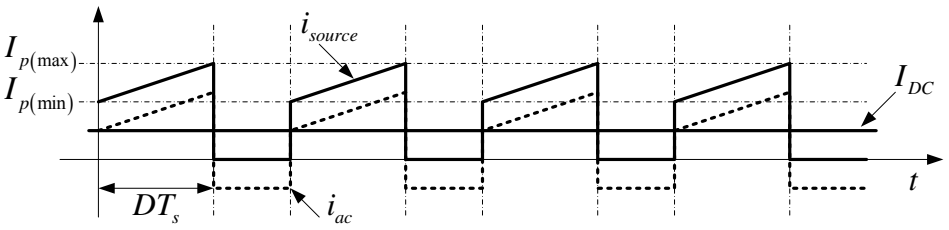


Figure 5-4 DC and AC component of current drawn by converter

The rms value of the AC component now needs to be calculated. The maximum value $\left(I_{source(\max)}\right)$ and minimum value $\left(I_{source(\min)}\right)$ of i_{source} are equal to the maximum inductor current $I_{L(\max)}$ and minimum inductor current $I_{L(\min)}$ transferred to the primary side of the transformer and are given by (E5-5), respectively.

$$I_{source(\max)} = \frac{N_2}{N_1} I_{L(\max)} \text{ and } I_{source(\min)} = \frac{N_2}{N_1} I_{L(\min)} \tag{E5-5}$$

N_2/N_1 represents the transformer winding ratio. Starting by calculating the DC component of i_{source}, it is found that

$$\begin{aligned} I_{DC} = I_{ave} &= \frac{1}{T}\int_0^T i_{source}(t)\, dt \\ &= 0.5(DT_s)\left(I_{source(\max)} + I_{source(\min)}\right) \end{aligned} \tag{E5-6}$$

This value of average current may be used to calculate the rms current through the bus capacitor. The equation describing the AC current $i_{ac}(t)$ through DC-bus capacitor is given by

$$\begin{aligned} i_{ac}(t) &= \begin{cases} \left(\dfrac{I_{source(\max)} - I_{source(\min)}}{DT_s}\right)t + \left(I_{source(\min)} - I_{ave}\right) & for \quad 0 < t < DT_s \\ -I_{ave} & for \quad DT_s < t < T_s/2 \end{cases} \\ &= \begin{cases} At + B & for \quad 0 < t < DT_s \\ -I_{ave} & for \quad DT_s < t < T_s/2 \end{cases} \end{aligned} \tag{E5-7}$$

Where

$$A = \left(\frac{I_{source(\max)} - I_{source(\min)}}{DT_s}\right) \text{ and } B = \left(I_{source(\min)} - I_{ave}\right).$$

Substituting (E5-7) into (E5-3), the square of the rms current is calculated as

$$\begin{aligned} I_{rms}^2 &= \frac{2}{T_2}\int_0^{DT_s}(At+B)^2\, dt + \frac{2}{T_2}\int_{DT_s}^{T_s/2}(-I_{ave})^2 dt \\ &= \frac{2}{3}D\left(I_{source(\max)} - I_{source(\min)}\right)^2 + 2D\left(I_{source(\max)} - I_{source(\min)}\right)\left(I_{source(\min)} - I_{ave}\right) \\ &\quad + 2D\left(I_{source(\min)} - I_{ave}\right)^2 + I_{ave}{}^2(1-2D) \end{aligned}$$

This value is not dependant of the capacitance of the capacitor used in the DC-bus and is at its maximum when the duty cycle D is at its maximum value.

Having calculated the rms current through the DC-bus capacitors caused by the ripple on the Spoornet power line and the switching of the converter, the maximum total rms current through these capacitors is calculated by summing the two rms components. Both these rms components were calculated for a "worst case" situation and the total current through the DC-bus capacitors will most likely be considerable less the calculated value. Figure 5-5 shows the total calculated rms current through the DC-bus capacitors as a function of input voltage and for different load conditions. It can be seen that the maximum value of rms current occurs when the input voltage is at its minimum and load current is at its maximum.

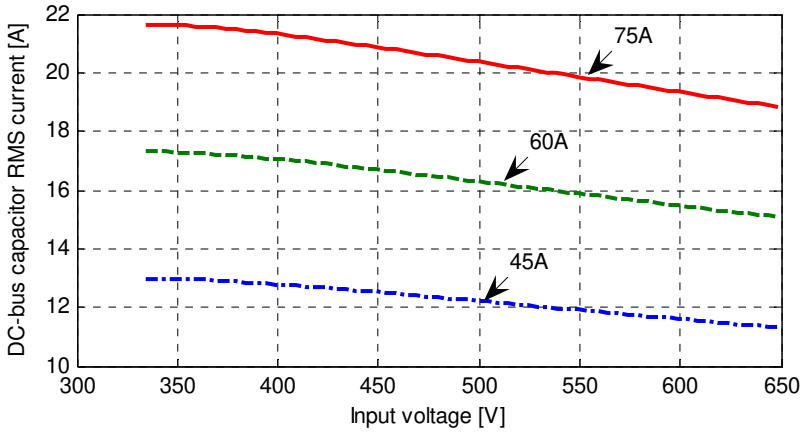


Figure 5-5 RMS current through DC-bus capacitors as a function of input voltage

The capacitors to be used for the DC-bus are those manufactured by FACON and have a maximum voltage rating of 2000V. The dissipation factor $\left(\tan(\delta)\right)$ for these capacitors is less than 2×10^{-3} at 50Hz. The maximum rms current rating is not specified on the datasheet but the maximum peak current that can by drawn from these capacitors is 470A.

5.3 FULL-BRIDGE CONVERTER OPERATION

The full-bridge converter topology is a buck-derived topology. For a buck converter, operating in continuous inductor current mode, the output voltage V_o is linearly related to the input voltage V_d by $V_o = DV_d$ where D is the duty cycle and $0 < D < 1$. For a full-bridge converter the exact relationship exists, except for the transformer winding ratio $\left(N_2/N_1\right)$ and the fact that the frequency of the rectified voltage on the secondary of the full-bridge converter is twice the switching frequency. With $0 < D < 0.5$ it is found that

$$V_o = 2\frac{N_2}{N_1}DV_d \tag{E5-8}$$

In discontinuous inductor current operation, the relationship between input and output voltage is not linear and involves the switching frequency $\left(1/T_s\right)$, filter inductance $\left(L\right)$ and output current $\left(I_o\right)$. For the buck topology the relation is given by [37]

$$V_o = \frac{V_d}{2I_oL/D^2T_sV_d + 1} \tag{E5-9}$$

For a full-bridge converter, V_d is replaced with $2V_dN_2/N_1$ (as in the continuous inductor current case) and (E5-9) becomes

$$V_o = \frac{2V_dN_2/N_1}{I_oLN_1/V_dD^2T_sN_2 + 1} \tag{E5-10}$$

Given the specified output voltage, these relationships are used to calculate the transformer winding ratio for any given duty cycle. To know what the input voltage range to each module in the stack will be, the number of modules that will be used in the converter needs to be calculated. The following factors influence the choice of the number of converters that will be used in the stack.

- A greater number of modules will result in less voltage stress on the power switches, but it will use more components in total.
- To keep the magnetisation inductance of the isolation transformer as high as possible the number of primary winding turns should be kept as high as possible. Due to the physical construction limitations of the coaxially wound transformer, i.e. either a n:1 or a 1:n winding ratio, it is only possible to increase the number of primary windings if a n:1 winding ratio is used. This implies that the input voltage to each module in the stack should be kept as high as possible, and this will result in the highest number of primary windings.

As the above factors indicate, there is a clear conflict between the least voltage stress on the power switches and the largest magnetisation inductance in the isolation transformer.

The maximum input voltage of the converter is 3.9kV. Figure 5-6 shows a plot of the maximum switch voltage per module (assuming no overshoot at switch turn-off) as a function of the number of modules in the stack.

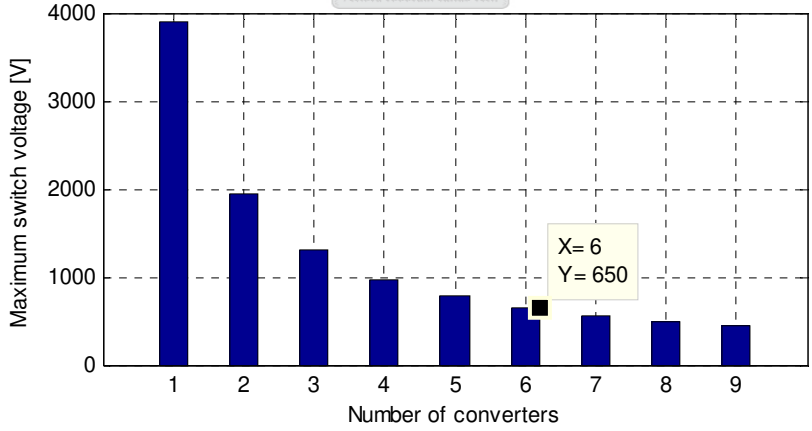


Figure 5-6 Maximum switch voltage against number of converter in stack

MOSFETs will be used as power switches. The specific MOSFET that will be used is the SPW17N80C3 (CoolMOS) from Infineon technologies. The maximum voltage rating of this MOSFET is 800V. From Figure 5-6 it can be seen that a minimum of 5 modules will have to be used in the converter to stay in the operating capabilities of this MOSFET. It was decided to use 6 modules in the stack to keep a good safety margin and allow room for overshoot at switch turn-off.

Given the maximum input voltage per module, (E5-8) may be used to calculate the transformer winding ratio and steady state duty cycle. Starting off by choosing a duty cycle of 0.25 with nominal input voltage (3kV or 500V per module), it is found that

$$\frac{N_2}{N_1} = \frac{V_o}{2DV_d} = \frac{110}{2(0.25)500} = 0.44 \quad \text{or} \quad \frac{N_1}{N_2} = 2.27$$

Rounding off a winding ratio of 2:1 is found. It was stated in chapter 3 that two primary windings would ensure a large enough magnetisation inductance to reduce magnetisation current satisfactorily. Using this duty cycle for minimum and maximum input voltages to ensure that duty cycle is in range $(0 < D < 0.5)$.

$$\frac{V_o N_1}{2V_{d(\max)} N_2} < D < \frac{V_o N_1}{2V_{d(\min)} N_2}$$

$$\frac{(110)(2)}{(2)(650)(1)} < D < \frac{(110)(2)}{(2)(333.3)(1)}$$

$$0.169 < D < 0.33$$

5.4 SWITCHING STRATEGY

Each module of the converter is switched by using the phase-shifted switching strategy discussed in [38]. Figure 5-7 shows the full-bridge converter with its four switches $(S_{A1},\ S_{A2},\ S_{B1}$ and $S_{B2})$ and free-wheeling diodes, the transformer with primary voltage (V_p) and secondary voltage (V_s), rectifying diodes $(D_{A1},\ D_{A2},\ D_{B1}$ and $D_{B2})$, filter inductor (L) and filter capacitor (C).

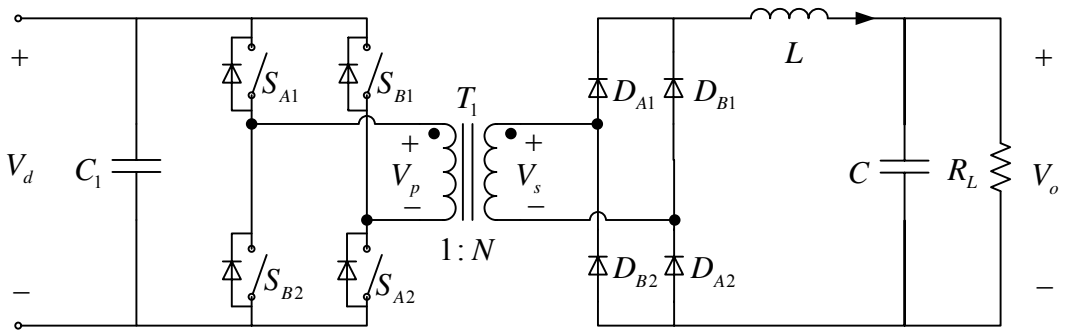


Figure 5-7 Full-bridge converter

A phase-shifted switching strategy for the full-bridge converter shown in Figure 5-7 will require gating signals as shown in Figure 5-8. Figure 5-8 also indicates the dead time inserted into the gaiting signals to allow switches to turn off properly before the next switching state commences. There are eight $(T_1$ to $T_8)$ switching states and the following sections are devoted to explain the

circuit operation during each switching state. Firstly the ideal case and then the non-ideal case will be discussed.

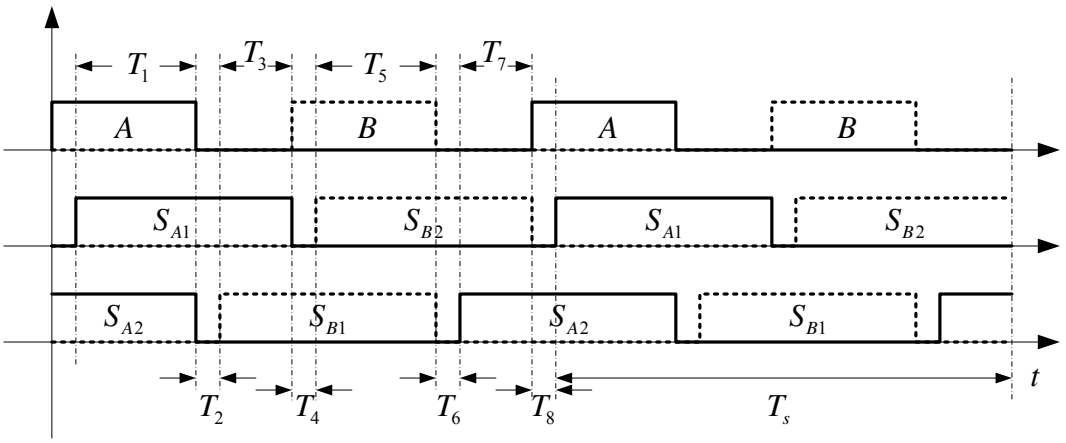


Figure 5-8 Power switch gaiting signals for one module

The voltage across the transformer primary may be one of three levels, viz. V_d, 0 and $-V_d$. Table 5-1 shows the voltage across the transformer for each valid switch combination.

Table 5-1 Full-bridge switching possibilities

S_{A1}	S_{B1}	S_{A2}	S_{B2}	V_p
On	Off	On	Off	V_d
On	On	Off	Off	0
Off	On	Off	On	$-V_d$
Off	Off	On	On	0

5.5 OPERATING STATES AND CIRCUIT WAVEFORMS – IDEAL CASE

The main reason for analysing the operating states of the converter is for constructing voltage and current waveforms for various parts of the converter. These waveforms are then used to calculate losses, rms voltages and currents, and average voltages and currents; which are used to design components' values and maximum ratings. For the ideal circuit operation the following assumptions are made:

- The converter operates in steady state and with continuous inductor current.
- There is no leakage inductance on either the primary or secondary side of the transformer.
- The magnetisation inductance of the coaxially wound transformer is large enough to eliminate magnetisation current.
- The power switches and rectifying diodes are ideal.

- The converter is connected to a stiff source.
- No dead time is present in switching signals since all the switches are ideal.

Since it was assumed that there is no dead time associated with the ideal case, there is only four switching intervals. Thus, intervals T_2, T_4, T_6 and T_8 do not form part of this analysis. Figure 5-9 shows circuit diagrams for all four converter operating states with the current paths indicated on each circuit diagram. Starting with the first switching interval (start of T_1) the converter operates as follows:

- T_1 - Switches S_{A1} and S_{A2} are closed. The voltage applied to the transformer primary is V_d. The inductor current rises with a slope equal to $\left(N_2 V_s / N_1 - V_o\right)/L$. Diodes D_{A1} and D_{A2} become forward biased and conduct the full inductor current. The inductor current transfers back to the primary side of the converter and flows through S_{A1} and S_{A2}.

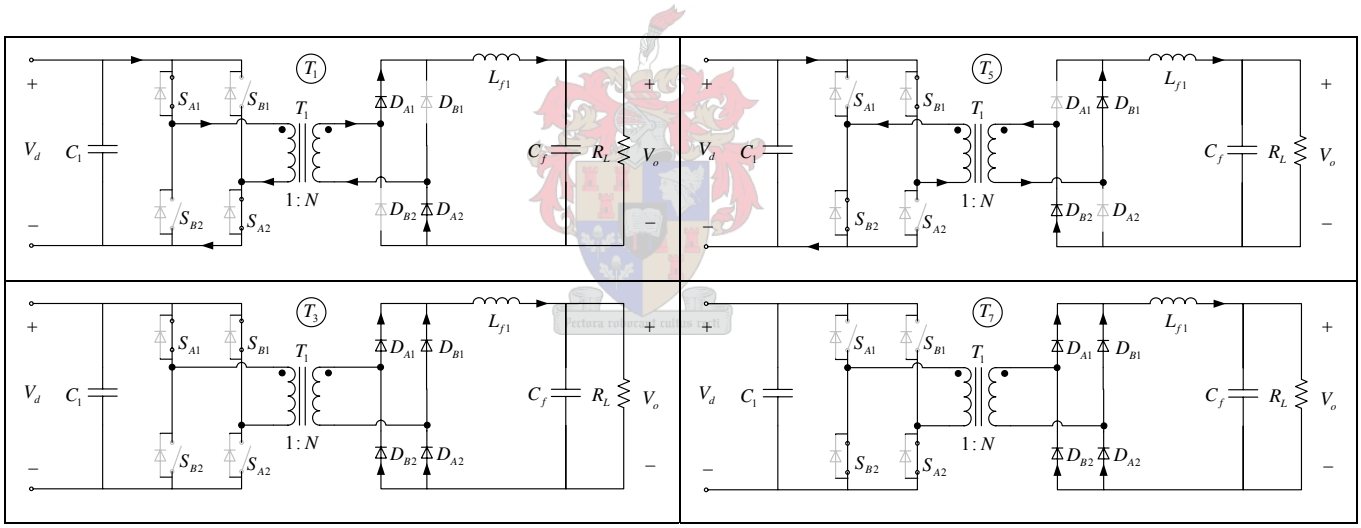


Figure 5-9 Circuit diagram of converter operating states for the ideal case

- T_3 - Switch S_{A2} is turned off and switch S_{B1} is turned on. 0V appears across the transformer primary. There is no current flowing in the transformer during this interval. The inductor current which is decreasing with a slope of V_o/L is shared equally among the rectifying diodes.
- T_5 - Switches S_{B1} and S_{B2} are closed. The voltage applied to the transformer primary is $-V_d$. The inductor current rises with the a slope equal to $\left(N_2 V_s / N_1 - V_o\right)/L$. Diodes D_{B1} and D_{B2} become forward biased and conduct the full inductor current. The inductor current transfers back to the primary side of the converter and flows through S_{B1} and S_{B2}.

- T_7 - Switch S_{B1} is turned off and switch S_{A2} is turned on. Again 0V appears across the transformer primary. There is no current flowing in the transformer during this interval. The inductor current, which is decreasing with a slope of V_o/L, is shared equally among the rectifying diodes.

The first waveforms are those of the transformer primary voltage v_p and current i_p and are shown in Figure 5-10.

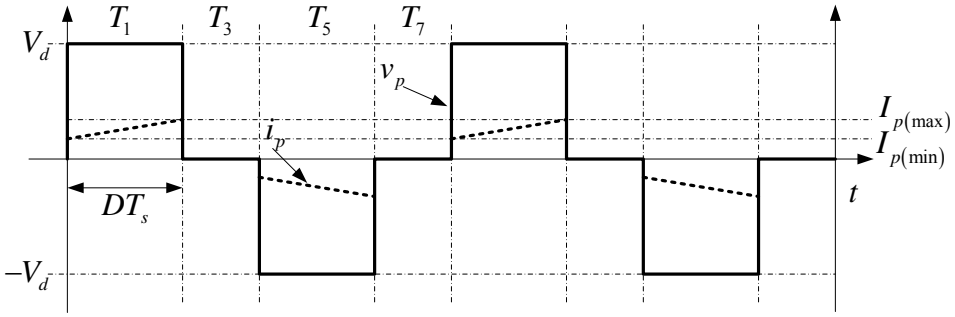


Figure 5-10 Transformer voltage and current waveforms – Ideal case

The current flowing in the transformer primary during T_1 is equal to the transferred inductor current. The minimum and maximum transformer currents, $I_{p(\max)}$ and $I_{p(\min)}$, are given by

$$I_{p(\max)} = \frac{N_2}{N_1} I_{L(\max)} \text{ and } I_{p(\min)} = \frac{N_2}{N_1} I_{L(\min)}$$

Figure 5-11 shows the voltage and current waveforms, v_{SA1} and i_{SA1}, of one of the power switches (S_{A1}). The minimum and maximum switch currents, $I_{SA1(\max)}$ and $I_{SA1(\min)}$, are given by

$$I_{SA1(\max)} = \frac{N_2}{N_1} I_{L(\max)} \text{ and } I_{SA1(\min)} = \frac{N_2}{N_1} I_{L(\min)}$$

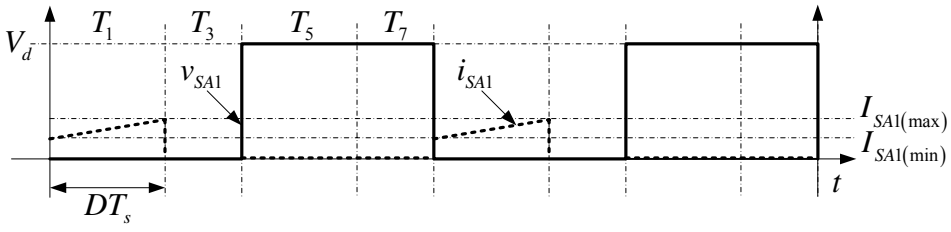


Figure 5-11 Switch voltage and current waveforms – Ideal case

Figure 5-12 shows the voltage and current waveforms, v_{DA1} and i_{DA1}, of one of the rectifying diodes (D_{A1}). The diode conducts the full inductor current during T_1 and half the inductor current during

T_3 and T_7. The diode does not conduct during T_5 and the transferred transformer primary voltage appears across the diode.

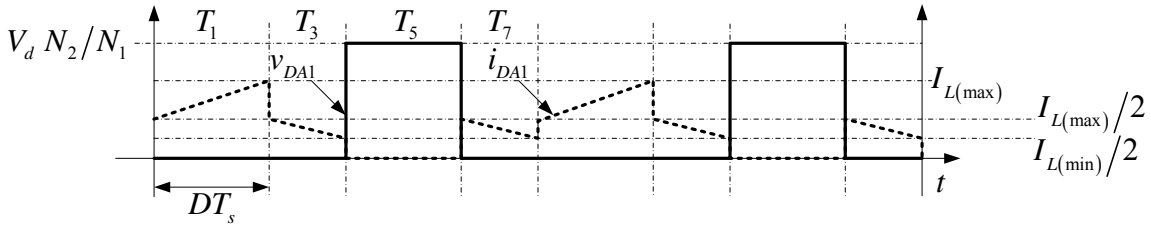


Figure 5-12 Diode voltage and current waveforms – Ideal case

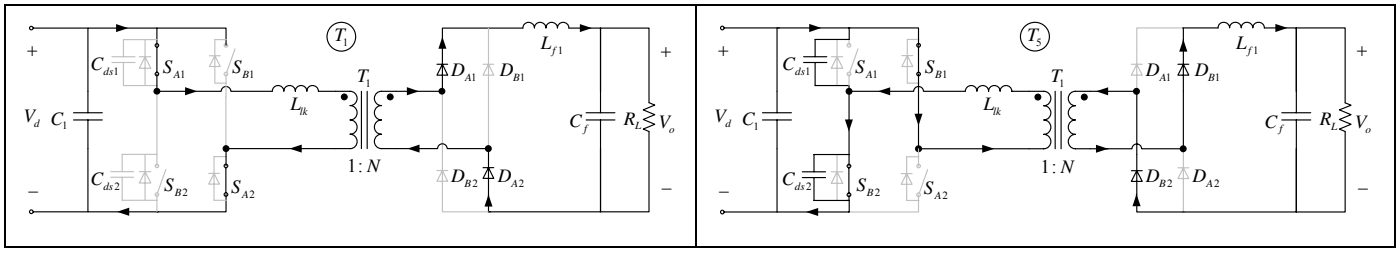
5.6 OPERATING STATES AND CIRCUIT WAVEFORMS – NON-IDEAL CASE

Before continuing with the discussion on the converter's operating states for the non-ideal case, remember that the switching strategy used for the converter and the physical configuration of the full-bridge power stage allow some switches to turn on with zero voltage across the switch. This will eliminate the switching loss of the switch at turn-on. In general, if a switch is turned on/off and there is no loss (caused by the switch) associated with the turn on/off process, the switch is turned on/off "soft". If a switch is turned on/off and there is loss (caused by the switch) associated with the process, the switch is turned on/off "hard".

For the non-ideal analysis, the same assumptions are made as in the previous section for the ideal case with the following exceptions:

- The primary side leakage inductance $L_{\Pr(leak)}$ is not zero.
- The primary side power switches used are ideal MOSFETs, with the exception of the presence of on state resistance R_{on} and drain-source capacitance C_{ds}.
- Dead time is inserted in the gating signals as shown in Figure 5-8

There are eight switching intervals in the non-ideal case. Figure 5-13 shows a circuit diagram of each interval with the current path indicated on each diagram. Starting with the first switching interval (start of T_1) the converter operates as follows:



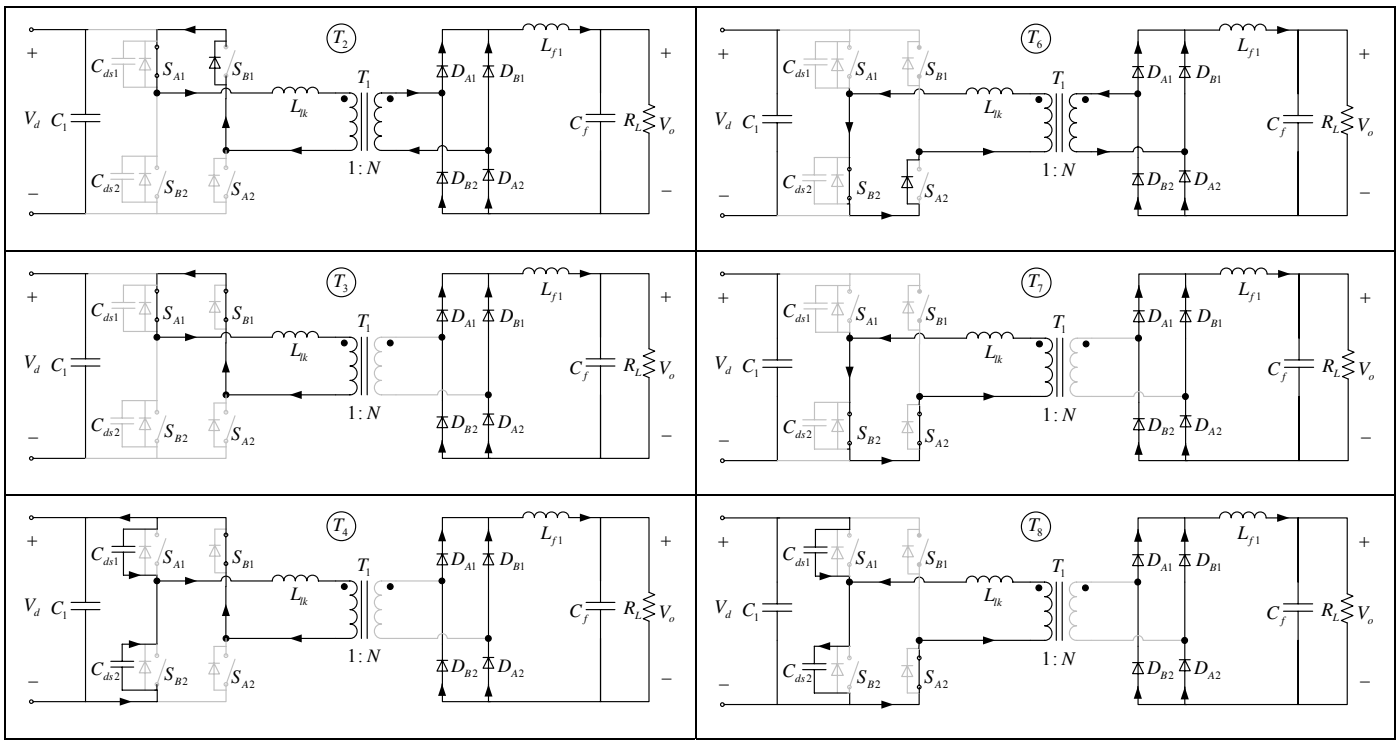


Figure 5-13 Circuit diagrams of converter operating states for the non-ideal case

- T_1 - Switches S_{A1} and S_{A2} are closed. The voltage seen by the primary of the transformer is equal to V_d. The inductor current i_L rises with a slope equal to $\left(\left(N_2/N_1\right)V_d - V_o\right)/L$. Diodes D_{A1} and D_{A2} become forward biased and conduct the full inductor current. The inductor current transfers back to the primary side of the converter as $\left(N_2/N_1\right)I_L$ and flows through S_{A1} and S_{A2}.
- T_2 - This is a dead time interval. Switch S_{A2} is turned off. D_{B1} provides a path for the primary transformer current i_{Pr}, which decreases exponentially and which is given by the following equation.

$$i_{\mathrm{Pr}}\left(t\right) = I_0 e^{-\frac{t}{\tau}} \quad \text{where} \quad \tau = \frac{L_{\mathrm{Pr}(leak)}}{R_{on}} \tag{E5-11}$$

R_{on} is the on-state resistance of S_{A1} and I_0 is the instantaneous current flowing in the primary of the transformer at the start of interval T_2. On the secondary side of the converter, the current through D_{A1} and D_{A2} starts to decrease with the transformed (transformed from primary to secondary) waveform as described by (E5-11). Concurrently the current through D_{B1} and D_{B2} starts to increase with a slope described by (E5-12)

$$i_{\mathrm{Pr}}\left(t\right) = I_0\left(1 - e^{-\frac{t}{\tau}}\right) \tag{E5-12}$$

- T_3 - Switch S_{B1} is turned on soft . The current on the primary side of the converter starts flowing back through S_{B1}, taking over the current that was flowing through the anti-parallel diode of S_{B1} during interval T_2. When this current reaches zero, the voltage across the primary side of the transformer will also be equal to zero. The voltage transferred to the secondary side of the transformer also approaches zero. Hence, the current on the secondary side of the converter divides equally among both branches of the full-bridge rectifier. All the diodes conduct half the inductor current.
- T_4 - This is a dead time interval. Switch S_{A1} is turned off. If the primary current has reached zero (determined by (E5-11)) no current will flow in the primary while on the secondary side of the transformer the inductor current is still equally divided among the rectifying diodes. If current is still circulating in the primary the drain-source capacitance of S_{A1} will start to charge and the drain-source capacitance of S_{A2} will start to discharge with half the circulating current.
- T_5 - Switch S_{B2} is turned on. The drain-source capacitance of S_{A1} will charge and the drain-source capacitance of S_{A2} will discharge more rapidly (subject to load current) since current is again actively transferred to the secondary. The voltage across S_{B2} decreases with a slope determined by the size of the drain-source capacitance. Diodes D_{B1} and D_{B2} conduct the full inductor current.
- T_6 - Switch S_{B1} is turned off "hard". The anti-parallel diode of switch S_{A2} provides a path for the circulating current which is the same as described for interval T_2. On the secondary side of the converter the current through D_{B1} and D_{B2} starts to decrease with the transformed (transformed from primary to secondary) waveform as described by (E5-11). Concurrently, the current through D_{A1} and D_{A2} starts to increase with a slope described by (E5-12).

$$i_{\mathrm{Pr}}(t) = I_0\left(1 - e^{-\frac{t}{\tau}}\right) \qquad \text{(E5-13)}$$

- T_7 - Switch S_{A2} is turned on soft. The current on the primary side of the converter starts flowing back through S_{A2}, taking over the current that was flowing through the anti-parallel diode of S_{A2} during interval T_6. The current circulating in the secondary divides equally between both branches of the rectifying diode bridge as described for interval T_3.

- T_8 - Switch S_{A1} is turned off. If the primary current has reached zero (determined by (E5-11)) no current will flow in the primary while on the secondary side of the transformer the inductor current is still equally divided among the rectifying diodes. If current is still circulating in the primary, the drain-source capacitance of S_{A2} will start to charge and the drain-source capacitance of S_{A1} will start to discharge with half the circulating current.

The voltage and current waveforms in various parts of the converter are now drawn for the non-ideal case. The primary voltage and current is shown in Figure 5-14.

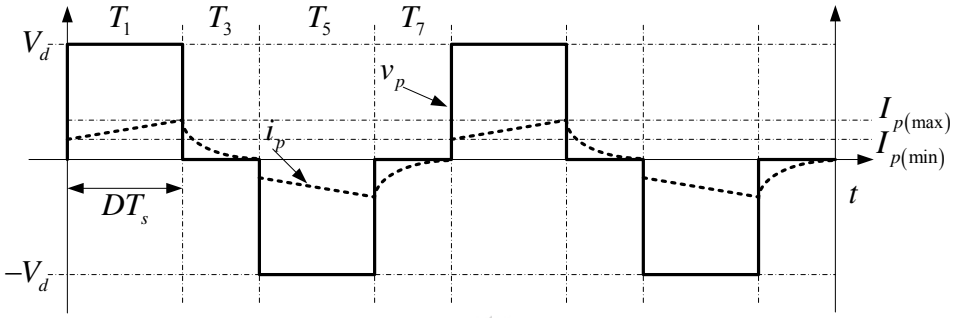


Figure 5-14 Transformer voltage and current waveforms – Non-ideal case

The voltage across the transformer primary remains the same as for the ideal case, but the circulating current, (during intervals T_3 and T_7) results in a different waveform of the primary transformer current in the non-ideal case.

As shown in Figure 5-15, the switch voltage waveform also remains the same but the circulating current in the primary side causes current to flow through the switches during intervals T_3 and T_7 in the non-ideal case.

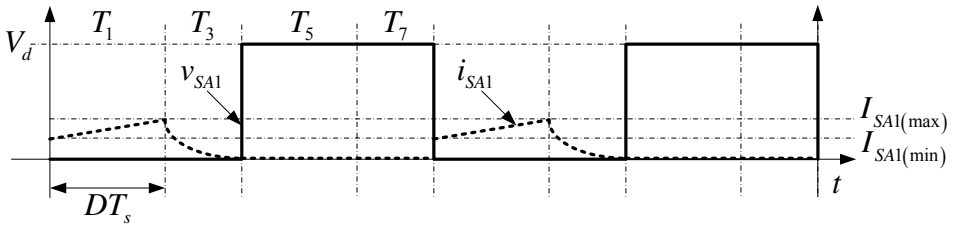


Figure 5-15 Switch voltage and current waveforms – Non-ideal case

The circulating current is "passive" because no power is transferred to the secondary side of the transformer during this interval. However, the circulating current adds to the rms current flowing through the MOSFETs on the primary side of the converter and this will increase conduction losses.

The voltage and current waveforms of the rectifying diodes change slightly as indicated in Figure 5-16.

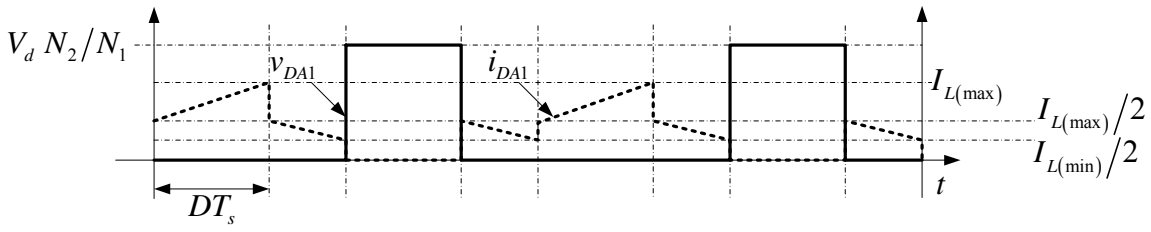


Figure 5-16 Diode voltage and current waveforms – Non-ideal case

5.7 PARALLELING OF POWER MOSFETS AND DIODES

The rated maximum average current through the power MOSFETs (SPW17N80C3) and the rectifying diodes (SDT12S60) is not enough to withstand the current that will be flowing through them in this application (see Table 5-2). Since similar components with larger current ratings were not available, it was decided to connect the MOSFETs in parallel and the diodes in parallel, since the SPW17N80C3 and SDT12S60 both have a positive temperature coefficient. A positive temperature coefficient ensures equal current sharing among the switches [5]. The following argument explains why a positive temperature coefficient will result in equal current sharing. Say two MOSFETs M_1 and M_2 were connected in parallel and start operating at the same temperature. If the on-state resistance of M_2 is higher than the on state resistance of M_1, M_1 will carry more current. M_1's on state resistance starts increasing and more current starts flowing through M_2. This forces the current to divide evenly and a balance is maintained.

Table 5-2 Rated MOSFET and rectifying diode current

Component	Rated $I_{F(cont)}$	Operating $I_{F(ave)}$	Switches in par.	New Rated $I_{F(cont)}$
SPW17N80C3	17A	16.5A	2	34A
SDT12S60	12A	37.5A	3	36A

5.8 POWER LOSS CALCULATIONS

The power dissipated by the MOSFETs and diodes is calculated by using the current waveforms discussed in the section 5.6. Starting with the MOSFET power switches, knowing that there will be switching losses P_{sw} and conduction losses P_{con}. Switching losses arise from the fact that a MOSFET cannot instantaneously switch on or switch off [5 (pp 583-587)]. The formula for calculating switching losses P_{sw} is discussed in [5 (p 23)] and is given by

$$P_{sw} = \frac{V_d}{2} f_s \left(i_{\max} t_{off} + i_{\min} t_{on} \right) \qquad \text{(E5-14)}$$

$i_{L(\min)}$ and $i_{L(\max)}$ are the minimum and maximum inductor current transferred across the transformer. t_{on} and t_{off} are the combined rise and fall times of the voltage across the MOSFET and current through the MOSFET. These two values are specified on the SPW17N80C3 datasheet and are given by

$$t_{on} = t_{off} = 24ns$$

The switching losses for one MOSFET with the converter operating at full load (75A and 10% current ripple) in steady state are given by

$$\begin{aligned} P_{sw} &= \frac{V_d}{2} f_s \left(i_{\max} t_{off} + i_{\min} t_{on} \right) \\ &= \frac{V_d}{2} f_s \left(\frac{1}{2} \frac{N_2}{N_1} I_{L(\max)} t_{off} + \frac{1}{2} \frac{N_2}{N_1} I_{L(\min)} t_{on} \right) \\ &= \frac{650}{4} 50000 \left(\left(20.625 \right) \cdot \left(24 \times 10^{-9} \right) + \left(16.875 \right) \cdot \left(24 \times 10^{-9} \right) \right) \\ &= 7.313W \end{aligned}$$

Keep in mind that one half of the switches are turned on soft. This implies that one half of the switches do not have turn-on losses. The switching losses for these switches is calculated by using

$$P_{sw} = \frac{V_d}{2} f_s \left(i_{\min} t_{on} \right) \qquad \text{(E5-15)}$$

Thus

$$\begin{aligned} P_{sw} &= \frac{V_d}{2} f_s \left(i_{\min} t_{on} \right) \\ &= \frac{V_d}{2} f_s \left(\frac{1}{2} \frac{N_2}{N_1} I_{L(\min)} t_{on} \right) \\ &= \frac{650}{4} 50000 \left(\left(16.875 \right) \cdot \left(24 \times 10^{-9} \right) \right) \\ &= 3.29W \end{aligned}$$

Conduction losses P_{con} of a MOSFET are calculated by using

$$P_{con} = R_{on} I_{rms}^2 \qquad \text{(E5-16)}$$

R_{on} is the on-state resistance of the MOSFET (0.29Ω for the SPW17N80C3) and I_{rms} is the rms current through the MOSFET. As discussed in section 5.6, the current through each MOSFET in this specific converter is given by the waveform shown in Figure 5-17.

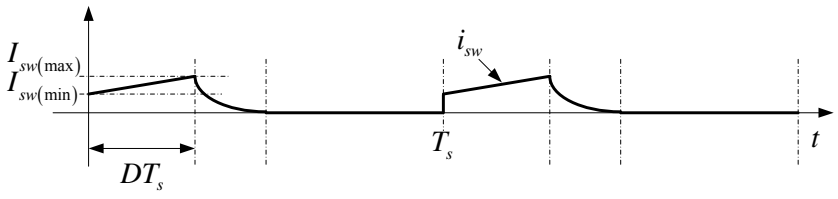


Figure 5-17 Current waveform of one primary power switch (MOSFET)

The waveform is described by (E5-17).

$$i_{sw}(t)=\begin{cases}\left(I_{sw(\max)}-I_{sw(\min)}\right)\Big/DT_s+I_{sw(\min)} & \text{for}\quad 0<t<DT_s\\ I_{sw(\max)}e^{-(R/L)t} & \text{for}\quad DT_s<t<T_s/2\end{cases} \tag{E5-17}$$

$I_{sw(\max)}$ and $I_{sw(\min)}$ are the transformed filter inductor current and L is the primary side leakage inductance of the transformer. R is the resistance of the path in which the primary current is circulating during the interval where power is not actively transferred to the secondary side of the converter. For the full-bridge topology the following relations can be derived [37].

$$D=\frac{V_oN_1}{2V_dN_2},\ m=\frac{1}{L}\left(\frac{N_2}{N_1}V_d-V_o\right)\ \text{and}\ \Delta I_L=mDT_s$$

From the relations above $I_{sw(\max)}$ and $I_{sw(\min)}$ may be calculated and is given by

$$\begin{aligned}I_{sw(\max)}&=\frac{1}{n}\left(I_o+\Delta I/2\right)=\frac{1}{n}\left(I_o+mDT_s/2\right)=\frac{1}{n}\left(I_o+m\frac{V_oN_1}{4V_dN_2}T_s\right)\\ I_{sw(\min)}&=\frac{1}{n}\left(I_o-\Delta I/2\right)=\frac{1}{n}\left(I_o-mDT_s/2\right)=\frac{1}{n}\left(I_o-m\frac{V_oN_1}{4V_dN_2}T_s\right)\end{aligned} \tag{E5-18}$$

After substituting (E5-18) into (E5-17), (E5-16) may be used to calculate the power dissipated by each MOSFET in the converter due to conduction. Figure 5-18 shows a plot of the total losses $\left(P_{con}+P_{sw}\right)$ of each MOSFET as a function of input voltage V_d. The plot is repeated for different values of the load current.

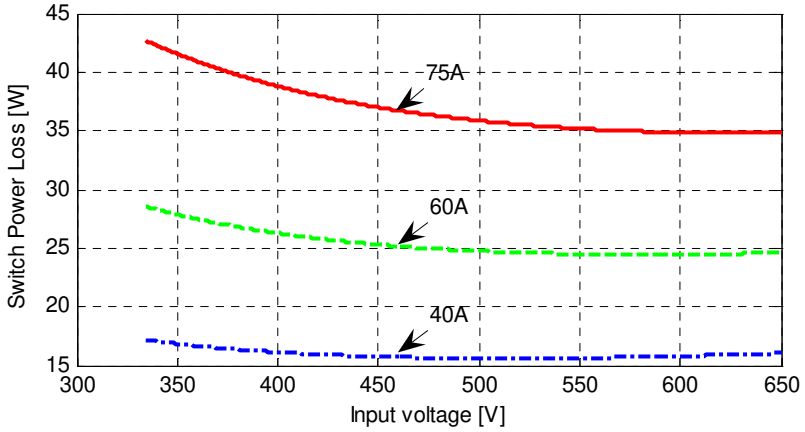


Figure 5-18 Conduction loss per MOSFET as a function of output current

From Figure 5-18 the maximum total loss per switch P_{Tot} is obtained.

$$P_{Tot}=42.19W$$

P_{Tot} is far below the maximum rated power dissipation for the MOSFET used (SPW17N80C3) which is specified in the datasheet as 208W.

For the rectifying diodes (E5-19) is used to calculate the conduction losses P_{con} per diode.

$$P_{con} = V_F I_{D(ave)} \tag{E5-19}$$

V_F is the forward voltage drop across the diode and $I_{D(ave)}$ is the average current flowing through the diode. The diodes to be used are the SDT12S60 Silicon Carbide diode from Infineon. These diodes have no reverse recovery time and this will eliminate switching losses. From the diode current waveform (Figure 5-12), it is easy to see that the average current through each diode is one half of the average inductor current. (one half of the output current). The full load, steady state, output current is equal to 75A and thus an average current of 37.5A will flow through each branch of the rectifying diode bridge. Three diodes will be connected in parallel so only one third of the current in each branch will flow through each diode. The conduction losses for each diode are given by

$$P_{con} = V_F I_{D(ave)} = 1.7(12.5) = 21.25W$$

The total power loss in one diode is thus 21.25W which is well below the maximum rated power dissipation of 88.2W specified in the SDT12S60 diode datasheet.

The losses associated with the power switches and transformer is summarized in Table 5-3

Table 5-3 Summary of converter power loss

Component	Power loss [W]	Number used per conv.	Total loss [W]
S_{A1}, S_{B2}	42.19	4	168.76
S_{A2}, S_{B1}	38.17	4	152.68
D_{A1}, D_{A1}, D_{A1}, D_{A1}	21.25	12	255
Coax. Transformer	116	1	116
			692.44

The efficiency of one converter operating at full load (rated output power of 8333.34W) may now be calculated and is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{8333.34}{8333.34 + 692.44} = 92.33\%$$

5.9 HEAT SINK DESIGN

The power dissipated by the MOSFETs and diodes at full load was calculated in the previous section. Now use these calculated values to carry out a proper heat sink design for the power switches. All the MOSFETs will be place on one heat sink and will be evenly distributed across the heat sink. The diodes will also be placed on one heat sink and will be evenly distributed across the heat sink. The concept of thermal resistance is used to design the heat sink [5 (p 733)].

Figure 5-19 shows the thermal equivalent circuit of a semiconductor device placed on a heat sink (or "sink"). Source P_{Tot} represents the total power dissipated by the device. $R_{\theta(JC)}$, $R_{\theta(CS)}$ and $R_{\theta(SA)}$ represent the thermal resistances (units in Kelvin per Watt or K/W) of the junction-to-case, case-to-sink and sink-to-ambient respectively. T_J, T_C, T_S and T_A represent the temperatures of the junction, case, sink and ambient respectively.

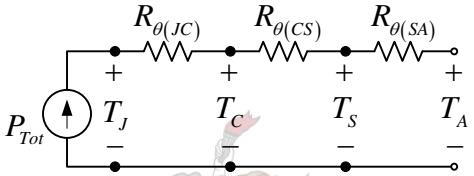


Figure 5-19 Thermal equivalent circuit of a semiconductor device placed on a heat sink

If multiple semiconductors are placed on a single heat sink, the thermal equivalent circuit has to be adjusted accordingly. Figure 5-20 shows the thermal equivalent circuit of two semiconductors $(M_1$ and $M_2)$ connected to a single heat sink. Sources P_{M1} and P_{M2} represent the power dissipated by M_1 and M_2 respectively.

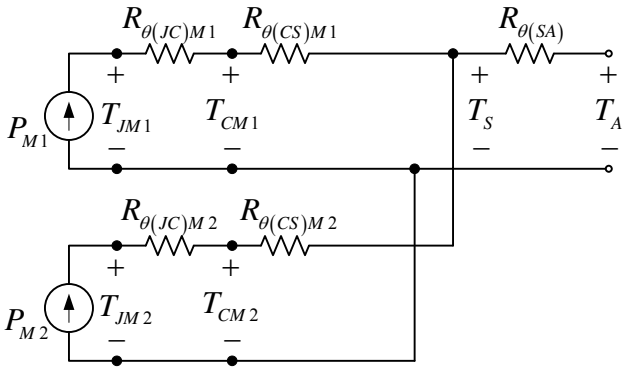


Figure 5-20 Thermal equivalent circuit of two semiconductor devices placed on a heat sink

Start by choosing the maximum value of the junction temperature (T_{JM1} and T_{JM2}) at which the power semiconductors will operate. Given the maximum power dissipated in each semiconductor

(P_{M1} and P_{M2}) and their thermal resistances, The maximum heat sink temperature T_S is calculated. T_S is given by (E5-20).

$$T_S = T_{JM1} - P_{M1}\left(R_{\theta(JC)M1} + R_{\theta(CS)M1}\right) \tag{E5-20}$$

The steady state temperature of the heat sink T_S may also be calculated by using the fact that the dissipated power from all the semiconductor devices (modeled as current sources) passes through the heat sink. Thus,

$$T_S = R_{\theta(SA)}\left(P_{M1} + P_{M2}\right) + T_A \tag{E5-21}$$

If N semiconductors are placed on a heat sink (E5-21) becomes

$$T_S = R_{\theta(SA)}\left(P_{M1} + P_{M2} + \ldots + P_{MN}\right) + T_A \tag{E5-22}$$

By substituting (E5-22) into (E5-20) a formula to calculating the maximum value of the heat sink's thermal resistance to keep the semiconductors' junction temperatures less than the specified value is found. Thus,

$$R_{\theta(SA)} = \frac{T_{JM1} - P_{M1}\left(R_{\theta(JC)M1} + R_{\theta(CS)M1}\right) - T_A}{\left(P_{M1} + P_{M2} + \ldots + P_{MN}\right)} \tag{E5-23}$$

For this converter the heat sinks will be designed to keep T_J less than $125^{\circ}C$. T_A is equal to $50^{\circ}C$ and $R_{\theta(CS)} = 0$. Table 5-4 summarises the MOSFET's and diode's parameters (from datasheets), required to design the heat sink. Table 5-4 also gives the maximum calculated value of heat sink thermal resistance to keep the semiconductors' junction temperature below $125^{\circ}C$.

Table 5-4 Calculated thermal resistances for MOSFETs' and diodes' heat sinks

Component	$P_{M1}\ [W]$	$R_{\theta(JC)}\ [K/W]$	N	$R_{\theta(SA)}\ [K/W]$
MOSFET	42.19	0.6	8	0.155
Diode	21.25	1.7	12	0.152

Table 5-4 shows that the maximum value of the thermal resistances of the MOSFETs' and diodes' heat sinks are relatively low. It is difficult to find a heat sink with such a low thermal resistance without the presence of forced convection to the heat sink. For this converter, a SEMIKRON heat sink (model P23) was chosen with a fan connected to the heat sink. The fan-heat sink combination has a thermal resistance of 0.145 K/W.

5.10 DRIVER CIRCUITRY

The MOSFET driver ICs get their power from the battery bank on the secondary side of the converter. To keep the 10.5kV isolation between the primary and secondary of the converter, an isolated supply (IS) is used with a rated breakthrough voltage higher than 10.5kV. There is one such supply for every module in the stack to ensure isolation between the driver circuits of the modules. Figure 5-21 shows a block diagram of the driver circuitry of one module.

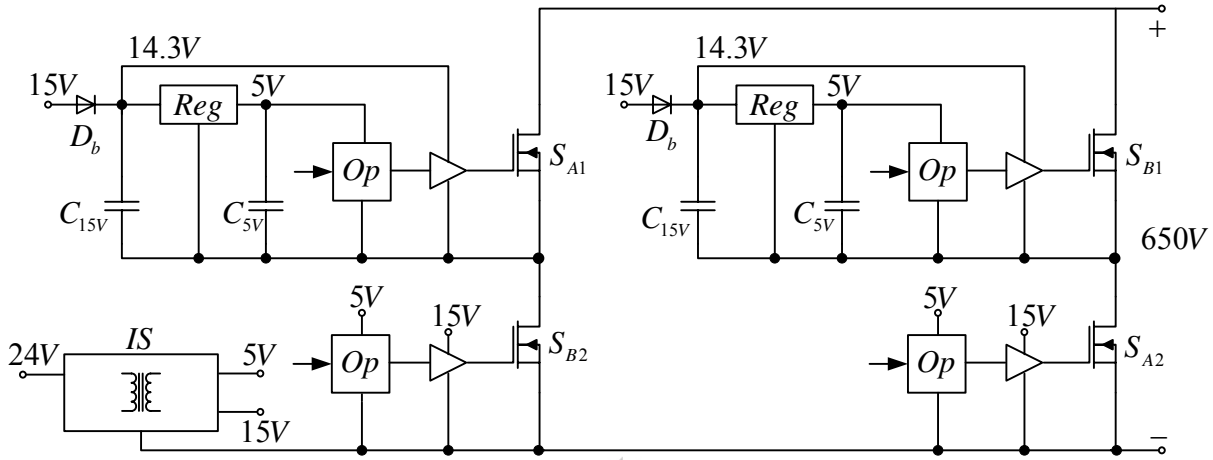


Figure 5-21 Block diagram of MOSFET driver circuitry

Each driver circuit consists of an optical receiver (Op) and driver IC. The optical receivers operate from 5V and the driver ICs operate from 15V. The output voltages of IS cannot be connected directly to the power terminals of the driver circuitry of the top two MOSFETs $(S_{A1}$ and $S_{B1})$ because the source voltages of these two MOSFETs are not fixed. For instance, when S_{B2} is on and S_{A1} is off the source voltage of S_{A1} (ground level of driver circuitry) is equal to V_x, for instance. If S_{B2} is off and S_{A1} is on this voltage level rises to $V_x + V_d$. V_d is the bus voltage and could be as high as 650V.

To overcome this problem, a diode, capacitor and regulator circuit is implemented (see Figure 5-21). The ground level of the regulator, optical receiver and driver IC, of each of the top two switches, are connected to the sources of each of these two switches. The 15V output of IS is connected to the input of the 5V regulator via a blocking diode D_b. The circuit operates as follows:

- When one of the bottom switches (S_{A2} or S_{B2}) is turned on, the ground level of its driver circuitry is equal to the ground level of IS.
- The diode becomes forward biased and capacitor C_{15} charges. C_{15} then act as a source for the voltage regulator.

- When the bottom switch is turned off, the ground level of the driver circuitry jumps to V_d. The voltage at the cathode of the diode jumps to $V_d + V_{C15}$, where V_{C15} is the voltage across capacitor C_{15}. The diode now blocks this high voltage $\left(\text{equal to } V_d\right)$ and stops current from flowing into IS.

Note that the blocking diode should have a maximum voltage rating of more than V_d and the capacitor C_{15} should have a large enough capacitance to store enough energy (during one switching cycle) to be able to supply power to the driver circuitry.

At converter startup, the capacitor C_{15} will not be charged and the top two switches will not be switching at first. However, this is will not result in the malfunction of the converter since the normal switching sequence is maintained. Capacitor C_{15} will simply charge during the first few switching cycles, when the bottom switches are turned on. The converter will then start to function normally.

5.10.1 MOSFET GATE RESISTANCE AND DEAD TIME

There are many essential requirements which the gate drive of a power MOSFET must meet, especially in high frequency applications [(pp 583-385), 36]. A high frequency model and an explanation of the turn-on and turn-off sequence, associated with power MOSFETs are discussed in detail in [5 (pp 583-385), 36]. It is shown that the turn-on and turn-off times of a power MOSFET are largely dependant on parameters such as the gate-source capacitance C_{GS}, gate-drain capacitance C_{GD} and the gate resistance R_G (see Figure 5-22). If $C_{GS} >> C_{GD}$ (as indicated in the for the SPW17N80C3 datasheet $C_{GS} = 2.26\times10^{-9}$ and $C_{GD} = 0.06\times10^{-9}$), it is primarily the time constant τ, given in (E5-24), that determines the switching times and this equation may be used to calculate R_G for a given τ.

$$\tau = R_G C_{GS} \tag{E5-24}$$

that determines the switching times of the power MOSFET. Of these two components, only R_G is an external component and is controllable by the designer.

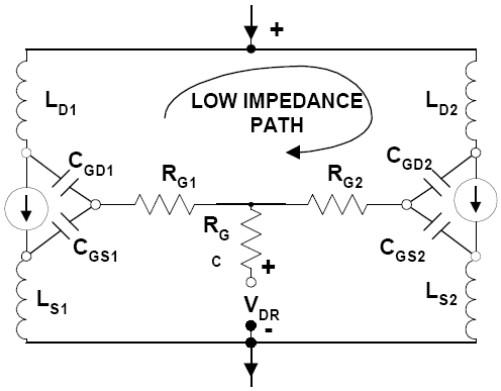


Figure 5-22 Two paralleled MOSFETs with parasitic inductances and capacitances [1]

Other than determining the switching times of the power MOSFET, R_G also has the following two functions:

- R_G has to limit the current sourced and sinked by the driver IC. Depending on the supply voltage V_C and the maximum rated source and sink current I_C of the driver IC, the minimum value of R_G may be calculated by using

$$R_{G(\min)} = V_C / I_C \tag{E5-25}$$

- The parasitic components C_{GS} and L_s (stray inductance in the gate-source path), together with R_G, form a resonant circuit [35]. The value of R_G will determine if this circuit is sufficiently damped. If R_G is too large the circuit will be under-damped and unwanted oscillations at the gait of the MOSFET will occur.

It is difficult to determine the exact value of L_s, because L_s include the inductances of the gate-source tracks on the PCB, gate resistors and the MOSFET package itself. The scope op this thesis is not to do an in-depth analysis on a MOSFET drive circuit and it was decided to calculate the minimum and maximum value of R_G by only using (E5-24) and (E5-25). If oscillations occur at the gate of a MOSFET, the value of R_G will by adjusted accordingly.

The dead time inserted in the PWM signals is equal to 300ns. The MOSFET needs to turn on and turn off in less than 300ns. Remembering that two MOSFETs are connected in parallel $\left(C_{GS} = 2\left(2.26\times10^{-9}\right)\right)$ and using (E5-24) the maximum allowable value of R_G is calculated

$$\begin{aligned} R_{G(\max)} &< \tau / C_{GS} \\ &= 300\times10^{-9} \Big/ \left(2\left(2.26\times10^{-9}\right)\right) \\ &= 66.4\Omega \end{aligned}$$

The minimum value of R_G is calculated using (E5-25). According to the driver IC datasheet (TPS2812 from TEXAS Instruments) $I_C = 2A$. The supply voltage to the driver IC is equal to 14.3V. It is found that

$$\begin{aligned} R_{G(\min)} &= V_C / I_C \\ &= 14.3/2 \\ &= 7.15\Omega \end{aligned}$$

Lastly, individual gate resistors (R_{G1} and R_{G1} in Figure 5-22) are used, together with a common gate resistor (R_G) as done in [(pp 583-385), 35]. A fast switching diode are connected across R_G (anode on the driver side) to decrease the turn-off time of the MOSFETs.

The following guidelines should also be used when paralleling MOSFETs [35]:

- Zener diodes in the gate drive circuit are commonly used to prevent over voltage at the gate of a MOSFET. The presence of a Zener diode at the gate of a MOSFET may cause oscillations. The Zener diode, if required, should be placed on the driver side of the gate resistor to prevent oscillations.
- Practical experimentation has shown that connecting a capacitor across the gate and source of a MOSFET to reduce voltage spikes on the gate signal could also result in oscillations.

5.11 CONTROLLER BOARD

Figure 5-23 shows a block diagram of the controller board. The battery voltage, battery current and inductor current are measured and fed to the controller IC. The controller IC used is the UC28025 and provides two PWM signals (Out A and Out B in Figure 5-23) which are phase-shifted by 180 degrees with respect to each other. These PWM signals are connected to an EPLD which generates the four required PWM signals, as shown in Figure 5-8, for each module in the converter stack. The PWM signals of the modules in the stack are interleaved. The VHDL code used to generate the gating signals is shown in appendix C. The gating signals are then connected to the power modules via fibre-optic links to ensure electrical isolation between various parts of the converter.

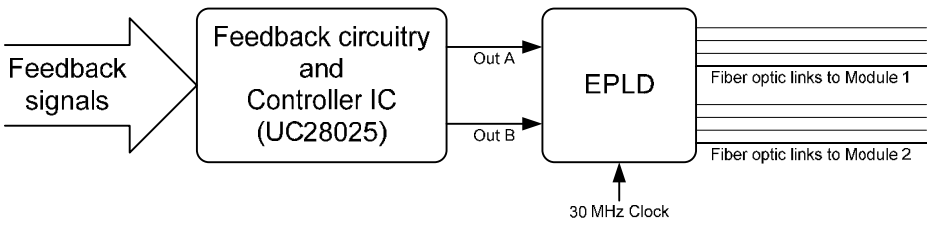


Figure 5-23 Block diagram of controller board

5.12 OUTPUT FILTER DESIGN

The theoretical waveforms of the voltage (v_L) across and the current (i_L) through the filter inductor are shown in Figure 5-24. The inductor current waveform is used to calculate the minimum inductance that the filter inductor must have to limit the ripple on the inductor current $\left(\Delta i_L = I_{L(\max)} - I_{L(\min)}\right)$ to be within a specified value.

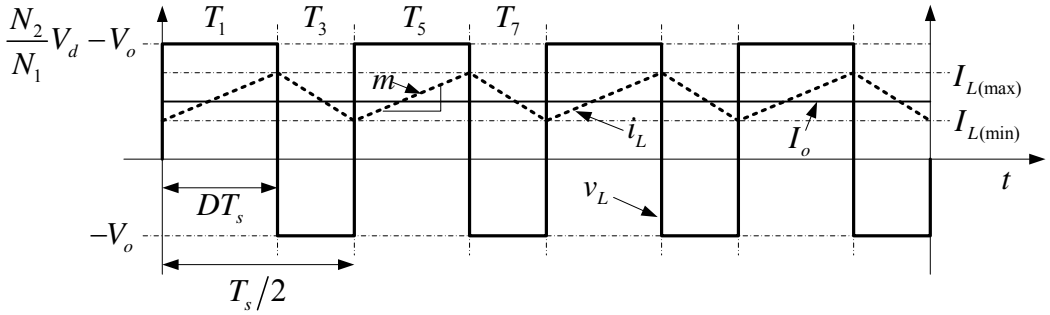


Figure 5-24 Filter inductor's voltage and current waveforms

The positive slope m of the inductor current is given by

$$m = \frac{1}{L}\left(\frac{N_2}{N_1}V_d - V_o\right) \tag{E5-26}$$

From Figure 5-24 it is found that

$$\Delta i_L = mDT_s \tag{E5-27}$$

Substituting (E5-26) into (E5-27) it is found that

$$\Delta i_L = \frac{DT_s}{L}\left(\frac{N_2}{N_1}V_d - V_o\right) \tag{E5-28}$$

For the full-bridge converter, the relation between input voltage and output voltage is given by (E5-8) and is repeated here for convenience.

$$V_o = 2\frac{N_2}{N_1}DV_d$$

Substituting (E5-8) into (E5-28) it is found that

$$\begin{aligned}\Delta i_L &= \frac{DT_s}{L}\left(\frac{N_2}{N_1}V_d - 2\frac{N_2}{N_1}DV_d\right)\\ &= \frac{T_s}{L}\frac{N_2}{N_1}V_d\left(D - 2D^2\right)\end{aligned} \tag{E5-29}$$

The maximum value of the ripple component on the inductor current may now be calculated using basic calculus. First (E5-29) is differentiated once, with respect to D and set the answer equal to 0. Then solve for D from the equation to find the value of D where the ripple component is at its maximum.

$$\frac{d}{dD}(\Delta i_L) = \frac{T_s}{L}\frac{N_2}{N_1}V_d(1-4D) = 0$$

$$\Rightarrow D = \frac{1}{4}$$

It need to be verified that this calculated value is indeed a maximum value by finding the second derivative of (E5-29) and checking that this value is less than zero.

$$\frac{d^2}{dD^2}(\Delta i_L) = -4\frac{T_s}{L}\frac{N_2}{N_1}V_d < 0$$

The filter inductor is designed so that the maximum value of the ripple component is equal to 10% of the maximum average inductor current $(75A)$. With $T_s = 50\times10^{-6}$, $N_2/N_1 = 0.5$, $V_d = 650$ and $D = 0.25$ it is found that

$$\begin{aligned} L &= \frac{T_s}{\Delta i_L}\frac{N_2}{N_1}V_d\left(D-2D^2\right) \\ &= \frac{50\times10^{-6}}{0.1(75)}(0.5)(650)\left(0.25-2(0.25)^2\right) \\ &= 108.33\mu H \end{aligned}$$

This calculated value of filter inductance is used to draw a graph of the ripple current component against duty cycle. This graph is shown in Figure 5-25. From the graph it can be seen that the maximum ripple component occurs when D is equal to 0.25 and its value is equal to 7.5A.

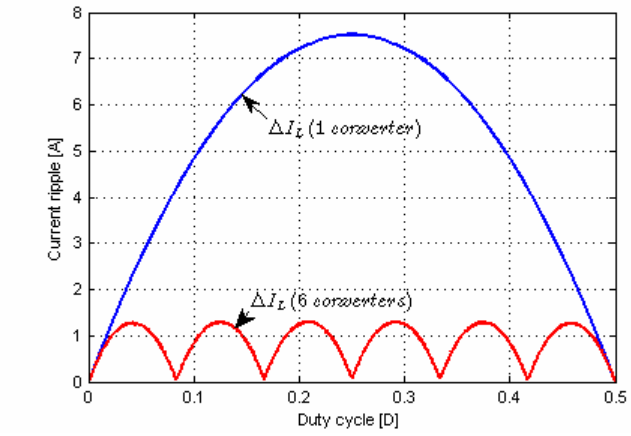


Figure 5-25 Graph of inductor ripple current against duty cycle

Also indicated in Figure 5-25 is the ripple component of the output current if six converters are used and their gate signals are interleaved. From Figure 5-25 it is clear that the ripple component on the output current is six times smaller when six converters are used than when one converter is used. A smaller ripple component on the output current results in a smaller filter capacitor.

To design the filter capacitor, the largest possible ripple current component is used and it is assumed that this ripple component flows through the filter capacitor (the filter capacitor provides a high impedance path for the ripple current). The theoretical waveforms of the voltage (v_C) across and the current (i_C) through the filter capacitor are shown in Figure 5-26.

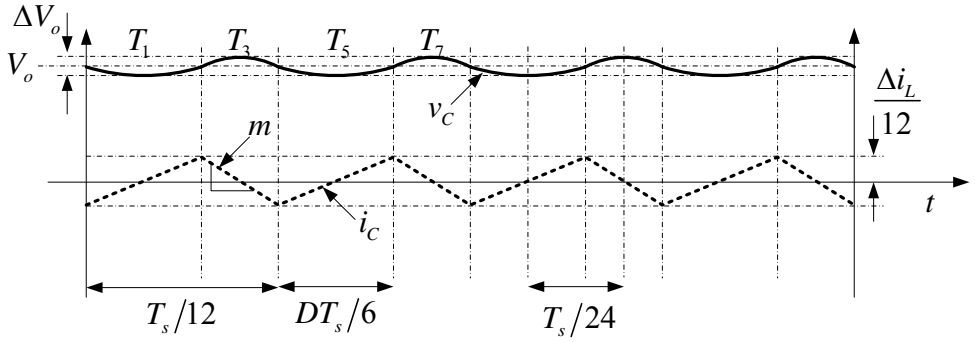


Figure 5-26 Filter capacitor's voltage and current waveforms

As shown in Figure 5-26 the maximum ripple current component is six times smaller and its frequency is six times faster. The filter capacitor C charges when the ripple current is positive. The amount of charge ΔQ is given by (E5-30) [37].

$$\Delta Q = \frac{1}{2} \cdot \frac{T_s}{24} \cdot \frac{\Delta i_L}{12} = \frac{T_s \Delta i_L}{576} \qquad \text{(E5-30)}$$

The change in output voltage ΔV_o is given by (E5-31).

$$\Delta V_o = \frac{\Delta Q}{C} \qquad \text{(E5-31)}$$

Given a specified change in output voltage the minimum value of capacitance to reduce the output voltage ripple to less than the specified value may be calculated. It is found that

$$C = \frac{T_s \Delta i_L}{576 \Delta V} = \frac{20 \times 10^{-6} (7.5)}{576 (110 \times 0.01)} = 237nF$$

To finally select the filter capacitor, it should kept in mind that the capacitor should be able to withstand the rms value of the current flowing through it (the ripple component of the output current) as well as the output voltage of 110V.

5.13 ISOLATION

This is a high voltage converter and sufficient isolation between components in various parts of the converter is crucial. The following steps were taken to provide the required isolation:

- Heat shrink with a break through voltage of greater than 25kV was placed between the primary and secondary windings of the isolation transformer (see chapter 3 for details).

- The power supplies, supplying power to the driver circuitry of all the converters in the stack, have isolation transformers with more than 10.5kV isolation.
- The gate signals are transferred via fibre optic cables from the controller board to the driver circuitry.

5.14 DC CAPACITOR TO ELIMINATE CORE SATURATION

As explained in chapter 4, average current mode control is used to control the converter. The inductor current of one module in the stack is measured and fed back to the controller. The current flowing through the inductor is directly measured at the inductor using a current sensor. This technique of control could cause the transformer core to saturate. The following argument will prove this statement.

The ideal, steady state transformer primary current waveform i_p is shown in Figure 5-27. Due to slight differences in MOSFET turn-on and turn-off delay times, the primary current will develop a DC offset (I_{DC}). The transformer primary current with a DC offset added to it is shown in Figure 5-27.

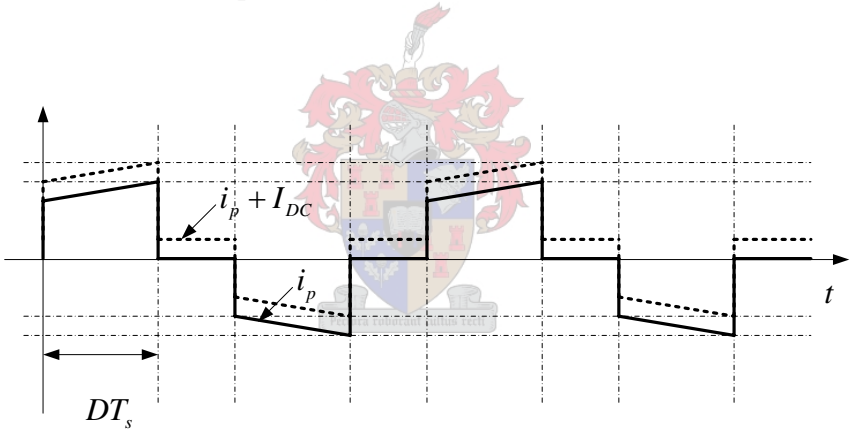


Figure 5-27 Ideal transformer primary current waveform

This DC component of the transformer primary current can not be "transformed" by the transformer and will not be seen on the secondary side of the transformer. The controller will thus not pick up any DC offset on the primary side of the transformer and the transformer's core will saturate.

To prevent the transformer core from saturating, a capacitor C_p was place in series with the primary winding of the transformer as shown in Figure 5-28.

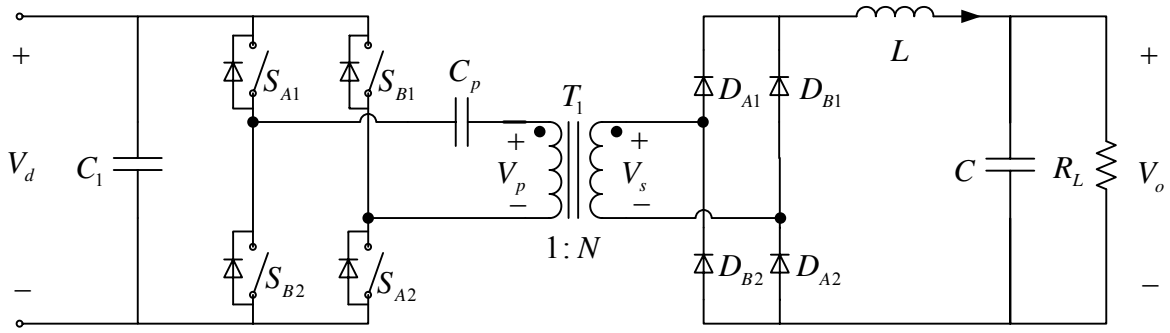
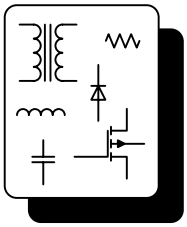


Figure 5-28 Full-bridge converter with primary winding series connected capacitor

5.15 SUMMARY

In this chapter, the focus was on designing all the essential hardware components of the converter. The worst case rms current through the DC-bus capacitors was analysed to aid the selection of the DC-bus capacitor. The switching strategy and switching sequence were analysed in order to obtain circuit waveforms for the calculation of losses in the power MOSFETs and rectifying diodes. These losses were used to do a proper heat sink design for the power MOSFETs and rectifying diodes. Gate drive circuits were designed for the case where two MOSFETs are connected in parallel. Lastly, the effect of interleaved switching was analysed to assist in the output filter design.



Chapter 6

RESULTS

6.1 INTRODUCTION

To verify the theoretical calculations and the simulations done in chapters 3, 4 and 5 a prototype two-level series stacked converter was built in the laboratory. A one level converter will be used to measure a majority of the steady state converter waveforms and a two-level series stacked converter will be used to test the converter's control system and to verify that the DC-bus capacitors balance during all operating conditions.

6.2 CONVERTER WAVEFORMS FOR A SINGLE MODULE CONVERTER

Figure 6-1 shows the gate signals for one converter module in the stack, as measured at the output pins of the EPLD. These signals correlate with the phase shifted gate signals shown in Figure 5-8. Channels 1 and 4 are the gate signals (measured at the outputs of the EPLD) for one half of the full-bridge phase arm and channels 2 and 3 are the gate signals for the other half of the full-bridge phase arm. The phase shift between the gate signals (ch1, ch4 with respect to ch2, ch3) is small because the duty cycle is nearly 0.5.

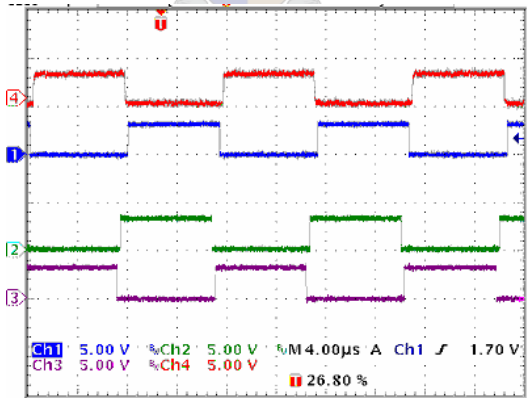
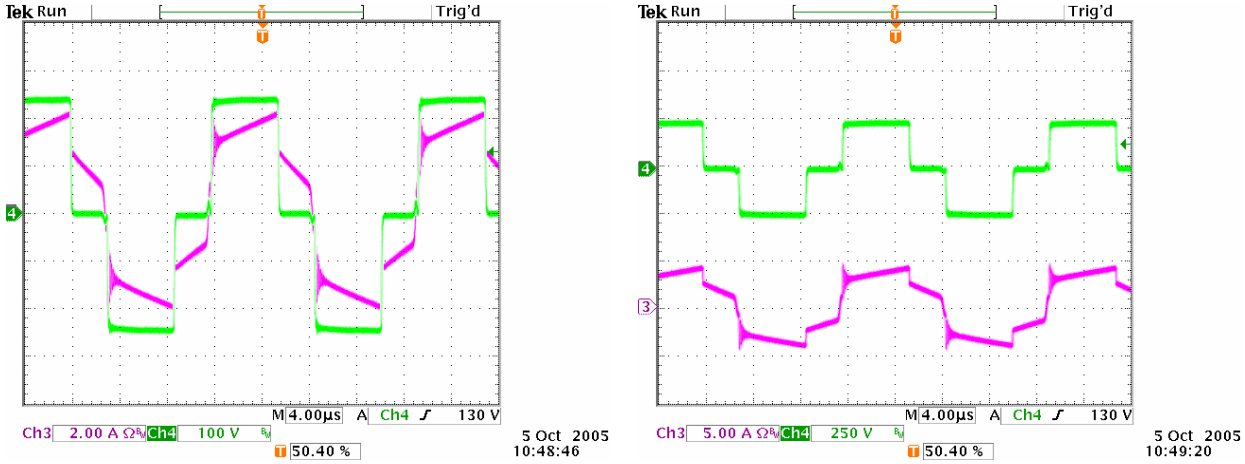


Figure 6-1 Gate signals for one converter module

The voltage and current waveforms, measured across the primary terminals of the isolation transformer, are shown in Figure 6-2 (a) and (b). These voltage and current waveforms correlate with the theoretical voltage and current waveforms shown in Figure 5-14. The current waveform obtained from the prototype converter has high frequency oscillations superimposed on it at the start of each switching cycle (indicated on Figure 6-2). These oscillations are caused by resonance between the transformer's leakage inductance and the junction capacitance of the rectifying diodes.

Unfortunately, three diodes had to be paralleled to meet the maximum current specification. This increased the junction capacitance of "one" (actually three) diode(s) and worsened the oscillations. A snubber circuit was implemented to dampen the oscillations.



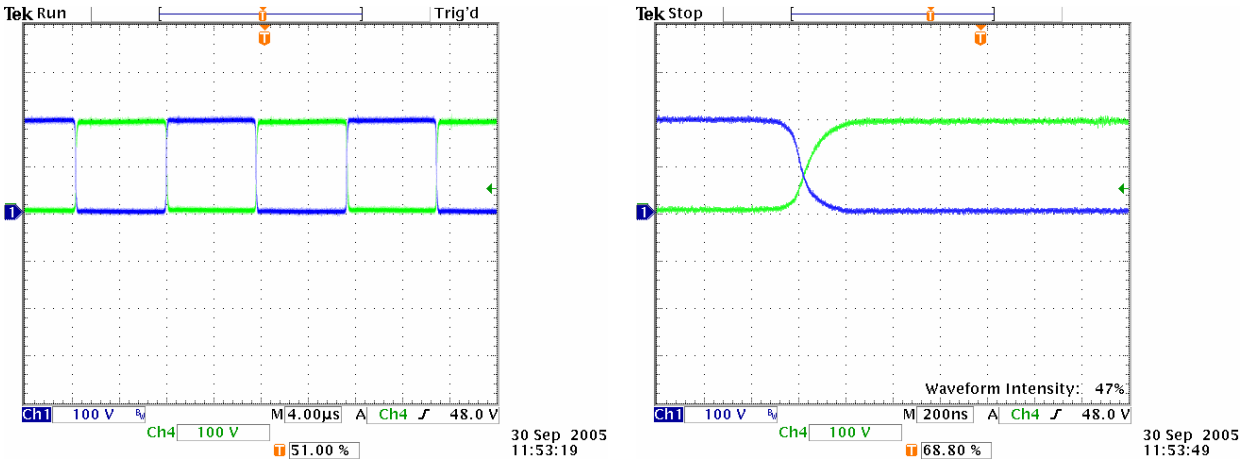
(a) **(b)**

Figure 6-2 Transformer primary waveforms (a) Voltage (b) Current

Figure 6-3 (a) and (b) show the voltage waveforms measured across switches S_{A1} and S_{B2} (channels 1 and 4 respectively) as indicated in Figure 5-7. At first, it appears as if the dead time inserted (allowing one MOSFET to completely turn off before the other MOSFET turns on) is not long enough, as the voltage across S_{A1} starts rising before the voltage across S_{B2} has reached zero (see Figure 6-3 (b)). However, this effect is not caused by insufficient dead time but is a result of the following (see section 5.6):

- The MOSFETs' drain-source capacitance
- Primary circulating current
- The specific switching strategy used

During the dead time interval, the drain-source "capacitor" of S_{A1} charges (with a time constant determined by the magnitude of the primary circulating current) and the drain-source "capacitor" of S_{B2} discharges. The bus voltage across S_{A1} and S_{B2} divides equally between the two drain-source "capacitors" and causes the effect shown in Figure 6-3 (b).

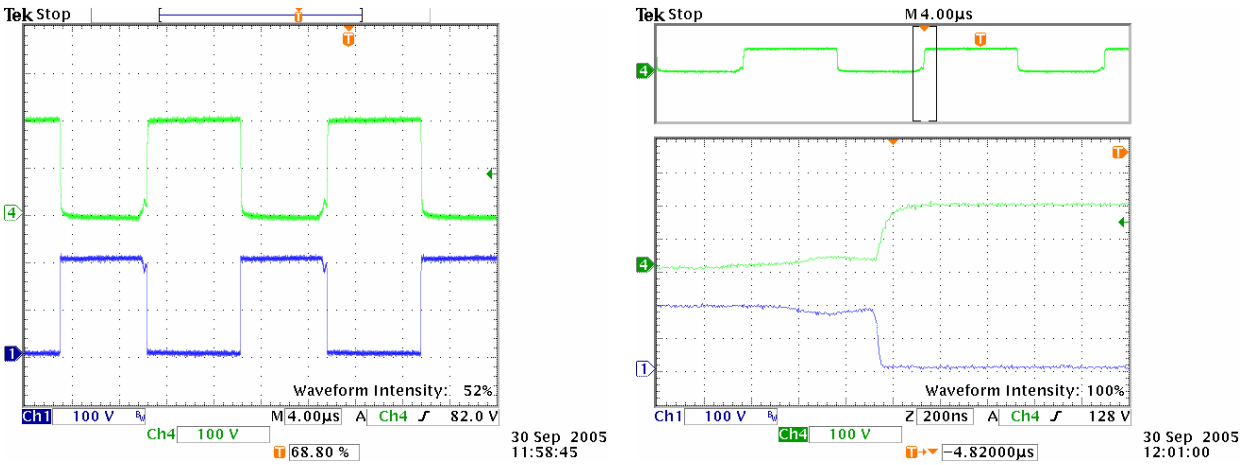


(a) **(b)**

Figure 6-3 Measured MOSFETs' voltage waveforms (S_{A1} and S_{B2})

Figure 6-4 (a) and (b) show the voltage waveforms measured across switches S_{A2} and S_{B1} (channels 1 and 4 respectively) as indicated in Figure 5-7. As a result of the switching strategy being used, these waveforms differ from the waveforms measured across switches S_{A1} and S_{B2} (see section 5.6). The voltages across these switches rise and fall almost instantaneously because the drain-source "capacitors" across S_{A2} and S_{B1} are instantaneously discharged by the switches themselves when they are turned on.

An interesting observation is the "hump" visible on the waveforms. This "hump" occurs during the dead time intervals when the free-wheeling diodes are conducting, and is caused by their relatively slow switching times in conjunction with the primary leakage inductance.



(a) **(b)**

Figure 6-4 MOSFETs' voltage waveforms (S_{A2} and S_{B1})

There is almost no overshoot visible at switch turn-off, indicating a good circuit layout with small stray inductances.

Figure 6-5 shows the voltage waveforms measured across one rectifying diode (channel 1) and one MOSFET (channel 4). High frequency oscillations are visible on the voltage waveform of the rectifying diode and are caused by resonance between the transformer's leakage inductance and the diode's junction capacitance. As expected, the voltage across the rectifying diode is one half of the voltage measured across the MOSFET. This indicates a transformer winding ratio of 2:1.

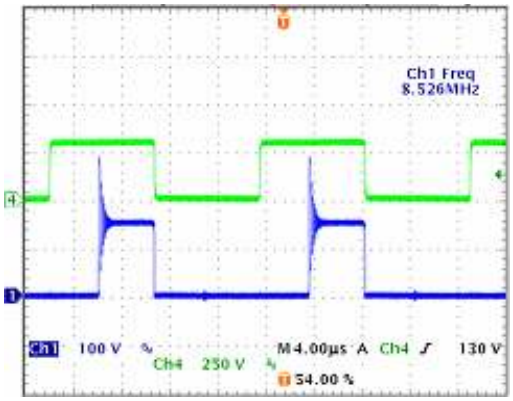
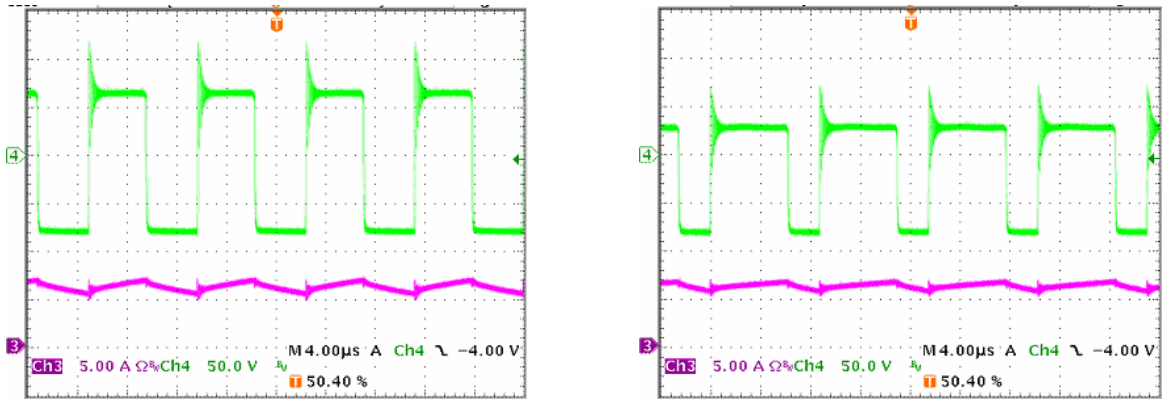


Figure 6-5 Voltage measured across a rectifying diode and a MOSFET

Figure 6-6 (a) and (b) show the voltage and current waveforms measured across the filter inductor, for two different cases. In both cases the output current is regulated at 6A. In Figure 6-6 (a) the input voltage to the converter is greater than in Figure 6-6 (b). From Figure 6-6 (a) and (b) the following observations are made:

- The magnitude of the ripple component on the inductor increases if the input voltage becomes larger. This is expected and can directly be related to (E5-29).
- The high frequency oscillations caused by resonance between the transformer leakage inductance and the junction capacitance of the rectifying diodes are visible on the voltage and current waveforms.



(a) **(b)**

Figure 6-6 Measured waveforms for inductor voltage and current

6.3 CONVERTER WAVEFORMS FOR A TWO MODULE CONVERTER

Figure 6-7 shows the voltage and current waveforms of a dual module converter. Channels 1 and 4 are the voltage waveforms measured across the primary terminals of the two modules. Channel 2 is the output current waveform which is regulated at 4A. Channel 3 is the waveform of the current flowing through the primary side of one module (corresponding to channel 1). From Figure 6-7 the following observations are made:

- From the voltage waveforms it is clear that the gate signals of the two modules are phase shifted by 90 degrees (180/2 degrees for a two module converter).
- The amplitudes of the voltage waveforms are equal, indicating that the DC-bus capacitors do balance. This is a significant result since the converter was built under the assumption that the DC-bus capacitors will balance.

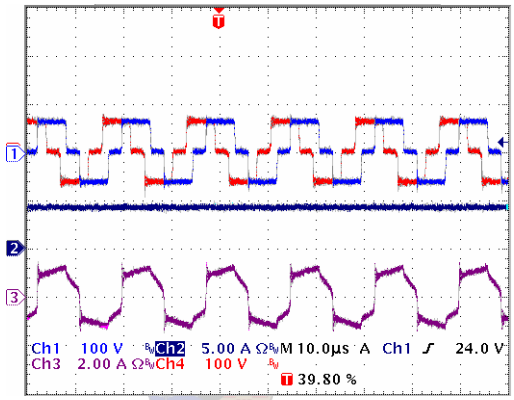


Figure 6-7 Dual module converter's voltage and current waveforms

Figure 6-8 shows the voltage and current waveforms of a dual module converter. Channel 1 is the voltage measured across the primary terminals of one module and channel 2 is the sum of the inductor currents of the two converters. From Figure 6-8 it is observed that the frequency of the ripple component on the output current is four times the frequency of the voltage measured across the primary of one module's transformer (or twice the frequency of the inductor current of one module). It can also be seen how the shape of the ripple component's waveform changes as the duty cycle changes. Note that the amplitude of the ripple component does not change when the duty cycle changes, as was previously discussed. This is because the input voltage was increased to change the duty cycle and the amplitude of the ripple component increases as the input voltage increases.

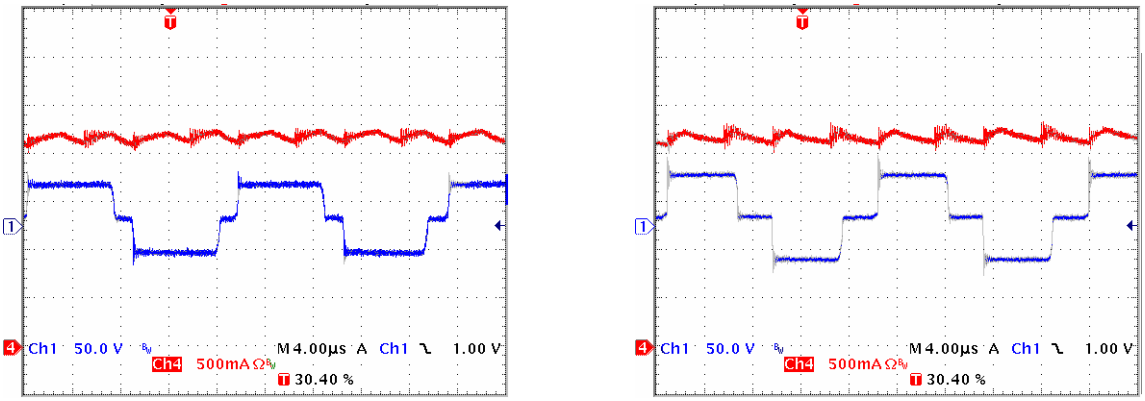


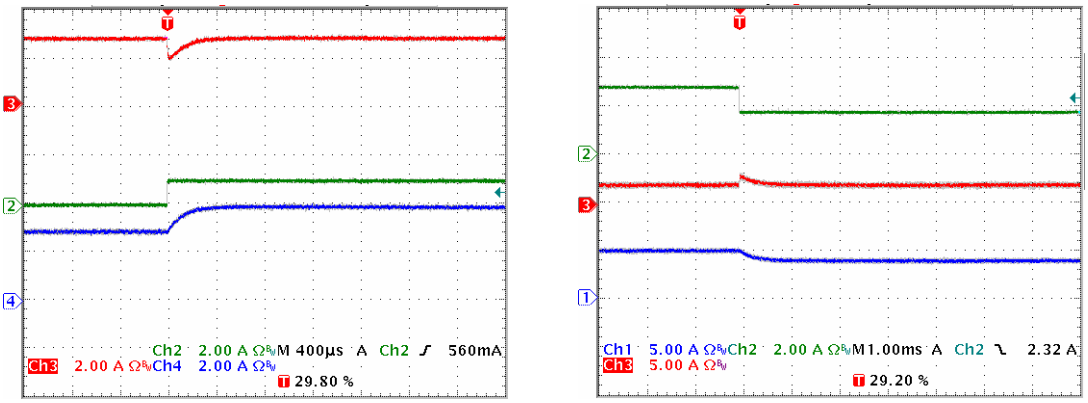
Figure 6-8 Dual module converter's voltage and current waveforms

6.4 SYSTEM RESPONSE

The following sections show the two module converter's response to changes in the load current and the input voltage. Results are given for the converter operating in bulk charge mode as well as float charge mode.

6.4.1 BULK CHARGE MODE

Figure 6-9 (a) shows the converter's response to a step in load current while the converter is operating in bulk charge mode. Channel 3 represents the current flowing into the battery. In this case, this current is regulated at 3A. Channel 2 represents the load current. In this case, the load current is increased from 0A to 1A. Channel 4 represents the sum of the two inductor currents (for the two module converter). The sum of the two inductor currents is equal to the sum of the battery current and the load current. More importantly, it can be seen that the system's response time to the step in load current is equal to 300us. This response time is of the same order of magnitude as the response time of the simulation conducted in chapter 4.



(a) **(b)**

Figure 6-9 Battery, inductor and load currents (a) Load step (b) Load drop

Figure 6-10 shows the converter's response to a step in load current while the converter is operating in bulk charge mode. Figure 6-10 is the same as Figure 6-9 (a) with the addition of the two bulk

capacitor voltages (ac component only) which are represented by channels 1 and 4. From Figure 6-10 it is clear that the bulk capacitors balances and stay balanced with the step in load current.

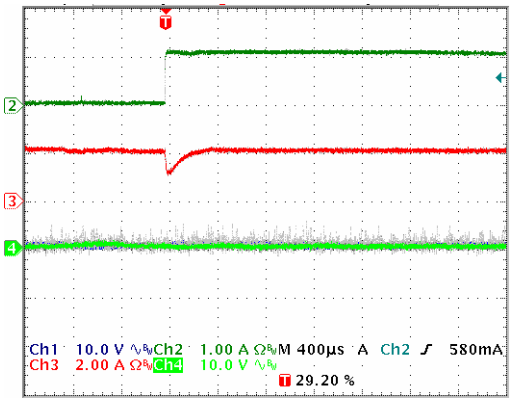


Figure 6-10 Battery current, load current and capacitor voltages during load step

6.4.2 FLOAT CHARGE MODE

Figure 6-11 shows the converter's response to a step in load current while the converter is operating in float charge mode. Channel 1 represents the regulated output voltage, which is in this case equal to 13.4V. Channel 2 represents the load current. The load current is increased from 0A to 1A. Channel 3 represents the battery current and is equal to 2A in this case. Channel 4 represents the sum of the two inductor currents of the converter. The sum of the two inductor currents is equal to the sum of the load current and the battery current. The system's response time is equal to 1.2ms for a 1A step in load current. As expected, in float charge mode the system's response is slower than in bulk charge mode. The effect of the step in load current is not visible on the battery voltage itself because of the battery's constant voltage source property.

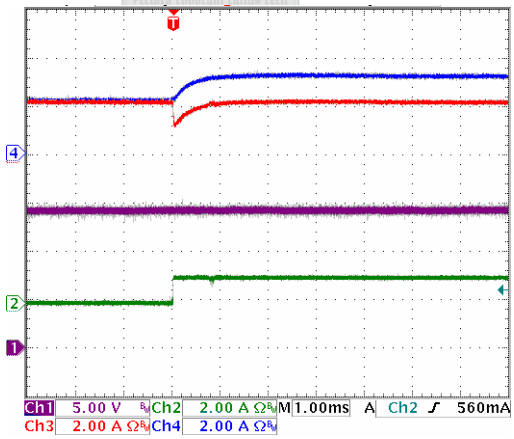
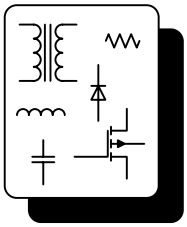


Figure 6-11 Battery current, inductor current, load currents and output voltage during load step

6.5 SUMMARY

In this chapter, the aim was to present and discuss all the measured waveforms that were obtained from the prototype converter. The measured waveforms correspond well to the theoretical waveforms. From the measured waveforms the following main observations were made:

- The voltage overshoot measured across the power MOSFETs at switch turn-off is minimal.
- Two of the power MOSFETs are turned on hard and the other two are turned on soft. The effect of this switching strategy is clearly visible on the voltage waveforms.
- The effect of the interleaved switching strategy is clearly visible on the ripple component of the output current waveform.
- It is clear that the DC-bus capacitors do balance during all operating conditions.
- It was shown that the converter operates in bulk charge mode and in float charge mode and has the desired response to changes in load current and line voltage.



Chapter 7

CONCLUSION

7.1 CONCLUSION

This thesis originated from a Spoornet requirement for high voltage DC-AC inverter, to be installed in Spoornet substations. The thesis covered the design, simulation, and hardware implementation of a high voltage DC-DC converter which forms part of the required DC-AC inverter. The main findings of each chapter are summarised below:

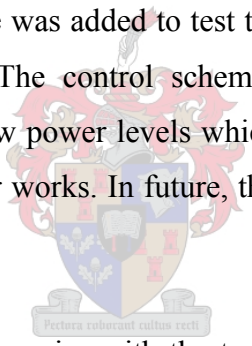
- In chapter two, potential high power DC-DC converter topologies were investigated and considered for possible implementation in the final converter design. It was found that the series stacked topology required the lowest number of DC-bus or flying capacitors and was the most economical solution.
- In chapter three, a high power high frequency coaxially wound transformer was fully analysed. The formulae for calculating the leakage inductance, magnetisation inductance and stray capacitance for the coaxially wound transformer were derived. A coaxially wound transformer was designed and prototypes were built and tested for the specific application. These test results correlate well with the theoretical calculations.
- In chapter four, different DC-DC converter control schemes were investigated and considered for possible implementation in the final converter design. It was found that average current mode control is best suited for the specific application and has advantages such as inherent pulse-by-pulse current limiting and good line regulation. A control scheme was developed to provide the required functionalities such as bulk charge operation and float charge operation. The converter was simulated with different line and load conditions to test the control scheme. The results obtained from the simulation showed that the converter's response to line and load changes is satisfactory. Simulations were also carried out to show that the DC-bus capacitors do balance during steady state operation.
- In chapter five, the focus was on the hardware design of the converter. The effects of the harmonics on the Spoornet power line and the switching of the converter on the total rms current through the DC-bus capacitors were analysed. The switching strategy used for the specific converter was discussed and circuit waveforms were constructed for the ideal and

non-ideal cases. The switching and conduction losses associated with the power MOSFETs and rectifying diodes were calculated. A thorough heat sink design was done for the power switches.

- In chapter six, the practical results obtained from a two-level series stacked prototype converter were shown and discussed. It was shown that the steady state converter waveforms correlate with the theoretically predicted waveforms. It was also shown that the converter responds similarly to changes in line voltage and load current in the practical system as in the simulations. The converter is able to operate in bulk charge mode and in float charge mode, according to the state of charge of the battery bank. Probably, the most important result obtained in this thesis is that the DC-bus capacitors balance and stay balanced during all steady state operating conditions.

7.2 FUTURE WORK

Although the converter was designed and built to have a power rating of 50kW (8.333kW per module), it was not tested at this power level. A single module converter was tested at a maximum power level of 1kW. A second module was added to test the DC-bus capacitors' voltage properties for multi-level converter operation. The control scheme was also tested using this two-level converter. These tests were done at low power levels which were sufficient to prove that the basic concept of the series stacked converter works. In future, this two-level converter could be tested at higher power levels.



The capacitor which was connected in series with the transformer's primary winding (to stop the transformer's core from saturating) requires a large maximum rms current rating. Such a capacitor is large and expensive and is difficult to implement in a practical circuit. The possibility of using an alternative method to prevent the transformer core from saturating should be investigated.

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Appendix A

FOURIER SERIES EXPANSION OF TRANSFORMER PRIMARY CURRENT WAVEFORM

The Fourier series expansion is given by

$$i_F(t) = a_0 + \sum_{k=1}^{\infty} a_k \cos(k\omega_0 t) + \sum_{k=1}^{\infty} b_k \sin(k\omega_0 t) \quad \text{for} \quad k = 0,\ 1,\ 2... \tag{EA1-1}$$

Where

$$\begin{aligned} a_0 &= \frac{1}{2T}\int_0^T i(t)\,dt \\ a_k &= \frac{1}{T}\int_0^T i(t)\cos(k\omega_0 t)\,dt \\ b_k &= \frac{1}{T}\int_0^T i(t)\sin(k\omega_0 t)\,dt \end{aligned} \tag{EA1-2}$$

The Fourier series representation of the current waveform shown below needs top be calculated.

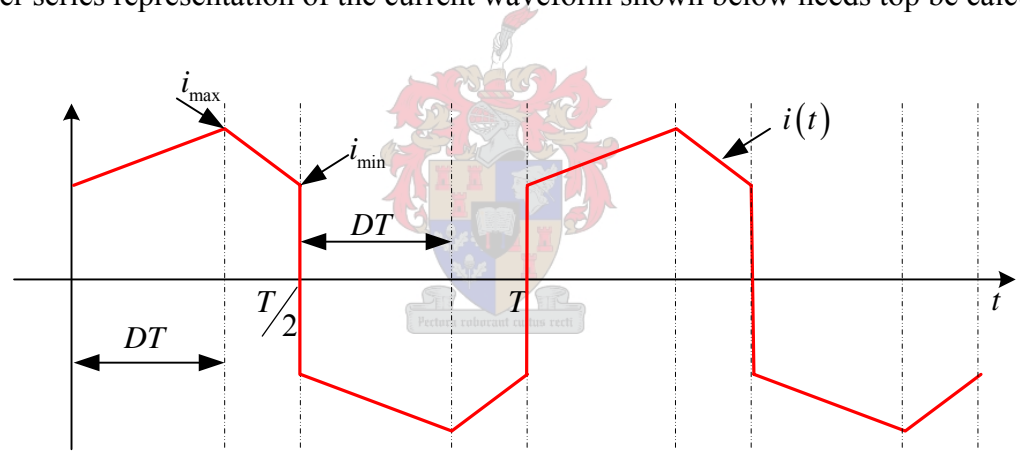


Figure A1-1 Current waveform

The following equation represents this current waveform.

$$i(t) = \begin{cases} \left(\dfrac{\Delta i}{DT}\right)t + i_{min} & \text{for } 0 < t \le DT \\ \left(\dfrac{-\Delta i}{T(1/2 - D)}\right)t + \left[\dfrac{\Delta i}{(1-2D)} + i_{min}\right] & \text{for } DT < t \le T/2 \end{cases} \tag{EA1-3}$$

$\Delta i = i_{max} - i_{min}$, D is the duty cycle and T is the period of the time-varying waveform. To simplify later equations the following constants are declared.

$$i(t) = \begin{cases} k_1 t + k_2 & \text{for } 0 < t \le DT \\ -k_3 t + k_4 & \text{for } DT < t \le T/2 \end{cases} \tag{EA1-4}$$

From this equation it can be seen that $i(t) = -i(t - T/2)$ and this implies that the Fourier coefficients may by calculated by [39]

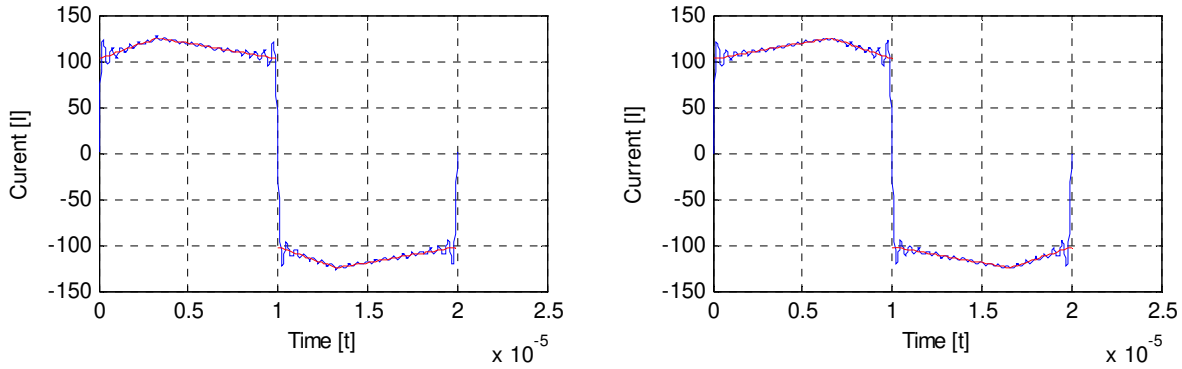
$$\begin{aligned} a_0 &= 0 \\ a_k &= \frac{4}{T}\int_0^{T/2} i(t)\cos(k\omega_0 t)\,dt \quad \text{for} \quad k = odd \\ b_k &= \frac{4}{T}\int_0^{T/2} i(t)\sin(k\omega_0 t)\,dt \quad \text{for} \quad k = odd \end{aligned} \tag{EA1-5}$$

The coefficients are calculated as follows

$$\begin{aligned} a_k &= \frac{4}{T}\left[\int_0^{DT} k_1 t\cos(k\omega_0 t)\,dt + \int_0^{DT} k_2\cos(k\omega_0 t)\,dt - \int_{DT}^{T/2} k_3 t\cos(k\omega_0 t)\,dt + \int_{DT}^{T/2} k_4\cos(k\omega_0 t)\,dt\right] \\ &= \frac{4k_1}{T}\left[\frac{\cos(k\omega_0 t)}{(k\omega_0)^2} + \frac{t\sin(k\omega_0 t)}{k\omega_0}\right]_0^{DT} + \frac{4k_2}{T}\left[\frac{\sin(k\omega_0 t)}{k\omega_0}\right]_0^{DT} - \frac{4k_3}{T}\left[\frac{\cos(k\omega_0 t)}{(k\omega_0)^2} + \frac{t\sin(k\omega_0 t)}{k\omega_0}\right]_{DT}^{T/2} + \frac{4k_4}{T}\left[\frac{\sin(k\omega_0 t)}{k\omega_0}\right]_{DT}^{T/2} \\ &= k_1 T\left[\frac{\cos(k2\pi D)}{(k\pi)^2} + \frac{2D\sin(k2\pi D)}{k\pi} - \frac{1}{(k\pi)^2} - 0\right] + 2k_2\left[\frac{\sin(k2\pi D)}{k\pi} - 0\right] \\ &\quad -k_3 T\left[-\frac{1}{(k\pi)^2} + 0 - \frac{\cos(k2\pi D)}{(k\pi)^2} - \frac{2D\sin(k2\pi D)}{k\pi}\right] + 2k_4\left[0 - \frac{\sin(k2\pi D)}{k\pi}\right] \\ &= \frac{Tk_1}{(k\pi)^2}\left[\cos(k2\pi D) + 2k\pi D\sin(k2\pi D) - 1\right] + \frac{Tk_3}{(k\pi)^2}\left[\cos(k2\pi D) + 2k\pi D\sin(k2\pi D) + 1\right] + \frac{2(k_2 - k_4)}{k\pi}\left[\sin(k2\pi D)\right] \end{aligned}$$

$$\begin{aligned} b_k &= \frac{4}{T}\left[\int_0^{DT} k_1 t\sin(k\omega_0 t)\,dt + \int_0^{DT} k_2\sin(k\omega_0 t)\,dt - \int_{DT}^{T/2} k_3 t\sin(k\omega_0 t)\,dt + \int_{DT}^{T/2} k_4\sin(k\omega_0 t)\,dt\right] \\ &= \frac{4k_1}{T}\left[\frac{\sin(k\omega_0 t)}{(k\omega_0)^2} - \frac{t\cos(k\omega_0 t)}{k\omega_0}\right]_0^{DT} - \frac{4k_2}{T}\left[\frac{\cos(k\omega_0 t)}{k\omega_0}\right]_0^{DT} - \frac{4k_3}{T}\left[\frac{\sin(k\omega_0 t)}{(k\omega_0)^2} - \frac{t\cos(k\omega_0 t)}{k\omega_0}\right]_{DT}^{T/2} - \frac{4k_4}{T}\left[\frac{\cos(k\omega_0 t)}{k\omega_0}\right]_{DT}^{T/2} \\ &= Tk_1\left[\frac{\sin(k2\pi D)}{(k\pi)^2} - \frac{2D\cos(k2\pi D)}{k\pi} - 0 + 0\right] - 2k_2\left[\frac{\cos(k2\pi D)}{k\pi} - \frac{1}{k\pi}\right] \\ &\quad -Tk_3\left[0 + \frac{1}{k\pi} - \frac{\sin(k2\pi D)}{(k\pi)^2} + \frac{2D\cos(k2\pi D)}{k\pi}\right] - 2k_4\left[-\frac{1}{k\pi} - \frac{\cos(k2\pi D)}{k\pi}\right] \\ &= \frac{Tk_1}{(k\pi)^2}\left[\sin(k2\pi D) - 2k\pi D\cos(k2\pi D)\right] - \frac{Tk_3}{(k\pi)^2}\left[k\pi - \sin(k2\pi D) + 2k\pi D\cos(k2\pi D)\right] \\ &\quad + \frac{2k_2}{k\pi}\left[1 - \cos(k2\pi D)\right] + \frac{2k_4}{k\pi}\left[1 + \cos(k2\pi D)\right] \end{aligned}$$

To verify these results a MATLAB program is used.



(a) **(b)**

Figure A1-2. Fourier series expansion check for (a) D=0.165 and (b) D=0.33

Appendix B

INTERNAL CURRENT DISTRIBUTION AND AC RESISTANCE OF THE COAXIALLY WOUND TRANSFORMER'S OUTER CONDUCTOR.

The current distribution of a solid cylindrical conductor is calculated in [26 p71]. This is done for sinusoidal excitation. For the coaxially wound transformer the current distribution for a hollow cylindrical conductor as shown in Figure A1-3 needs to be calculated.

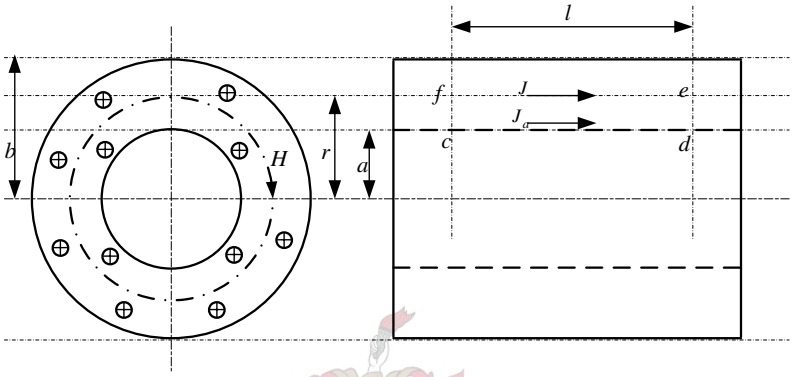


Figure A1-3 Hollow cylindrical conductor

Start by using the emf law [26 p62] on the path $cdefc$ and find that

$$J\rho l - J_a \rho l = -\frac{d\phi}{dt} \tag{EA1-6}$$

Where ϕ is the flux linking the path and given by

$$\phi = l\int_r^a B dr \tag{EA1-7}$$

Assuming sinusoidal excitation with $J = J_m e^{j\omega t}$ and $B = B_m e^{j\omega t}$ (EA1-8) is obtained

$$\rho J_m - \rho J_{ma} = -j\omega \int_r^a B_m dr \tag{EA1-8}$$

Taking the derivative on both sides it is fount that

$$\rho \frac{dJ_m}{dr} = j\omega B_m$$

Replacing B_m with μH_m it is found that

$$\rho \frac{dJ_m}{dr} = j\omega \mu H_m \tag{EA1-9}$$

Now use the mmf law [26 p62, p72] and obtain the differential equation describing the current distribution,

$$\frac{d^2J}{dr^2}+\frac{1}{r}\frac{dJ}{dr}=j\frac{\omega\mu}{\rho}J \qquad \text{(EA1-10)}$$

It is recognised that this is a Bessel's modified differential equation which is commonly written as

$$x^2y''+xy'-\left(x^2+n^2\right)y=0 \quad \text{for} \quad n\geq 0$$

The solutions of this equation is called modified Bessel functions of order n. The general solution of Bessel's differential equation is given by

$$y=AI_n\left(x\right)+BK_n\left(x\right) \quad \text{all } n$$

In our case the differential equation looks as follow.

$$\frac{d^2J}{dr^2}+\frac{1}{r}\frac{dJ}{dr}-j\frac{\omega\mu}{\rho}J=0 \qquad \text{(EA1-11)}$$

$n=0$ and there is a constant $k^2=j\frac{\omega\mu}{\rho}=j\frac{2}{\delta^2}$ with $\delta=\sqrt{\frac{2\rho}{\omega\mu}}$ See [26]. The general solution now takes the form [26]

$$J=AI_0\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)+BK_0\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right) \qquad \text{(EA1-12)}$$

Constants A and B need to be calculated by using (EA1-9) and the following boundary conditions.

- The magnetic field is zero at the outside of the conductor because the enclosed current is zero.
- The magnetic field on the inner surface of the conductor is tangential.

Substituting the general solution into (EA1-9) it is found that

$$\begin{aligned}H_m&=\frac{\rho}{j\omega\mu}\frac{dJ_m}{dr}\\&=\frac{\rho}{j\omega\mu}\frac{d}{dr}\left(AI_0\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)+BK_0\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)\right)\\&=\frac{\rho}{j\omega\mu}\left(\frac{\sqrt{2}}{\delta}e^{\frac{j\pi}{4}}\right)\left(AI_1\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)-BK_1\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)\right)\end{aligned}$$

Using the boundary condition at the outer surface it is found that

$$0=\frac{\rho}{j\omega\mu}\left(\frac{\sqrt{2}}{\delta}e^{\frac{j\pi}{4}}\right)\left(AI_1\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)-BK_1\left(\frac{\sqrt{2}}{\delta}re^{\frac{j\pi}{4}}\right)\right)_{r=a}$$

or

$$A=\frac{BK_1\left(a_0\right)}{I_1\left(a_0\right)} \qquad \text{(EA1-13)}$$

Where

$$a_0 = \frac{\sqrt{2}a}{\delta} e^{\frac{j\pi}{4}}$$

Using the second boundary condition it is found that

$$\left(\frac{I_{enc}}{2\pi b}\right) = \left(\frac{\rho}{j\omega\mu}\right)\left(\frac{\sqrt{2}}{\delta} e^{\frac{j\pi}{4}}\right)\left(AI_1\left(\frac{\sqrt{2}}{\delta} re^{\frac{j\pi}{4}}\right) - BK_1\left(\frac{\sqrt{2}}{\delta} re^{\frac{j\pi}{4}}\right)\right)_{r=b}$$

or

$$C = AI_1(b_0) - BK_1(b_0) \qquad \text{(EA1-14)}$$

where

$$b_0 = \frac{\sqrt{2}b}{\delta} e^{\frac{j\pi}{4}} \text{ and } C = \left(\frac{I}{2\pi r_{in}}\right) \cdot \left(\frac{j\omega\mu}{\rho}\right) \cdot \left(\frac{\delta}{\sqrt{2}e^{\frac{j\pi}{4}}}\right)$$

Solving A and B in (EA1-13) and (EA1-14) it is found that

$$A = \frac{CK_1(a_0)}{K_1(b_0)I_1(a_0) - K_1(a_0)I_1(b_0)}$$

$$B = \frac{CI_1(a_0)}{K_1(b_0)I_1(a_0) - K_1(a_0)I_1(b_0)}$$

A and B can now be substituted back into the general solution and finally the current density is given by

$$J = C\left(\frac{I_0(r_0)K_1(a_0) + I_1(a_0)K_0(r_0)}{I_1(a_0)K_1(b_0) - I_1(b_0)K_1(a_0)}\right) \qquad \text{(EA1-15)}$$

With

$$r_0 = \frac{\sqrt{2}r}{\delta} e^{\frac{j\pi}{4}}$$

To verify this result the solution is substituted back into the differential equation and we find the three terms to be.

$$\left.\frac{d^2J}{dr^2}\right|_{r=b} = \left(\frac{I}{2\pi r_{in}}\right) \cdot \left(\frac{j\omega\mu}{\rho}\right) \cdot \left(\frac{\sqrt{2}}{\delta} e^{\frac{j\pi}{4}}\right) \cdot \left(AI_0(b_0) + BK_0(b_0)\right) - \left(\frac{I}{2\pi r_{in}^2}\right) \cdot \left(\frac{j\omega\mu}{\rho}\right) \cdot \left(AI_1(b_0) - BK_1(b_0)\right)$$

$$\left.\frac{1}{r}\frac{dJ}{dr}\right|_{r=b} = \left(\frac{I}{2\pi r_{in}^2}\right) \cdot \left(\frac{j\omega\mu}{\rho}\right) \cdot \left(AI_1(b_0) - BK_1(b_0)\right)$$

$$\left.-j\frac{\omega\mu}{\rho}J\right|_{r=b} = \left(\frac{I}{2\pi r_{in}}\right) \cdot \left(\frac{j\omega\mu}{\rho}\right) \cdot (-j) \cdot \left(\frac{-j\sqrt{2}e^{\frac{j\pi}{4}}}{\delta}\right) \cdot \left(AI_0(b_0) + BK_0(b_0)\right)$$

The sum of these three terms equals zero and this verifies that (EA1-15) is a solution to the differential equation.

This result may be used to find the impedance of the hollow cylindrical conductor

$$Z = \frac{J\rho}{I}$$

The ac resistance is given by the real part of Z. Thus at the inner surface of the outer conductor,

$$R_{ac} = \mathrm{Re}\left[j\frac{f\mu}{b_0}\left(\frac{I_0(b_0)K_1(a_0)+I_1(a_0)K_0(b_0)}{I_1(a_0)K_1(b_0)-I_1(b_0)K_1(a_0)} \right) \right] \qquad \text{(EA1-16)}$$

For the inner conductor the following boundary conditions are used:

- The magnetic field on the inside of the conductor is zero because the enclosed current is zero
- The magnetic field on the outside surface of the conductor is tangential.

In a similar way as deriving (EA1-17) we find that the ac resistance on the outside surface of the inner conductor is given by

$$R_{ac} = \mathrm{Re}\left[j\frac{f\mu}{a_0}\left(\frac{I_0(a_0)K_1(b_0)+I_1(b_0)K_0(a_0)}{I_1(a_0)K_1(b_0)-I_1(b_0)K_1(a_0)} \right) \right] \qquad \text{(EA1-17)}$$

Appendix C

VHDL CODE

```
--------------------------------------------------------------------------------------------------------

--   Auther:       P.D. van Rhyn
--   Date:         07/11/2005
--   Descripion :  This program generates interleaved gate signals for a two module, full-bridge
--                 topology, series stacked converter. Phase shift control is used as switching
--                 stratagy for each module in the stack.

--   Switch configuration
--   ------------
--        |        |
--        A1       B1
--        |        |        Converter 1
--        B2       A2
--        |        |
--        --------
--        |        |
--        A11      B11
--        |        |        Converter 2
--        B21      A21
--        |        |
--   ------------

--------------------------------------------------------------------------------------------------------

library ieee ;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

entity pwm is

port(    clock                  : in std_logic;          -- 30Mhz Clock
         PWM_A1_IN, PWM_B1_IN   : in std_logic;            -- 2 inputs from controller
                                                          -- Phase shifted by 180 degrees
         PWM_A1_OUT,PWM_B1_OUT, PWM_A2_OUT, PWM_B2_OUT       : out std_logic ; -- Outputs for
                                                                                 -- converter 1
         PWM_A11_OUT, PWM_B11_OUT, PWM_A21_OUT, PWM_B21_OUT    : out std_logic); -- Outputs for
                                                                                 -- converter 2
end pwm;

--------------------------------------------------------------------------------------------------------

architecture behv of pwm is

    signal A1_not, B1_not  : std_logic;
    signal no_pwm          : std_logic;

    type state_type2 is (ABwait, Acount, Bcount );
    signal duty       : state_type2;

    type state_type3 is (delay_on, delay_off );
    signal delay  : state_type3;
    signal delay1 : state_type3;

    type state_type is (wait_sig, del_S0, S0, del_S1, S1, del_S2, S2, del_S3, S3);
    signal state  : state_type;

    signal delay_enable    : std_logic;
    signal delay_done          : std_logic;

    signal PWM_A1_OUT_int, PWM_B1_OUT_int, PWM_A2_OUT_int, PWM_B2_OUT_int : std_logic;

    signal current_pulse_width     : integer range 0 to 511;

    type state_type1 is (SS0, SS1, SS2);
    signal A1_new_state    : state_type1;
    signal B1_new_state    : state_type1;
    signal A11, B11        : std_logic;
```

```
    signal state1              : state_type;
    signal delay_enable1   : std_logic;
    signal delay_done1         : std_logic;

    signal PWM_A11_OUT_int, PWM_B11_OUT_int, PWM_A21_OUT_int, PWM_B21_OUT_int :std_logic;

    type state_type4 is (noPWM, PWM);
    signal outstate : state_type4;

    type state_type5 is (Alow, Ahigh);
    signal A : state_type5;
    type state_type6 is (Blow, Bhigh);
    signal B : state_type6;

-------------------------------------------------------------------------------------------------------

BEGIN

-- In process CheckNoPWM signal no_pwm is checked. If an error condition occurred, no_pwm will have
-- been set to 1 and process SetOutputs will set all the outputs to 0.

CheckNoPWM:
process (clock)
    Begin
        if clock'event and clock = '1' then
            case outstate is
                when PWM =>
                    if no_pwm <= '1' then
                        outstate <= noPWM;
                    end if;
                when noPWM =>
                    if no_pwm <= '0' then
                        outstate <= PWM;
                end if;
            end case;
        end if;
    end process;

SetOutputs:
process (outstate)
    Begin
        case outstate is
            when PWM =>
                PWM_A1_OUT <= PWM_A1_OUT_int;
                PWM_B1_OUT <= PWM_B1_OUT_int;
                PWM_A2_OUT <= PWM_A2_OUT_int;
                PWM_B2_OUT <= PWM_B2_OUT_int;
                PWM_A11_OUT <= PWM_A11_OUT_int;
                PWM_B11_OUT <= PWM_B11_OUT_int;
                PWM_A21_OUT <= PWM_A21_OUT_int;
                PWM_B21_OUT <= PWM_B21_OUT_int;
            when noPWM =>
                PWM_A1_OUT <= '0';
                PWM_B1_OUT <= '0';
                PWM_A2_OUT <= '0';
                PWM_B2_OUT <= '0';
                PWM_A11_OUT <= '0';
                PWM_B11_OUT <= '0';
                PWM_A21_OUT <= '0';
                PWM_B21_OUT <= '0';
        end case;
    end process;

-------------------------------------------------------------------------------------------------------

-- Processes LatchA and LatchB are used to latch signals A and B coming from the controller

LatchA:
process (clock)
    Begin
        if clock'event and clock = '1' then
            case A is
                when Alow =>
                    if PWM_A1_IN = '1' then
                        A <= Ahigh;
                    end if;
                when Ahigh =>
                    if PWM_A1_IN = '0' then
                        A <= Alow;
                    end if;
```

```
            end case;
        end if;
    end process;

process (A)
    Begin
        case A is
            when Alow => A1_not <= '0';
            when Ahigh => A1_not <= '1';
        end case;
    end process;

LatchB:
process (clock)
    Begin
        if clock'event and clock = '1' then
            case B is
                when Blow =>
                    if PWM_B1_IN = '1' then
                        B <= Bhigh;
                    end if;
                when Bhigh =>
                    if PWM_B1_IN = '0' then
                        B <= Blow;
                    end if;
            end case;
        end if;
    end process;

process (B)
    Begin
        case B is
            when Blow => B1_not <= '0';
            when Bhigh => B1_not <= '1';
        end case;
    end process;
-------------------------------------------------------------------------------------------------

-- Process Findstate is used to find the current state of input signals A and B

Findstate:
process (clock)

    variable count    : integer range 0 to 511;

    begin
        if clock'event and clock = '1' then
            case state is
                when wait_sig =>
                    if A1_not = '1' then
                        state <= del_S0;
                        count := 0;
                    end if;
                when del_S0 =>
                        count := count + 1;
                        if count >= 7 then
                            state <= S0;
                        end if;
                when S0 =>
                    if A1_not = '0' then
                        state <= del_S1;
                        count := 0;
                    end if;
                when del_S1 =>
                    count := count + 1;
                        if count >= 7 then
                            state <= S1;
                        end if;
                when S1 =>
                    if B1_not = '1' then
                        state <= del_S2;
                        count := 0;
                    end if;
                when del_S2 =>
                    count := count + 1;
                        if count >= 7 then
                            state <= S2;
                        end if;
                when S2 =>
                    if B1_not = '0' then
```

```
                        state <= del_S3;
                        count := 0;
                    end if;
                when del_S3 =>
                    count := count + 1;
                        if count >= 7 then
                            state <= S3;
                        end if;
                when S3 =>
                    if A1_not = '1' then
                        state <= del_S0;
                        count := 0;
                    end if;
            end case;
        end if;
end process;

-------------------------------------------------------------------------------------------------

-- Process Setouts sets the outputs for converter 1 according to the state determined in process
-- Findstate

Setouts:
process (state)
    begin
        case state is
            when wait_sig => PWM_A1_OUT_int <= '0'; PWM_A2_OUT_int <= '0';
                             PWM_B1_OUT_int <= '0'; PWM_B2_OUT_int <= '0';

            when del_S0 =>    PWM_A1_OUT_int <= '0'; PWM_A2_OUT_int <= '1';
                              PWM_B1_OUT_int <= '0'; PWM_B2_OUT_int <= '0';

            when S0 =>    PWM_A1_OUT_int <= '1'; PWM_A2_OUT_int <= '1';
                          PWM_B1_OUT_int <= '0'; PWM_B2_OUT_int <= '0';

            when del_S1 =>    PWM_A1_OUT_int <= '1'; PWM_A2_OUT_int <= '0';
                              PWM_B1_OUT_int <= '0'; PWM_B2_OUT_int <= '0';

            when S1 =>    PWM_A1_OUT_int <= '1'; PWM_A2_OUT_int <= '0';
                          PWM_B1_OUT_int <= '1'; PWM_B2_OUT_int <= '0';

            when del_S2 =>    PWM_A1_OUT_int <= '0'; PWM_A2_OUT_int <= '0';
                              PWM_B1_OUT_int <= '1'; PWM_B2_OUT_int <= '0';

            when S2 =>  PWM_A1_OUT_int <= '0'; PWM_A2_OUT_int <= '0';
                        PWM_B1_OUT_int <= '1'; PWM_B2_OUT_int <= '1';

            when del_S3 =>    PWM_A1_OUT_int <= '0'; PWM_A2_OUT_int <= '0';
                              PWM_B1_OUT_int <= '0'; PWM_B2_OUT_int <= '1';

            when S3 =>    PWM_A1_OUT_int <= '0'; PWM_A2_OUT_int <= '1';
                          PWM_B1_OUT_int <= '0'; PWM_B2_OUT_int <= '1';

        end case;
end process;

-------------------------------------------------------------------------------------------------

-- Process Pulsewidth is used to calculate the current pulse width of inputs A and B

Pulsewidth:
process (clock)

    variable temp_pulse_width : integer range 0 to 511;
    variable new_value_ready, A1_pulse, B1_pulse  : integer range 0 to 1;

    begin
        if clock'event and clock = '1' then

            case duty is

                when ABwait =>

                    if A1_not = '1' then
                        duty <= Acount;
                    elsif B1_not = '1' then
                        duty <= Bcount;
                    else
                        temp_pulse_width := 0;
                    end if;
```

```
                when Acount =>

                        if A1_not = '1' then
                            temp_pulse_width := temp_pulse_width + 1;
                        elsif A1_not = '0' then
                            if temp_pulse_width <= 20 then
                                no_pwm <= '1';
                                current_pulse_width <= 0;
                                temp_pulse_width := 0;
                                duty <= ABwait;
                            else
                                no_pwm <= '0';
                                current_pulse_width <= temp_pulse_width;
                                duty <= ABwait;
                                temp_pulse_width := 0;
                            end if;
                        end if;

                when Bcount =>
                        if B1_not = '1' then
                            temp_pulse_width := temp_pulse_width + 1;
                        elsif B1_not = '0' then
                            if temp_pulse_width <= 20 then
                                no_pwm <= '1';
                                current_pulse_width <= 0;
                                temp_pulse_width := 0;
                                duty <= ABwait;
                            else
                                no_pwm <= '0';
                                current_pulse_width <= temp_pulse_width;
                                duty <= ABwait;
                                temp_pulse_width := 0;
                            end if;
                        end if;
                end case;
        end if;
    end process;

-------------------------------------------------------------------------------------------------------

-- Process NewA is used to generate a new "A" signal which is phase shifted by 90 degrees with
-- respect to signal A.

NewA:
process (clock)

    variable count    : integer range 0 to 511;
    variable temp : integer range 0 to 511;

    begin
        if clock'event and clock = '1' then
            case A1_new_state is
                when SS0 =>
                        if A1_not = '1' then
                            temp := current_pulse_width;
                            A1_new_state <= SS1;
                        end if;
                when SS1 =>
                    count := count + 1;
                        if count >= 140 then
                            count := 0;
                            A1_new_state <= SS2;
                        end if;
                when SS2 =>
                    count := count + 1;
                        if (count >= temp) then
                            count := 0;
                            A1_new_state <= SS0;
                        end if;
            end case;
        end if;
    end process;

process (A1_new_state)
    begin
        case A1_new_state is
            when SS0 => A11   <= '0';
            when SS1 => A11   <= '0';
            when SS2 => A11   <= '1';
```

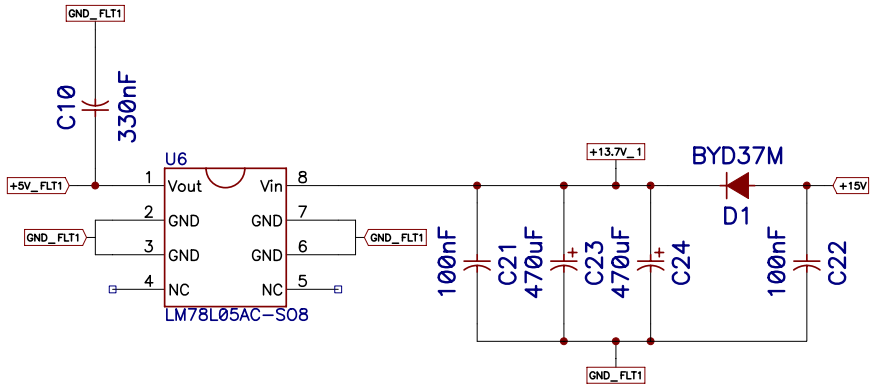
```
          end case;
     end process;

-------------------------------------------------------------------------------------------------------

-- Process NewB is used to generate a new "B" signal which is phase shifted by 90 degrees with
-- respect to signal B.

NewB:
process (clock)

     variable count    : integer range 0 to 511;
     variable temp : integer range 0 to 511;

     begin
          if clock'event and clock = '1' then
               case B1_new_state is
                    when SS0 =>
                              if B1_not = '1' then
                                   temp := current_pulse_width;
                                   B1_new_state <= SS1;
                              end if;
                    when SS1 =>
                         count := count + 1;
                              if count >= 140 then
                                   count := 0;
                                   B1_new_state <= SS2;
                              end if;
                    when SS2 =>
                         count := count + 1;
                              if (count >= temp) then
                                   count := 0;
                                   B1_new_state <= SS0;
                              end if;
               end case;
          end if;
     end process;

process (B1_new_state)
     begin
          case B1_new_state is
               when SS0 => B11   <= '0';
               when SS1 => B11   <= '0';
               when SS2 => B11   <= '1';
          end case;
     end process;

-------------------------------------------------------------------------------------------------------

Findstate1:
process (clock)

     variable count    : integer range 0 to 511;

     begin
          if clock'event and clock = '1' then
               case state1 is
                    when wait_sig =>
                         if A11 = '1' then
                              state1 <= del_S0;
                              count := 0;
                         end if;
                    when del_S0 =>
                              count := count + 1;
                              if count >= 7 then
                                   state1 <= S0;
                              end if;
                    when S0 =>
                         if A11 = '0' then
                              state1 <= del_S1;
                              count := 0;
                         end if;
                    when del_S1 =>
                         count := count + 1;
                              if count >= 7 then
                                   state1 <= S1;
                              end if;
                    when S1 =>
                         if B11 = '1' then
                              state1 <= del_S2;
```

```
                        count := 0;
                    end if;
                when del_S2 =>
                    count := count + 1;
                        if count >= 7 then
                            state1 <= S2;
                        end if;
                when S2 =>
                    if B11 = '0' then
                        state1 <= del_S3;
                        count := 0;
                    end if;
                when del_S3 =>
                    count := count + 1;
                        if count >= 7 then
                            state1 <= S3;
                        end if;
                when S3 =>
                    if A11 = '1' then
                        state1 <= del_S0;
                        count := 0;
                    end if;
            end case;
        end if;
end process;

-------------------------------------------------------------------------------------------------------

-- Process Setouts1 sets the outputs for converter 2 according to the state determined in process
-- Findstate

Setouts1:
process (state1)
    begin
        case state1 is
            when wait_sig => PWM_A11_OUT_int <= '0'; PWM_A21_OUT_int <= '0';
                             PWM_B11_OUT_int <= '0'; PWM_B21_OUT_int <= '0';

            when del_S0 =>    PWM_A11_OUT_int <= '0'; PWM_A21_OUT_int <= '1';
                              PWM_B11_OUT_int <= '0'; PWM_B21_OUT_int <= '0';

            when S0 =>    PWM_A11_OUT_int <= '1'; PWM_A21_OUT_int <= '1';
                          PWM_B11_OUT_int <= '0'; PWM_B21_OUT_int <= '0';

            when del_S1 =>    PWM_A11_OUT_int <= '1'; PWM_A21_OUT_int <= '0';
                              PWM_B11_OUT_int <= '0'; PWM_B21_OUT_int <= '0';

            when S1 =>    PWM_A11_OUT_int <= '1'; PWM_A21_OUT_int <= '0';
                          PWM_B11_OUT_int <= '1'; PWM_B21_OUT_int <= '0';

            when del_S2 =>    PWM_A11_OUT_int <= '0'; PWM_A21_OUT_int <= '0';
                              PWM_B11_OUT_int <= '1'; PWM_B21_OUT_int <= '0';

            when S2 =>  PWM_A11_OUT_int <= '0'; PWM_A21_OUT_int <= '0';
                          PWM_B11_OUT_int <= '1'; PWM_B21_OUT_int <= '1';

            when del_S3 =>    PWM_A11_OUT_int <= '0'; PWM_A21_OUT_int <= '0';
                              PWM_B11_OUT_int <= '0'; PWM_B21_OUT_int <= '1';

            when S3 =>    PWM_A11_OUT_int <= '0'; PWM_A21_OUT_int <= '1';
                          PWM_B11_OUT_int <= '0'; PWM_B21_OUT_int <= '1';
        end case;
    end process statechangel;

END behv;

-------------------------------------------------------------------------------------------------------
```

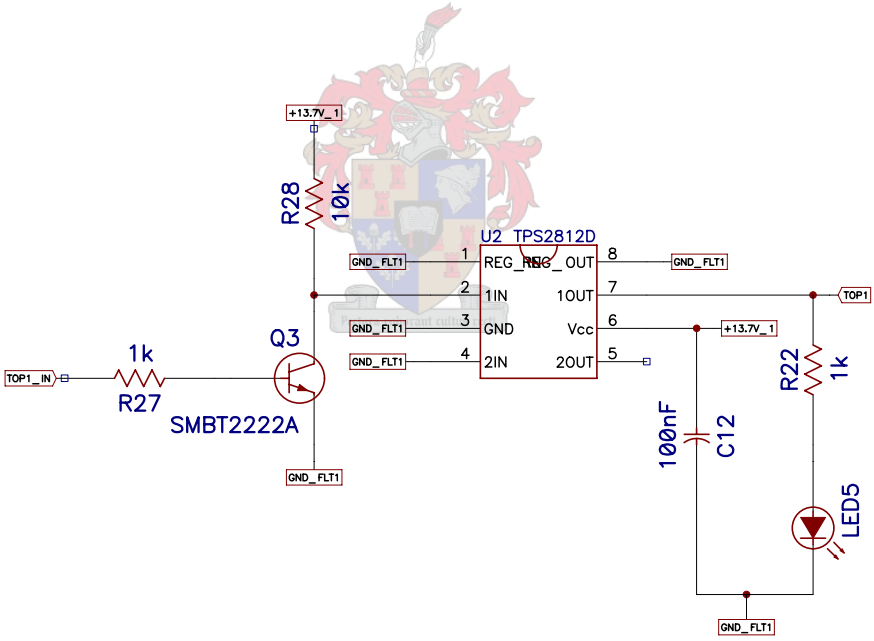
Appendix D

PCB SCHEMATICS

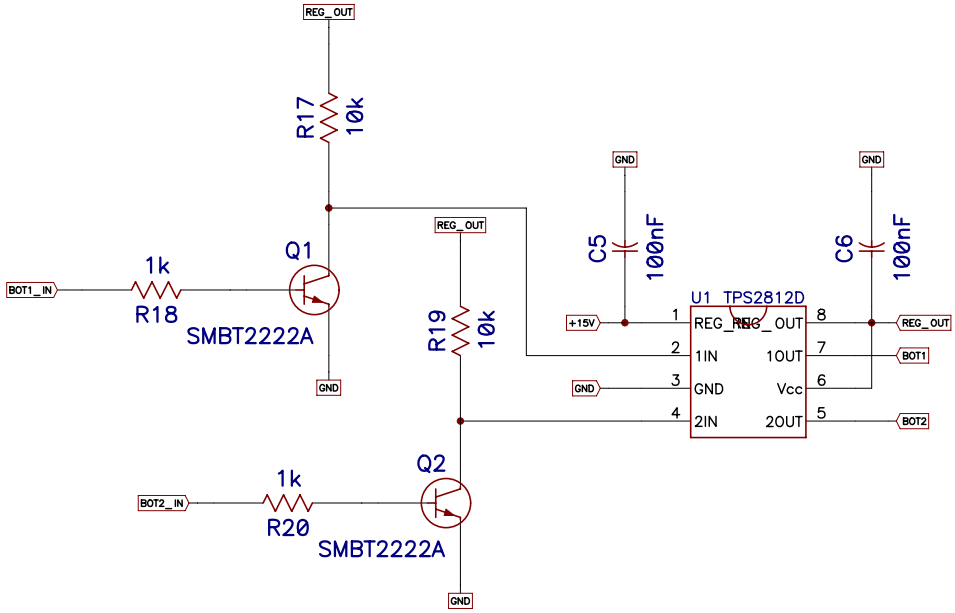
Bootstrap Supply



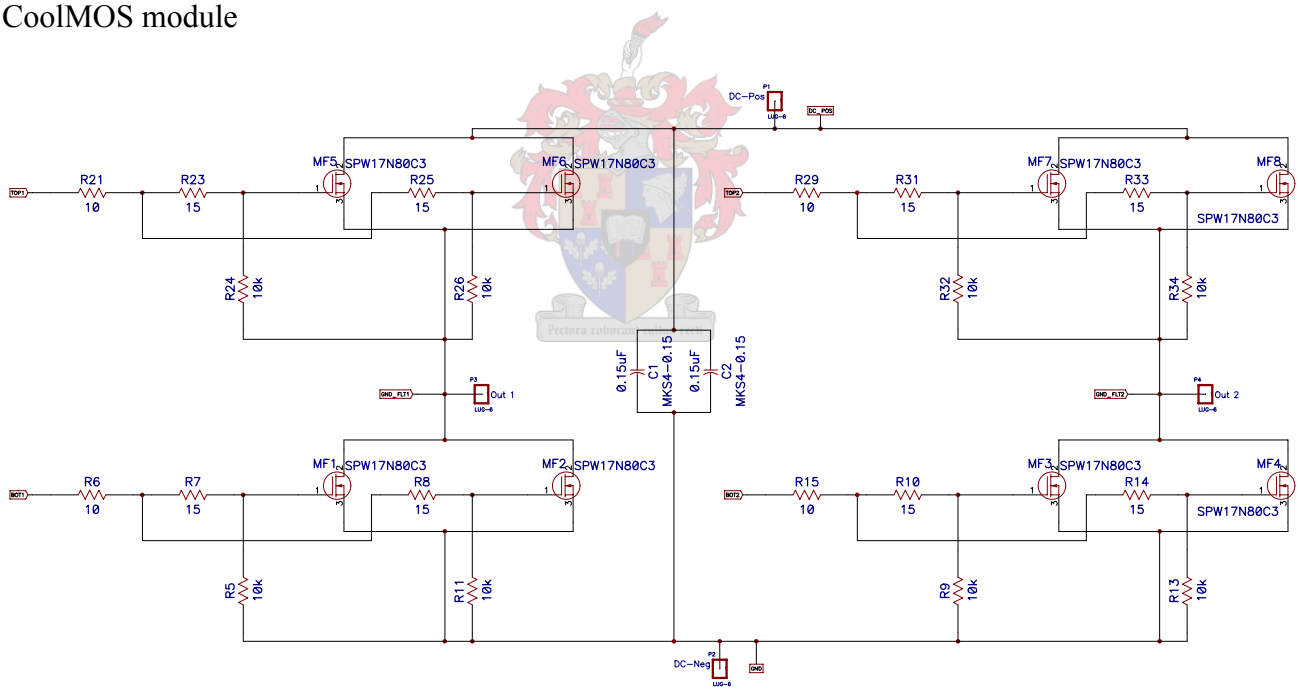
Top Driver



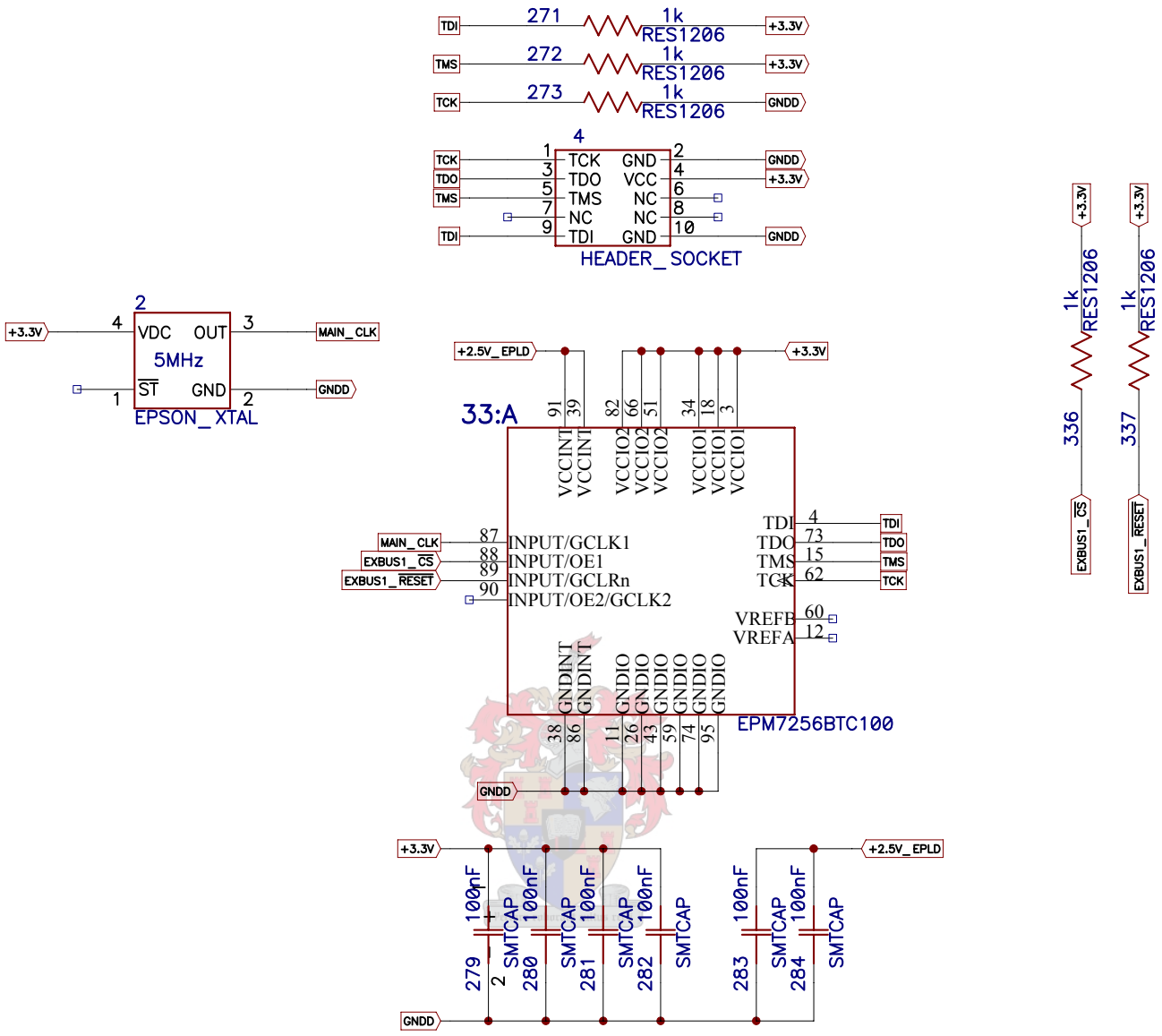
Bottom Driver



CoolMOS module



Controller board. (EPLD main)



Controller board (EPLD I/Os)