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High Voltage Gain DC/DC Converter Using Coupled Inductor and VM Techniques

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ABSTRACT In this study, a new non-isolated high voltage gains dc/dc converter using coupled inductor and voltage multiplier techniques (diode/capacitor) is presented. The voltage gain will be increased by increasing the turns ratio (N) and the number of stages of the VM units. The proposed converter capable to more increase the output voltage gains with transfer energy which is stored in coupled inductance. Also, the voltage multiplier unit causes to further increase in the output voltage level of the proposed converter. Besides, the nominal value of the semiconductors is low due to these are clamped to the capacitors available on the voltage multiplier units. The normalized voltage stress across the semiconductors is low which this case is compared in the comparison section. Therefore, the power loss of switch can be reduced by using a switch with a lower rating (lower $R_{DS(on)}$) and power diodes with the low nominal rating. As a result, the overall efficiency of the proposed converter will be high. To confirm the benefits of working in this paper, comparison results for different items with other works are provided in section 4. The principle of operation, the theoretical analysis and the experimental results of a laboratory prototype for $N(N2/N1) = 2$ and $n = 2$ stage in about 260W with operating at 40kHz are provided.

INDEX TERMS DC/DC converter, high voltage gain, coupled-inductor techniques, lower losses.

I. INTRODUCTION

Recently, the deficiency of fossil fuels and environmental problems due to global warming causes to increase the utilization of green sources. However, the output voltage level of the green sources (PV panel, fuel cell, etc.) is not large which is the basic issue of the green sources. Generally, to improve the efficiency of the system include green sources should be utilized proper power converters dc-dc-ac. Consequently, dc-dc converters with high voltage conversion ratio and high efficiency need to increase the voltage level of the green sources and overall efficiency of the system. Also, dc-dc power convertors used in green sources require to design in terms of voltage gain, maximum voltage/current stress on semiconductors (MOSFET/diode), input current ripple, overall efficiency and output voltage ripple [1], [2].

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Dc-dc boost converters that cannot produce high voltage gain and high efficiencies such as conventional boost converter due to high power losses in high power level and limits on increasing duty cycle value [3]. To increase the output voltage level, conventional boost converter should increase the duty cycle value and this causes to more increase the reverse recovery issue of the diode in the output side, impressively. Besides, it also limits the voltage gain and increases the normalized voltage stress on semiconductors, so conventional boost converters are not proper for high power ranges [4]. As a result, the overall efficiency will be decreased and also electromagnetic interference (EMI) will be a big problem [5]. To obtain a high voltage level at the output side of dc-dc converters with high efficiency and high power level, more methods are proposed by researchers. Generally, high voltage gain dc-dc converters can include as 1) using coupled inductor techniques, 2) using voltage multipliers (VM) techniques such as diode/capacitor, diode/capacitor/inductor,

diode/capacitor/coupled inductor and 3) combination of interleaving techniques with VM cells and coupled inductors [2], [6]. Generally, it can be said that the coupled inductor techniques can play roles of a transformer in non-isolated high voltage gain converters. The voltage gains of these converters are more increased by adding the VM units and selecting an appropriate amount for the turn's ratio of the coupled inductor. Also, the detection of the leakage energy of the coupled inductor leads to increases efficiency. In addition, using the VM cells in dc-dc converters consisting of coupled inductor causes to decrease the nominal value used power semiconductors (by clamping the power semiconductors to the VM capacitors) [7], [8]. These converters have a high voltage gain and it is more increases using inductors/transformers techniques. Consequently, it can be said that more converters are needed a complex VM cell or combination of diode/capacitor/inductor/coupled inductor is provided with a large voltage level in the output side which can be a major drawback for the converter. Combining both the coupled inductor techniques and VM units can be provided a high voltage level at the output side and raise the efficiency [9], [6]. Generally, these converters have a large voltage conversion ratio with large efficiency, small maximum voltage across power semiconductors (switch/diode), and low switching losses in high power. The recovery of the output power diode is one of the important drawbacks for these converters which this issue can be improved through leakage inductance for converters including coupled inductor techniques. Using diode/switch/capacitor techniques in some dc-dc high gain converters can be produced a suitable ultra-high voltage gain converter lower normalized voltages stress on semiconductors (switches and diodes). The converters from this category that have a low current ripple percent at the input side and high efficiency can be decreased the EMI problems. Also, these converters can be a good candidate for renewable applications. The important worriment of these converters is large maximum voltage on output power diode [5], [10]. Therefore, converters using interleaving techniques with the lower value of magnetic, low volume and small current ripple percent at the input side can be a good candidate for large power ranges. The voltage converter will more increase in high duty cycle values, but the converter will be limitations in practical built such as voltage/current ripple across MOSFETs, maximum voltage on MOSFETs, power losses of switching and reverse recovery of power diode at the output side [11].

In this study, a new high voltage gains dc-dc converter using coupled inductor techniques is presented. The voltage level at the output side will rise by adding the number of VM stages and turns ratio value. Also, the semiconductors are clamped by the VM cells, in facts, VM units cause to limit the normalized voltage stress on semiconductors (MOSFET/diode). Since the proposed structure has one switch, so this makes simple to control the operation of the converter, the operation of the presented converter in fifth modes at CCM operation (continuous conduction mode) and DCM operation (discontinuous conduction mode) is provided. Also, the experimental results of the proposed converter at 260W are provided in section 6 which includes output voltage, maximum voltage on semiconductors (MOSFETs/diodes) and current of the inductors.

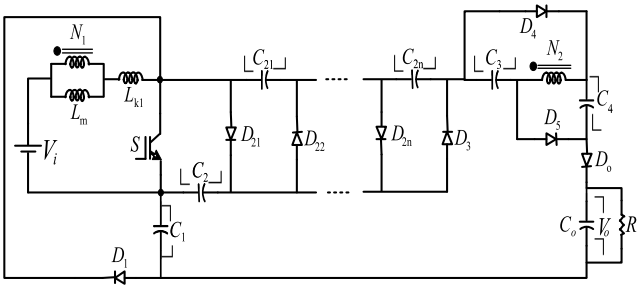

FIGURE 1. Circuit schematic of the proposed topology.

II. PROPOSED TOPOLOGY AND ANALYSIS OF THE OPERATION MODES

Fig. 1 illustrates the circuit schematic of the proposed topology. The proposed converter used a coupled inductor with the primary and secondary turns of N_1 and N_2, respectively to achieve high voltage gain. Also, the voltage gain of the proposed converter can go up with adding the number of VM units (diode/capacitor). Also, adding the number of stages leads to a decrease in the normalized voltage stress on semiconductors. Adding VM units and increasing the value of turns ratio ($N = N_2/N_1$) leads to more rise in the voltage gains and decrease the normalized voltage stress on MOSFET/diode. In power circuit, S is the main power MOSFET, D_1, D_2, D_3, D_4 and D_5 are the power diodes, $C_1, C_{21}, \ldots, C_{2n}$ are the capacitors of the voltage multiplier circuit, also C_3 and C_4 are the capacitors of the voltage multiplier unit (diode/capacitor/inductor) which are used at the proposed converter. C_o is the output capacitor. The stored energy of the coupled inductor at the first and second side is forwarded to the capacitors in parallel state and finally, the stored energy is transferred to the output capacitor by series capacitors. Therefore, using lower rating power MOSFET and diodes causes to decrease the overall cost and increase the efficiency of the proposed converter. For simplicity of theoretical calculation of the proposed topology, some assumptions are considered as:

- The input voltage source has a constant value and without a ripple,
- All power components are ideal,
- The voltage of all capacitors has a constant value in one switching period (all capacitors are large enough).

A. CCM OPERATION

Generally, the two-time interval for power MOSFET is considered at one period of the proposed converter (T_S). At the first time interval (DT_S), Switch S is on-state which consists of two modes. In the second time interval ((1-D) TS), power MOSFET is off-state which consists of three modes.

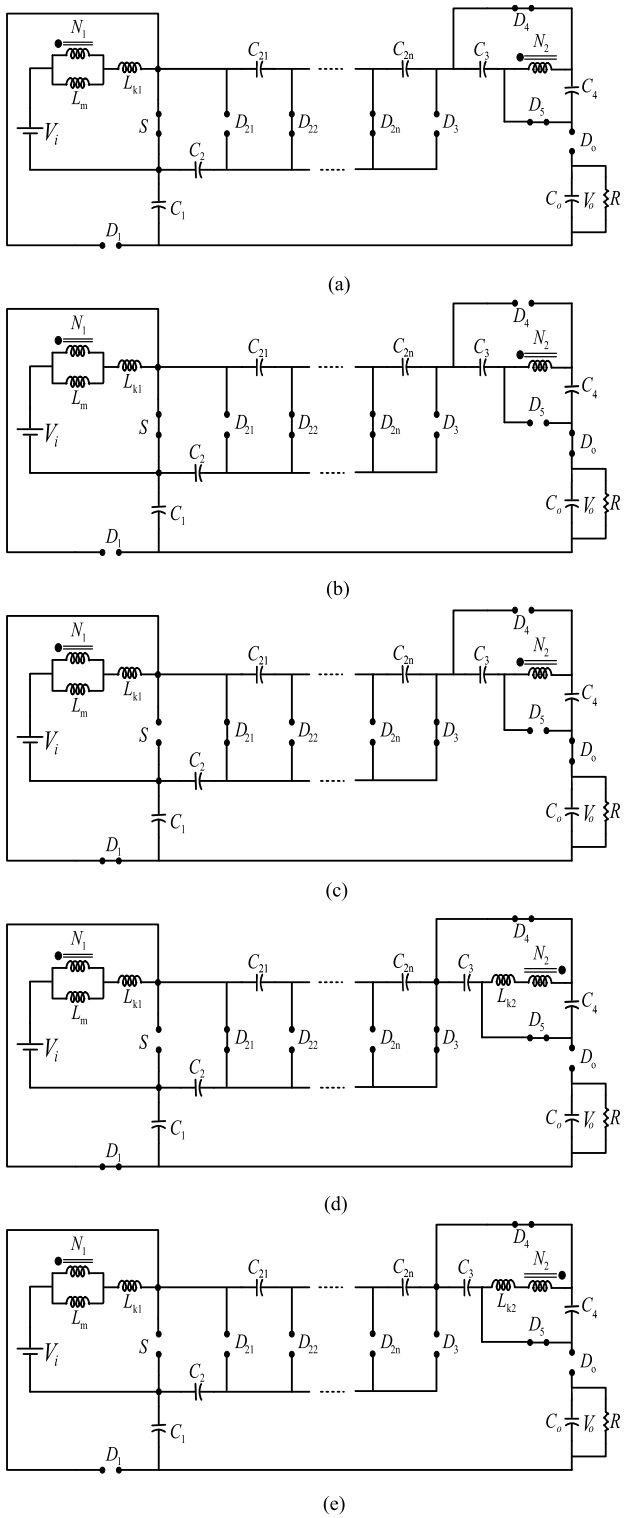

FIGURE 2. The equivalent circuit of the proposed converter at CCM operation, (a) mode 1, (b) mode 2, (c) mode 3, (d) mode 4, (e) mode 5.

For theoretical analysis, the coupled inductor is considered as magnetizing inductor Lm, primary leakage inductor Lk1, secondary leakage inductor Lk2, and an ideal transformer. Fig. 2 illustrates the operation modes of the proposed converter in CCM operation. In the CCM operation, the proposed converter operating is provided as:

Mode 1 [$t_0 \le t \le t_1$]: In this mode, the power switch S is turned on and all power diodes are in reverse biased condition except the diodes $D_{22}, \ldots, D_{2n}, D_4$ and D_5. The capacitor C_1 is charged through the input power supply and magnetizing inductor L_m. The current of magnetic inductor is linearly decreased

The energy of the magnetizing inductor discharges to the secondary side and finally, this energy is discharged to the capacitors C_3 and C_4. The current of the diodes is linearly decreased and they will be taken in reverse biased at the end of this mode. The secondary leakage inductor current is decreased based on the turns ratio value (i_{Lm}/N). Also, the output load is supplied through the stored energy of the output capacitor C_o. Based on Fig. 2(a), can be written as follows equations:

$$v_{Lm} = L_m \frac{di_{Lm}}{dt} \tag{1}$$

$$v_{Lk1} = V_i - v_{Lm} = L_{k1} \frac{di_{Lk1}}{dt} \tag{2}$$

$$i_{Lm} - i_{Lk1} = N i_{Lk2} \tag{3}$$

$$\begin{cases} V_{C21} = V_{C1} \\ V_{C22} = V_{C23} \\ V_{C24} = V_{C25} \\ \vdots \\ V_{C2(n-2)} = V_{C2(n-1)} \end{cases} \tag{4}$$

$$V_{C3} = V_{C4} \tag{5}$$

Mode 2 [$t_1 \le t \le t_2$]: In this mode, the power switch S remains in ON state and all diodes remain in their previous state except diodes D_4, D_5 and D_o. The magnetizing inductor $L_{\rm m}$ and the primary leakage inductance $L_{\rm k1}$ are charged by the input power supply (V_i). Therefore, the current of these inductors is linearly increased. By observing Fig. 2(b), it is clear that the output load R is supplied by input DC source and capacitors $C_{21}, C_{23}, \ldots, C_{2(n-1)}, C_{2n}$. The equations in this mode can be written as (6)–(10), as shown at the bottom of the next page.

Mode3 [$t_2 \le t \le t_3$]: In this mode, the power switch S is turned off. Power diodes $D_{21}, D_{23}, \ldots, D_{2(n-1)}, D_1, D_3$ and D_o are in forward biased condition, and other power diodes are in reverse biased condition. The stored energy in primary leakage inductance is transferred to the capacitors C_1 and C_2. The stored energy in the secondary leakage inductance is transferred to the output capacitor. Therefore, the current of the primary and secondary leakage inductance is linearly decreased. The current of secondary leakage inductance will change quickly and reach zero at the end of this mode. The magnetizing inductor also charging through the input power supply and also receives energy from secondary leakage inductance. Then, the current of the magnetizing inductor is linearly increased. In this mode, the following equations can be written as:

$$i_{Lm} = i_{Lk1} - N i_{Lk2} \tag{11}$$

$$\frac{di_{Lk1}}{dt} = \frac{V_i - V_{C1} - v_{Lm}}{L_{k1}} \tag{12}$$

$$\begin{cases} V_{C21} = V_{C23} \\ V_{C24} = V_{C25} \\ \vdots \\ V_{C2(n-1)} = V_{C2n} \end{cases} \tag{13}$$

$$\frac{di_{Lk2}}{dt} = \frac{V_{C3} + V_{C4} + (V_{C21} + \ldots + V_{C2n}) + Nv_{Lm} - V_o}{L_{k2}} \tag{14}$$

$$i_{Lk1} = i_{D21} - i_{D1} \tag{15}$$

Mode 4 [$t_3 \le t \le t_4$]: In this mode, the power switch S remains in the OFF state. Power diodes $D_1, D_{21}, \ldots, D_{2(n-1)}$, D_3, D_4 and D_5 are in forward biased condition and other diodes are in reverse biased condition. The stored energy in the magnetizing inductor charges the capacitors C_1 and C_2. The current of primary leakage inductance and current of the magnetizing inductor (i_{Lm}) is linearly decreased. The current of primary leakage inductance (i_{Lk1}) with changes rapidly will reach zero at the end of this mode. Also, the secondary leakage inductance L_{k2} will be recharged in the reverse direction. The stored energy in the capacitor Co is discharged to the output load R. For this mode, the following equations can be obtained as:

$$\frac{di_{Lk2}}{dt} = \frac{Nv_{Lm} + V_{C4}}{L_{k2}} = 2\frac{di_{D5}}{dt} \tag{16}$$

$$\frac{di_{Lk2}}{dt} = \frac{Nv_{Lm} + V_{C3}}{L_{k2}} = 2\frac{di_{D4}}{dt} \tag{17}$$

Mode 5 [$t_4 \le t \le t_5$]: In this mode, the power switch S remains in OFF state and all diodes are in reverse biased condition except the diodes D_4 and D_5. The stored energy in magnetizing inductor L_m is discharged to the capacitors C_3 and C_4 through the secondary winding. The current of the magnetizing inductor is linearly decreased. The current of the primary leakage inductance is zero during this mode. Also, the current of the secondary leakage inductance in linearly increased, however, its current will be negative. The stored energy in the capacitor C_o is discharged to the output load R. By observing Fig. 2(e), can be written as follows equations:

$$v_{Lm} = L_m \frac{di_{Lm}}{dt} \tag{18}$$

$$i_{Lk1} = 0 \tag{19}$$

$$\frac{di_{Lk2}}{dt} = \frac{Nv_{Lm} + V_{C4}}{L_{k2}} = 2\frac{di_{D5}}{dt} \tag{20}$$

$$\frac{di_{Lk2}}{dt} = \frac{Nv_{Lm} + V_{C3}}{L_{k2}} = 2\frac{di_{D4}}{dt} \tag{21}$$

In theoretical analysis of CCM operation, the secondary leakage inductance L_{k2} of the coupled inductor is transferred to its primary side (L'_{k2}). The equivalent primary leakage inductance is considered L_k which is equal to the sum of the primary leakage inductance L_{k1} and L'_{k2}. For simplicity analysis of CCM operation of the proposed converter can be ignored modes first and third due to the time duration of these modes are very short. Thus, only modes second, fourth and fifth are considered for CCM operation. If the current ripple of the magnetizing inductor is considered zero, the relationship between the clamp capacitors and discharge current of the proposed topology can be obtained as Fig. 3(b). In fact, by ignoring modes first and third, t_C is the fourth time duration mode and D_cT_s are considered equal to t_C so that D_c is its corresponding duty cycle.

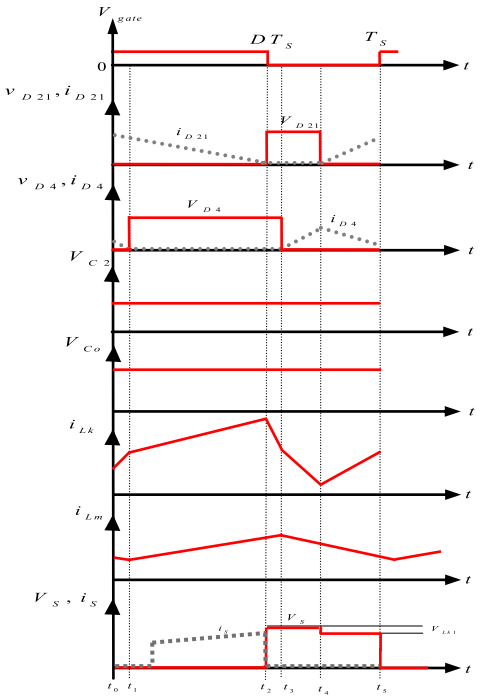

FIGURE 3. Key waveforms at CCM operation.

The stored energy in the total primary leakage inductance L_k at the during time t_C is discharged into the clamp capacitors C_1 and C_2. Based on current-second law, the average

$$i_{Lm} = i_{Lk1} - Ni_{Lk2} \tag{6}$$

$$i_i = i_{Lk1} = i_{Lm} + Ni_{Lk2} \tag{7}$$

$$i_i = i_{DS} + i_{C2} + Ni_{Lk2} \tag{8}$$

$$\frac{di_{Lk2}}{dt} = \frac{di_{Do}}{dt} = \frac{V_{C21} + V_{C23} + \ldots + V_{C2(n-1)} + V_{C2n} + V_{C3} + V_{C4} + V_i - V_{Co}}{L_{k2}} \tag{9}$$

$$V_{C1} = V_{C2} \tag{10}$$

capacitor currents (I_{Cap}) are zero in one period switching, then it is clear that the average currents of the diodes $D_1, D_{21}, D_{22}, \ldots, D_{2n}, D_4$ and D_5 are equal to the average current of the output diode (I_{Do}). Also, the average current of the output diode is equal to the output current (I_o). By considering the charge energy equal to the discharge energy, can be written as follows equations:

$$L_{k2} = L_{k1} + L'_{k2} = L_{k1} + N^2 L_{k2} \tag{22}$$

$$\begin{aligned} I_{D1} &= I_{D21} = I_{D22} = \ldots = I_{D2n} = I_{D3} \\ &= I_{D4} = I_{D5} = I_{Do} = I_o \end{aligned} \tag{23}$$

$$\frac{D_C \times T_s \times I_{Lm}}{2T_s} = \frac{(1-D)T_s + (1-D-D_C)T_s}{2T_s} \times \frac{I_{Lm}}{n} \tag{24}$$

$$D_C = \frac{2(1-D)}{1+n} \tag{25}$$

The coupling coefficient of the coupled inductor K is equal to $L_m/(L_m + L_k)$. Based on mode 2 in Fig. 2, can be written as follows equations:

$$v_{Lm} = \frac{L_m}{L_m + L_k} V_i = KV_i \tag{26}$$

$$v_{Lk} = \frac{L_k}{L_m + L_k} V_i = (1-K)V_i \tag{27}$$

$$v_{N2} = N v_{Lm} = NKV_i \tag{28}$$

$$V_i = v_{Lm} + v_{Lk1} = L_m \frac{di_{Lm}}{dt} + L_{k1} \frac{di_{Lk1}}{dt} \tag{29}$$

$$\begin{cases} V_{Co} = V_{C21} + V_{C23} + \ldots + V_{C2(n-1)} \\ \quad + V_{C2n} + V_{C3} + V_{C4} + V_i + V_{C1} \\ \quad - v_{N2} - v_{Lm} - v_{Lk} \end{cases} \tag{30}$$

By applying the volt-second balancing law on the inductors L_m, L_k and the secondary inductance in one period at CCM operation, following equations are obtained as:

$$\int_0^{DT_s} v_{Lm} dt + \int_{DT_s}^{T_s} v_{Lm} dt = 0 \tag{31}$$

$$\int_0^{DT_s} v_{Lk} dt + \int_{DT_s}^{T_s} v_{Lk} dt = 0 \tag{32}$$

$$\int_0^{DT_s} v_{N2} dt + \int_{DT_s}^{T_s} v_{N2} dt = 0 \tag{33}$$

Using (22) -(33), the voltage of the inductors at during time (1-D) Ts can be expressed by:

$$v_{Lm|(DT_s \sim T_s)} = \frac{-DK}{1-D} V_i \tag{34}$$

$$v_{Lk|(DT_s \sim T_s)} = \frac{D(N+1)(K-1)}{2(1-D)} V_i \tag{35}$$

$$v_{N2|(DT_s \sim T_s)} = \frac{-NDK}{1-D} V_i \tag{36}$$

Based on achieved equations from modes in CCM operation and (34) -(36), the voltage of the capacitors can be obtained as:

$$\begin{cases} V_{C2} = V_{C21} = V_{C23} = \ldots = V_{C2n} = -v_{Lm} - v_{Lk} + V_i \\ \quad = \left[\dfrac{(N+3) + (1-N)K - 2D}{2(1-D)} \right] \times DV_i \end{cases} \tag{37}$$

$$V_{C3} = V_{C4} = -v_{N2} = \frac{NDK}{1-D} V_i \tag{38}$$

By substituting (37) and (38) into (30), can be written as the follows equation:

$$\begin{cases} V_{Co} = V_o = \left[\dfrac{(N+3) + (1-N)K - 2D}{2(1-D)} \right] \times nDV_i \\ \quad + \dfrac{3NDK}{1-D} V_i + V_i + \dfrac{DK}{1-D} V_i \\ \quad - \dfrac{D(N+1)(K-1)}{2(1-D)} V_i \end{cases} \tag{39}$$

Using (39), the voltage gain of the proposed converter in CCM operation can be obtained as:

$$\frac{V_o}{V_i} = \frac{nD(N-2D+K+3) + ND(5K-nK+1) + D(K-1) + 2}{2(1-D)} \tag{40}$$

When the coupling coefficient of the coupled inductor is equal to 1 ($K = 1$), the ideal voltage gain of the proposed converter in CCM operation equal to (41):

$$\frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{nD(2-D) + 3ND + 1}{1-D} \tag{41}$$

where n is the number of voltage multiplier units and N is the turns ratio of the coupled inductor.

Fig. 3 shows the key waveforms of the proposed topology in CCM operation.

B. DCM OPERATION

For simplicity theoretical analysis of the proposed converter in DCM operation, the primary and secondary leakage inductance is neglected. The proposed converter has three modes in DCM operation which are shown in Fig. 4.

Mode 1 [$t_0 \le t \le t_1$]: In this mode, the power switch S is turned on and power diodes $D_2, D_3, \ldots, D_{2n}$ and D_o are in forward biased and other power diodes are in revere biased. The magnetizing inductor L_m is charged by the input power supply (V_i). Therefore, the current of magnetizing inductor is linearly increased. Also, the secondary inductor side of the coupled inductor stores the energy in this mode, then the secondary current of the coupled inductor (i_{N2}) is linearly increased. Based on Fig. 4(a), the following equations can be written for this mode as:

$$v_{Lm} = V_i = L_m \frac{di_{Lm}}{dt} \tag{42}$$

$$i_i = i_{Lm} + N i_{N2} \tag{43}$$

$$i_i = i_{DS} + i_{C2} \tag{44}$$

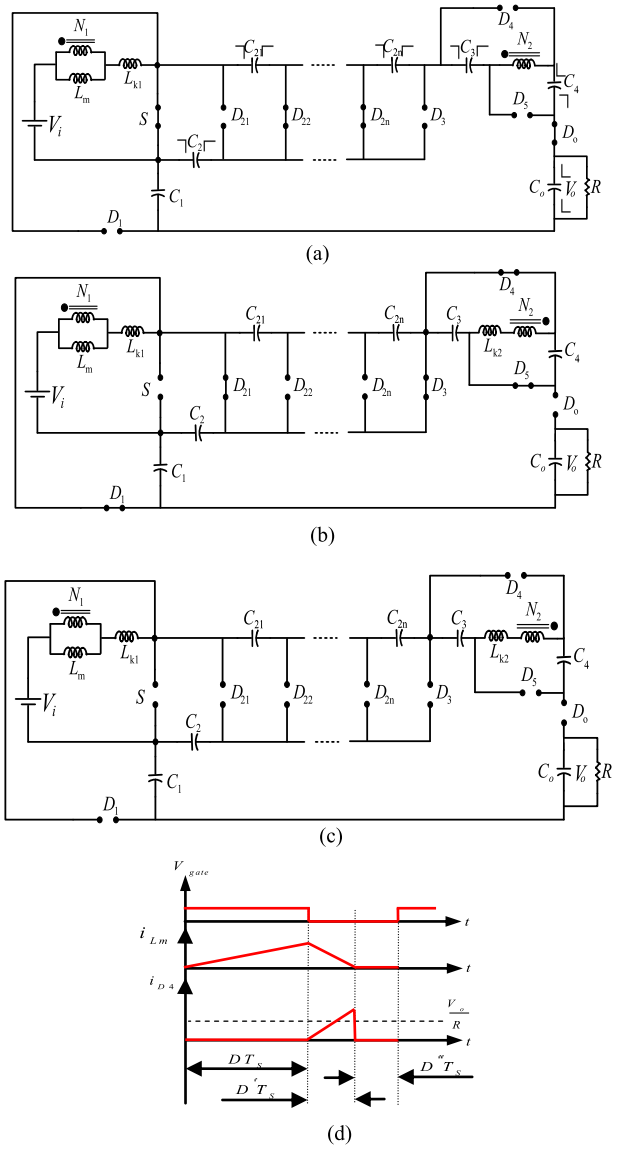

FIGURE 4. Analysis of the proposed converter at DCM operation, (a) mode 1, (b) mode 2, (c) mode 3, (d) the main waveform.

$$\begin{cases} V_{Co} = V_{C21} + V_{C23} + \ldots + V_{C2(n-1)} \\ \qquad +V_{C2n} + V_{C3} + V_{C4} + V_i + V_{C1} \\ \qquad -v_{N2} - v_{Lm} \end{cases} \tag{45}$$

$$\begin{cases} V_{C21} = V_{C1} \\ V_{C22} = V_{C23} \\ V_{C24} = V_{C25} \\ \vdots \\ V_{C2(n-2)} = V_{C2(n-1)} \end{cases} \tag{46}$$

Mode 2 [$t_1 \le t \le t_2$]: In this mode, the power switch S is turned off. Power diodes D_1, $D_{21}, \ldots, D_{2(n-1)}$, D_3, D_4 and D_5 are in forward biased condition and other diodes are in reverse biased condition. The stored energy in the magnetizing inductor charges the capacitors C_2. The current of the magnetizing inductor (i_{Lm}) is linearly decreased. Also, the secondary inductor is discharged and its current is linearly decreased and will reach zero at the end of this mode. The stored energy in the capacitor C_o is discharged to the output load R. For this mode, the following equations can be written as:

$$\frac{di_{Lm}}{dt} = \frac{V_i - V_{C2}}{L_m} \tag{47}$$

$$i_i = i_{Lm} + Ni_{N2} \tag{48}$$

$$V_{C3} = V_{C4} = -v_{N2} \tag{49}$$

$$\begin{cases} V_{C21} = V_{C23} \\ V_{C24} = V_{C25} \\ V_{C26} = V_{C27} \\ \vdots \\ V_{C2(n-1)} = V_{C2n} \end{cases} \tag{50}$$

Mode 3 [$t_2 \le t \le t_3$]: In this mode, the power switch S remains in OFF state and all power diodes are in reverse biased condition. The input current, current of the magnetizing inductor and current in the secondary side of the proposed converter are zero. The stored energy in the capacitor C_o is discharged to the output load R. Based on Fig. 4(c), can be written as follows equations:

$$i_{Lm} = 0 \tag{51}$$

$$i_{N2} = 0 \tag{52}$$

$$i_i = 0 \tag{53}$$

By applying the volt-second balancing law on the inductors L_m and secondary inductor in DCM operation can be written as follows equations:

$$v_{Lm} = v_{N2} = 0 \tag{54}$$

$$V_{C2} = V_{C21} = V_{C23} = \ldots = V_{C2n} = \frac{N(D+D')}{D'} V_i \tag{55}$$

$$V_{C3} = V_{C4} = -v_{N2} = \frac{2nND(D+D')V_i - NDD'V_o}{D'(D'-2D)} \tag{56}$$

By substituting (55) and (56) into (54), can be written as the follows equation:

$$V_{Co} = V_o = \frac{nN(D+D')}{D'} V_i + \frac{6nND(D+D')V_i - 3NDD'V_o}{D'(D'-2D)} \tag{57}$$

Using (57), the voltage gain of the proposed converter at DCM is equal to (58):

$$\frac{V_o}{V_i} = \frac{5nNDD' + 4nND^2 + nND'^2}{D'^2 + (3N-2)DD'} \tag{58}$$

Also, the relationship between the output voltage and output current can be achieved as:

$$V_o = RI_o \tag{59}$$

The peak magnetizing inductor current ($i_{Lm\text{-}peak}$) can be obtained as:

$$v_{Lm} = V_i = L_m \frac{di_{Lm-peak}}{dt} \tag{60}$$

$$i_{Lm-peak} = \frac{V_i}{L_m} DT_s \tag{61}$$

Generally, the average current of each capacitor is zero in one period, then, the average current of the power diodes D_1, D_{21}, $D_{21}, \ldots, D_{2n}, D_3, D_4$ and D_5 are equal to the output average current (I_o). Also, the average current of the magnetizing inductor L_m, leakage inductance in the primary and secondary side and the average current of the power switch can be expressed by:

$$I_{D_{1,21,22,\ldots,2n,3,4,5}} = I_o \tag{62}$$

$$I_s = \frac{2D(1-D)}{nD(4-2D)+6ND+2} I_o \tag{63}$$

$$I_{L_{k1}} = I_i = \frac{2(1-D)}{nD(4-2D)+6ND+2} I_o \tag{64}$$

$$I_{L_{k2}} = I_o \tag{65}$$

$$I_{L_m} = \frac{2(1-D)-nND(4-2D)+6N^2D+2N}{nD(4-2D)+6ND+2} I_o \tag{66}$$

By observing Fig. 4(d), the current of the power diodes became zero before the interval off-time of the power switch is over. Therefore, it can be said that the sum of the average current of all power diodes is equal to the sum of the average current of all inductors which is as:

$$I_{Inductors} = \frac{1}{2} D' \times I' = I_{Diodes} \tag{67}$$

where I' is the sum of the maximum current of the inductors.

$$I' = (DV_i / f_s L_m) \tag{68}$$

Using (62) -(67), equation (69), as shown at the bottom of the next page. Using (70), as shown at the bottom of the next page, the voltage gain value of the proposed converter at DCM operation can be achieved as equation (71), as shown at the bottom of the next page.

III. CALCULATION THE VOLTAGE/CURRENT STRESS ON THE SWITCH, THE EFFICIENCY OF THE PROPOSED CONVERTER AND INDUCTOR/CAPACITOR DESIGN IN CCM OPERATION

A. VOLTAGE/CURRENT STRESS ON THE SWITCH

By observing Fig. 2(d), the voltage stress on the switch of the proposed topology can be obtained as:

$$V_S = \left[\frac{(N+3)+(1-N)K-2D}{nD(N-2D+K+3)+ND(5K-nK+1)+D(K-1)+2}\right] \times DV_o \tag{72}$$

Therefore, the normalized voltage stress on switch versus duty-cycle, turns ratio, the coupling coefficient of the coupled inductor and number of voltage multiplier units can be obtained as:

$$M_S = \frac{V_s}{V_o} = \frac{D[(N+3)+(1-N)K-2D]}{nD(N-2D+K+3)+ND(5K-nK+1)+D(K-1)+2} \tag{73}$$

Based on Fig. 2(b), the RMS current across the power switch can be expressed by (the current value of the capacitor C_{21} is approximated with its value in mode II):

$$\begin{cases} i_{S-RMS} = \sqrt{\frac{1}{T_s}\int_0^{DT_S} (I_{Lk1} + I_{C21})^2 dt} \\ \quad = \frac{2(1-D)I_o}{nD(4-2D)+6ND+2} + \frac{I_o}{D} \end{cases} \tag{74}$$

B. INDUCTOR SELECTION

If the peak-to-peak magnetizing inductor current ripple is considered ΔI_L. Generally, it can be concluded that $\Delta I_L = ri\%I_L$, then the follows equation can be written for magnetizing inductor selection with continuous current:

$$L_m = \frac{DV_i^2}{f_s \times r_1 \% P_i} - L_k \tag{75}$$

C. EFFICIENCY CALCULATION

For calculation the overall efficiency of the proposed converter ($\eta_{Converter}$), the parasitic resistance of the power components are considered as:

- $R_{DS\text{-}on}$: on-state resistance of the power switch,
- R_{LN1}, r_{LN2}: the equivalent series resistance (ESR) of the primary and secondary inductors L_{N1}, L_{N2}, respectively,
- R_D: the equivalent series resistance of all diodes,
- R_C: the equivalent series resistance of all capacitors.

As a result, the overall efficiency of the proposed topology is obtained as:

$$\eta_{Converter} = \frac{P_o}{P_o + P_{losses}} \times 100\% \tag{76}$$

Generally, the total power losses of the switch consist of the sum of the power loss of the switch (when the power MOSFET is on-state) and switching losses. Hence, total power losses of the switch (P_{switch}) can be obtained as (77), as shown at the bottom of the next page.

The average current of the inductors is obtained in equations (64)-(66). Then, the conduction losses of the inductors can be expressed by:

$$\begin{cases} R_{L_{N1}} = R_{L_{N1}} = R_L \\ P_{L_{N1},L_{N2}} = R_L \times (\frac{I_o}{D})^2 + R_L \\ \quad \times (\frac{2(1-D) - nND(4-2D) + 6N^2D + 2N}{nD(4-2D)+6ND+2} I_o)^2 \end{cases} \tag{78}$$

The forward resistance losses ($P_{RF_{(Diodes)}}$) and voltage drop losses ($P_{VF_{(Diodes)}}$) of the power diodes can be achieved as (79), as shown at the bottom of the next page.

Power losses of the capacitors can be achieved as:

$$\begin{cases} P_{R_{Capacitors}} = R_{R_C} \times \frac{n+6}{2}(\frac{I_o}{D})^2 + R_{R_C} \times \frac{n-2}{2}(\frac{I_o}{1-D})^2 \\ \quad + R_{R_C} \times (\frac{2D^2+2-4D}{nD(4-2D)+6ND+2} I_o)^2 \\ \quad + R_{R_C} \times I^2_{R_{C_{o(rms)}}} \end{cases} \tag{80}$$

Based on (76) -(80), the overall efficiency of the proposed structure can be expressed by (81), as shown at the bottom of the next page.

IV. COMPARISON STUDY

To illustrate the advantages and disadvantages of the proposed structure, some comparisons between the proposed structure and other topologies are done in terms of voltage gain, normalized voltage stress across semiconductors (power switch/diode), number of components and overall efficiency. Therefore, to illustrate the main advantages of the proposed converter, a comparison study between the proposed structure and other converters is shown in Table 1 and its results are shown in Fig. 5 as different curves. Generally, almost all high step-up converters have low normalized voltage stress on semiconductor (switch/ diode), capable to transfer an about large power rating with proper efficiency [13]–[15]. Besides, can be said that the cost of the system will be low due to selecting with a lower rating of power semiconductors [16]–[18]. The proposed converter has lower normalized voltage stress on semiconductors (switch/ diode), then the total efficiency of the proposed converter is about high [25].

A. THE VOLTAGE GAINS VERSUS DUTY-CYCLE

Fig. 5(a) illustrates the voltage gain curves of the proposed converters versus the duty cycle. The voltage gains curves of the proposed structure for $K = 1$, different turns ratio and the different number of voltage multiplier units are provided and these are compared with other structures. By observing Fig. 5(a), it can be said that the voltage gain curves of the proposed structure are above the other structures [10]–[12]. Generally, the proposed converter has a high gain for different turn's ratio and different VM stages. Then, the proposed converter capable to use for high voltage level applications [20].

B. THE MAXIMUM VOLTAGE STRESS ON THE SWITCH

Fig. 5(b) shows the normalized voltage stress on switch comparison between the proposed converter and other structures. By comparing the shown curves on this figure, the normalized voltage stress on the switch curve for the proposed converter is located lower than curves for other structures [13], [14].

$$\frac{1}{2}D' \times \frac{DV_i}{f_s L_m} = (\frac{n+2}{2D} + \frac{n+8}{2(1-D)})I_o \tag{69}$$

$$\begin{cases} \frac{1}{2} \times D' \times \frac{DV_i}{f_s L_{tot}} = (\frac{n+2}{2D} + \frac{n+8}{2(1-D)})\frac{V_o}{R} \\ D' = \frac{5nNV_i - 3nDV_o + 2DV_o + \sqrt{(5nNVi - 3nDV_o + 2DV_o)^2 + 16(V_o - nNVi)nND^2V_i}}{2V_o - 2nNV_i} \end{cases} \tag{70}$$

$$\frac{V_o}{V_i} = \frac{5nNV_i - 3nDV_o + 2DV_o + \sqrt{(5nNVi - 3nDV_o + 2DV_o)^2 + 16(V_o - nNVi)nND^2V_i}}{f_s L_{tot}(n+2+6D)(2V_o - 2nNV_i)} \times \frac{D^2(1-D)R}{1} \tag{71}$$

$$\begin{cases} P_{switch} = P_{r_{DS-ON}} + \frac{1}{2}P_{Switching} = R_{DS-ON} \times I^2_{S(rms)} + \frac{1}{2}(C_S V_S^2 \times f_S) \\ \quad = R_{DS-ON}(\frac{2(1-D)I_o}{nD(4-2D)+6ND+2} + \frac{I_o}{D})^2 + \frac{1}{2}C_S(\frac{D(N+3)+(1-N)KD-2D^2}{nD(N-2D+K+3)+ND(5K-nK+1)+D(K-1)+2_o})^2 V_o^2 f_S \end{cases} \tag{77}$$

$$\begin{cases} P_{Losses_{(Diodes)}} = P_{RF_{(Diodes)}} + P_{VF_{(Diodes)}} = \left[\frac{n+8}{2}(\frac{I_o}{D})^2 R_{F_D} + \frac{n+2}{2}(\frac{I_o}{1-D})^2 R_{F_D}\right] + \frac{n+2}{2}(\frac{(N+3)+(1-N)K-2D}{2(1-D)})V_i I_o \\ \quad + \frac{n+2}{2}(\frac{DI_o V_i}{1-D})(\frac{(N+3)+(1-N)K-2D}{2(1-D)}) + n(\frac{I_o V_i}{1-D})\frac{(N+3)+(1-N)K-2D}{2(1-D)} \\ \quad \times \frac{nD(N-2D+K+3)+ND(5K-nK+1)+D(K-1)+2}{2(1-D)} + \frac{NDK}{1-D}V_i \end{cases} \tag{79}$$

Also, the normalized voltage stress across the power switch is more decreased by adding VM stages [16], [25].

The normalized voltage stress across the power switch for $N = 2$ and $n = 1$ is limited to 0.18 and also this value for $N = 2$ and $n = 2$ limited to 0.18. Therefore, using a power MOSFET with lower $R_{DS\text{-}ON}$ causes to decrease the power losses of the power MOSFET.

C. THE MAXIMUM VOLTAGE STRESS ON THE DIODE

Fig. 5(c) illustrates the comparison between the normalized voltage stresses on diodes versus duty-cycle. By observing Fig. 5(c), it is clear that the normalized voltage stress on the diode curves of the proposed converter (with $n = 2, N = 2$) is lower than the other curves [15], [16], [19]. The maximum voltage stress across the power diodes of the VM cells are clamped to the capacitors of the VM cells. The normalized voltage stress on these diodes will be decreased by adding the number of VM cells [21]–[24]. Therefore, using the lower rating values of the power diodes (voltage/current) causes to decrease the cost of the proposed structure [12], [26].

V. EXPERIMENTAL RESULTS

The experimental results of a laboratory prototype are provided. The proposed converter with about 260 W, $D = 0.6$, $N = 2$ and $n = 2$ are built and tested. Figs. 6(a) and (b) show the efficiency of the proposed converter versus power level and load current variation for $n = 2$ and $N = 2$, respectively. In this section, the experimental results are provided in Figs. 6-8 to confirm the theoretical analysis of the proposed converter. Fig. 6(a) illustrates the efficiency curve of the proposed converter versus power variations for duty cycle 0.6 value. Based on Fig. 6(a), the maximum efficiency happens at 90W for $n = 2$ and $N = 2$ which is equal to 96.55%. The measured efficiency of the proposed converter is achieved at about 95.35, 260W for $n = 2$ and $N = 2$. Regarding Fig. 6(b), the overall efficiency has 4.7% tolerances for load current variations. The maximum efficiency (95.35%) is happened in about 0.69A load current. The load current is changed from about 0.1A to 0.8A and the efficiency of the proposed structure is fixed in 91.85% for all variation of load current. Generally, the current/voltage level of the proposed converter is increased by adding VM stages and thus increases the power level. However, the efficiency of the proposed structure is higher than 91.85% for all power ranges and this shows that the power losses of the semiconductors are not significantly. By observing Figs. 6(a) and (b), the efficiency of the proposed converter is limited to 91.85% for about all power levels, then it is clear that the overall efficiency has lower tolerance (about 4.7%). Generally, major losses of the proposed converter are related to the conductive losses of the semiconductors. However, the low nominal values of the semiconductors cause to do not make much significantly.

The cost and characteristics of the power components are shown in Table 2. Also, the used components have a low rating value to transfer the specified power level. Also, the power level of the proposed topology can be significantly increased by adding the VM cells, the stress of the power components does not significantly change. Therefore, it causes to decrease the cost of the converter and also have good efficiency for different power levels.

Table 3 illustrates the simulation and experimental results for switch S and diode D_{21}.

Fig. 7(a) illustrates the output voltage of the proposed converter which is about 360V. Figs. 7(b) and (c) illustrate the voltage waveforms of the capacitors C2 and C2n. The voltage values of the capacitors C2 and C2n are about 71.8V and 71.6V which are confirm (37). Fig. 7(d) shows the voltage value of the capacitor C3. The obtained voltage value of the capacitor C3 is about 53 which confirms (38).

$$\eta_{Converter} = \frac{P_o \times 100\%}{P_o + \left\{ \begin{array}{l} R_{DS-ON}\left(\frac{2(1-D)I_o}{nD(4-2D)+6ND+2} + \frac{I_o}{D}\right)^2 \\ \quad + \frac{1}{2}C_S\left(\frac{D(N+3)+(1-N)KD-2D^2}{nD(N-2D+K+3)+ND(5K-nK+1)+D(K-1)+2}\right)^2 V_o^2 f_S \\ \quad + R_L \times \left(\frac{I_o}{D}\right)^2 + R_L \times \left(\frac{2(1-D)-nND(4-2D)+6N^2D+2N}{nD(4-2D)+6ND+2} I_o\right)^2 \\ \quad + \left[\frac{n+8}{2}\left(\frac{I_o}{D}\right)^2 R_{F_D} + \frac{n+2}{2}\left(\frac{I_o}{1-D}\right)^2 R_{F_D}\right] + \frac{n+2}{2}\left(\frac{(N+3)+(1-N)K-2D}{2(1-D)}\right) V_i I_o \\ \quad + \frac{n+2}{2}\left(\frac{DI_oV_i}{1-D}\right)\left(\frac{(N+3)+(1-N)K-2D}{2(1-D)}\right) + n\left(\frac{I_oV_i}{1-D}\right)\frac{(N+3)+(1-N)K-2D}{2(1-D)} \\ \quad \times \frac{nD(N-2D+K+3)+ND(5K-nK+1)+D(K-1)+2}{2(1-D)} \\ \quad + \frac{NDK}{1-D}V_i + R_{R_C} \times \frac{n+6}{2}\left(\frac{I_o}{D}\right)^2 + R_{R_C} \times \frac{n-2}{2}\left(\frac{I_o}{1-D}\right)^2 + R_{R_C} \\ \quad \times \left(\frac{2D^2+2-4D}{nD(4-2D)+6ND+2} I_o\right)^2 + R_{R_C} \times I^2_{R_{C_{o(rms)}}} \end{array} \right\}} \tag{81}$$

TABLE 1. Comparison between the proposed structure and other structures.

converter	Voltage gain	Switch normalized voltage stress	Diodes normalized voltage stres	Max. current on switch	No. of switch	No. of diode	No. of inductor	No. of capacitor	Efficiency [%] for 260W
Conventional boost	$\frac{1}{1-D}$	1	1	$\frac{D}{1-D}I_o$	1	1	1	1	-
[21]	$\frac{N+2}{1-D}$	$\frac{1}{N+2}$	$\frac{N+1}{N+2}$	$\frac{N+2}{1-D}I_o + \frac{2NI_o}{D}$	1	3	3	1	93
[22]	$\frac{(1-N)(1+D)}{1-D}$	$\frac{M_{CCM}+N+1}{2M_{CCM}(N+1)}$	$\frac{M_{CCM}+N+1}{2M_{CCM}(N+1)}$	$\frac{2(N+1)}{D(1-D)}I_o$	1	4	5	2	94.6
[23]	$\frac{3+D}{1-D}$	$\frac{M_{CCM}-1}{4M_{CCM}}$	$\frac{M_{CCM}-1}{2M_{CCM}}$	$\frac{4+N}{1-D}I_o$	2	n	2	$2n$-1	95.3
[24]	$\frac{2(N+1)}{1-D}$	0.25	0.25	$\frac{N+1}{1-D}I_o \quad \frac{2}{D}I_o$	2	4	2	4	95.6
[25]	$\frac{2+2nD+nN-n}{2(1-D)}$	$\frac{2M_{CCM}-2n}{M_{CCM}(n+nN)}$	$\frac{2n(M_{CCM}-n)}{M_{CCM}(n+nN)}$	$\frac{1+2nD+nN-n}{2(1-D)}I_o \quad \frac{1}{1-D}I_o$	1	n+2	2	n+3	95.1
[26]	$\frac{2+N(1-D)}{1-D}$	$\frac{M_{CCM}+N}{2M_{CCM}(2+N)}$	$\frac{(N+1)(M_{CCM}-N)}{2M_{CCM}(2+N)}$	$\frac{2+N(1+D)}{D(1-D)}I_o$	1	4	1	4	96
[27]	$\frac{N}{1-D}$	$\frac{1}{N}$	$\frac{1}{N}$	$\frac{N}{1-D}I_o$	2	2	2	4	95.3
[28]	$\frac{N+2}{1-D}$	$\frac{1}{N-2}$	$\frac{1}{N-2}$	$\frac{N+2}{1-D}I_o$	1	2	3	3	93.8
[29]	$\frac{N+2}{1-2D}$	$\frac{1}{N+2}$	$\frac{N+1}{N+2}, \frac{1}{N+2}$	$\frac{1+2D(N+1)}{D(1-2D)}I_o$	1	4	2	5	91.90
[30]	$\frac{2(N+1)}{1-D}$	$\frac{1}{2(N+1)}$	$\frac{2N+1}{2(N+1)}$	$\frac{3N+1}{1-D}I_o$	4	2	2	3	94.80
[31]	$\frac{N+2}{1-D}$	$\frac{1}{N+2}$	$\frac{1}{N+2}, \frac{N+1}{N+2}$	$\frac{N+2}{1-D}I_o + \frac{2(N+1)I_o}{D}$	1	3	2	4	95.40
Pro. Conv.	$\frac{nD(2-D)+3ND-1}{1-D}$	$\frac{D(2-D)}{nD(2-D)+3ND+1}$	$\frac{D(2-D)}{nD(2-D)+3ND+1}$	$\frac{2(1-D)I_o}{nD(4-2D)+6ND+2} + \frac{I_o}{D}$	1	n+5	1	n+4	95.35
	N, n	N= turns ratio	n= voltage multiplier sell	$D \quad \frac{3N-M_{CCM}-2n-\sqrt{9N^2+6NM_{CCM}+12nN-M_{CCM}^2+4n^2+4n}}{2n}$					

TABLE 2. Cost and characteristics of the power components.

Components	Magnitude	Cost ($)
Input/Output voltages	24/361 V	-
Switching frequency	40 kHz	-
Magnetizing Inductor L_m	0.5 mH	Core: 5.77$
Leakage Inductor L_K	2 µH	-
C_2, C_{21}, C_{22}, ..., C_{2n}, C_3, C_4	330 µF	7×0.58$
C_o	470 µF, 450 V	1.26$
Power switch	TK55S10N1	0.99$
All diodes	MUR1560	8×0.9$

TABLE 3. Simulation and experimental results for Switch S and diode D21.

Components	Simulation	Experimental
Peak voltage across switch S [V]	59.9	59.93
Average current switch S [A]	11.40	11.35
RMS current switch S [A]	15.14	15.20
Peak voltage across diode D_{21} [V]	59.60	59.50
Average current diode D_{21} [A]	0.70	0.71
RMS current diode D_{21} [A]	1.25	1.26

By observing Fig. 8(a), the average current of the coupled inductor (L_K) is about 11.36A which validates the theoretical analysis and feasibility of the proposed structure. According to Fig. 8(b), the maximum voltage stress across the power diode D_{21} is about 59.5V which this value conforms the obtained value of theoretical analysis for D_{21} based on by applying KVL law in Fig. 2(a) and (37). Fig. 8(c) illustrates the maximum voltage value of the power diode D_4 which is obtained about 58.6V. Fig. 8(d) shows the current waveform and maximum voltage stress on the MOSFET. The average current of the MOSFET is obtained about 11.35A and the maximum voltage stress is achieved by about 60V. Generally, based on Figs. 6-8, it can be said that the experimental results and theoretical analysis confirm each other well.

For dynamic response, two voltage sources are connected series each other. The values of which are about $V_{in1} = 15V$

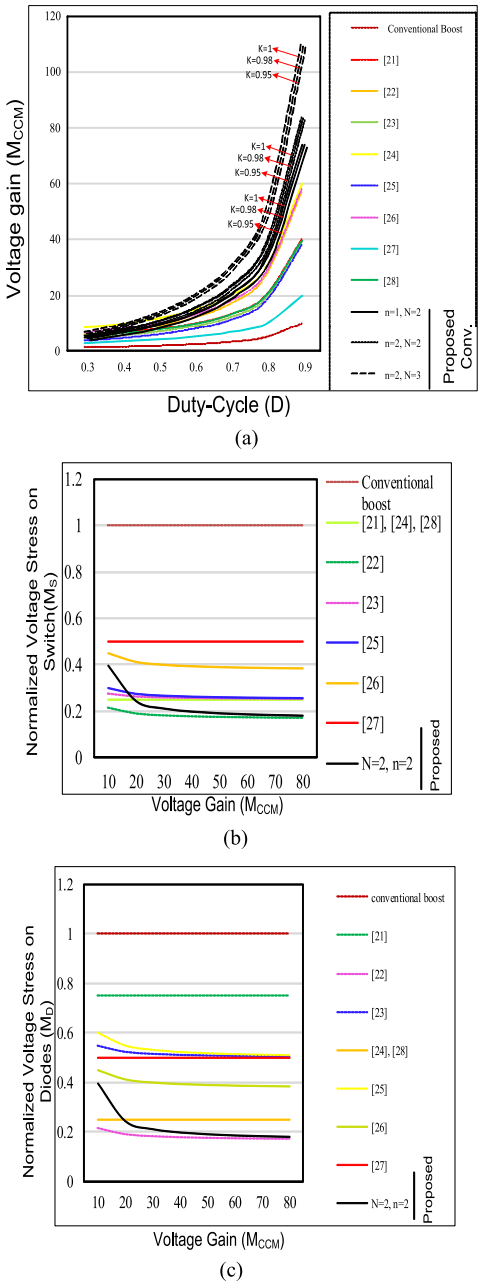

FIGURE 5. Comparison of curves based on theoretical analysis with other topologies, (a) Voltage gain versus duty-cycle, (b) Normalized voltage stress on switch versus duty-cycle, (c) Normalized voltage stress on diode versus duty-cycle.

and $V_{in2} = 9V$ respectively and output power is 300W. As can be seen from Fig. 3 at first, for the input voltage of 24V, the output voltage is 361V. After a small-time, the input voltage source of V_{in1} is failed suddenly and the input voltage is decreased to 9V. Therefore, after a small interval (about 980msec), the output voltage is decreased to 140V and stays constant. Also, the output power is decreased to 40W. As a result, the voltage drop in the input source will not affect the load regulation. The dynamic response of the proposed

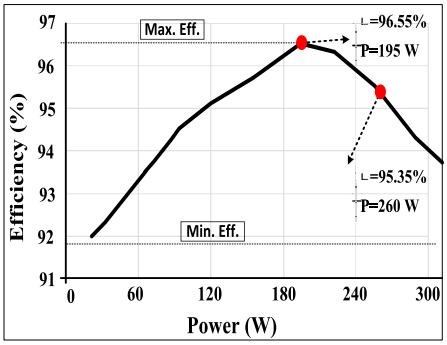

FIGURE 6. Efficiency versus power variations.

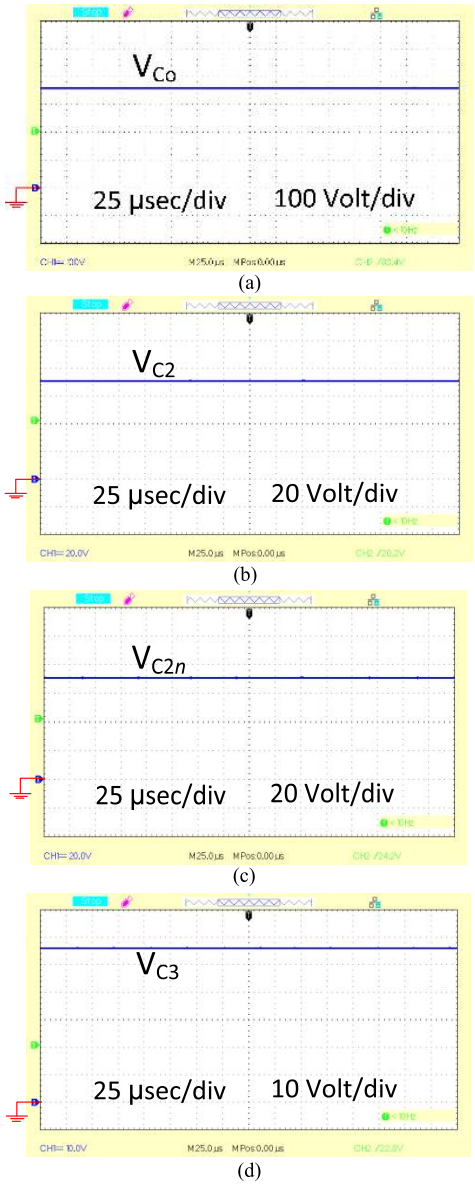

FIGURE 7. The voltage waveforms of the capacitors, (a) Capacitor Co, (b) Capacitor C2, (c) Capacitor C2n, n = 2 (d) Capacitor C3.

converter for 62.5% voltage drop at the input side is shown in Fig. 9.

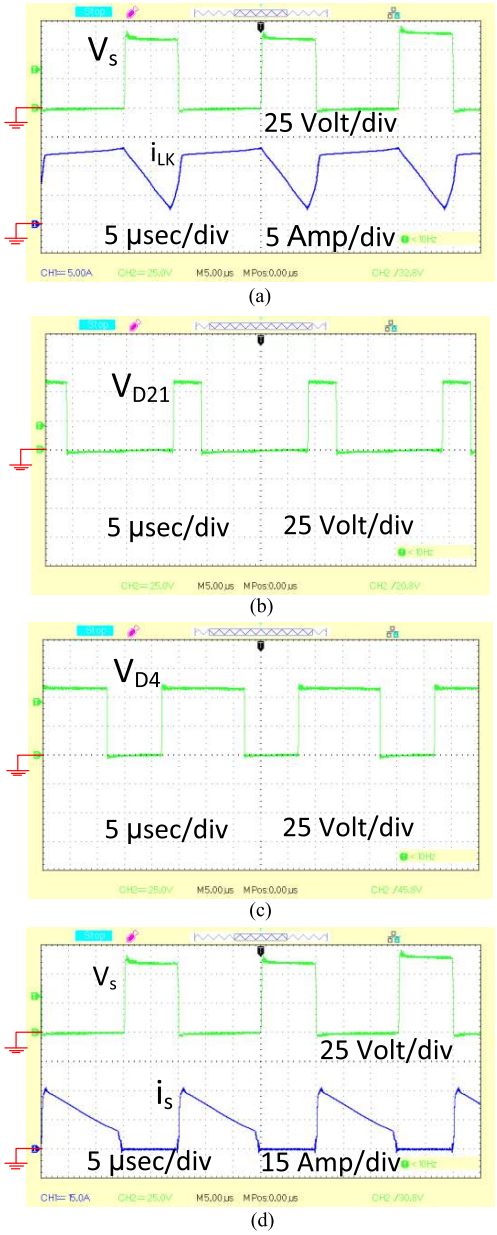

FIGURE 8. The current/voltage waveforms of inductor LK and semiconductors (MOSFET/diode), (a) Current of inductor LK, (b) Maximum voltage of diode D21, (c) Maximum voltage of diode D4, (d) Maximum voltage/current of MOSFET.

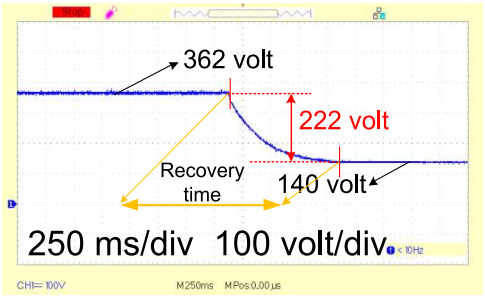

FIGURE 9. Dynamic response for 62.5% voltage drop at the input voltage value.

Fig. 10 illustrates the experimental prototype of the proposed converter.

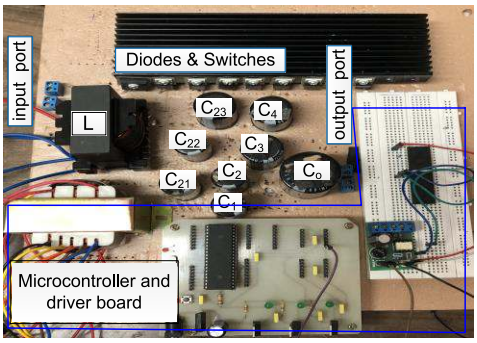

FIGURE 10. Experimental prototype of the proposed converter. {R2}

VI. CONCLUSION

In this study, a new high voltage gains dc/dc converter using coupled inductor and voltage multiplier cell is presented suitable for renewable sources. In addition, the voltage gains of the proposed converter more increases by rising the turns ratio value and number of VM cells. Also, the maximum voltage of the power semiconductors (power switch/diode) is clamped to the capacitor's voltage of the VM cells which it causes to decrease the normalized voltage stress on switch/diode. Therefore, the power losses of the converter are decreased by selecting the power switch and power diodes with a lower rating. Using just one switch with lower $R_{DS\text{-}ON}$ leads to decrease the total power losses and decrease the cost of the system. Consequently, the overall efficiency of the converter is high about for al power ranges. The overall efficiency of the proposed converter is about upper than 91.85 for all power levels. A laboratory prototype of the proposed converter is built and tested in about 260W level with 40kHz switching frequency. As the experimental results are provided and to be well-confirmed the theoretical analysis, also it was shown that the proposed converter capable to obtain 95.35% efficiency value. The tolerance efficiency of the converter is about 4.7% for all power ranges.

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