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***Abstract*— This paper proposes a modified coupled-inductor SEPIC dc-dc converter for high voltage gain ($2 < G < 10$) applications. It utilizes the same components as the conventional SEPIC converter with an additional diode. The voltage stress on the switch is minimal, which helps the designer to select a low voltage and low $R_{DS\text{-}on}$ MOSFET, resulting in a reduction of cost, conduction and turn ON losses of the switch. Compared to equivalent topologies with similar voltage gain expression, the proposed topology uses lower component-count to achieve the same or even higher voltage gain. This helps to design a very compact and lightweight converter with higher power density and reliability. Operating performance, steady-state analysis and mathematical derivations of the proposed dc-dc converter have been demonstrated in the paper. Moreover, extension of the circuit for higher gain ($G > 10$) application is also introduced and discussed. Finally, the main features of the proposed converter have been verified through simulation and experimental results of a 400 W laboratory prototype. The efficiency is almost flat over a wide range of load with the highest measured efficiency of 96.2%, and the full-load efficiency is 95.2% at a voltage gain of 10.**

***Index Terms*— Boost converter, coupled-inductor, dc-dc converter, flyback transformer, SEPIC converter, Switched-Mode Power Supply (SMPS)**

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I. INTRODUCTION

High conversion gain dc-dc power converters have recently seen an increased demand in variety of power electronics applications. In fact, the main reasons behind this increased attention have three folds. Firstly, fast deployment of Renewable Energy (RE) based power systems has intensified the need for high conversion gain power converters. This is due to the low voltage generation inherent in most RE sources such as Photovoltaic (PV) modules and fuel-cells, where stepping up the low input voltage (e.g., 20 V - 40 V) to higher voltage levels (e.g., 200 V - 400 V) is required in order to have a properly function grid-forming or grid-feeding converter [1], [2]. Secondly, prevalence of applications demanding higher voltage levels for better performance, from few hundreds of Volts such as for Light Emitting Diode (LED) in lightning [3] up to few kilovolts in pulsed power applications [4]. Lastly, one of the most relevant is the possibility of distributing electrical energy more efficiently at higher dc voltage levels (e.g., 380 V-400 V or even higher). This is the case in applications such as telecommunication and dc power systems where electrical energy can be transferred with higher efficiency, reliability and power quality [5], [6].

Conventionally, the boost and buck-boost topologies can be employed in order to step-up the output voltage. However, practically achieving conversion gains of beyond six due to presence of parasitic elements is not feasible [2]. Moreover, operating at high duty cycles compromise the boost converter efficiency as small turn-off times which may incline Electromagnetic Interference (EMI) and ripple current levels, indicating a requirement for larger magnetic components [2], [7]. Another derivation of a buck-boost topology suitable for high voltage applications is the flyback converter [4], [8], [9]. Although this topology is well employed for high voltage applications with low parts count, it is only suitable for very low power levels (i.e., < 300 W). This is due to the high dc magnetization current requirement of its flyback transformer, which increases the size of the transformer and consequently the losses for higher power levels under continuous conduction mode operation [8].

From this standpoint, many research efforts have been devoted towards developing high voltage gain power converters without imposing extreme duty ratio. In general, the demanded performance can be obtained through utilizing coupled-inductor, switched inductors and switched capacitor cells [7], [10]-[16] and/or employing multi-cell configurations [4], [17]-[21]. All these attempts are made in order to overcome the existing technological limits (i.e., power switch breakdown voltage and limited power ratings) and to reach the required output voltage level with minimum duty ratio (i.e., obtaining better efficiency). However, in many practical situations, in order to obtain the required voltage gain and reduce voltage stress across the power switch many switched-cells are typically required. Furthermore, using an impedance network is also considered as another topological variant. The impedance network based power converters. known as Z-source, is initially proposed for dc-ac inverter operation [22], but it can be modified to operate as a high voltage gain dc-dc converter [23]. Recently, with the aim of reducing start-up inrush

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current and improving the voltage gain of conventional Z-source converter, a variety of modified impedance networks have been introduced. These modifications can be summarized as switched inductor, extended boost, switched inductor quasi Z-source and enhanced boost [24]-[29].While using the aforementioned topologies a high voltage gain with small duty cycle (*D*) is achievable, but the demerits of the aforementioned topologies are high parts counts (i.e., diodes, inductors and capacitors) and particularly the conduction of most diodes in (*1-D*) of the switching period, which lead to high power loss and low efficiency.

In spite of topological improvements, connecting two or more power converters in to multi-cell configurations is an alternative way to achieve a high conversion ratio. This can be obtained by series/parallel connection of power converter units [4], [9], cascaded cells [18]-[20] or multilevel approach [21]. With no doubt, multi-cell connection of power converters is an effective way to match the required power rating, voltage gain and reduce voltage stresses across the power switches, but high component count and lower efficiency may limit their performance. Thereby, it is preferable to first maximize the converter performance at the topology level before applying multi-cell connection. It is worth noting that obtaining high voltage gain, high efficiency and high power density at the same time are contradicting targets and a compromise is required to match specific application requirements. As a result designing a power converter with minimum number of components is always desirable. Low parts count can be a good design factor as it may lead to a cost-effective, simple, compact and efficient power converter.

Among aforementioned techniques, using coupled inductor is an effective technique to increase the voltage gain while avoiding high parts count [30], [31]. The main concept in this approach is to obtain the desirable voltage gain by increasing the coupled inductors turns ratio without including more components to the power converter. Therefore, the power loss may be lowered and consequently the efficiency can be improved. The coupled inductor technique associated with the SEPIC topology is introduced in [32]-[34]. Other variants of this converter with higher voltage gain ratio are presented in [35]-[39]. Generally, two main drawbacks can be identified in the introduced methods. Firstly, using two magnetic elements [32]-[37] and necessity of including extra diodes and capacitors cells to further extend the voltage ratio significantly impair the power density. Secondly, in order to mitigate the adverse effect of coupled-inductor leakage inductance, a snubber circuit is mandatory [40]. The presence of snubber circuit impose additional losses on the power converter. However, with suitable coupled-inductor design it is possible to minimize the leakage inductance and consequently the snubber circuit, which in return improves the system efficiency. In [41]-[42], high gain DC-DC converters, using taped inductor technique are introduced where their operations are very similar to converters using coupled inductor technique. However, without minimizing the leakage inductance effects and without using the low power loss snubber circuit, the voltage spike across the power switch is high and the efficiency is degraded. Step-up current-fed converters [43]-[45] with low input current ripple are appropriate solutions

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in renewable energy applications, particularly in fuel cell systems. High efficiency is achieved in these converters using soft switching techniques. However, their complicated structures and using more than one active power switch make their controller system more complicated.

From the above discussions, the present work focuses on coupled-inductor method as a suitable candidate to obtain high voltage with low power losses in low to medium power applications. The proposed method is based on the SEPIC dc-dc converter topology. Here using a coupled-inductor, less number of components are employed comparing with prior-art methods. The voltage stress across the active power switch is minimized, which highlights the possibility of utilizing low voltage power switches (i.e., low switching losses) with low turn-on resistance (i.e., low conduction losses), which lead to an efficient and cost-effective design. Moreover, by improving the magnetic coupling the leakage inductance effect is minimized. The principle of operation, theoretical analysis of the proposed converter are investigated in comparison with its similar counterparts. The reported analysis is validated by key experimental results of a 400 W prototype. This paper is improved version of the conference paper [46]. In [46], this converter was introduced for very low power (5 W) applications as a front end DC-DC converter for piezoelectric systems and here are the following improvements for the current work:

a) This converter is introduced as a high step-up and high efficiency converter in renewable energy application with nominal input voltage 40 V and output voltage 400 V as well as having considerable higher power (400 W).
b) In addition to CCM mode, the converter is analyzed in the boundary conduction mode (BCM) and discontinuous conduction mode (DCM). Moreover, a design guideline in order to select the appropriate components value is added to this paper.
c) A derivative converter with higher voltage gain (section IV) based on the proposed converter is also presented.
d) In order to minimize the leakage inductance effects and prevent the voltage spike across the power switch, an improved magnetic coupling is designed and a RCD snubber circuit with low power loss is added in the experimental prototype as well as an efficiency measurement and loss distribution. A peak efficiency of 96.2% confirms the effectiveness of this converter in renewable energy applications.

This paper is structured as follows: Section II describes the proposed topology operation principle and design guidelines under steady state conditions. Analyzing the prior-art methods in comparison with the proposed topology through highlighting key aspects of their performance are addressed in Section III. Section IV is dedicated to further

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extend the proposed topology for higher voltage gain ratios. In Section V, experimental results are presented to substantiate the effective performance of the proposed method. Finally, conclusions are drawn in Section VI.

II. Operating Principle and Steady State Analysis of the Quasi-SEPIC dc-dc Converter

This section starts first by illustrating the operating principle of the proposed converter in continuous conduction mode (CCM). Then, its operation in the discontinuous conduction mode (DCM) is introduced, considering the critical case between the CCM and the DCM, which is called the boundary conduction mode (BCM). Finally, it shows the design steps or guidelines of a 400 W converter.

A. CCM Operation

Compared to the basic coupled-inductor SEPIC converter, as shown in Fig. 1(a), the proposed converter, which is shown in Fig. 1(b), utilizes the same number of components with an additional diode. It is worth noting that this structure does not require an isolated gate drive circuitry for the employed MOSFET, resulting in lower cost and volume. Furthermore, a capacitor is connected in series with the transformer secondary winding, preventing the flow of the dc current in the transformer and, hence, avoiding saturation due to dc current.

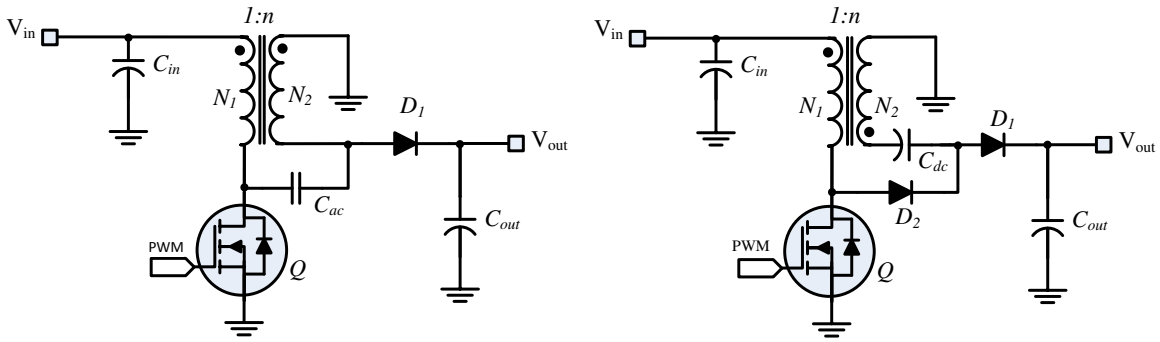

Fig. 1. Circuit schematic showing (a) traditional coupled-inductor SEPIC dc-dc converter and (b) proposed coupled-inductor quasi-SEPIC dc-dc converter.

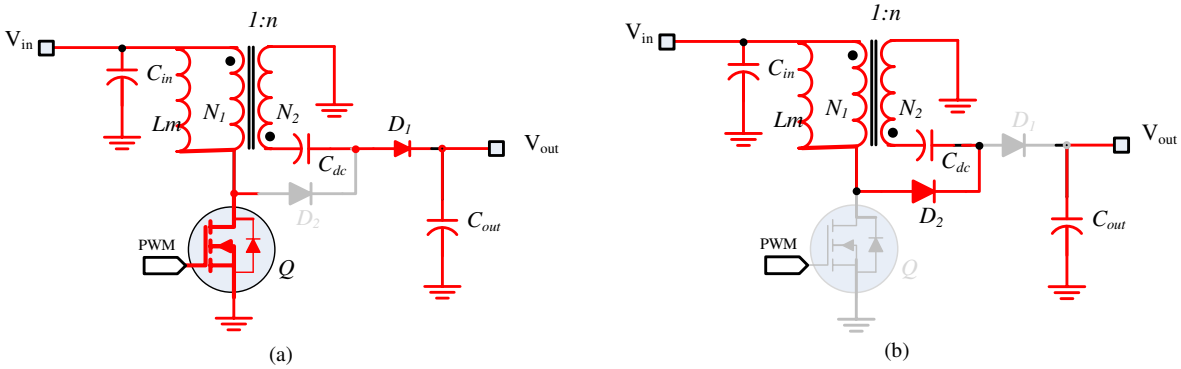

Fig. 2. Equivalent circuits of the proposed converter in one switching cycle (a) Mode 1 (Q_{ON}), and (b) Mode 2 (Q_{OFF}).

In order to do further analysis on the converter operation, several assumptions are taken into account as follows:

1) The MOSFET and the diodes are ideal, i.e. the ON resistances of the MOSFET and voltage drop across the diodes are neglected;

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2) All the employed capacitors are large enough, i.e. the voltage ripples across them are negligible; and

3) The leakage inductance of two coupled inductors are negligible and they are modeled as an ideal transformer with a turns ratio of N_1:N_2 and a magnetizing inductance of L_m, parallel connected to the primary winding.

According to the prior art assumptions, each switching cycle is divided into two modes of operation as shown in Fig. 2(a) and Fig. 2(b). The key waveforms in one switching cycle in CCM are shown in Fig. 3. In Mode 1, as shown in Fig. 2(a), the power switch is turned ON, and the voltage across L_m is equal to the input voltage. Moreover, D_1 is ON and D_2 is OFF during this mode, where C_{dc} is delivering energy to the load, connected across C_{out}. Hence, from Fig. 2(a)

$$V_{Lm(mode1)} = V_{in} \tag{1}$$

Then, applying the KVL in secondary winding, the following equation can be obtained as:

$$V_O = V_{Cdc} + nV_{dc} \qquad \text{Where } n = \frac{n_2}{n_1} \tag{2}$$

Mode 2 starts when the power switch is turned OFF, in which D_2 is ON and providing a current path for the magnetizing inductance current. During this mode, D_1 is OFF and the output capacitor delivers the required energy to the load. Thus, applying KVL again, the voltage across L_m is given by

$$V_{Lm(mode2)} = \frac{V_{in}-V_{dc}}{1+n} \tag{3}$$

Due to the voltage-second balance of L_m, the following expression can be obtained:

$$DV_{in} + \frac{(1-D)(V_{in}-V_{Cdc})}{1+n} = 0 \tag{4}$$

Therefore, the voltage across C_{dc} is obtained as

$$V_{C_{dc}} = \frac{(1+nD)}{1-D} V_{in} \tag{5}$$

Substituting (5) into (2), the output voltage is given by

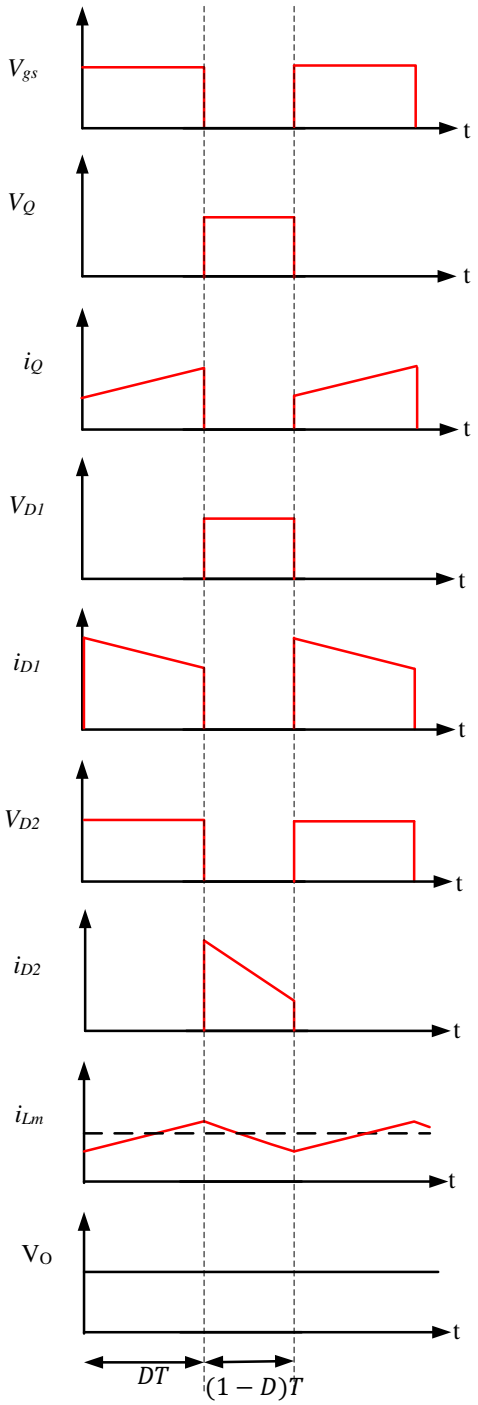

Fig. 3. Key waveforms of the proposed converter in continuous conduction mode.

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$$V_O = \frac{1+n}{1-D} V_{in} \tag{6}$$

Using (6), the voltage gain of the proposed converter is

$$G = \frac{1+n}{1-D} \tag{7}$$

Hence, it is obvious that the output voltage is a function of the transformer turns ratio (n) or the duty cycle (D).

The voltage stress across the power switch is obtained by applying KVL in Fig. 2(b) as follows:

$$V_S = V_{in} - V_{Lm(mode2)} \tag{8}$$

Using (3) and (5), we have

$$V_S = V_{in} - \frac{(V_{in} - V_{C1})}{1+n} = \frac{V_{in}}{1-D} \tag{9}$$

Comparing (6) and (9), it is clear that voltage stress on the power switch is always lower than output voltage for any turns ratio.

The switching loss can be obtained as

$$\mathrm{P_S} = \mathrm{C_S f_s V_S^2} = \mathrm{C_S f_s}(\frac{\mathrm{V_{in}}}{1-\mathrm{D}})^2 \tag{10}$$

Where, Cs is MOSFET drain-source intrinsic capacitor, f_s is the switching frequency and V_s is the voltage stress across the power switch. From (10), it is obvious that the power loss can be decreased n^2 times compared to the conventional coupled inductor SEPIC converter. Moreover, the low voltage power MOSFET has lower turn-on resistance that can lead to lower conduction losses and consequently gives a better efficiency.

Similarly, the $R_{DS,on}$ of the device increases with the blocking voltage capability of the device. Hence, lower voltage device as implemented in the circuit has lower $R_{DS,on}$, which consequently have lower conduction loss. Hence, with the reduction of the voltage stress both switching and conduction losses are reuced.

Similarly, the voltage stress across D_1 and D_2 can be obtained by

$$V_{D1} = \frac{nV_{in}}{1-D} \tag{11}$$

$$V_{D2} = V_O = \frac{1+n}{1-D} V_{in} \tag{12}$$

The current stress of the different components can be determined using the charge balance of the capacitors. According to Fig. 2(b), the output capacitor current is equal to the output current in Mode 2. Therefore,

$$I_{Cout}(Mode\ 2) = -I_O \tag{13}$$

Similarly, due to the charge balance in C_{out}, the following equation can be obtained:

$$I_{Cout}(Mode\ 1) = \frac{(1-D)I_O}{D} \tag{14}$$

The average value of the current in D_1 ($<I_{D1}>$) is equal to output current, i.e.

$$< I_{D1} >= I_O \tag{15}$$

Thus, the maximum current in D_1 can be determined by

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$$I_{D1} = \frac{I_o}{D} \tag{16}$$

Using Fig. 2, the average values of the transformer primary and secondary current are equal to zero. Therefore, the average current in D_2 ($<I_{D2}>$) is given by

$$< I_{D2} >= I_O \tag{17}$$

The maximum current in D_2 is given by

$$I_{D2} = \frac{I_o}{1-D}. \tag{18}$$

Moreover, from Fig. 2(a), the average value of the MOSFET current ($<I_Q>$) is given by

$$< I_Q >= < I_{Lm} > -n < I_{D1} > \tag{19}$$

The average value of the magnetizing inductor current is equal to the average input current. Since the average value of the transformer primary current is zero, the following equation can be obtained:

$$< I_Q >= < I_{in} > -n\, I_o, \tag{20}$$

which results in

$$< I_Q >= \frac{1+Dn}{1-D} I_o. \tag{21}$$

Therefore, the maximum current in the MOSFET can be calculated by using

$$I_S = \frac{1+Dn}{D(1-D)} I_o. \tag{22}$$

B. BCM and DCM operations

The proposed converter goes to boundary conduction mode (BCM) when the magnetizing inductor current drops to zero exactly in the next switching cycle. The magnetizing inductance current and voltage in this mode are shown in Fig. 4. This phenomenon occurs when the magnetic inductance or switching frequency values are small or the converter works under light load conditions. If the inductor current goes to zero before the next switching cycle, the converter works in discontinuous conduction mode (DCM). In the following context, the condition under which the converter goes to the BCM is derived, and then the voltage gain of the converter under DCM is obtained. From Fig. 4, the current ripple across the magnetic inductance is given by

$$\Delta i_{Lm} = \frac{V_{in} D T_S}{L_m}. \tag{23}$$

Also, the average value of the magnetizing current ($<i_{Lm}>$) is

$$< i_{Lm} > = \frac{\Delta i_{Lm}}{2} = \frac{V_{in} D T_S}{2 L_m}. \tag{24}$$

The average current value of the transformer primary and secondary winding is equal to zero due to the series capacitor (C_{dc}) with secondary winding. Thus, applying KCL results in

$$< i_{Lm} > =< i_{in} >, \tag{25}$$

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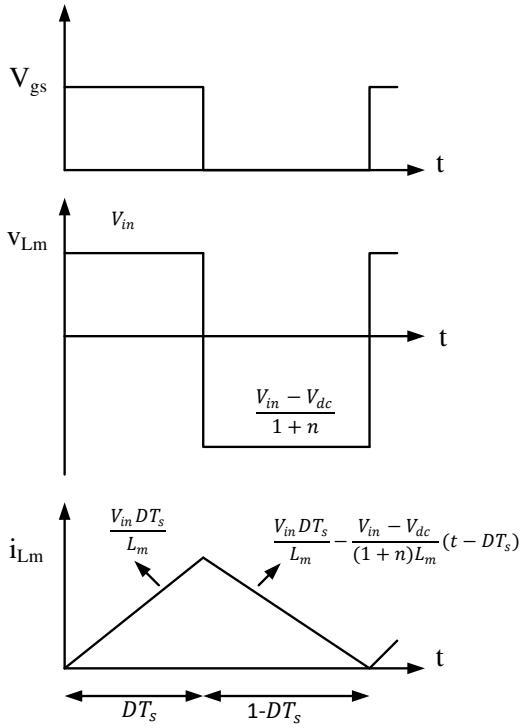

Fig. 4. Magnetizing inductance voltage and current in BCM.

where,$< i_{in} >$ is the average value of the input current. If all parasitic effects are neglected the input power is equal to output power, i.e.

$$P_o = P_{in}. \tag{26}$$

Or in another way

$$v_{in} i_{in} = v_o i_o \tag{27}$$

The voltage gain of the converter in the BCM can be obtained using (6). Therefore, substituting (6) and (25) into (27) can lead to

$$\frac{V_{in} D}{2 L_m f_s} = \frac{(1+n)}{1-D} i_{OB}, \tag{28}$$

where f_s is the switching frequency and i_{OB} is the output current under BCM.

Therefore, the boundary output current can be obtained from

$$i_{OB} = \frac{D(1-D)^2 V_O}{2 L_m f_s (1+n)^2}. \tag{29}$$

Using the above equation, the normalized boundary output current is given by

$$i_{OB} \Big/ \frac{V_O}{2 L_m f_s} = \frac{D(1-D)^2}{(1+n)^2}, \tag{30}$$

Using (28), the minimum value of the magnetizing inductor that is required in order to operate the converter in CCM can be obtained by

$$L_m \geq \frac{D(1-D)^2 V_O}{2 f_s i_{OB} (1+n)^2} \tag{31}$$

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The converter goes to DCM if the magnetizing inductance value is lower than (31) for a certain load.

The boundary load resistance and its normalized value can also be obtained as in (32) and (33) respectively, where

$$R_{OB} = \frac{2L_m f(1+n)^2}{D(1-D)^2}, \tag{32}$$

$$R_{OB}/2L_m f_s = \frac{(1+n)^2}{D(1-D)^2}. \tag{33}$$

The normalized output current and the normalized output resistance are plotted in Fig. 5(a) and Fig. 5(b) respectively for n=1 and n=2. It is clear that the CCM region can be extended with increasing the coupled inductors turn ratio. The maximum value of the boundary output current can be obtained from the derivative of (29), that occurs under *D=1/3* and gives the maximum value of the boundary output current as

$$i_{O(\max)} = \frac{V_o}{54L_m f_s(1+n)^2}. \tag{34}$$

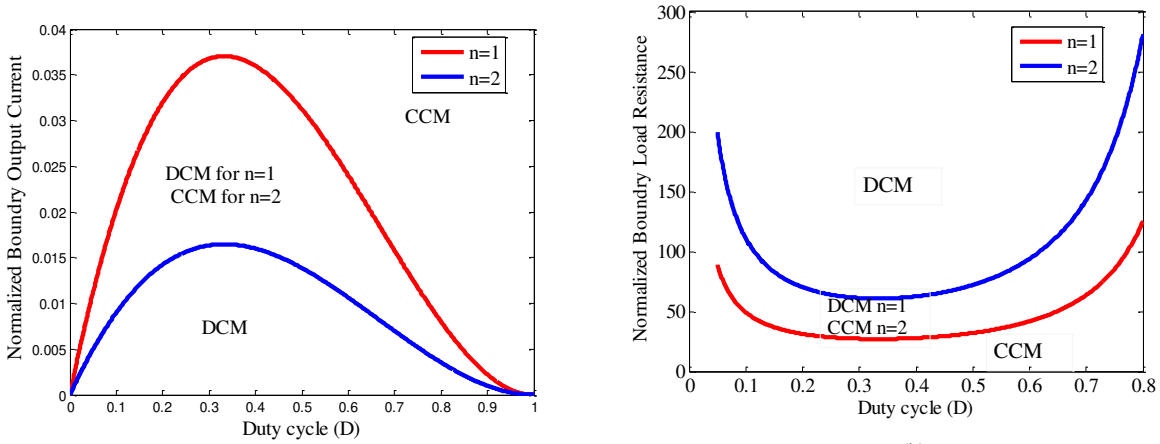

Fig. 5. Normalized (a) load current and (b) load resistance under n = 1, and n = 2.

There are three regions in DCM. Modes 1 and 2 are similar to Fig. 2(a) and Fig. 2(b) respectively, while Mode 3 is shown in Fig. 6.

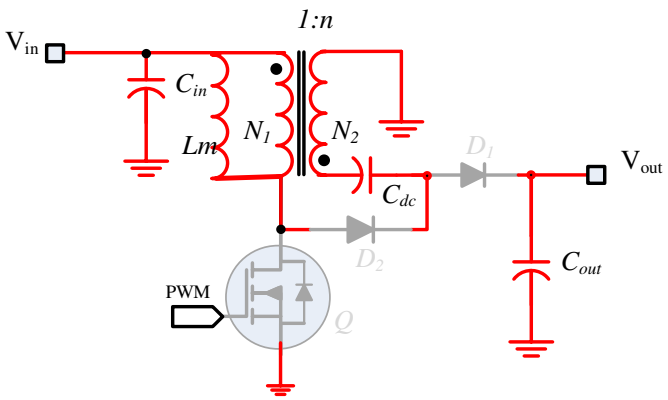

Fig. 6. Mode 3 in Discontinuous Conduction Mode (DCM).

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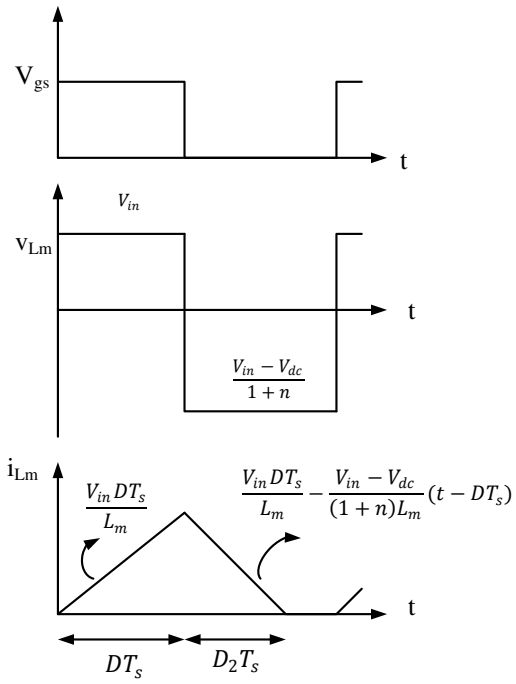

Fig. 7. Magnetizing inductance voltage and current in DCM.

In this mode, the switch and the two diodes are turned OFF and the magnetizing inductor current fall to zero before the next switching cycle. The magnetizing current under DCM is shown in Fig. 7. Hence, the following equations can be derived by using Fig. 7.

$$i_{PK} = \frac{V_{in}DT_s}{L_m}, \tag{35}$$

$$< i_{Lm} > = \frac{i_{PK}(D+D_2)}{2} = \frac{V_{in}D(D+D_2)}{2L_m f_s}, \tag{36}$$

As shown in Fig. 7, D_2T_s is the time taken by the inductor current i_{Lm} to fall to zero from its peak value (i.e. at the end of V_{gs} ON).

As discussed before, the average value of the magnetizing inductor current is equal to input current, i.e.

$$< i_{Lm} > =< i_{in} >. \tag{37}$$

Also, the output power is equal to the input power if all parasitic effects are neglected i.e.

$$P_{in} = P_O \Rightarrow \frac{V_{in}^2 D(D+D_2)}{2L_m f_s} = \frac{V_O^2}{R}. \tag{38}$$

Due to the voltage-second balance of the magnetizing inductance, the following relation can be obtained:

$$DV_{in} + \frac{D_2(V_{in}-V_{Cdc})}{1+n} = 0. \tag{39}$$

Substituting (2) into (39) leads to

$$D_2 = \frac{D(n+1)V_{in}}{V_O-(n+1)V_{in}}. \tag{40}$$

The relationship between D and the voltage gain of the converter during the DCM can eventually be derived by substituting (40) into (38) as follows:

$$D = \sqrt{2\tau M_{DCM}(M_{DCM}-(n+1))}, \tag{41}$$

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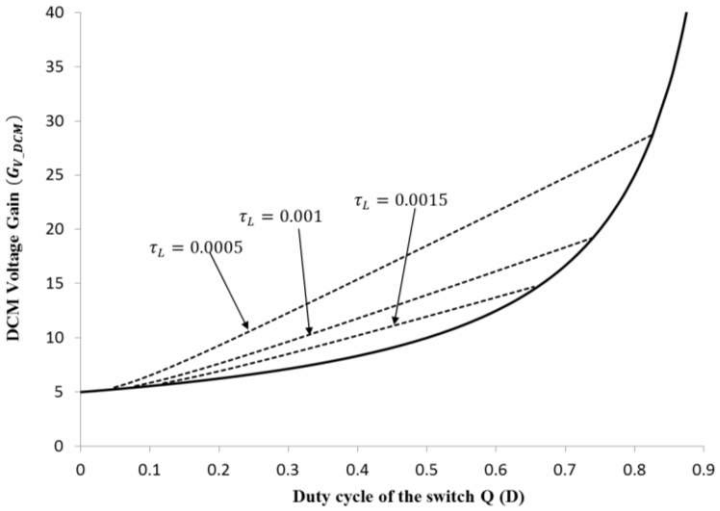

Fig. 8. Voltage gain versus duty ratio at DCM operation under various τ_L values and n = 4.

where the normalized input time constant τ_L is given by

$$\tau_L = \frac{L}{RT_S} = \frac{Lf_S}{R}, \tag{42}$$

Where f_s is the switching frequency and R is the equivalent load resistance. Curves illustrating (41) are shown in Fig. 8 for different τ_L values during the DCM operation. From (41), it is quite obvious that the voltage gain is load dependent during the DCM. Finally, the DCM is not recommended in general.

C. Design guidelines

The component values in the proposed converter can be determined considering the following specifications:

1) input voltage varies between *30 V* and *50 V* and its nominal value is *40 V;*
2) output voltage is fixed to *400 V*;
3) switching frequency is set to be *100 KHz*;
4) nominal output power equals *400 W*, corresponding to I_O*=1 A*;
5) converter works in CCM;
6) voltage stress on power switch should be lower than *150 V*, which is the rated value of the selected MOSFET; and
7) Voltage ripple across the capacitors should be lower than *1%* of their nominal values.

Using (11), the voltage stress across the switch can be determined as

$$\mathrm{V_S} = \frac{\mathrm{V_O}}{1+\mathrm{n}} \tag{43}$$

Using (43), in order to restrict the voltage stress across the switch to *80 V*, n should be equal to or higher than *4*.Therefore, in the experimental prototype n=4 is selected

The minimum and maximum value of the duty cycle is determined using (7)

$$\mathrm{D_{min}} = 1 - \frac{(1+\mathrm{n})\mathrm{V_{in_{max}}}}{\mathrm{V_O}} = 1 - \frac{5\times 50}{400} = 0.375 \tag{44}$$

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$$D_{max} = 1 - \frac{(1+n)V_{in_{min}}}{V_O} = 1 - \frac{5\times30}{400} = 0.625 \quad (45)$$

Also, the nominal value of the duty cycle is determined as D=0.5

Using (31), in order to maintain the converter operates in CCM in half load (I_O=*0.5 A)* and maximum input voltage, the minimum value of the magnetizing inductance can be determined as

$$L_m(min) \geq \frac{0.375\times(1-0.375)^2\times400}{2\times100\times10^3\times25\times0.5} = 23.43\ \mu H \quad (46)$$

Finally, a coupled inductor with n=4 and $L_m = 39\ \mu H$ is utilized in the experimental prototype.

Moreover, the maximum value of the voltage across D_1, obtained from (11) is

$$V_{D1} = \frac{nV_{in(max)}}{1-D} = \frac{4\times40}{1-0.5} = 320\ V. \quad (47)$$

The voltage stress on D_2 is equal to the output voltage that is *400 V*.

The output capacitor current is equal to the output current in Mode 2. Therefore, the voltage ripple across this capacitor can be determined as

$$\Delta V_{Cout} = \frac{(1-D)I_O}{C_{out}f} \quad (48)$$

$$\text{Therefore,} \qquad C_{out(min)} = \frac{(1-D_{max})I_O}{f\Delta V_{Cout}} = \frac{(1-0.55)\times1}{100\times10^3\times4} = 1.125\ \mu F \quad (49)$$

As a result, a 1 µF ceramic capacitor is selected in the experimental prototype. At nominal input voltage, the output voltage ripple is slightly higher than 1% of the output voltage value. However, the output voltage ripple can be lower with increasing the size of output capacitor.

C_{dc} current is equal to the D_1 current during Mode 1. This capacitor is discharged in Mode 1 and its voltage is decreased. Therefore, the voltage ripple is

$$\Delta V_{Cdc} = \frac{DI_{D1}}{C_{dc}f} \quad (50)$$

Substituting (16) into (50) gives

$$\Delta V_{Cout} = \frac{I_O}{C_{dc}f} \quad (51)$$

That determines the minimum value of C_{dc} as

$$C_{dc}(min) \geq \frac{I_O}{f\Delta V_{Cdc(min)}} = \frac{1}{100\times10^3\times2.4} = 4.17\ \mu F \quad (52)$$

A 4.4 µF, 400 V ceramic capacitor is used in the experimental prototype.

Using (16) and (18) the maximum current stress on D_1 and D_2 can be obtained by

$$I_{D1_{max}} = \frac{I_o}{D_{min}} = \frac{1}{0.375} = 2.66\ A \quad (53)$$

$$I_{D2_{max}} = \frac{I_o}{1-D_{min}} = \frac{1}{1-0.6255} = 2.66\ A. \quad (54)$$

As a result, power diode C3D03060 with a DC blocking voltage *600 V* and continuous forward current at*11 A* at

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T_C=25^0C is selected for D_1 and D_2.

The maximum current stress on the power switch can be obtained using (21)

$$I_{Q_{max}} = \frac{(1+nD_{max})I_o}{D_{max}(1-D_{max})} = \frac{(1+4\times0.625)\times1}{0.625\times(1-0.6255)} = 14.93\ A. \quad (55)$$

Therefore, a power MOSFET IRFB4321PBF with V_{DS} =*150 V* and I_D = *85 A* is selected.

III. COMPARISON WITH CONVENTIONAL TOPOLOGIES

A. Comparison with conventional SEPIC converter

In this section, the proposed converter is compared with conventional coupled inductor SEPIC converter. The voltage gain in the proposed converter is higher for any duty cycle by adding only one diode. With higher voltage gain, the switch voltage stress in the proposed converter is lower than the conventional SEPIC converter when n>1. In order to achieve a high voltage gain, usually n is more than one, which helps to choose a low voltage and low $R_{DS,\ ON}$ MOSFETs. This can lead to lower conduction and switching loss and thereby the efficiency can be improved. Another feature of the proposed converter is that the current on the primary and secondary winding, power switch, intermediate capacitor (C_{dc} in compare with C_{ac}) is always lower than the conventional SEPIC converter when n ≥ 1. Table I compares the proposed Quasi-SEPIC converter with its conventional counterpart.

TABLE I.
COMPARISON OF THE PROPOSED CONVERTER FEATURES WITH CONVENTIONAL ISOLATED SEPIC CONVERTER

Parameters		SEPIC (Fig. 1(a))	Proposed quasi-SEPIC (Fig. 1(b))
Voltage gain expression $\left[\frac{V_O}{V_{in}}\right]$		$\frac{nD}{1-D}$	$\frac{1+n}{1-D}$
Total no. of components (including C_{in} and C_{out})		6	7
No. of switch		1	1
No. of diode		1	2
No. of capacitor		3	3
No. of coupled inductor		1	1
Voltage stress on switch Q		$\frac{n}{1-D}V_{in}$	$\frac{V_{in}}{1-D}$
Current stress on switchQ		$\frac{nDI_O}{D(1-D)}$	$\frac{(n+D)I_O}{D(1-D)}$
Voltage Stress on diode	D_1	$\frac{n}{1-D}V_{in}$	$\frac{n}{1-D}V_{in}$
	D_2	NA	$\frac{1+n}{1-D}V_{in}$
Voltage stress on capacitor	C_{ac}	nV_{in}	NA
	C_{dc}	NA	$\frac{1+nD}{1-D}V_{in}$
Current stress on winding	i_{N1}	Mode 1: $\frac{-n(n+1)I_O}{D}$ Mode 2: $\frac{(n+1)I_O}{1-D}$	Mode 1: $\frac{nI_O}{D}$ Mode 2: $\frac{nI_O}{1-D}$
	i_{N2}	Mode 1: $\frac{-(n+1)I_O}{D}$ Mode 2: $\frac{(n+1)I_O}{n(1-D)}$	Mode 1: $\frac{I_O}{D}$ Mode 2: $\frac{I_O}{1-D}$
Current stress on capacitor	C_{ac}	Mode 1: $\frac{-(n+1)I_O}{D}$ Mode 2: $\frac{(n+1)I_O}{1-D}$	NA
	C_{dc}	NA	Mode 1: $\frac{I_O}{D}$ Mode 2: $\frac{I_O}{1-D}$
Current stress on diode	D_1	$\frac{I_O}{1-D}$	$\frac{I_O}{D}$
	D_2	NA	$\frac{I_O}{1-D}$
Note: NA is not applicable.			

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B. Comparison with other converter with similar voltage gain

Higher boost converter topologies are also available in the literature using multi-stage and/or voltage multiplier cells or using multiple winding coupled inductors. However, for a fair comparison, only topologies with one two-winding coupled inductor type converter with one active switching device and similar voltage stress are considered for comparison. Hence quadratic boost type and topologies with two or more than two switches are excluded from the comparison along with three winding coupled inductor topologies. Table II compares the proposed converter with other two winding coupled inductor converters.

Topologies presented in [32]-[34] produce the same voltage gain as of the proposed topology; however the number of capacitors and diodes are higher than the proposed topology. With two magnetic elements in [35]-[37], these converters require more space whilst their voltage gains are significantly lower. Similarly, the voltage gain for the topology presented in [38] and [39] are higher than the proposed converter; however, the number of components is higher than the proposed topology. These two topologies are considered to be compared fair with the extended circuit of the proposed topology and hence will be discussed in Section IV. Fig. 9 compares the voltage gain of the proposed converter and the presented converters in [32]-[39].

TABLE II
COMPARISON OF THE PROPOSED CONVERTER WITH DIFFERENT TWO WINDING COUPLED INDUCTOR BASED SINGLE SWITCH HIGH VOLTAGE DC-DC CONVERTERS.

Ref.	Voltage Gain ($G_v = \frac{V_o}{V_{dc}}$)	Voltage Stress on Switch	No. of components				
			Coupled-inductor	L	D	C*	S/W
Proposed Converter	$\frac{1+n}{1-D}$	$V_{dc}/(1-D)$	1	0	2	3	1
Converter in [32]	$\frac{1+\mathrm{n}}{1-\mathrm{D}}$	$V_{dc}/(1-D)$	1	1	2	4	1
Converter in [33]	$\frac{1+\mathrm{n}}{1-\mathrm{D}}$	$V_{dc}/(1-D)$	1	1	4	5	1
Converter in [34]	$\frac{1+\mathrm{n}}{1-\mathrm{D}}$	$V_{dc}/(1-D)$	1	0	3	4	1
Converter in [35] and [36]	$\frac{D(1+\mathrm{n})}{1-\mathrm{D}}$	$V_{dc}/(1-D)$	1	1	2	2	1
Converter in [37]	$\frac{1+\mathrm{nD}}{1-D}$	$V_{dc}/(1-D)$	1	1	2	3	1
Converter in [38], And[39]	$\frac{1+\mathrm{n}+\mathrm{nD}}{1-\mathrm{D}}$	$V_{dc}/(1-D)$	1	0	4	5	1
*Including input and output capacitor							

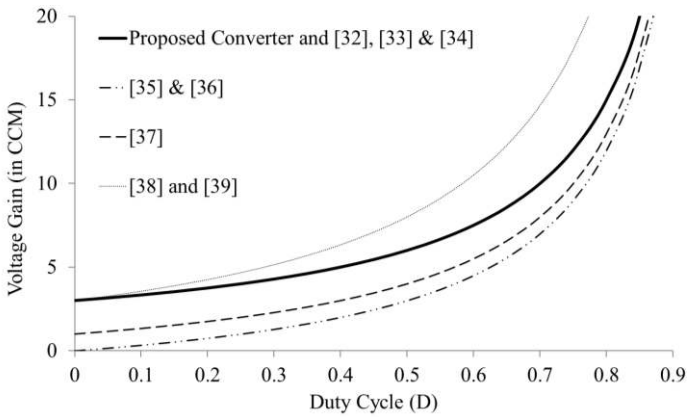

Fig. 9. Comparison of voltage gain of the proposed converter with different two-winding inductor based high boost single switch-switch dc-dc converter in CCM (n = 2).

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IV. DERIVATIVE CONVERTER WITH HIGHER VOLTAGE GAIN

The voltage gain of the proposed converter can be raised further by adding one diode and one capacitor to its structure as shown in Fig. 10. The output capacitor C_o is split into two capacitors (C_{o1} & C_{o2}) and D_3 is inserted between the negative terminal of the load and the secondary winding of the transformer. In CCM as shown in Fig. 11, there are two modes in one switching cycle. When the power switch is turned ON, the diode D_1 becomes forward biased while diodes D_2 and D_3 become reverse biased. When the power switch is turned OFF, the diode D_1 is turned OFF while D_2 and D_3 are ON. Similar analysis can be made for this extended gain converter as well.

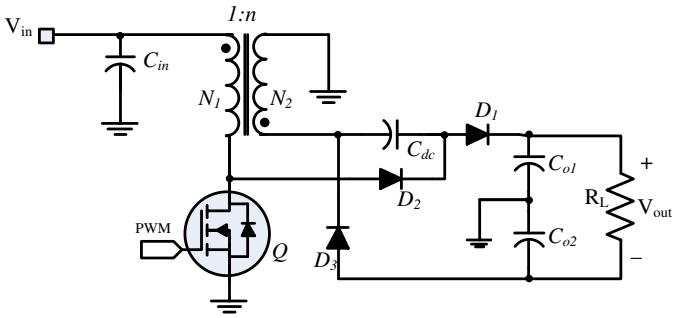

Fig. 10. Derivative circuit of quasi-SEPIC for higher voltage gain.

Appling the voltage-second balance principle on the magnetizing inductance leads to

$$DV_{in} + (1-D)\frac{V_{in}-V_{Cdc}}{1+n} = 0 \tag{56}$$

That results in

$$V_{Cdc} = \frac{1+nD}{1-D} \tag{57}$$

Using KVL in Mode 1

$$V_{Co1} = V_{Cdc} + nV_{in} = \frac{1+n}{1-D}V_{in} \tag{58}$$

Also, the voltage across V_{Co2} can be obtained using KVL in Mode 2

$$V_{Co2} = \frac{Dn}{1-D} \tag{59}$$

Therefore, the output voltage can be obtained using (58) - (59)

$$V_o = V_{Co1} + V_{Co2} = \frac{1+n+nD}{1-D}V_{in} \tag{60}$$

The voltage stress across the power switch and diodes can be expressed as given in the following equations

$$V_{D1} = \frac{nV_{in}}{1-D} \tag{61}$$

$$V_{D2} = \frac{(1+n)V_{in}}{1-D} \tag{62}$$

$$V_{D3} = \frac{nV_{in}}{1-D} \tag{63}$$

$$V_s = \frac{V_{in}}{1-D}. \tag{64}$$

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Comparing (61) – (64) with the output voltage, it is clear that the voltage stress on all semiconductor devices is lower than the output voltage. Particularly, although the voltage gain can be raised compared with the elementary converter proposed in Fig. 1, the voltage stress on the switch remains unchanged. Therefore, the power switch with low ON resistance ($R_{DS,ON}$) can be utilized that can lead to lower conduction loss and higher efficiency.

From the voltage gain view-point, the derivative of the proposed converter has equal voltage gain with converters that have been presented in [38]-[39]. However, there are fewer components in the proposed converter in Fig.10. Refer to Table II, there are five capacitors and four diodes in the presented converters in [38]-[39], while there are four capacitors and three diodes in the proposed extension of the converter shown in Fig. 11.

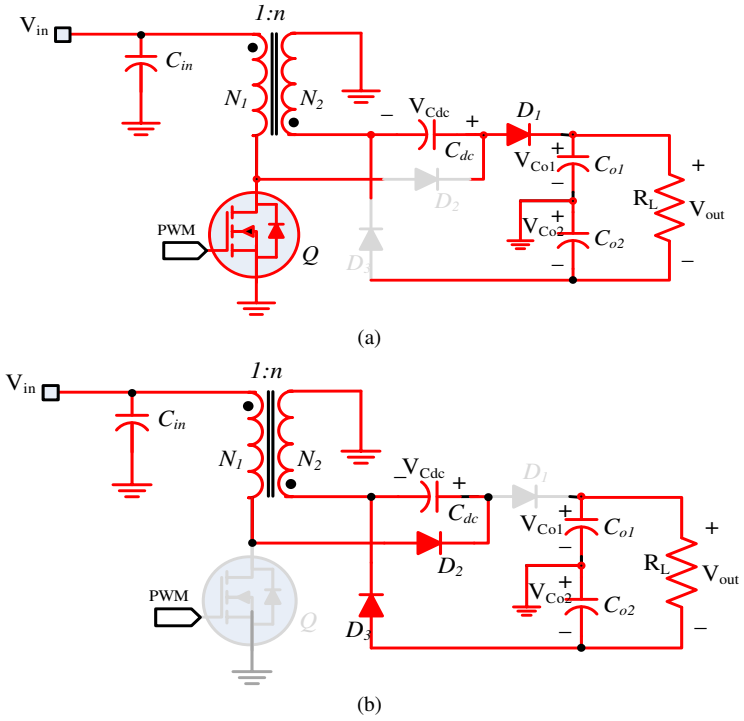

Fig. 11. Equivalent circuits during one switching cycle (a) Mode 1 (Q_{ON}), and (b) Mode 2 (Q_{OFF}).

V. Simulation and Experimental Results

Simulations were carried out in Matlab-Simulink with PLECS toolboxes included to verify the performance of the proposed converter. The converter was simulated with $N = 4$, $(N_1 : N_2 = 1 : 4)$, $D = 0.5$ and $f_s = 100\ kHz$. With these conditions, the output voltage is boosted to $V_O = 398$ V using a $V_{dc} = 40\ V$, which is consistent with (6) as shown in the sisth trace of Fig. 12 (a). The drain source voltage of the switch are around 80 V as shown in the first trace of Fig. 12 (b), which helps to select a low voltage and a low $R_{DS\text{-}on}$ switch. Other simulated waveforms are also noted to be in agreement with the theoretical values derived in Section-II. The performances expected from the converter are thus verified in simulations.

In order to verify the functionality and validate the reported analysis, a 400 W prototype of the proposed quasi-SEPIC converter (Fig. 1(b)) is implemented as shown in Fig. 13. This prototype is designed to achieve a voltage gain of 10

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from a dc input voltage (V_{in}) of 40 V, i.e. the output voltage (V_{out}) is set to be 400 V. Hence, for the selected value of $n = 4$, the duty cycle (D) is set to be 50 %. The parameters of this prototype are as listed in Table III, where these parameters are designed as explained before.

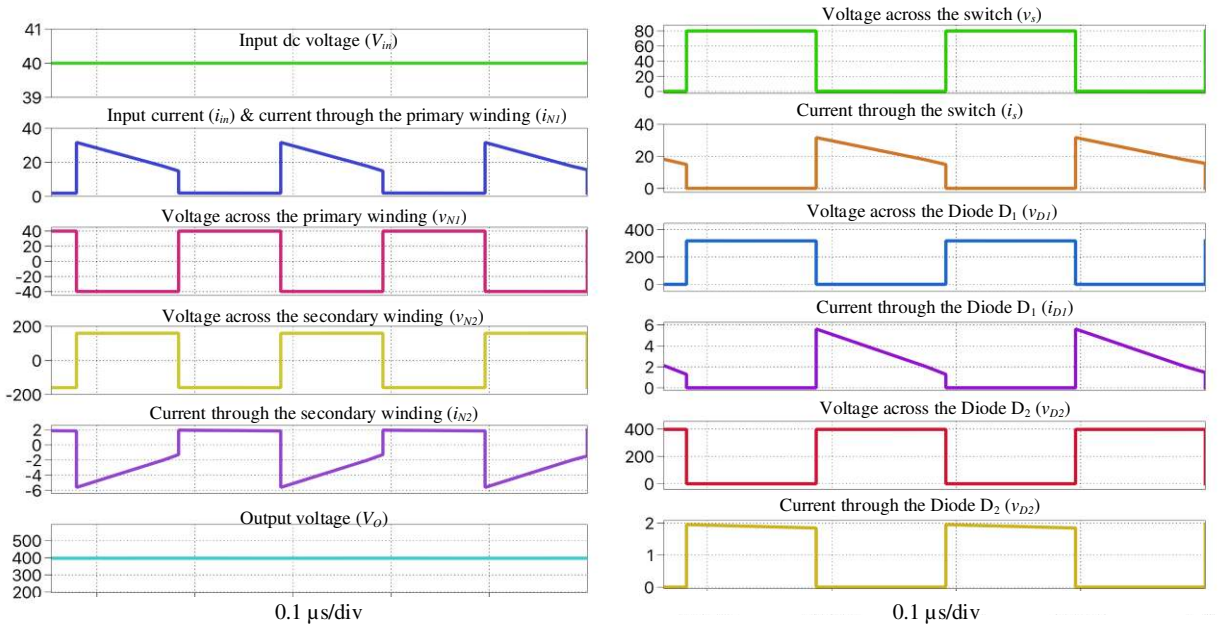

Fig. 12. Simulated waveforms of the proposed converter at $N = 4$, $D = 0.5$, $V_{in} = 40$ V and $f_s = 100\ kHz$ at full load: (a) input-output voltage and coupled inductor winding voltage/current waveforms, and (b) semiconductor voltage and current waveforms.

The steady-state open-loop experimental results of this prototype are shown in Fig. 14, in which Fig. 14(a) shows the output voltage (v_{out}), the voltage across C_{dc} ($v_{C_{dc}}$), and the voltage across the switch (v_s), while Fig. 14(b) shows the input current (i_{in}) and the switch current (i_Q) with v_s. Then, Fig. 14(c) shows the coupled inductors primary and secondary side voltages (v_{pr} and v_{sr} respectively) with v_s. Note that an output voltage of 385 V has been achieved at full-load under open-loop condition due to the voltage drop in the parasitic resistances and the non-ideal coupled inductors.

It is worth to note that this prototype utilizes an RCD snubber across the primary side in order to mitigate the effect of the leakage inductance of the coupled inductors and prevent the switch from any voltage spikes. In order to emphasize the importance of this snubber, Fig. 15 shows the voltage across the switch (v_s) without and with the RCD snubber at full-load. Fig. 15(a) shows v_s without the RCD snubber and the peak voltage of the spike is lower than the rated voltage of the switch, i.e. smaller that 150 V. Meanwhile, Fig. 15(b) shows v_s with the RCD snubber and the voltage is effectively clamped. Note that the coupled inductors have been implemented with an interleaved design in order to minimize the leakage inductance, minimize the snubber circuit requirements, and improve the efficiency as a consequence.

Finally, the efficiency of the proposed converter has been measured using KinetiQ PPA5530 power analyzer, and the obtained results are as shown in Fig. 16(a). This figure shows that a maximum efficiency of 96.2 % has been obtained.

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As shown in Fig. 16(b), the I^2R losses in the switch and the snubber accounts the major losses in the converter. This is as expected from the converter, as the current in the primary winding and hence the current in the switch is proportional to the voltage gain of the converter (55). However, the reduction of voltage stress on the switch helps to select a lower voltage and lower $R_{DS,on}$ switch with lower conduction loss. These different results verify the prior introduced analysis and discussions, and confirm the functionality of the proposed converter.

TABLE III
PARAMETERS OF THE 400 W QUASI-SEPIC CONVERTER PROTOTYPE

V_{in}	40 V	V_{out}	400 V
n	4	D	50 %
C_{dc}	4.4 μF	C_{out}	1 μF
f_s	100 kHz	L_m	39 μH

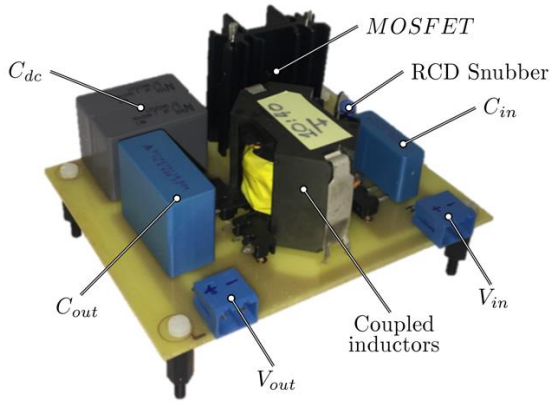

Fig. 13. A 400 W quasi-SEPIC converter prototype. Note that the converter diodes (D_1 and D_2) are on the bottom of the PCB.

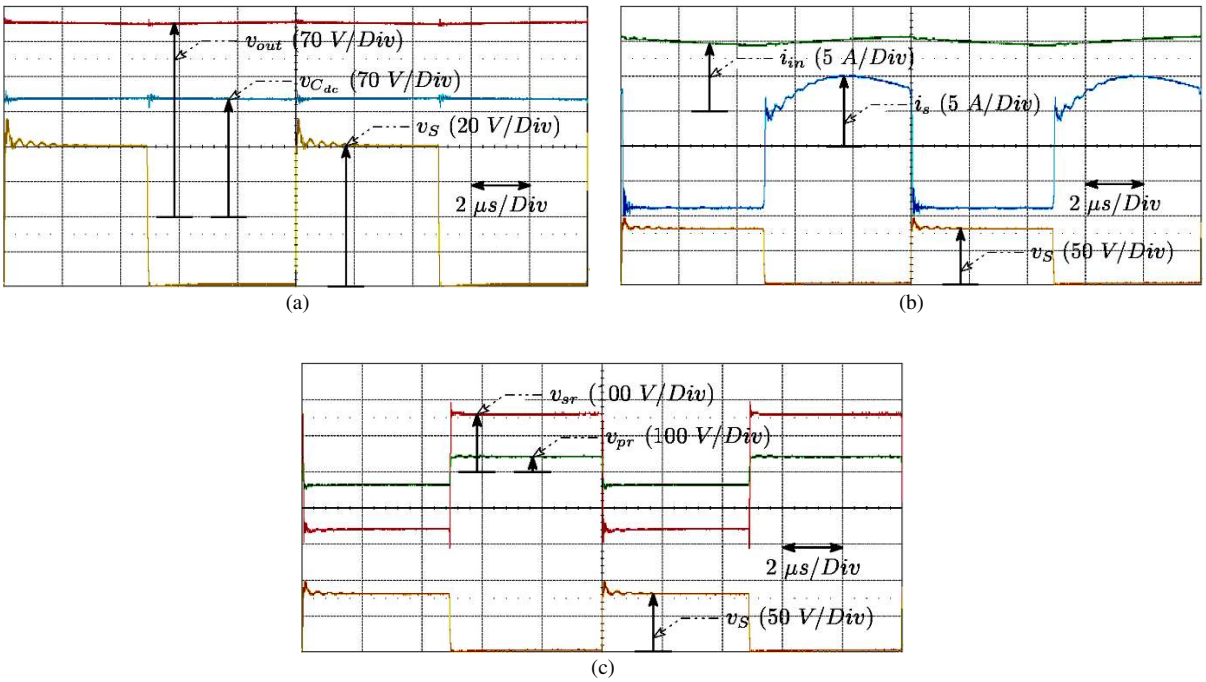

Fig. 14. Obtained steady-state experimental results of the 400 W quasi-SEPIC converter at full-load. (a) Output voltage (v_{out}), voltage across C_{dc} ($v_{C_{dc}}$), and voltage across the switch (v_s); (b) input current (i_{in}), switch current (i_s), and voltage across the switch (v_s); and (c) coupled inductors primary side voltage (v_{pr}), coupled inductors secondary side voltage (v_{sr}), and voltage across the switch (v_s).

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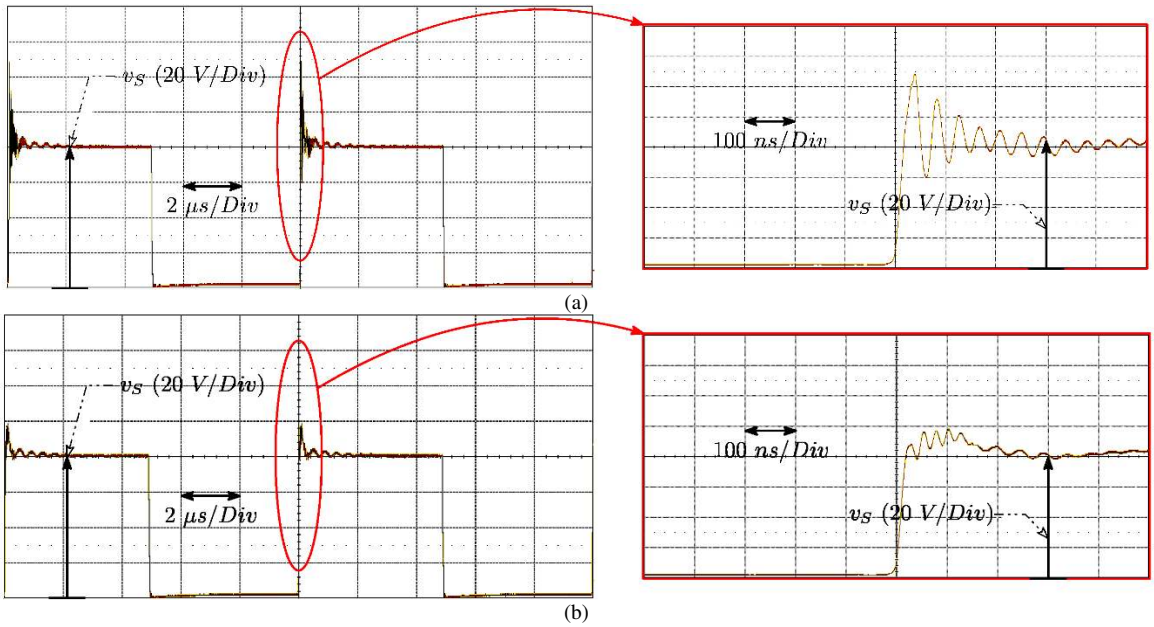

Fig. 15. Experimental results of the 400 W quasi-SEPIC converter switch voltage (v_s) at full-load, where (a) shows v_s without the RCD snubber, while (b) shows v_s with the RCD snubber.

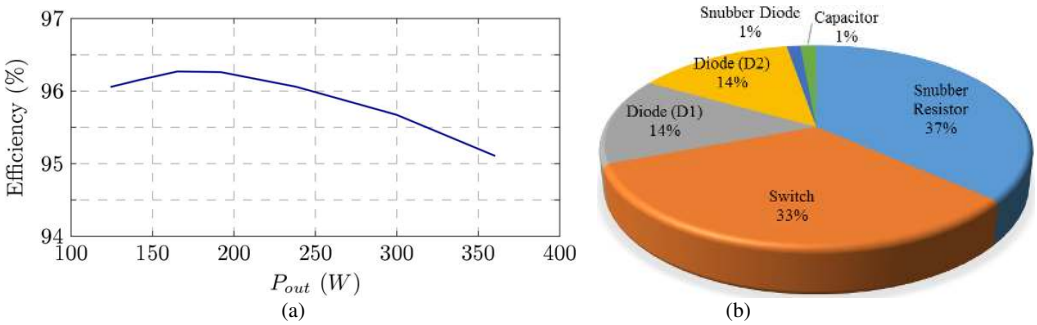

Fig. 16. (a) Measured efficiency of the 400 W quasi-SEPIC converter at a voltage gain of 10 (V_{in} = 40 V), and (b) major power loss distribution at full load.

VI. Conclusion

An efficient and high voltage gain modified coupled-inductor SEPIC dc-dc converter has been introduced in this paper with detailed theoretical explanations. Additionally, steady-state analysis and mathematical derivations of the proposed converter has been shown sequentially. Compared to equivalent topologies with similar voltage gain expression, the proposed topology uses lower component-counts to achieve the same or even higher voltage gain. This helps to design a very compact and light-weight converter with higher power density and reliability. The voltage stress on the switch is minimal, which helps the designer to use a low voltage and $R_{DS\text{-}on}$ MOSFET, resulting in a reduction in cost, conduction losses and turn ON losses of the switch. Simulation and experimental results have verified these features in addition to practicality of the proposed converter for various power applications.

The measured efficiency of the converter over a wide range of load is above 95% with a peak efficiency of 96% at a voltage gain of 10, which is comparatively higher than the conventional converter having similar voltage gains and power levels. These demonstrated performances clearly show the proposed topology as a competitive alternative for a practical application where a high voltage gain is demanded, such as for a fuel cells, PV and high voltage Light Emitting Diode (LED) lamps.

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