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High Voltage Gain Switched- Z-Source Bidirectional DC-DC Converter

Anish Ahmad[1,2], Sr. Member, IEEE, Md. Motiur Reza[2], Member, IEEE, Abdul R. Beig[2], Sr. Member, IEEE, Jamal Alsawalhi[2], Sr. Member, IEEE, Khaled Al Jaafari[2], Sr. Member, IEEE

[1]Department of Electrical Engineering, Tezpur University, Assam India

[2]Advanced Power and Energy Center, Department of Electrical Engineering and Computer Science, Khalifa University, Abu Dhabi, UAE

Corresponding author: Anish Ahmad (e-mail: anishahmad.ee@gmail.com).

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ABSTRACT: The DC-DC converters are the essential modules in electric vehicles, grid interface of renewable energy sources and DC power supplies. This paper presents a novel high gain bidirectional switched Z-source DC-DC converter. The proposed bidirectional converter utilizes switched-capacitor concept with inductors for high voltage gain. The proposed bidirectional converter presents wide operating range of operation in both boost and buck mode of operation. The proposed converter has common ground between input and output, and uses only 5 active switches and 4 passive elements with reduce switch voltage stress. The current drawn from the low voltage side input source is continuous with reduced ripple. The operating principle, circuit analysis, design, mathematical model and closed loop operation of the proposed converter are presented. The proposed converter is verified through computer simulation and laboratory experiments. The simulation and experimental results are presented.

INDEX TERMS: Switched Boost converter, Switched Capacitor, DC-DC converters, Bidirectional Converter, High Voltage conversion

I. INTRODUCTION

High voltage gain DC to DC converters are used in a variety of applications such as electric vehicles, renewable energy systems, battery-powered systems, battery chargers, uninterrupted power supplies and grid interface of DC storage systems [1]. Most of these applications prefer bidirectional energy flow so the same converter should act as Boost with high gain in one direction and buck with a high reduction in the reverse direction. One typical example is electric vehicles (EV). The schematic of EV is shown in Fig. 1. In EV battery DC bus is connected to the DC bus of the inverter. The DC bus of inverter need to be at high voltage DC levels (say 400V to 1.2kV) and the battery DC bus is preferred to be with low voltage (LV) DC levels say 12V to 96V [2]. Similar requirements can be seen, in grid interfaced photovoltaic (PV) sources and microgrids with battery energy storage systems (BESS) [3-4]. The conventional bidirectional DC-DC converters have a low voltage conversion ratio [5-6]. To enhance the voltage conversion ratio, several techniques are reported in the literature such as cascading techniques, switched inductor, switched capacitor, coupled inductor topologies. The wide voltage conversion ratio is achieved with the cascading of converters. The major drawback of cascading is that it suffers from large numbers of passive components, and multi-stage conversion leads to poor power efficiency and poor reliability [7-8]. Switched inductor and switched capacitor topologies give improved voltage conversion but a high number of passive components make them bulky and these are switched with the help of diodes/switches, which leads to increased parasitic and decreased efficiency [9-21]. The coupled inductor topologies have voltage conversion ratio but suffer from leakage inductance problems [22]. The maximum voltage conversion ratio is 3 or less than 3 for a non-isolated bidirectional converter [23,1,2]. The converters having higher voltage conversion ratios also suffers from high current stress at the input terminals [24]. In order to reduce THD sometime two identical Z-source converters are used, but number of

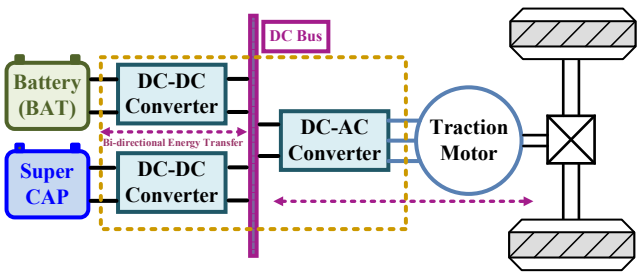

FIGURE 1. Converters in EV/HEV applications.

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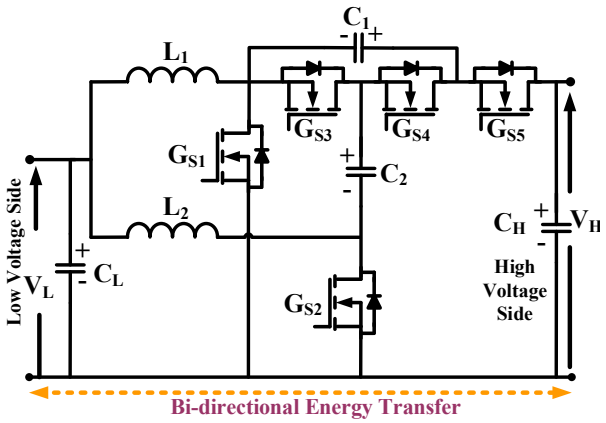

FIGURE 2. Circuit diagram of proposed Z-source switched bidirectional DC-DC converter

components are higher [25]. Due to non-availability of high gain DC –DC, some systems connect the battery cells in series to form high voltage DC bus and DC-DC converter with a low gain is used to interface with the inverter DC bus. However, there are severe problems in series-connected battery cells. Voltage balancing, cell matching are the challenges when replacing a faulty cell in an aging pack of series-connected cells. So, it is desirable to have converter with high voltage conversion ability to avoid series-connection of battery cells [26-28].

The above limitations have motivated the authors to develop a high gain switched Z- source bidirectional DC-DC converter [29]. In this paper, the detailed circuit analysis, effect of circuit parasites on circuit performance, loss calculation, simulation results for higher power rating and experimental verification are given. The proposed converter combines the features of switched boost and alternate pulse width modulation (PWM) control strategies. The main contribution and advantages of the converter are given as follows

1) The boost mode gain is always greater than 6 as against the maximum gain of 3 reported in the many literatures.
2) The proposed converter has bidirectional energy flow capability and seamless energy transfer from low voltage side to high voltage side and vice versa is possible.
3) The current stress on the input side inductor is reduced and the current ripple of the input current that is the current drawn from the battery is low.
4) The converter has common ground between the input and output sides.
5) Number of passive elements and active switches is low.
6) The voltage and current stress on devices are low.
7) Wide variation of voltage conversion is achieved.

The paper is organized as follows. The operating principle of converter and PWM strategies are discussed in section II. The steady-state analysis for boost and buck mode of operations are presented in section III. The design criteria for converter design are presented in section IV. The power loss analysis and comparative analysis with other bidirectional converters are discussed in section V and VI respectively. The small signal modelling and controller design are discussed in section VII. The simulation and experimental verifications are given in section VIII and section IX respectively. Finally, conclusions are given in section X

II. OPERATING PRINCIPLE OF Z-SOURCE SWITCHED BIDIRECTIONAL CONVERTER

The proposed Z-source switched bidirectional DC-DC converter is shown in Fig. 2. The proposed Z-source converter consists of two inductors (L_1 ,L_2), five switches (S_1, S_2, S_3, S_4 and S_5), and two capacitors (C_1,C_2). The filter capacitors are C_H at the high voltage (HV) side and C_L low voltage (LV) side. The proposed Z-source converter can be operated in boost mode as well as buck mode. Operating only two switches S_1 and S_2 leads to boost mode of operations and energy is transferred from LV to HV. In buck mode of operation, only switches S_3, S_4 and S_5 are operated and energy is transferred from HV to LV. So, if the unidirectional converter is required, it requires only two active switches (S_1 & S_2) and 3 diodes for boost operation and only 3 active switches (S_3, S_4 & S_5) and two diodes for buck operation. The equivalent circuits for boost mode of operation and buck mode of operation are shown in Fig 3 and Fig 4 respectively.

A. OPERATING PRINCIPLE OF BOOST MODE

In the boost mode operation, the two switches S_1 and S_2, are gated and other three switches S_3, S_4 and S_5 are permanently OFF. The gate pulses (G_{s1} & G_{s2}) for switches S_1 and S_2 are complementary as shown in Fig 5 (a) trace 1 and 2. In boost mode only the body diode of S_3, S_4 and S_5 participate in energy transfer, so the gate pulses are off that is $G_{s3} = G_{s4} = G_{s5} = 0$. The ON time is described as $T_{ON} = DT$, where T is the switching period, D is the duty cycle given by $D = T_{ON}/T$ and $(1-D)T$ is OFF time. When S_1 is ON, S_2 is OFF, the equivalent circuit is shown in Fig. 3(a) and 3(b) for DT interval and (1-D)T interval respectively and corresponding theoretical waveforms are shown in Fig 5(a). The inductor current i_{L1} is charged up to maximum value and inductor current i_{L2} discharges energy from their maximum value. The energy from LV source (V_L) is stored in L_1 and the energy stored in L_2 in the previous cycle is transferred to capacitors C_1 and C_2 through anti-parallel diode of S_4 as shown in Fig. 3(a). When S_1 is OFF and S_2 is ON (i.e $(1-D)T$), the equivalent circuit is presented in Fig. 3(b). The energy from LV source (V_L) is stored in L_2 and the energy stored in L_1 in the previous cycle is transferred to output HV side capacitor (C_H) through anti-parallel diode of S_5 as shown in Fig. 3(b). Part of this energy is used to reset the voltage across C_2 through antiparallel diode across switch S_3. The inductor current waveforms (i_{L1} and i_{L2}) are is shown in Fig. 5(a). From Fig. 5(a) it is clear that the charging and discharging are opposite in the boost mode of

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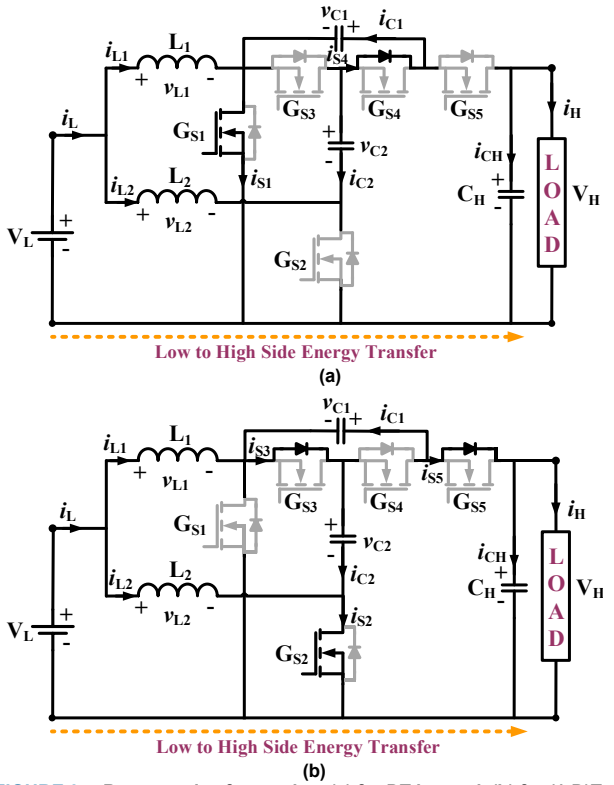

FIGURE 3. Boost mode of operation, (a) for DT interval, (b) for (1-D)T interval

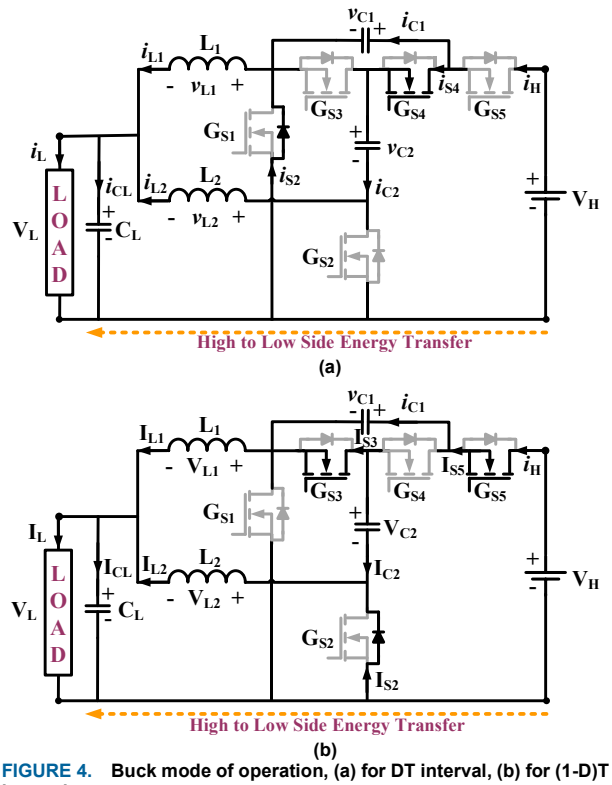

FIGURE 4. Buck mode of operation, (a) for DT interval, (b) for (1-D)T interval

operations. Since, total input current form source $i_L = i_{L1} + i_{L2}$, the ripple current (Δi_L) in input source current i_L is reduced. The voltage across the inductors (V_{L1} and V_{L2}), and voltage across the switches (V_{s1} and V_{s2}) are shown in Fig. 5(a).

B. OPERATING PRINCIPLE OF BUCK MODE

In buck mode of operation, the energy flow is from HV side to LV side. Fig. 4 shows the equivalent circuits for the buck mode of operation. In the buck mode the switches (S_3, S_5) and switch S_4 operated alternately. The switches S_1, and S_2 are permanently OFF but only the body diodes of the switches S_1, and S_2 participate in the energy transfer. The gate pulses (G_{s4}) and (G_{s3} , G_{s5}) for switches S_4 and (S_3, S_5) are complementary as shown in Fig 5 (b) traces 1, 2 and 3. The gate pulses for S_1 and S_2 is zero as only antiparallel body diode of these MOSFETS participate in energy transfer. During DT interval only S_4 is ON, and both S_3 and S_5 are OFF. During this interval, the inductor current i_{L2} keep charging whereas inductor current i_{L1} discharges its energy. For $(1-D)T$ interval, only the switch S_4 is OFF, and both S_3 and S_5 are ON and the switch S_2 body diode participate in energy transfer as shown in Fig. 5 (b). In buck mode the ripple current (Δi_L) in LV side input source current i_L is reduced because the ripple currents in inductors L_1 and L_2 are opposite to each other and $i_L = i_{L1} + i_{L2}$. The voltages across inductors and switches are given in Fig. 5(b).

III. STEADY STATE ANALYSIS

A. BOOST MODE

The equivalent circuits shown in Fig. 3(a) are utilized for the inductor voltages and capacitors current expressions. The expressions for the DT interval are written as follows,

$$v_{L1} = V_L \text{ and } v_{L2} = V_L - v_{C1} + v_{C2} \quad (1)$$

$$i_{C1} = i_{L2},\ i_{C2} = -i_{L2} \text{ and } i_{CH} = -i_H \quad (2)$$

From Fig. 3(b), for the interval $DT \le t \le (1-D)T$, the inductor voltages and capacitors current expression are written as follows,

$$v_{L1} = V_L - v_{C2} \text{ and } v_{L2} = V_L \quad (3)$$

$$i_{C1} = i_{c2} - i_{L1};\ i_{C2} = i_{L1} + i_{c1} \text{ and } i_{CH} = -i_{c1} - i_H \quad (4)$$

Applying volt-seconds balance principle to the L_1 and L_2 over one switching interval, capacitor voltages at steady state are calculated as:

$$V_{C1} = \frac{V_L}{D(1-D)} \quad \text{and} \quad V_{C2} = \frac{V_L}{(1-D)} \quad (5)$$

$$V_H = V_{C1} + V_{C2} = \frac{(1+D)V_L}{D(1-D)} \quad (6)$$

Applying capacitor charge balance principle to the capacitors over one switching interval, the current relations are calculated as:

$$I_{L1} = \frac{2I_H}{(1-D)} \quad ; \quad I_{L2} = \frac{I_H}{D} \quad \text{and } I_H = \frac{D(1-D)I_L}{(1+D)} \quad (7)$$

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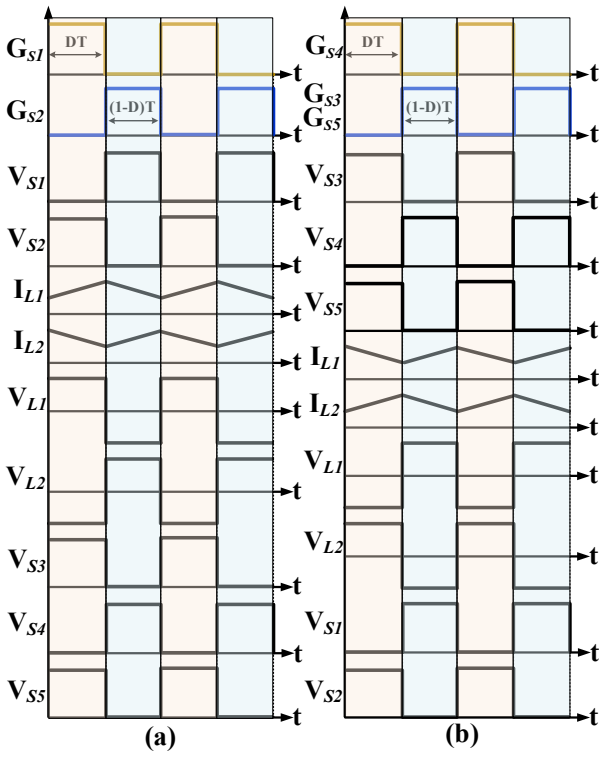

FIGURE 5. Typical waveform (a) Boost mode (b) Buck mode

The boost voltage conversion ratio $G = V_H/V_L$ is calculated from (6). It is clear from (6) that minimum boost gain 5.82 occurs at $D = 0.586$.

B. BUCK MODE

The equivalent circuit for buck mode operation for the interval DT is shown in Fig. 4(a) and the inductor voltages, capacitors current expressions are written as follows,

$$v_{L1} = -V_L; \quad v_{L2} = -V_L + v_{C1} - v_{C2} \tag{8}$$

$$i_{C1} = -i_{L2}; \quad i_{C2} = i_{L2} \text{ and } i_{CH} = i_H \tag{9}$$

The equivalent circuit for buck mode in the interval $(1-D)T$ is showing in Fig. 4(b). The inductor voltages and capacitor current expressions are written as follows,

$$v_{L1} = -V_L + v_{C2} \quad \text{and} \quad v_{L2} = -V_L \tag{10}$$

$$i_{C1} = i_{C2} + i_{L1} \text{ and } \quad i_{C2} = -i_{L1} + i_{C1} \tag{11}$$

$$i_{CH} = -i_{c1} + i_H \quad \text{and} \quad i_{CL} = i_{L1} + i_{L2} - i_L \tag{12}$$

Applying volt-seconds balance principle to the L_1 and L_2 over one switching interval, capacitor voltages are calculated as:

$$V_{C1} = \frac{V_H}{(1+D)} \quad \text{and} \quad V_{C2} = \frac{DV_H}{(1+D)} \tag{13}$$

The buck voltage conversion ratio $G = V_L/V_H$ is given by (14)

$$V_L = \frac{D(1-D)V_H}{(1+D)} \tag{14}$$

Applying capacitor charge balance principle to the capacitors over one switching interval, the current relations are calculated as:

$$I_{L1} = \frac{(1+D)I_H}{(1-D)} \; ; \; I_{L2} = \frac{(1+D)I_H}{D} \quad \text{and } I_H = \frac{D(1-D)I_L}{(1+D)} \tag{15}$$

It is clear from (14) that the minimum buck voltage conversion ratio of 0.17 is when D =0.414. The buck voltage ratio is reciprocal of boost voltage gain.

From (6) and (14) it is clear that wide range of voltage conversion ratio is achieved by varying D in both boost mode as well as buck mode operation.

IV. DESIGN CRITERIA & SELECTION OF COMPONENTS

The desired value of the inductors and capacitors are calculated on the basis of allowable current ripple and voltage ripple respectively. In order to ensure the continuous conduction mode (CCM) operation it is important to select the desired value.

The inductors and capacitors values are obtained as follows

$$L_i = \frac{DV_{Li}}{\Delta i_{Li}\, I_{Li}\, f} \quad \text{and} \quad C_i = \frac{DI_{cj}}{\Delta V_{ci}\, V_{ci}\, f} \tag{16}$$

where i = 1 and 2 and j = 1, 2 and 3. V_{L1} and V_{L2} are the voltages across the inductors L_1 and L_2, I_{L1} and I_{L2} are the currents flowing through L_1 and L_2, Δi_{L1} and Δi_{L2} represent ripple currents in L_1 and L_2. V_{c1} and V_{c2} are the voltages across the capacitors C_1 and C_2, $I_{c1}$and I_{c2} are the currents flowing through C_1 and C_2. ΔV_{c1} and ΔV_{c2} represent percentage ripple voltages in C_1 and C_2 and f is the switching frequency. The design procedures for boost as well as buck mode are same as, for the proposed bidirectional converter the ripple will be same for boost mode as well as buck mode of operations. Let ΔV_{cH} be the ripple voltage across C_H. The capacitor on high voltage side is given by

$$C_H = \frac{D^2(1-D)I_H}{\Delta v_{cH}\, f\, (1+D)\, V_L} \tag{17}$$

For the converter to operate in continuous conduction mode (CCM) the critical values of the inductors are

$$L_{1CR} = \frac{D(1-D)V_L}{\Delta i_{L1}\, f\, 4\, I_H} \quad \text{and} \quad L_{2CR} = \frac{D(1-D)V_L}{\Delta i_{L1}\, f\, 2\, I_H} \tag{18}$$

The inductor values in (18) are the minimum inductor values for the continuous conduction operations. The selection of voltage and current rating of switches are based on the peak reverse voltage across the switches as well as peak current through the switches.

V. POWER LOSS ANALYSIS

The power loss analysis of the bidirectional converter has three factors 1) losses in switches, 2) losses in diodes and 3) losses in passive elements.

Let t_r and t_f are the rise time and fall time respectively, f is the switching frequency. For boost mode of operation, the switching losses for the switches S_1 and S_2 are given as

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TABLE I
COMPARASION WITH SIMILAR CONVERTERS

Topology	QB [7]	ZSC [9]	[11]	BHDC [19]	SQ [24]	Proposed
L count	2	2	2	2	2	2
C count	1	2	1	2	2	2
Switches	2	2	4	3	3	5
Boost Gain	$\frac{1}{(1-D)^2}$	$\frac{1}{1-2D}$	$\frac{1}{(1-D)^2}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{(1+D)}{D(1-D)}$
Buck Gain	D^2	$2D-1$	D^2	$\frac{D}{2-D}$	$\frac{D}{2-D}$	$\frac{D(1-D)}{(1+D)}$
Peak Switch votlage stress	$\frac{1}{(1-D)^2}$	$\frac{1}{1-2D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Peak Capacitor voltage stress	$\frac{1}{(1-D)^2}$	$\frac{1-D}{1-2D}$	$\frac{2-D}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$
Curent ripple in LVS	Low	High	Medium	Low	Low	Very Low
(SDP/P_o) max	$\frac{4-4D+2D^2}{(1-D)^2}$	$\frac{3}{1-3D+2D^2}$	$\frac{4}{1-D}$	$\frac{4+D}{1-D^2}$	$\frac{4}{1-D^2}$	$\frac{2+D+D^2}{D(1-D^2)}$
Rated Power	50 W	1000W	160 W	2000W	300W	300 W
Max. efficiency boost mode	94%	/	96.5%	98.6%	96.44 %	97.5%
Max. efficiency buck mode	93%	/	94.2%	/	96.24 %	96.7%
Common Ground	Yes	No	Yes	No	Yes	Yes

$$P_{SW_{S1}} = \frac{1}{2}V_{C2}(I_{L1} + I_{C1})(t_r + t_f)f \quad (19)$$

$$P_{SW_{S2}} = \frac{1}{2}(V_{C1} - V_{C2})(I_{L2} + I_{C2})(t_r + t_f)f \quad (20)$$

Similarly, for buck mode of operation the switching losses for the switch S_3, S_4 and S_5 can be written as

$$P_{SW_{S3}} = \frac{1}{2}V_{C1}(I_{L1} - I_{C1})(t_r + t_f)f \quad (21)$$

$$P_{SW_{S4}} = \frac{1}{2}V_{C1}\, I_{L2}(t_r + t_f)f \quad (22)$$

$$P_{SW_{S5}} = \frac{1}{2}(V_H - V_{C1})\, I_H(t_r + t_f)f \quad (23)$$

The conduction losses for boost mode of operation are calculated as

$$P_{CO_{S1}} = R_{ON}(I_{L1} + I_{C1})^2 D \quad (24)$$

$$P_{CO_{S2}} = R_{ON}(I_{L1} + I_{C2})^2 D \quad (25)$$

Similarly, for buck mode of operation the conduction losses are given by (26)-(28)

$$P_{CO_{S3}} = R_{ON}(I_{L1} - I_{C1})^2 D \quad (26)$$

$$P_{CO_{S5}} = R_{ON} I_{L2}^2 D \quad (27)$$

$$P_{CO_{S5}} = R_{ON} I_H^2 D \quad (28)$$

For boost mode of operation the body diode of the switch S_3, S_4 and S_5 operates. So, the switching losses for the boost mode operation is given as

$$P_{SW_{S3}} = P_{SW_{S4}} = fQ_r V_{C1} \quad (29)$$

$$P_{SW_{S5}} = fQ_r(V_H - V_{C1}) \quad (30)$$

where Q_r is the reverse recovery charge of the diode.

Similarly, for buck mode of operation the switching losses in the body diode of the switches S_1 and S_2 are calculated as

$$P_{SW\_S1} = fQ_r V_{C2} \quad (31)$$

$$P_{SW\_S2} = fQ_r(V_{C1} - V_{C2}) \quad (32)$$

The average conduction losses in the body diodes of the MOSFET during boost mode of operation are given as

$$P_{CO\_S3} = (I_{L1} + I_{C1})(1-D)V_F = I_H(1+D)V_F \quad (33)$$

$$P_{CO\_S4} = (I_{C1})DV_F = I_H V_F \quad (34)$$

$$P_{CO\_S5} = (I_{C1})(1-D)V_F = I_H(1-D)V_F \quad (35)$$

Similarly, the average conduction losses in the body diodes of the MOSFET during buck mode of operation are given as

$$P_{CO\_S1} = (I_{L1} - I_{C1})DV_F = \frac{1+D}{1-D} I_H V_F \quad (36)$$

$$P_{CO\_S2} = (I_{L2} - I_{C2})(1-D)V_F = \frac{1-D^2}{D} I_H V_F \quad (37)$$

whereas V_F is the forward voltage drop across the body diode of the switch. The equivalent series resistor (ESR) losses of the inductors and capacitors are calculated as

$$P_{ESR} = I_{rms} r_d \quad (38)$$

Where r_d is the DC equivalent resistance in case of an inductor and ESR in case of capacitance and I_{rms} is the

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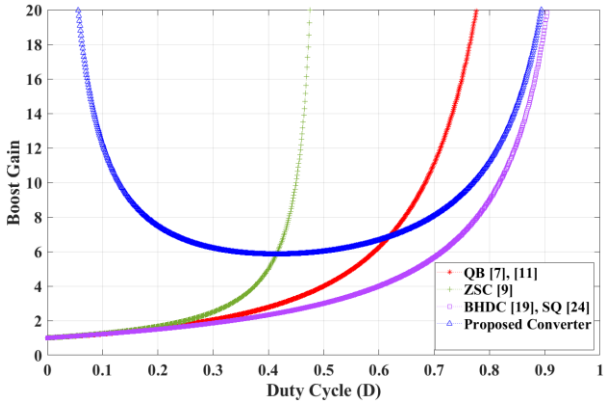

FIGURE 6. Boost mode voltage gain comparison

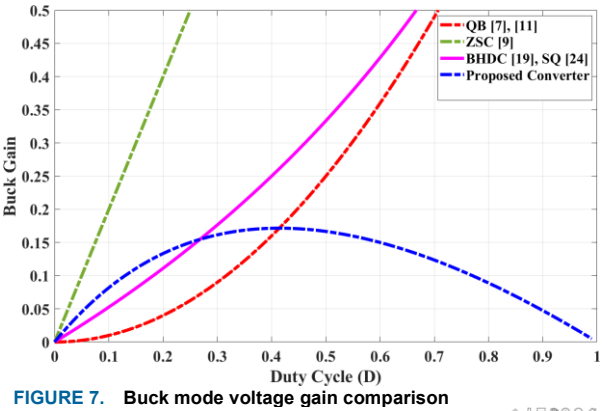

FIGURE 7. Buck mode voltage gain comparison

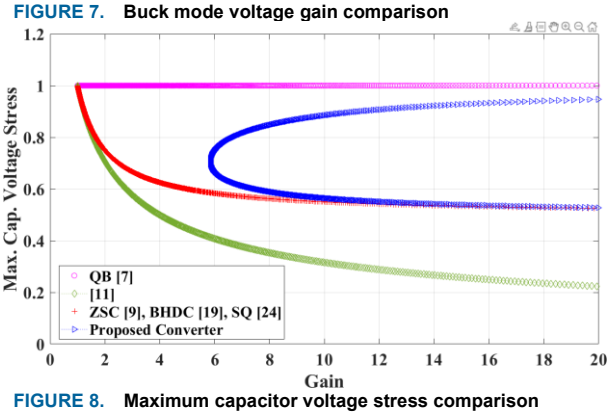

FIGURE 8. Maximum capacitor voltage stress comparison

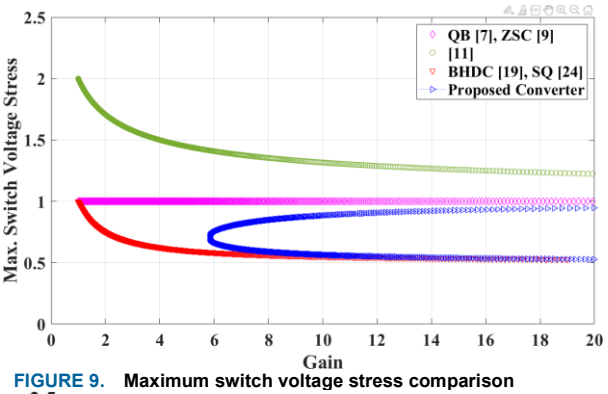

FIGURE 9. Maximum switch voltage stress comparison

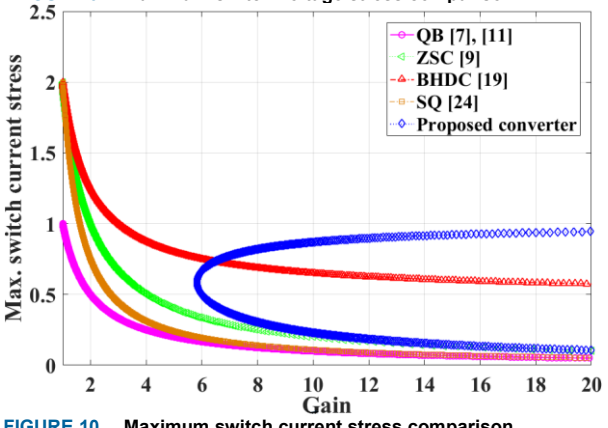

FIGURE 10. Maximum switch current stress comparison

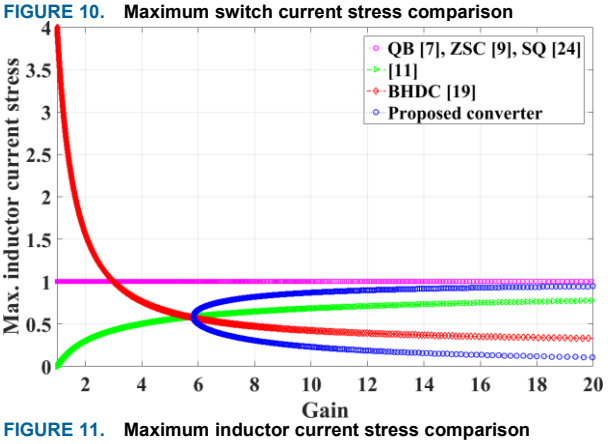

FIGURE 11. Maximum inductor current stress comparison

RMS current through the passive elements. The total efficiency for boost mode of operation and buck mode of operation are calculated from (19) - (38).

VI. COMPARATIVE ANALYSIS

The proposed Z-source converter is compared with the closely related bidirectional converter having similar characteristic. The comparative analysis in terms of voltage gain (both buck and boost mode), number of components, peak switch voltage stress, peak capacitor voltage stress, low voltage side (LVS) current ripple, maximum switching device power (SDP) value, efficiency and common ground are given in Table I.. The table shows that the number of passive components is same as that of other conventional bidirectional converters and the proposed converter has comparable number of switches with the others. However, additional switch is utilised for bidirectional operation. The boost mode of gain is compared with the other converters as shown in Fig. 6. From Fig. 6, it is clear that proposed converter has high voltage gain and also have wide range of duty cycle operation capability. The problem with the conventional ZSC [9] is that its performance is degraded after gain 4. The converter in [11], [19] and [24] need to operate high duty cycle to achieve high voltage conversions which is not recommended from the control point of view. Similarly, the buck mode voltage conversion comparison is given in Fig. 7. It is clear that the proposed converter operates for wide and high voltage conversion ratio. The converters in [11], [19] and [24] achieve higher buck conversion only for low duty cycles (D < 0.4) again not a

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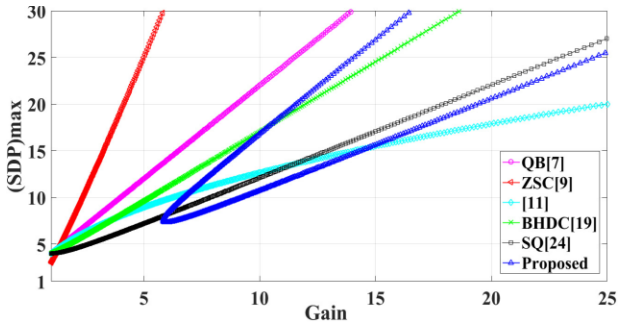

FIGURE 12. Maximum switching device power (SDP) comparison with gain

TABLE II
CONVERTER PARAMETERS

Parameter	Value	Parameter	Value
L_1	170 µH	L_2	340 µH
C_1	220 µF	C_2	300 µF
C_L	2200 µF	C_H	96 µF
r_{L1}	27 mΩ	r_{L2}	52 mΩ
$r_{C1} = r_{C2}$	20 mΩ	V_D	0.8 V
f	50 kHz	$\Delta i_{L1} = \Delta i_{L2}$	20%
$\Delta V_{c1} = \Delta V_{c2}$	1%	r_{dson}	19 mΩ

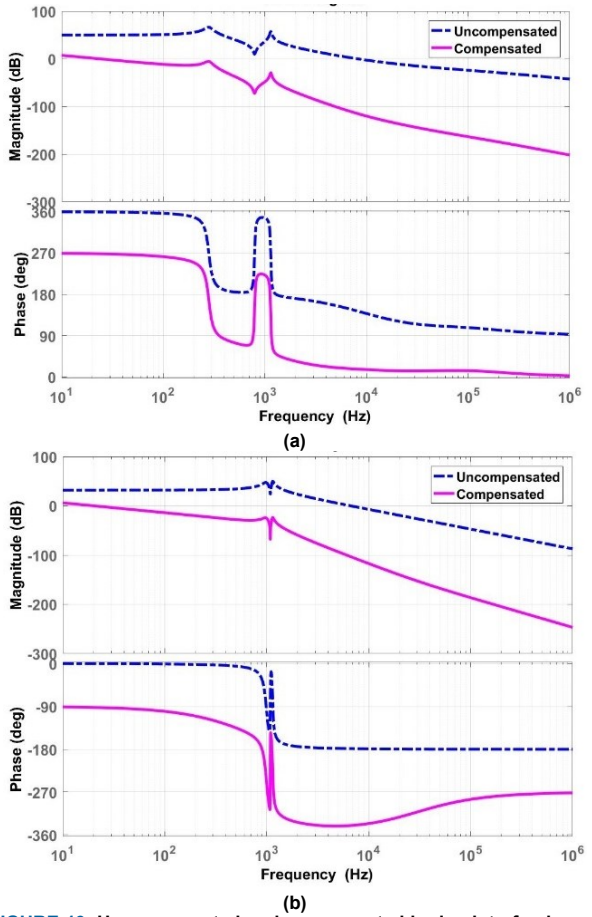

FIGURE 13. Uncompensated and compensated bode plot of gain and phase (a) Boost Mode (b) Buck Mode

useful criterion for control operation. The maximum capacitor voltage stress comparisons are given in Fig. 8. It shows that converter [7] has highest capacitor voltage stress. Moreover, the proposed converter capacitor stress is comparable with [11]. The maximum capacitor voltage stress of proposed converter is same as that of [9], [19] and [24]. Fig. 9 shows that the proposed Z-source converter has less switch voltage stress compared to [7], [9], [11], [19] and [24]. The maximum switch current stress comparison is shown in Fig. 10. The switch current stress is low for the proposed Z-source converter compared to that of [7], [9], [11], [19] and [24]. The maximum SDP rating is decided by peak voltage across the switch and average current flowing through the device, as per the comparative analysis in Fig. 9 and Fig. 10, the voltage stress of the switch and current stress of the switches are less in the proposed converter compared to the other converters. The maximum inductor current stress comparisons are shown in Fig.11. From Fig. 11, it is clear that the proposed converter has least inductor current stress as compared to that of [7], [9], [11], [19], and [24]. So, the components stress factor (CSF) of the proposed converter is comparable as per Fig.9, Fig. 10 and Table I. The maximum SDP variation with boost operation gain is given in Fig. 12. The mathematical expression of SDP w.r.t output power is given in Table I. From Fig. 12, it can be concluded that the proposed converter has low SDP compared to other converters. The proposed converter has very low current ripple in the low voltage side source compared to other converters, this is due to proposed alternating switching PWM. The proposed Z-source converter has higher efficiency in the boost mode as well as buck mode. The power rating used for efficiency measurement is given in Table I The experimentally measured efficiency for buck and boost mode for stated operating point are 97.5 % and 96.7% respectively. The comparative analysis shows that the proposed converter has high voltage gain over wide duty cycle, low switch voltage stress, higher efficiency, low voltage ripple in low voltage side and common ground as compared to the conventional converters.

VII. SMALL SIGNAL MODELING AND CONTROLLER DESIGN

The control signal to output transfer function for both mode (i.e., Boost mode of operation and Buck mode of operation) are given below.

A. SMALL SIGNAL ANALYSIS FOR BOOST MODE OF OPERATIONS

Let r_{L1}, r_{L2} are the parasitic DC resistances of the inductors L_1 and L_2. Let r_{C1}, r_{C2}, r_H are the ESR of the capacitances C_1, C_2 and C_H respectively. The components specifications are given in Table II.

After applying perturbation and linearization technique to equations leads to following state space model.

$$K\hat{x} = A\hat{x} + B\hat{v}_L + [(A_1 - A_2)X + (B_1 - B_2)V_L]\hat{d} \qquad (39)$$

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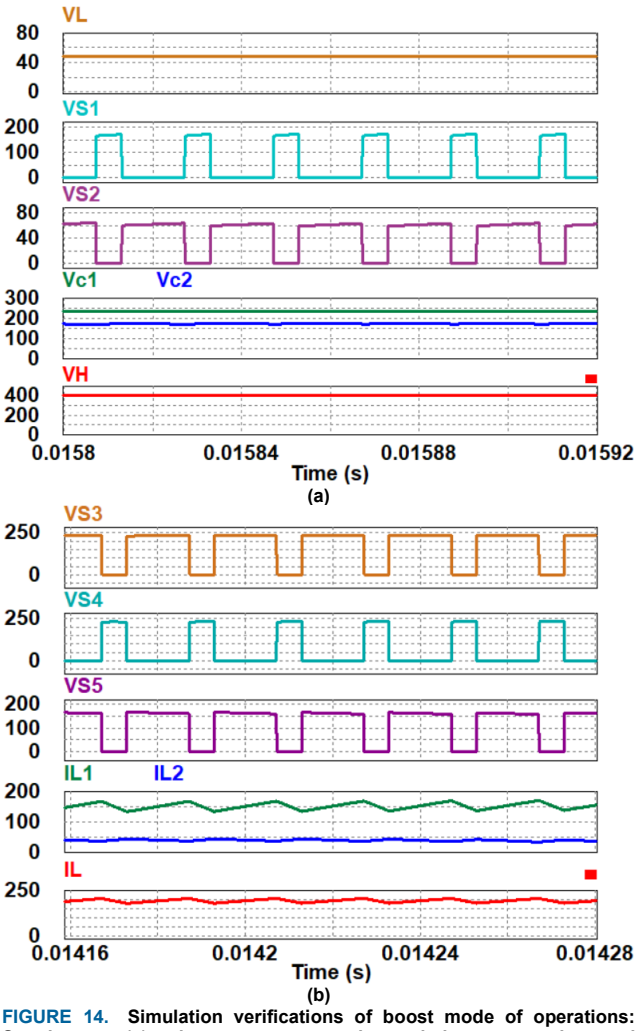

FIGURE 14. Simulation verifications of boost mode of operations: Steady state (a) voltage across operating switches S_1 and S_2 and capacitors (b) voltage across the switches $S_3, S_4 \& S_5$ and currents i_{L1}, i_{L2} & i_L

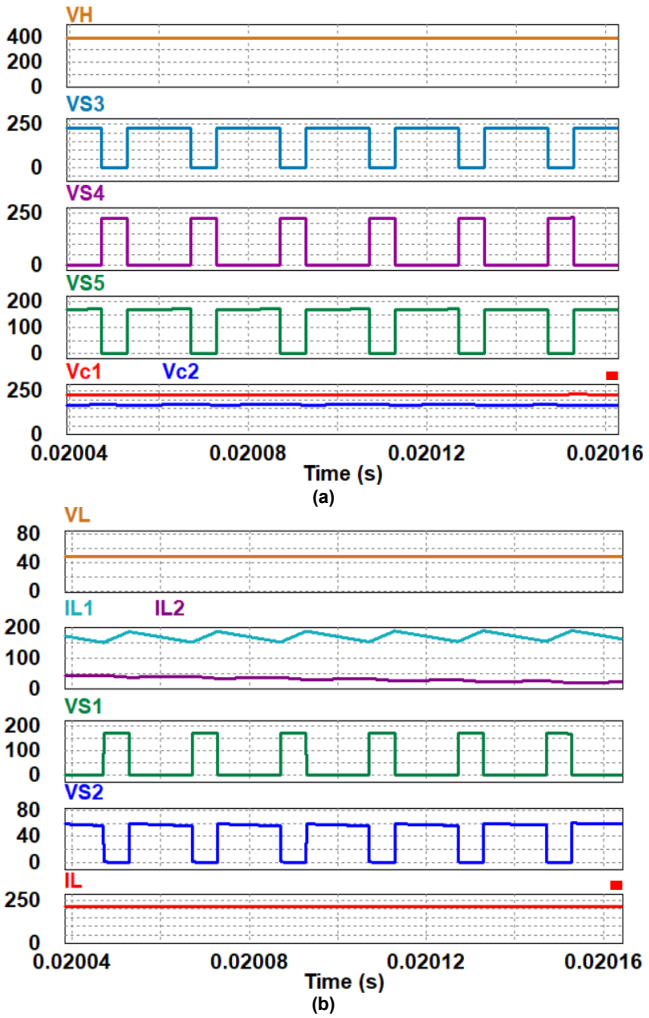

FIGURE 15. Simulation verifications of buck mode of operations: Steady -state (a) voltage across operating switches $S_3, S_4 \& S_5$ and capacitors (b) voltage across the switches S_1, S_2 and currents i_{L1}, i_{L2} & i_L.

$$\hat{\dot{x}} = (\mathrm{K}^{-1}\mathrm{A})\hat{x} + (\mathrm{K}^{-1}\mathrm{B})\hat{v}_L + \mathrm{K}^{-1}[(\mathrm{A}_1 - \mathrm{A}_2)\mathrm{X} + (\mathrm{B}_1 - \mathrm{B}_2)\mathrm{V}_\mathrm{L}]\hat{d} \quad (40)$$

Let $\mathrm{S}_1 = (\mathrm{K}^{-1}\mathrm{A})$;

$\mathrm{S}_2 = (\mathrm{K}^{-1}\mathrm{B})$;

$\mathrm{S}_3 = \mathrm{K}^{-1}[(\mathrm{A}_1 - \mathrm{A}_2)\mathrm{X} + (\mathrm{B}_1 - \mathrm{B}_2)\mathrm{V}_\mathrm{L}]$

After simplifying above,

$$\hat{\dot{x}} = \mathrm{S}_1\hat{x} + \mathrm{S}_2\hat{v}_L + \mathrm{S}_3\hat{d}$$

$\mathrm{A} = \mathrm{A}_1 D + \mathrm{A}_2(1 - \mathrm{D})$,

and $\mathrm{B} = \mathrm{B}_1\mathrm{D} + \mathrm{B}_2(1 - D)$

From (39), the control signal to output transfer function for the proposed converter deduced as follows:

$$\frac{\hat{v}_H}{\hat{d}} = [0 \quad 0 \quad 0 \quad 0 \quad 1][sI - S_1]^{-1}S_3 \quad (41)$$

So, the boost mode of operation in the DT interval can be written as:

$$K\dot{X} = A_1X + B_1V_L$$

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & C_H \end{bmatrix} \quad (42)$$

$$A_1 = \begin{bmatrix} r_{L1} & 0 & 0 & 0 & 0 \\ 0 & -(r_{L2} + r_C) & -1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{R_H} \end{bmatrix} \quad (43)$$

$$B_1^T = [1 \quad 1 \quad 0 \quad 0 \quad 0] \quad (44)$$

Where $r_C = r_{C1} + r_{C2}$

In the $(1 - D)T$ interval:

$$K\dot{X} = A_2X + B_2V_L$$

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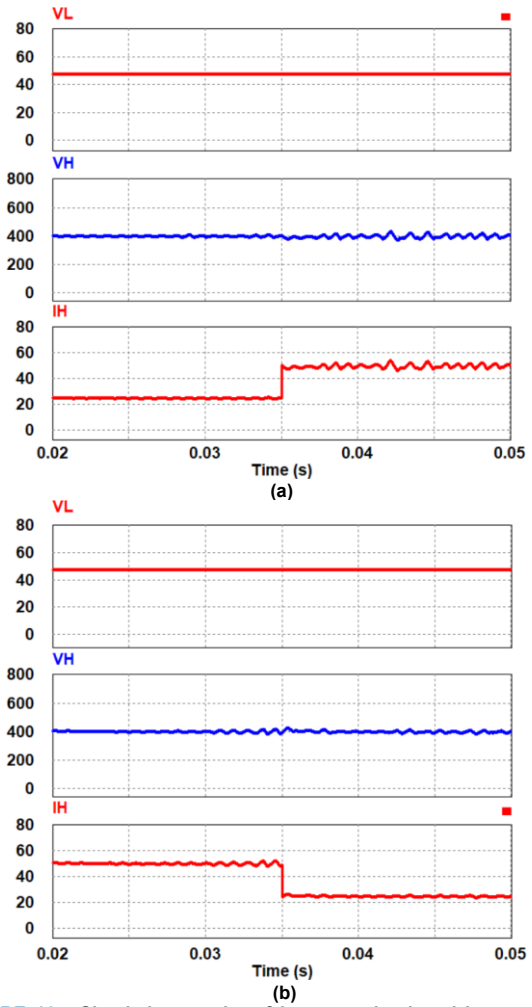

FIGURE 16. Simulation results of boost mode closed loop control dynamic performance for (a) step decrease in load (b) for step increase in load.

$$A_2 = \begin{bmatrix} -(r_{L1} + \frac{r_{C1}r_{C2}}{r_C}) & 0 & \frac{r_{C2}}{r_C} & -\frac{r_{C1}}{r_C} & -\frac{r_{C2}}{r_C} \\ 0 & -r_{L2} & 0 & 0 & 0 \\ -\frac{r_{C2}}{r_C} & 0 & -\frac{1}{r_C} & -\frac{1}{r_C} & \frac{1}{r_C} \\ \frac{r_{C1}}{r_C} & 0 & -\frac{1}{r_C} & -\frac{1}{r_C} & \frac{1}{r_C} \\ \frac{r_{C2}}{r_C} & 0 & \frac{1}{r_C} & \frac{1}{r_C} & -(\frac{1}{r_C} + \frac{1}{R_H}) \end{bmatrix} \quad (45)$$

$$B_2^T = [0 \quad 1 \quad 0 \quad 0 \quad 0] \quad (46)$$

The representation (~) denotes the small signal ac variation of the signal. The lower cases correspond to the instantaneous values, and upper cases correspond to the steady state values.

$$X^T = [i_{L1} \quad i_{L2} \quad v_{C1} \quad v_{C2} \quad v_H]$$

From (40) and using the parameters of the proposed converter (Table II), the control to output transfer function can be written as:

$$\frac{\tilde{V_H}}{\tilde{d}} = \frac{-1.9*10^5\, S^4 - 7.37*10^{10} S^3 + 8.33*10^{15} S^2 - 2.34*10^{17} S + 2.42*10^{23}}{4S^5 + 2.9*10^{10} S^4 + 1.5*10^9 S^3 + 1.58*10^{14} S^2 + 3.85*10^{16} S + 4.64*10^{20}} \quad (47)$$

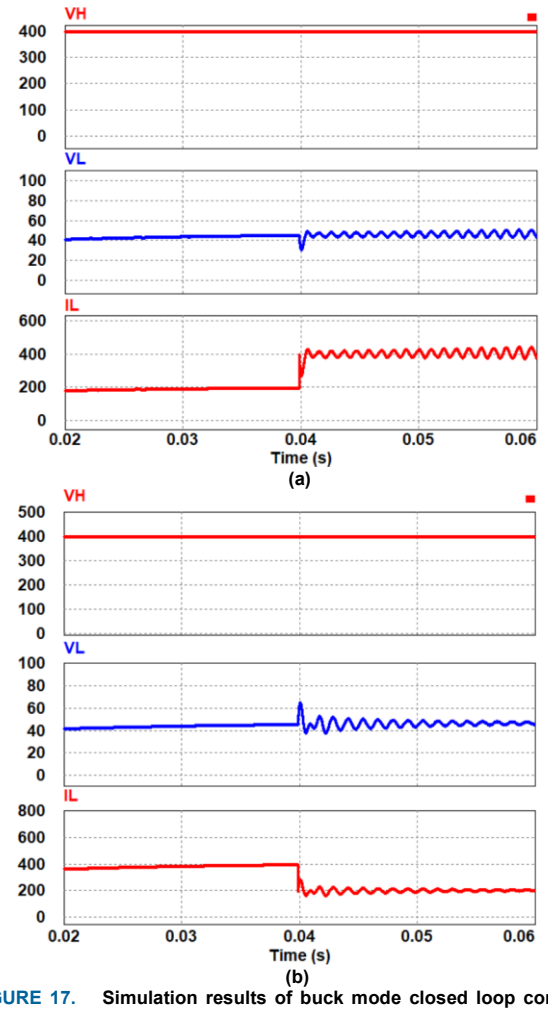

FIGURE 17. Simulation results of buck mode closed loop control dynamic performance for (a) step decrease in load (b) step increase in load

B. SMALL SIGNAL ANALYSIS FOR BUCK MODE OF OPERATIONS

The small signal analysis of buck mode of operation is similar to that of same as boost mode.

In the DT interval:

$$\dot{KX} = A_1 X + B_1 V_H$$

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 \\ 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & C_L \end{bmatrix} \quad (48)$$

$$A_1 = \begin{bmatrix} -r_{L1} & 0 & 0 & 0 & -1 \\ 0 & -(r_{L2} + r_C) & 1 & -1 & -1 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & -\frac{1}{R_L} \end{bmatrix} \quad (49)$$

$$B_1^T = [0 \quad 0 \quad 0 \quad 0 \quad 0] \quad (50)$$

Where $r_C = r_{C1} + r_{C2}$

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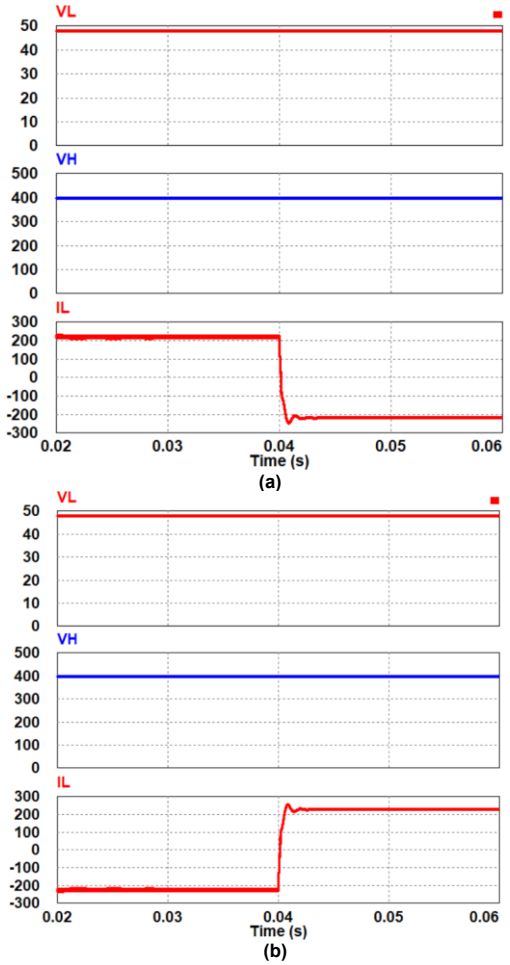

FIGURE 18. Simulation results for transition (a) from boost to buck (b) from buck to boost

In the $(1-D)T$ interval:

$$\dot{X} = A_2X + B_2V_H$$

$$A_2 = \begin{bmatrix} -(r_{L1} + \frac{r_{C1}r_{C2}}{r_C}) & 0 & -\frac{r_{C2}}{r_C} & \frac{r_{C1}}{r_C} & -1 \\ 0 & -r_{L2} & 0 & 0 & -1 \\ \frac{r_{C2}}{r_C} & 0 & -\frac{1}{r_C} & -\frac{1}{r_C} & 0 \\ -\frac{r_{C1}}{r_C} & 0 & -\frac{1}{r_C} & -\frac{1}{r_C} & 0 \\ 1 & 1 & 0 & 0 & -\frac{1}{R_L} \end{bmatrix} \quad (51)$$

$$B_2^T = \begin{bmatrix} \frac{r_{C2}}{r_C} & 0 & \frac{1}{r_C} & \frac{1}{r_C} & 0 \end{bmatrix} \quad (52)$$

The representation (~) denotes the small signal ac variation of the signal. The lower cases correspond to the instantaneous values, and upper cases correspond to the steady state values.

$$X^T = [i_{L1} \quad i_{L2} \quad v_{C1} \quad v_{C2} \quad v_L]$$

By using equation (41) and using the parameters used in the proposed converter (Table II), the control to output transfer function can be written as:

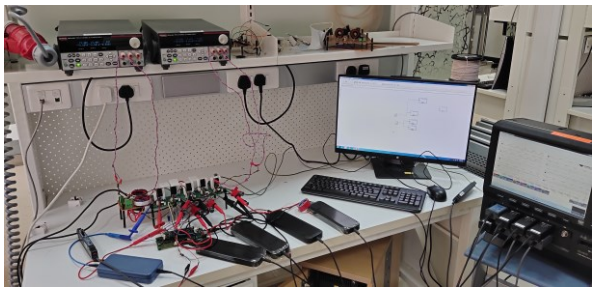

FIGURE 19. Experimental set up

$$\frac{\widehat{V_L}}{\hat{d}} = \frac{1.2*10^{10}S^2+8*10^{11}S+5.76*10^{17}}{7.2S^4+7.12*10^3S^3+6.54*10^8S^2+3.43*10^{11}S+1.45*10^{16}} \quad (53)$$

The plots of gain and phase of the boost and buck mode are given in Fig. 13. The bode plots of the uncompensated open loop transfer function (47) and (53) are shown in Fig 13. For the stable controller, boost mode controller is designed for 18 dB gain margin and 85° phase margin with the type II compensator, which is clear from Fig 13(a) of compensated graph. Similarly, the buck controller is designed for 15 dB gain margin and phase margin of 85° with the type II compensator. The compensated bode for buck mode of control is shown in Fig. 13(b). From Fig. 13, it is clear that the closed loop controller is stable with the desired dynamic response.

VIII. SIMULATION VERIFICATIONS

The steady state operation of proposed bidirectional converter is verified through simulation using PSIM. The low voltage side voltage is 48 V and high voltage side voltage is set as 400 V. The output power is 10 kW. The switching frequency is 50 kHz. The system parameters are given in Table II.

A. SIMULATION VERIFICATION OF BOOST MODE

The simulation results of the proposed converter in boost mode of operation with the duty cycle D = 0.712, are given in Fig.14. From Fig. 14(a), it can be observed that S_1 is ON for $D = 0.712$ interval and $S_2$is ON for (1-D) = 0.288 interval. For $V_L = 48$ V, with D = 0.712, the measured value of V_H is 400 V. For this operating point, the voltage gain from LV to HV is 8.33 which is in agreement with the theoretical derivation in (6). The voltage across the switches S_1 and S_2 are expressed as Vs_1, and V_{S2} respectively in Fig. 14(a). The voltage across the two capacitors are V_{C1} = 234 V and V_{C2} = 166 V which agree with the theoretical derivations in (5).

The voltage across the body diode of the switches S_3, S_4 and S_5, currents in the inductors (I_{L1} and I_{L2}) and LV side input source current I_L are shown in Fig. 14(b). The input current ripple (Δi_L) is reduced as $i_L = i_{L1} + i_{L2}$ and the ripple current in two inductors L_1 and L_2 are opposite and cancel each other. For output power of 10 kW, the output load current (I_H) is 25 A. These results match with the theoretical derivations given in section III.

B. SIMULATION VERIFICATION OF BUCK MODE

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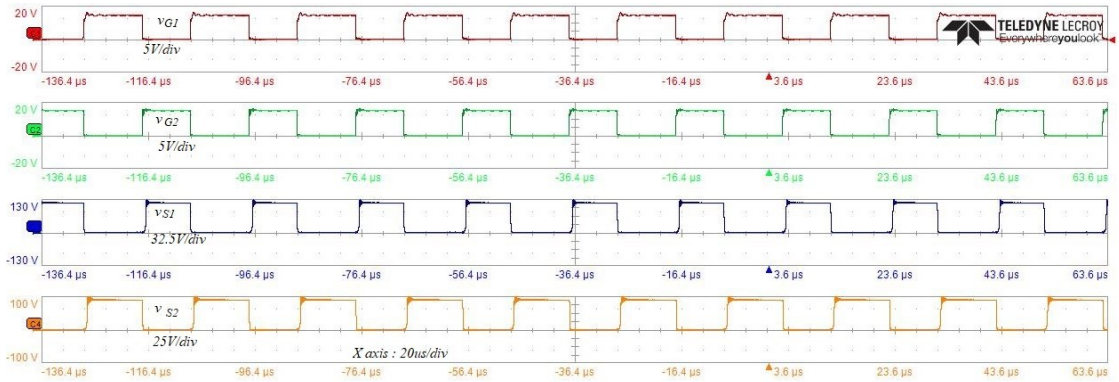

FIGURE 20. Experimental results for boost mode of operations at steady state: v_{G1}, v_{G2}, v_{S1}, and v_{S2}

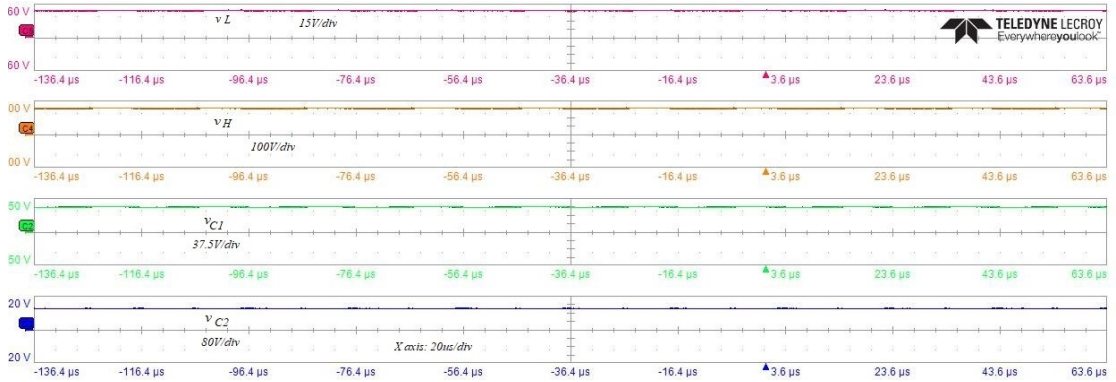

FIGURE 21. Experimental results for boost mode of operations at steady state: i_{L1}, i_{L2}, i_H, and i_L

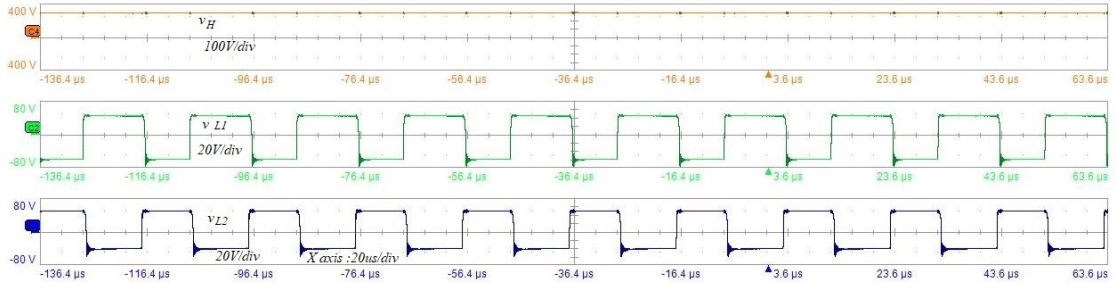

FIGURE 22. Experimental results for boost mode of operations at steady state: v_H, v_{L1} and v_{L2}

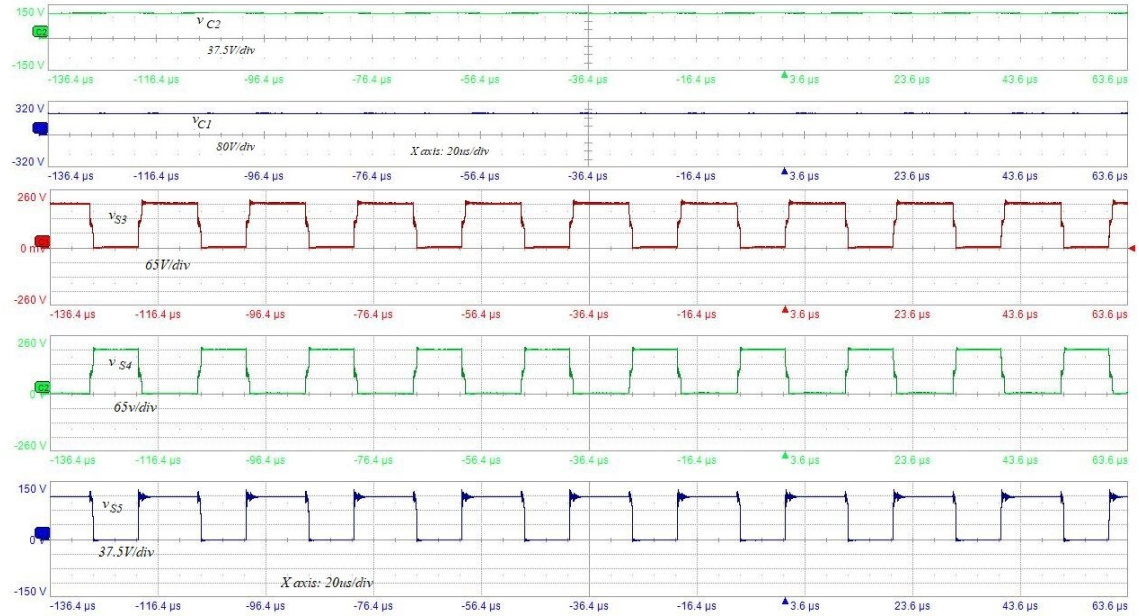

FIGURE 23. Experimental results for boost operations at steady state: v_{C2}, v_{C1}, v_{S3}, v_{S4} and v_{S5}

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For the same operating point, the simulation results of buck mode of operation, are given in Fig. 15. In buck mode, the energy is transferred from HV side to LV side (reverse of boost mode). In buck mode of operation, no PWM signal is applied for switches S_1, and S_2. It is also clear from the Fig. 15(a) that the switch S_4 is ON for the duty cycle interval of D = 0.712 and switches S_3- S_5 are conducting for (1-D)T = 0.288 duty interval. Fig. 15(a) shows the HV side voltage is 400 V, V_{C1} = 234 V, V_{C2} = 166 V, and voltage across the switches S_3, S_4 and S_5 as V_{S3}, V_{S4} and V_{S5} respectively. From Fig. 15(b) it is clear that the LV side current ripple is eliminated, as it is the sum of both the inductor currents. The

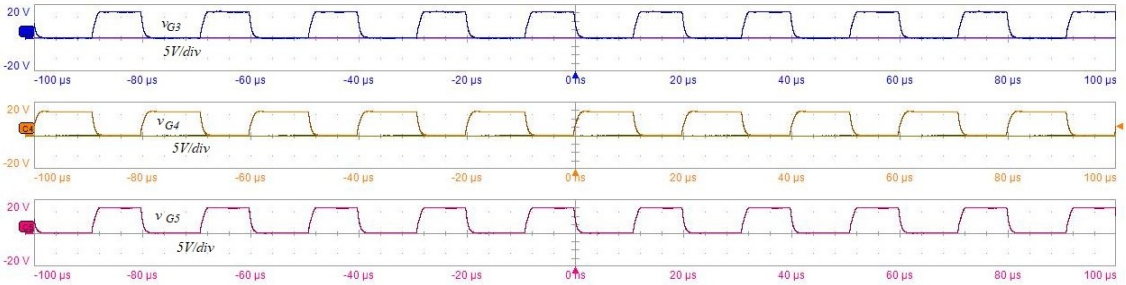

FIGURE 24. Experimental results for buck operations: PWM gate signals v_{G3}, v_{G4} and v_{G5}

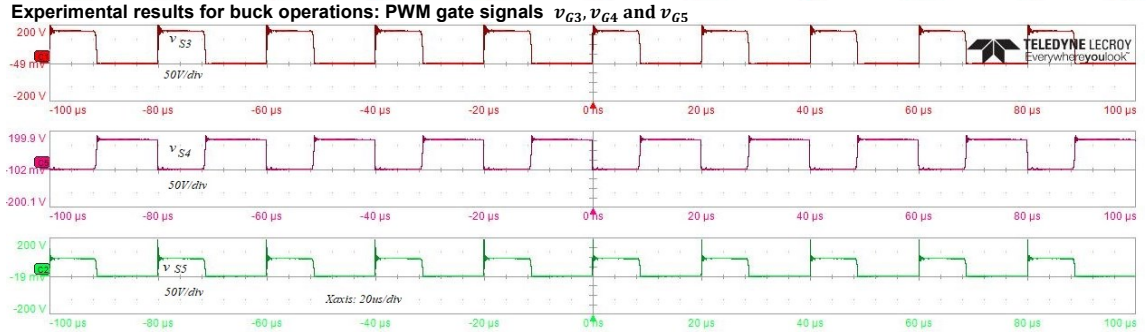

FIGURE 25. Experimental results for buck operations at steady state: v_{S3}, v_{S4}, v_{S5},

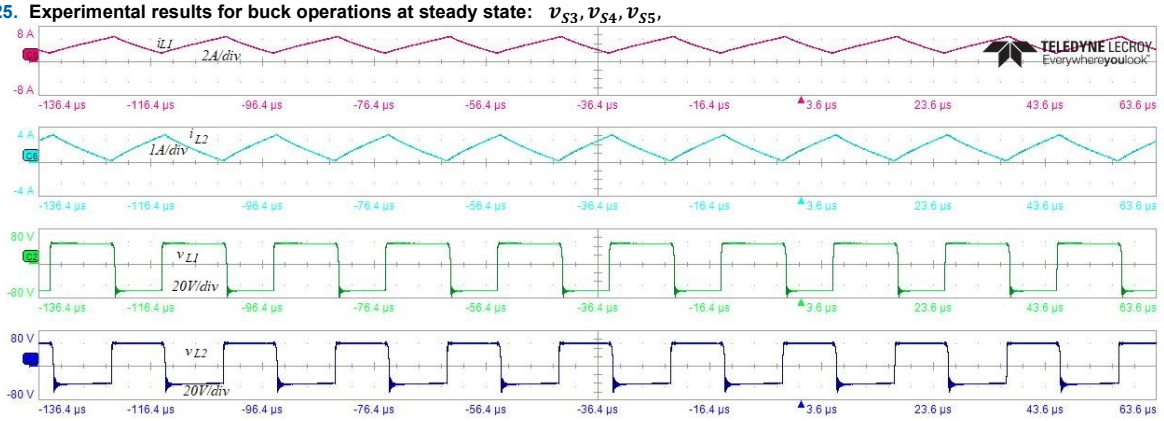

FIGURE 26. Experimental results for buck operations at steady state: i_{L1}, i_{L2}, v_{L1}, and v_{L2}.

FIGURE 27. Experimental results for buck operations at steady state: v_{C1}, v_{C2}, and i_L,

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simulation verification shows that the for V_H = 400 V, V_L is 48 V for the duty cycle of 0.712 and agree with the theoretical derivation in (13)-(14). The switches S_1, S_2 are non-operated and the voltage across the body diode of the switches are shown in Fig. 15(b). The results given in Fig 15 match with the theoretical derivations given in section III.

C. CLOSED LOOP CONTROL VERIFICATION

The closed loop operation of the proposed converter is also verified for load regulation. A type-II controller is used. Fig. 16 shows the boost mode dynamic responses for step change in load. The load is increased by 50% at 0.035 sec as shown in Fig. 16(a). In Fig 16(b), load current is reduced by 50%. In both cases the output voltage (V_H) remains constant demonstrating good load regulation. Similarly, the dynamic response of the converter against step load variation is studied for buck mode operation. In buck mode operation,

FIGURE 28. Experimental results for buck operations at steady state: v_{S1}, v_{S2}, v_H, and v_L.

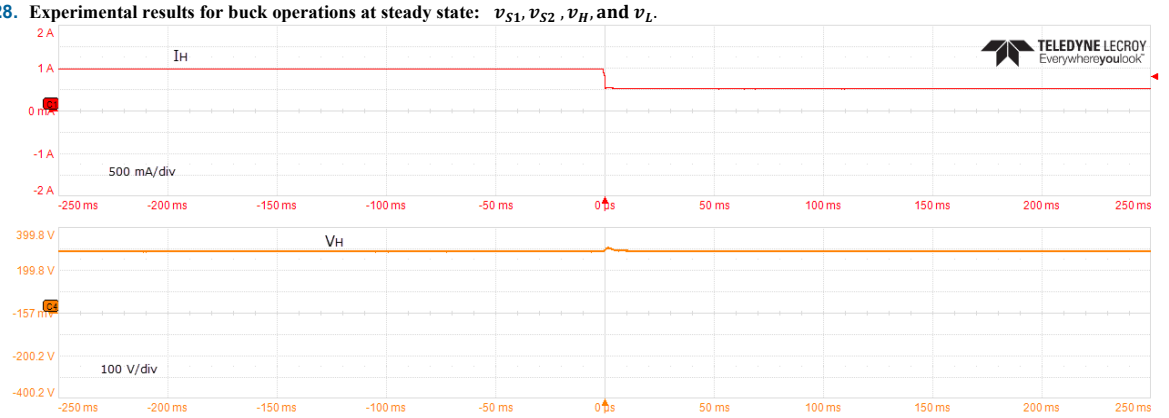

FIGURE 29. Experimental result for closed loop boost operation of 50% decrease in load current

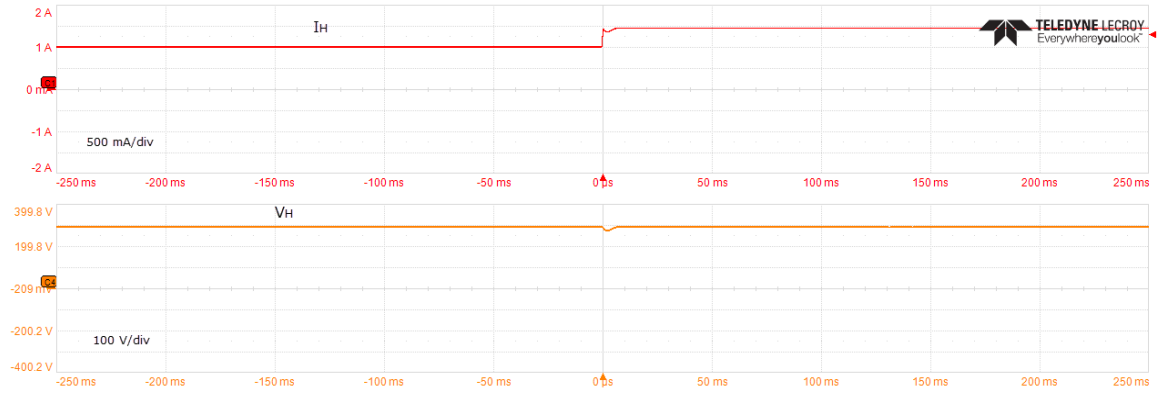

FIGURE 30. Experimental result for closed loop boost operation of 50% increase in load current

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the LV side current is increased by 50% at t = 0.04 sec. The LV side voltage (V_L) response is shown in Fig. 17(a). In Fig 17(b) the LV side current is decreased by 50%. In both the cases, that the LV side voltage is well regulated by the controller during the step change in load current.

Seamless operation from boost to buck and vice versa is verified through simulation [30]. In the proposed converter the boost mode operation and buck mode of operation are symmetrical. The operating duty cycle for the particular voltage is same for the boost as well as buck which is clear from (6) and (14). The mode operation is identified by the direction of the current flowing through the input side inductors. The low side voltage and high side voltage will be same and the power is flow from high to low voltage or low voltage to high voltage is decide by the current flow. Fig. 18 (a) shows the boost mode of operation for $0 \leq t < 0.04$ and at t = 0.04 sec the converter mode is changed from boost to buck. The low side voltage current (I_L) changes from 208 A to -208 A at t = 0.04 sec. Similarly, buck mode to boost mode transition is also verified in Fig. 18(b). In Fig. 18(b), the low side voltage current (I_L) changes from 208 A to -208 A at t = 0.04 sec So, both the results in Fig. 18 show the smooth transition between two modes of operation.

IX. EXPERIMENTAL VERIFICATIONS

The proposed converter operation is experimentally verified with scale down prototype of 300 W. Fig 19 shows the picture of the experimental set up. The switching frequency of the experimental prototype is used as 50 kHz. The current ripple in the inductor is limited to 40% and capacitor voltage ripple is 1%. The low voltage side voltage is set as 48 V and high voltage is design for 300 V. TMS320F28335 DSP controller is used to control the proposed bidirectional converter. The experimental results for boost mode are given in Fig.20, Fig. 21, Fig. 22 and Fig. 23. From Fig. 20, it is clear that the switches S_1 and S_2 switch alternately. The conduction interval of the switch S_1 is 0.55 duty cycle and switch S_2 is 0.45. For the input voltage of 48 V, the experimentally measured output voltage is 285.5 V. The load resistance is 300 Ω and measured load current is 0.95 A. The two inductors current charging and discharging are opposite in nature which is clear from Fig. 21. With this the input current ripple is reduced which is clear from the plot of i_L in Fig. 21. Inductor voltages are shown in Fig. 22. The measured capacitor voltages of V_{c1}, V_{c2} are 184.5 V and 101 V respectively. The capacitors voltages and voltages across switches S_3, S_4 and S_5 are given in Fig. 23. The steady-state experimental results of boost mode of operation have good match with the simulation results which is presented in Fig. 10 and agree with the theoretical derivations of section III.

The experimental results for buck mode of operation are given in Fig.24, Fig. 25, Fig. 26, Fig. 27 and Fig. 28. The parameters are unchanged and operated for the same operating point as that of boost mode operation. The HV side voltage for buck mode is taken as 300 V. The steady-state operation of the PWM signal and voltage across the switches are shown in Fig. 24. From Fig. 24, it is clear that the switches S_4 and (S_3, S_5) switch alternately. The conduction interval of

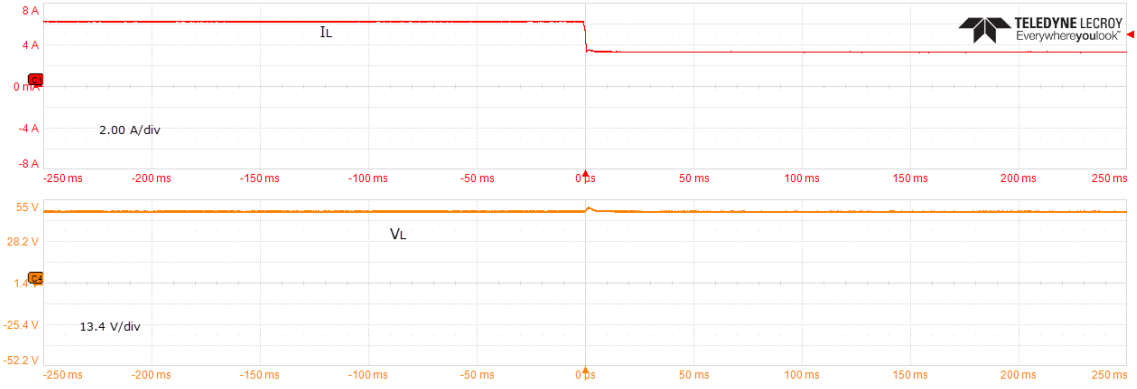

FIGURE 31. Experimental result for closed loop buck operation for 50% decrease in load current

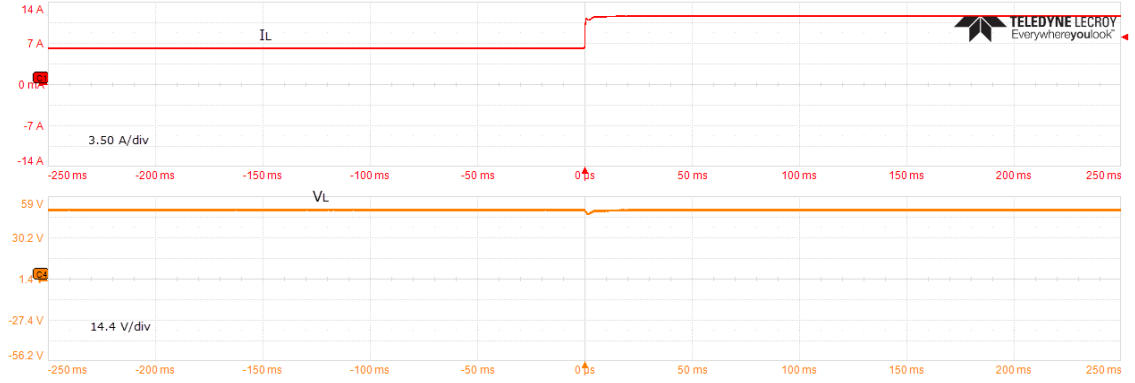

FIGURE 32. Experimental result for closed loop buck operation for 50% increase in load current

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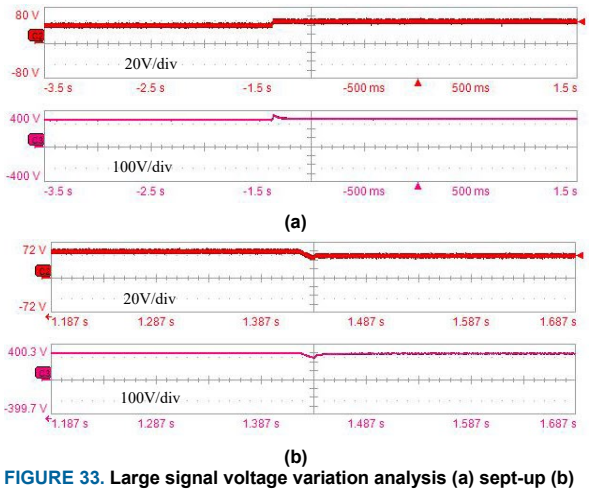

FIGURE 33. Large signal voltage variation analysis (a) sept-up (b) step-down

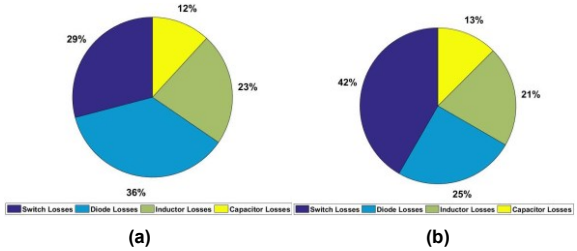

FIGURE 34. Loss distribution in (a) Boost Mode (b) Buck Mode

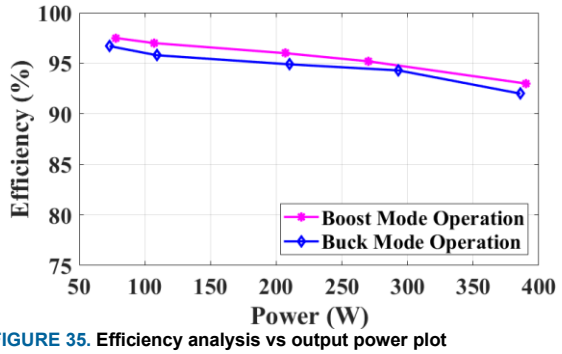

FIGURE 35. Efficiency analysis vs output power plot

the switch S_4 is 0.55 duty cycle and switch (S_3, S_5) is 0.45. Voltage across the switches is shown in Fig. 25. The two inductors current charging and discharging are opposite in nature. By this the LV side current ripple is reduced which is clear from Fig. 26. The measured capacitor voltages V_{c1}, V_{c2} are 193 V and 106 V respectively. The load current is 0.98 A which is clear from Fig. 27. The steady-state operation of buck mode operation is verified with input-output voltages, and voltage across the switches, are shown in Fig. 28. The load resistance at low voltage side is taken as 7 Ω. For the buck operation the HV side voltage is given as 300 V and the LV side voltage is found to be 45.3 V. These results match with the theoretical derivations given in section III and also agree with the simulation results given in section VIII.

The closed loop control of the proposed converter in boost mode and buck mode operation is also verified using the experimental prototype. As mentioned previously, type II controllers are used. Fig. 29 shows the output voltage response for a 50% step change in load current (1.0 A to 0.5 A). Similarly, the output voltage response for a 50 % step increase of load current (1 A to 1.5 A) is shown in Fig.30. So, from Fig. 29 and Fig. 30, it is clear that the proposed converter is able to regulate the output voltage for sudden variation of the load. Similarly, for buck mode of operation, the results of the step load change are given in Fig 31 and Fig.32. In Fig. 31 for buck mode of operation, the LV side load is suddenly increase by 50% and the output voltage remains constant. The sudden 50% decrease of current and the LV side voltage response is shown in Fig. 32. A small rise in output voltage for step decrease in load and small dip output voltage for step increase in load is observed but the controller is able to bring the output voltage to set value, thus the controller is having fast dynamics under large signal variations. The results in Figs. 29, 30, 31, 32 and 33 demonstrate the closed loop operations of the proposed converter. The response of the converter for sudden change in input voltage is shown in Fig 33. For boost mode, the input voltage is varied from 40 V to 60 V and it is observed from Fig. 33 (a) that output voltage remains constant at 300 V. Similarly, Fig. 33(b) shows the step-down the input voltage from 60V to 40 V and result shows the output voltage constant at 300 V. A small rise in output voltage for step increase in input voltage and small dip output voltage for step decrease in input voltage is observed but the controller is able to bring the output voltage to set value, thus the controller is having fast dynamics under large signal variations. The results in Figs. 29, 30, 31, 32 and 33 demonstrate the closed loop operation of the proposed converter. These experimental results are in agreement with the simulation as well as theoretical results. However, the minor difference between theoretical and experimental is obvious due to parasitic resistance of passive components, resistance of copper wire, voltage drop of switches etc.

The efficiency of the converter in boost as well as buck mode of operation over a range of output power varying from 50 W to 380 W is measured. Fig 34(a) shows the losses distribution in boost mode of operation and Fig. 34(b) shows the losses distribution in buck mode of operation. The measured efficiency is plotted in Fig. 35. In boost mode, for the above operating point the measured value of efficiency is 95.2% and maximum efficiency of 97.5% is measured at 78 W. In buck mode, the measured value of efficiency for the above operating point is 94.3% and maximum efficiency is 96.7% at 73 W. Compared to conventional Z-source converter, the efficiency of the proposed converter is improved by 1~2% which is clear from the Table 1.

X. CONCLUSION

This paper presents, a high voltage gain switched Z-source bidirectional DC-DC converter. The proposed converter has low input current stress on the inductors, high voltage conversion and low input source current ripple over entire range of duty cycle. Additionally, the converter has common ground between input and output ports. The steady-state

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analysis shows that in the boost mode of operation the minimum voltage conversion ratio is 5.8. For the buck mode of operation, the maximum voltage conversion ratio is 0.17. The operation, steady-state analysis, power loss analysis, small signal modeling, controller design, simulation and experimental verifications are presented. The proposed bidirectional Z- source switched converter is suitable for renewable energy sources, battery storage systems, electric vehicles and other applications where high voltage gain as well as bidirectional power flow are required.

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