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High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination

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An approach to realizing high-voltage, high-current vertical GaN-on-GaN power diodes is reported. We show that by combining a partially compensated ion-implanted edge termination (ET) with sputtered SiN_x passivation and optimized ohmic contacts, devices approaching the fundamental material limits of GaN can be achieved. Devices with breakdown voltages (V_{br}) of 1.68 kV and differential specific on resistances (R_{on}) of 0.15 mΩ cm^2, corresponding to a Baliga figure of merit of 18.8 GW/cm^2, are demonstrated experimentally. The ion-implantation-based ET has been analyzed through numerical simulation and validated by experiment. The use of a partially compensated ET layer, with approximately 40 nm of the p-type anode layer remaining uncompensated by the implant, is found to be optimal for maximizing V_{br}. The implant-based ET enhances the breakdown voltage without compromising the forward characteristics. Devices exhibit near-ideal scaling with area, enabling currents as high as 12 A for a 1 mm diameter device. https://doi.org/10.1063/1.5035267

Vertical GaN power devices based on bulk GaN substrates are attractive for their potential for high performance and efficiency as well as for enabling power supplies and converters with reduced size and weight.[1–3] However, for GaN diodes, there are several challenges. First, the reverse leakage current in vertical devices is sensitive to defect density and in particular the density of screw-type threading dislocations.[4] A second challenge is associated with realizing low-resistance p-GaN ohmic contacts due to the unavailability of metals with a sufficiently high workfunction and the comparatively deep level of Mg acceptors in GaN.[5] Additionally, designing and fabricating an effective edge termination (ET) to manage the high fields at the edge of the active region by tailoring the lateral doping profile by implant or diffusion is especially difficult in GaN, necessitating alternative approaches.

Despite these challenges, vertical GaN power p-n diodes with high Baliga's figure of merit (BFOM) and critical electric field have been demonstrated (see, e.g., Refs. 6–18). In many cases, however, these prior reports required complex fabrication processes (e.g., use of sloped mesa sidewalls and field plates) or reflected results obtained on small-area devices that are of limited value in scaling to larger absolute currents as needed in power applications. In this paper, the design and fabrication of GaN p-n diodes with breakdown voltages above 1.6 kV, in a process scalable to forward currents in excess of 12 A, and specific on-resistances of 0.15 mΩ cm^2 is reported, resulting in a BFOM of 18.8 GW/cm^2. These results demonstrate device performance very close to the fundamental limits of GaN.

Figure 1 depicts the device structures reported here. The epitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD) on 2-in. native GaN substrates. Two device structural variants—one with an 8 μm drift layer and the other with a 12 μm drift layer—were used. P-GaN ohmic contacts with low resistance were obtained using a two-step surface treatment and thermal annealing of evaporated Ni/Au (20/500 nm) contacts;[19,20] large-area cathode Ti/Al/Ni/Au contacts on the back of the wafer were used. To avoid sidewall leakage currents and the complications associated with terminating the junction fields in a mesa isolated structure (e.g., field plates),[10] an ion-implantation based edge termination with a SiN_x surface passivation layer has been used. The edge termination consists of fully compensated and partially compensated regions achieved by a shallow ring etch and N^{14} implant.

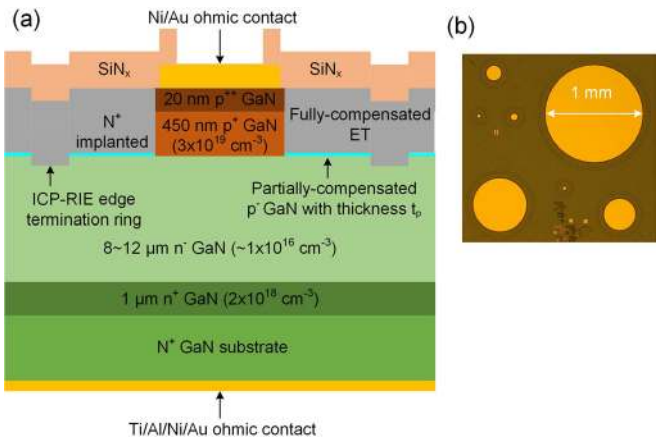

FIG. 1. (a) Cross-sectional schematic and (b) top view of fabricated p-n diodes with ion-implanted ET and SiN_x passivation.

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A critical issue for vertical GaN diodes is the design of the ET. The ET must control the electric field along the surface and perimeter of the device to prevent the onset of localized impact ionization and avalanche breakdown along the device periphery. Effective termination schemes are well developed for mature semiconductor systems such as Si and SiC; these typically rely on tailoring the lateral doping profile in the devices and are implemented using diffusion or ion implantation. Unfortunately, this approach is difficult in GaN[21] and so other approaches are required. Implantation-based isolation has been studied in the GaN material system using either compensating or complexing species (e.g., O, H, and Zn) or inert species (e.g., Ar, N, He, and Kr) to create deep levels.[9,22–26] Other approaches include beveled or sloped sidewall field plates,[7,10] although this approach can result in increased process complexity and additional capacitance. In this work, we investigated N^{14} ion implantation to form a damage-based edge termination. A flat defect density profile from the surface of the p-GaN to just short of the metallurgical junction—achieved using a triple-energy implant—compensates the p-GaN by implant damage, leading to a nominally insulating layer that can distribute the field laterally by fringing (grey part in Figs. 1 and 2). By adjusting the highest ion-implantation energy, the range of the implant [and thus the thickness of the partially compensated layer, t_p (light blue region in Figs. 1 and 2)], can be fine-tuned to achieve the highest breakdown voltage. Examples of defect density versus depth, calculated using SRIM,[27] are shown in Fig. 2. For the 470 nm thick p-type GaN epitaxial anode layers in our devices, energies of 30, 100, and 200–220 keV were simulated using SRIM to estimate the damage profile.[9] The superposition of these implants results in an approximately constant defect density ($4 \times 10^{20}\,cm^{-3}$) to a depth of 300 nm, followed by a gradual tailing off at greater depths. Under reverse bias, ionized acceptors in the partially compensated p-GaN layer help to terminate the lateral electric field lines, increasing the breakdown voltage. Under the assumption that each implant damage site contributes one singly charged deep level, t_p can be estimated as shown in Fig. 2.

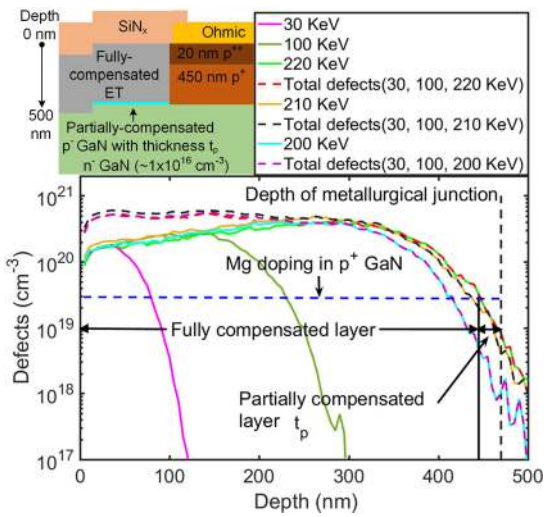

FIG. 2. Details of the ET structure and SRIM simulation of a triple energy implant for a partially compensated ET. The implant-induced defect concentration is smaller than the Mg doping (blue dashed line) from 440 to 470 nm in the p-GaN with the highest ion-implantation energy of 220 keV, leading to partial compensation layer thickness, t_p, of 30 nm.

To protect the unimplanted regions, 1.6 μm of photoresist (Shipley S1813) was used as a masking layer. SRIM simulations of the photoresist/GaN layers at the highest implant energy were performed to ensure that the ion range was confined to the photoresist and did not reach the semiconductor.

To study the effect that implantation conditions and surface dielectric passivation have on device breakdown, the device structure with an 8 μm drift layer was simulated numerically using Synopsys TCAD.[28] To explore the design space for the ET, the thickness of the partially compensated p-type GaN layer, t_p, was varied over the range from 0 to 80 nm. Figure 3 shows the lateral electric field for several partial-compensation thicknesses, t_p. When the p-GaN layer is fully compensated ($t_p = 0$ nm, red curve), the electric field peaks at the corner formed by the metallurgical junction and the edge of the implant. The inclusion of a partially compensated layer between the anode region and the shallow ring etch results in a second peak in the field that increases the breakdown voltage. As t_p approaches the optimum value ($t_p = 40$ nm, blue curve), the electric field peaks are evenly spread between the edge of the anode region and the transition to the fully depleted region due to the edge termination etch ring. When t_p is larger than optimal ($t_p = 80$ nm, green curve), the partially compensated region is not depleted in reverse bias and the electric field peaks prematurely at the edge where the device becomes fully depleted. From our simulations, we find that the lateral ET width should be made equal to or larger than the drift layer thickness (12 μm in the case of the structure reported here) to avoid compromising the breakdown voltage due to increased surface fields, but so long as it exceeds this minimum, the breakdown voltage is not strongly affected. This approach is conceptually similar to the reduced surface field (RESURF) approach, except in this case the surface field tailoring is done through partial depletion of a buried layer.

As can be seen from Fig. 3, the thickness of the partially compensated layer, t_p, significantly impacts the electric field

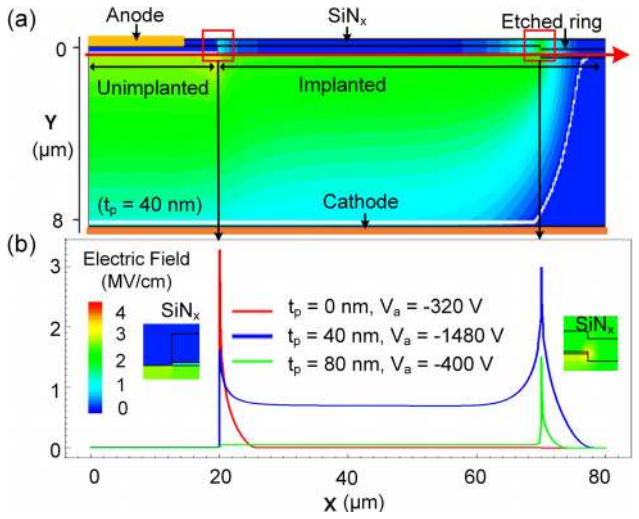

FIG. 3. (a) Computed electric-field distribution showing where the electric field peaks occur in devices with SiN_x passivation for the optimal case. Note that unequal vertical and horizontal scales have been used to improve visibility. (b) Electric field profile along the ET [red arrow in (a)] for different t_p. Balanced electric field peaks (blue curve) are obtained when t_p is close to the optimum.

distribution within the device and thus the V_{br}. From the data in Fig. 3, the breakdown voltage as a function of t_p was obtained and is shown in Fig. 4; the highest V_{br} achieved (defined in simulation as the bias at which the peak field in the device reaches 3.3 MV/cm) is 1.48 kV for t_p of 40 nm.

To confirm these numerical predictions, diodes with different t_p and different passivation treatments were fabricated and characterized. To achieve high breakdown voltage, a lightly doped drift layer is essential. A doping concentration of $1–1.5 \times 10^{16}\,cm^{-3}$ was measured for the drift layer in our structures by both capacitance-voltage (C-V) measurement and secondary-ion mass spectrometry (SIMS). This doping is sufficiently low to enable breakdown voltages >1500 V.

The inclusion of a surface passivation layer is well-known to be useful for enhancing the breakdown of devices, due to both termination of surface states and moderation of the permittivity contrast along the device surface. It has been observed that the on-state characteristics of n-type GaN Schottky diodes can be compromised if SiN_x or SiO_2 deposited by plasma-enhanced chemical vapor deposition (PECVD) is used;[29] it is speculated that hydrogen present in the deposition process may de-activate the Mg acceptors through the formation of MgH complexes.[29] In contrast, sputtered SiN_x was found not to increase the reverse leakage current with respect to the unpassivated n-type Schottky diodes.[30] In this work, sputtered SiN_x was evaluated as the passivation for implant-isolated planar p-n junction diodes (i.e., on a p-type GaN surface as shown in Fig. 3). A comparison of the current voltage characteristics of diodes with PECVD SiN_x and sputtered SiN_x is shown in Fig. 4(a). As can be seen in the inset, sputtered and PECVD SiN_x result in nearly identical V_{br}, while sputtered SiN_x results in better performance in forward bias, compared to a noticeably higher specific on-resistance for PECVD passivation.

The ET designs were also evaluated experimentally. Figure 4(b) shows the measured breakdown of devices with an 8 μm thick drift layer as a function of partially compensated p-layer thickness. The highest measured V_{br} occurred for t_p of 40 nm, in good agreement with numerical simulation. Experimentally, diodes with 40 nm t_p, 8 μm drift layer, and sputtered SiN_x surface passivation exhibited 1220 V breakdown, only modestly below that predicted in simulation. It should be noted that the t_p value for the experimental data is estimated from SRIM simulations due to the difficulty in directly measuring damage profiles.

A critical issue for power devices is device area scalability. To evaluate scalability, devices with diameters from 70 μm up to 1 mm were fabricated and tested. We define the active area of the devices as the area of the anode contact metallization. For the devices reported here, the measured breakdown voltages were independent of the size of the diodes, as shown in Fig. 5. Since the breakdown voltage is independent of the area, this indicates that the diode perimeter does not contribute significantly to the breakdown behavior. The apparent increase in reverse leakage for small devices at low bias voltages is an artifact from the measurement noise floor and the current/area normalization. As

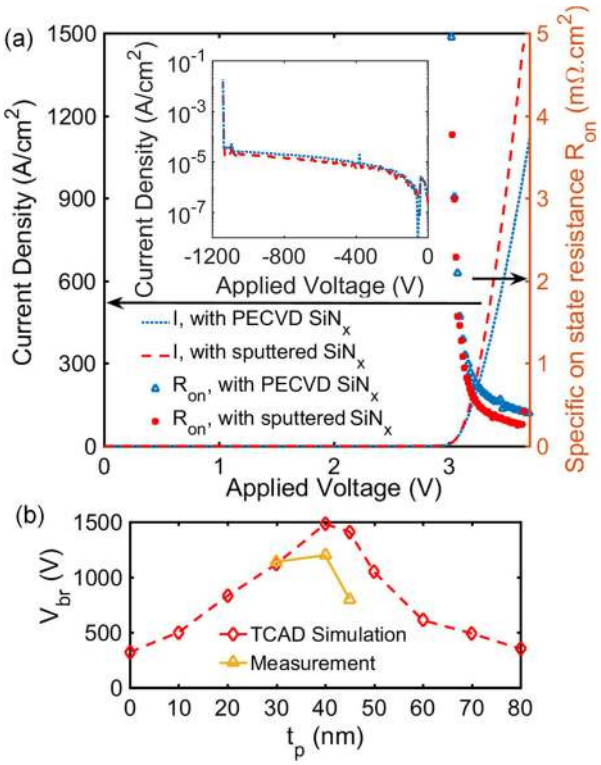

FIG. 4. Measured I-V characteristics of GaN p-n diodes with 8 μm drift layer (155 μm diameter). (a) Comparison of forward I-Vs and R_{on} and (inset) reverse I-Vs and V_{br} for p-n diodes ($t_p = 40$ nm) with sputter- and PECVD-deposited SiN_x. At 3.6 V, R_{on} is 0.25 and 0.41 mΩ cm^2 for these diodes, respectively. (b) V_{br} vs. t_p from simulation and measurement. The highest measured V_{br} occurred at $t_p = 40$ nm.

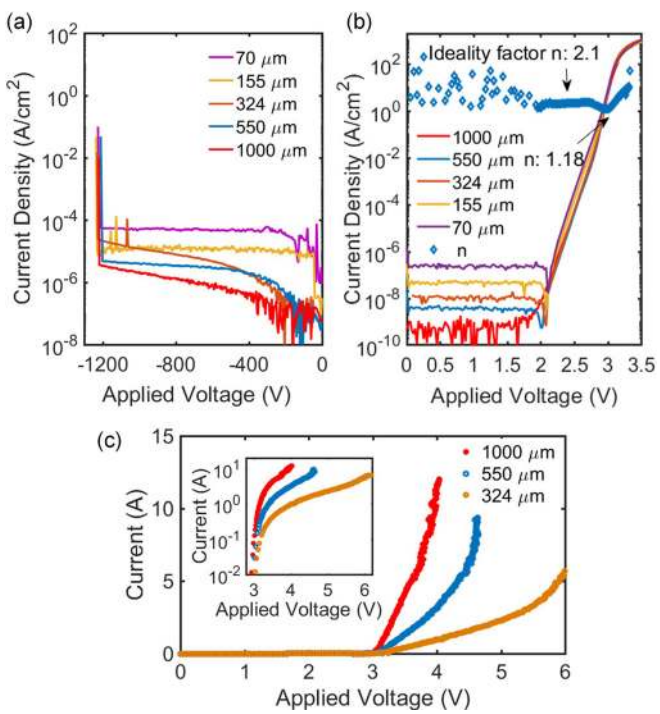

FIG. 5. Measured I-V characteristics of GaN p-n diodes with 8 μm drift layer as a function of device area. (a) Reverse I-Vs, showing that the breakdown voltage V_{br} is not affected by the device area; (b) forward I-Vs on a semi-log scale, showing that the device area does not affect the forward current density. The increase in SRH current for small devices suggests a modest edge-related recombination current; (c) forward-bias pulsed I-V on large diodes. Currents as high as 12 A are carried by 1 mm diameter devices at 4 V.

shown in Fig. 5(a), for small size diodes (i.e., 70 μm and 155 μm), the reverse current is below the measurement noise floor, resulting in an artificially high current density. For the larger size devices (324–1000 μm), the measured reverse currents are larger than the noise floor and the resultant current densities in Fig. 5(a) reflect the diode performance. In forward bias as shown in Fig. 5(b), the devices exhibit near-ideal behavior for current densities spanning 13 orders of magnitude. Below 2 V, the diode current is too low to be measured. For applied voltages from 2 V to approximately 2.5 V, the extracted ideality factor n is 2.1, indicating Shockley-Read-Hall (SRH) recombination dominated operation. In this regime, a small area dependence can be seen, suggesting that the diode perimeter contributes modestly to the SRH recombination. Above approximately 2.5 V, the ideality factor shows a transition from 2.1 down to approximately 1.18 at 3 V, signifying that the diode diffusion current (with ideality factor of 1) overwhelms the SRH current in this region. A turn-on voltage of 3.1 V (at 100 A/cm^2) is measured, as expected given the bandgap of GaN. Above the turn-on voltage, n rises due to the diode series resistance. As can be seen in Fig. 5(b), the current density scales almost perfectly with the junction area in the on-state.

To evaluate the ultimate current-carrying capability of these structures, pulsed I-V measurements were performed on the larger-sized devices. To limit the effects of self-heating during measurements, 500 μs pulses and a pulse period of 500 ms were used during the measurement. The sample was also mounted on a thermal probe station chuck with the surface actively held at 25 °C. As shown in Fig. 5(c), the current in a 1 mm diameter diode can reach 12 A at 4 V. No apparent degradation with additional measurement sweeps was observed.

In addition to the 8 μm drift layer devices shown above, a thicker 12 μm drift layer has also been evaluated through simulation and experiment in order to achieve higher breakdown voltages. As shown in Fig. 6, measurement and simulation for these devices exhibit turn-on voltages of 3.1 V, and the measured R_{on} of 0.15 mΩ cm^2 is within 0.02 mΩ cm^2 of the prediction from simulation. Measured breakdown

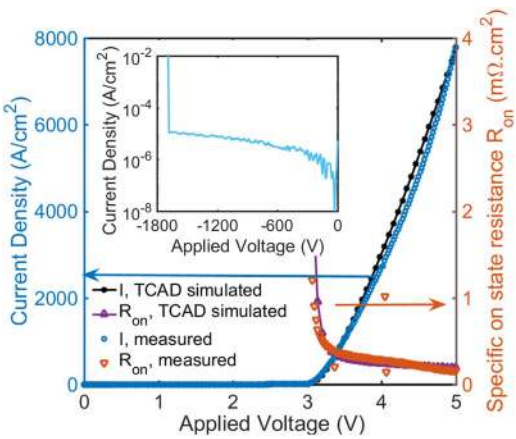

FIG. 6. I-V performance of measured and simulated GaN p-n diodes. (12 μm drift layer, 155 μm diameter, and t_p = 40 nm) From the measurement, 1680 V V_{br} and 0.15 mΩ cm^2 R_{on} (at 5 V) are obtained. Both the simulated and measured diodes have the same turn-on voltage of 3.1 V at 100 A/cm^2.

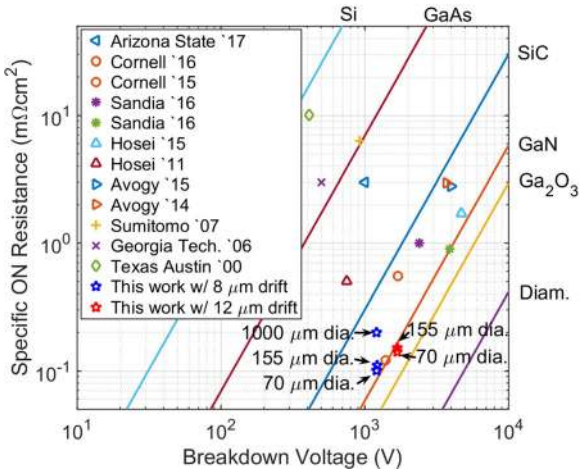

FIG. 7. Benchmark of R_{on} vs. V_{br} for reported power GaN p-n diodes. The blue stars are the results obtained for diodes in this work with 8 μm drift layers, while red stars indicate devices with 12 μm drift layers. Performance approaching the fundamental limits of GaN [with the electron mobility of 1470 cm^2/V s (Ref. 8) and the critical field of 3.9 MV/cm (Ref. 10)] with a simple device and ET design has been achieved.

voltages of 1680 V are obtained, in good agreement with the simulation projected breakdown of 1730 V. A comparison of these GaN p-n diodes to prior reports is shown in Fig. 7. The devices presented exhibit BFOMs very close to the fundamental limitations of GaN, with an estimated critical electric field, E_c, of 3.4 ± 0.3 MV/cm (following the approach described in Refs. 7 and 31), and are competitive with the best prior reports. However, the devices reported here achieve this performance without the use of complex multi-step ET or field plates, resulting in a simpler fabrication process.

In summary, vertical GaN power diodes with an optimized partially compensated ET design and sputtered SiN_x passivation are explored through simulation and experiment. The 40 nm partially compensated p-GaN layer within the ET laterally distributes the electric field to support a high V_{br} of 1680 V, without adversely impacting the forward characteristics. As an alternative to PECVD SiN_x, sputtered SiN_x is shown to enable low on-resistance (R_{on} = 0.15 mΩ cm^2) in GaN p-n junctions. A high BFOM of 18.8 GW/cm^2 is obtained for these vertical GaN-on-GaN p-n diodes, and the scalability of the devices to mm-scale areas and high current densities is demonstrated. The high performance attained with a single-step ET without field plates offers advantages for cost and yield.

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