High-Voltage Isolated Gate Drive Circuit for 10 kV, 100 A SiC MOSFET/JBS Power Modules

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Abstract—**A high-current, high-voltage-isolated gate drive circuit developed for characterization of high-voltage, high-frequency 10 kV, 100 A SiC MOSFET/JBS half-bridge power modules is presented and described. Gate driver characterization and simulation demonstrate that the circuit satisfies the gate drive requirements for the SiC power modules in applications such as the DARPA WBST-HPE Solid State Power Substation (SSPS). These requirements include 30 kV voltage-isolation for the high-side MOSFETs, very low capacitance between the ground and floating driver sides, and 20 kHz operation. Block diagram and detailed discussion of principles of operation of the gate drive circuit are given, together with measured and simulated waveforms of performance evaluation.** †

I. INTRODUCTION

The DARPA Wide Bandgap Semiconductor Technology (WBST) High Power Electronics (HPE) program is satisfying the critical need for silicon carbide (SiC) power semiconductor devices and packaging technology capable of fulfilling the high-voltage (HV) and high-frequency (HF) requirements of power conditioning systems in emerging industrial and military applications [1]. Under the ongoing WBST-HPE Phase II program, significant investment has been made to accelerate the development of 10 kV, 20 kHz SiC power semiconductor devices and associated packaging technology [2]. Particularly, substantial progress has been made in developing 10 kV SiC MOSFETs [3] and Junction Barrier Schottky (JBS) diodes [4] suitable for pursuing the WBST-HPE Phase II goal of developing 100 A, 10 kV, 20 kHz SiC MOSFET/JBS half-bridge power modules. These modules are needed in order to demonstrate a 13.8 kV, 2.75 MVA Solid State Power Substation (SSPS), which is the goal of the Phase III program [1]. The significant reduction of weight and volume and the improved power quality are SSPS features that are expected to have a positive impact not only for military, but also industrial electric power distribution systems as well.

Current efforts supporting the ongoing HPE programs include the recently developed electro-thermal model for a 10 kV, 100 A, 20 kHz SiC MOSFET/JBS power module [5, 6]. Module performance has been evaluated and optimized using this model, leading to an improved understanding of on-state and switching losses [7]. Although a gate resistance is included in the performance analysis in [7], further analysis and characterization must be performed in order to evaluate and fulfill gate driver requirements for the SSPS application.

The purpose of this paper is to present a new high-current, high-voltage-isolated gate drive circuit for the HV-HF SiC half-bridge power modules. The gate drive requirements for the module are evaluated in detail by area scaling results for single die 10 kV SiC power MOSFETs with die areas of up to 0.309 cm^2 (10 A rating) and for modules with multiple die in parallel. In this paper, measured and simulated results of the gate drive circuit performance are given for a 10 kV MOSFET half-bridge module with an area of 1.55 cm^2 (50 A rating) obtained using five paralleled die.

II. GATE DRIVER REQUIREMENTS

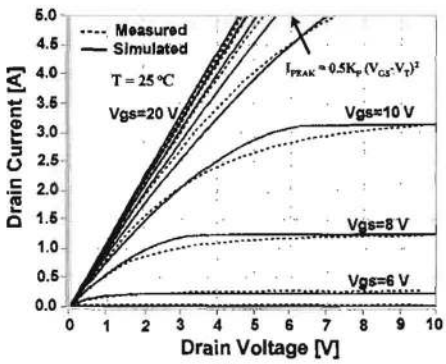
The 100 A, 10 kV SiC MOSFET/JBS modules being developed in HPE Phase II will be used in a 13.8 kV SSPS being developed in Phase III. The 13.8 kV line-to-line voltage has a peak voltage of approximately 20 kV requiring a gate driver with voltage isolation greater than 30 kV to provide adequate margin. The SSPS design may consist of a four-level converter or four-series-connected inverters each being operated at 20 kHz and having a nominal 5 kV bus. To minimize the switching losses, the SiC power MOSFETs must be switched in less than 100 ns, requiring a high gate current. The high dV/dt (50GV / s) imposed on the MOSFETs also requires a very low capacitance to ground through the gate driver to reduce common-mode EMI current.

In order to determine the gate drive requirements for the 10 kV, 100 A SiC modules, a careful examination of characterization results for smaller 10 kV SiC MOSFETs is useful. Fig. 1 shows the simulated and measured output characteristics of a 0.15 cm^2 (5 A rated) SiC power MOSFET at 25 °C and 125 °C. The gate driver needs to provide 20 V to maintain a low on-state voltage at high temperature and a high peak current at low temperature. Fig. 2 shows measured and simulated resistive load switching waveforms for the MOSFET with different gate drive resistances [8]. These waveforms indicate that the gate driver resistance has to be less than 10 Ω to achieve high switching speed for the 5 A rated die. It is shown in [6,7] that the resistance must be

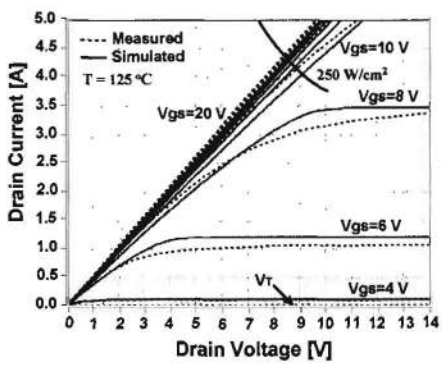
scaled to 0.5 Ω for a 100 A (3.09 cm^2) multi-chip MOSFET module.

In this paper, results are given for a half-bridge 10 kV 50 A SiC module that contains five 0.309 cm^2 MOSFET chips for each transistor. Figs. 3 and 4 show measured MOSFET transfer characteristics at both 25 °C and 100 °C. These five-chip MOSFETs are packaged in a module size that can accommodate approximately ten 0.309 cm^2 chips, and such multi-chip MOSFET modules are expected to meet the HPE Phase III nominal goal of 100 A per switch. It can be seen from the transfer characteristics that a full 20 V PWM driver is required to provide the highest MOSFET peak current at the lower temperature.

The 20 V, 0.5 Ω, 30 kV voltage-isolated gate drive circuit described in this paper provides the capability necessary to test the multi-chip modules developed in HPE Phase II and serve as a prototype for HPE Phase III. This drive circuit is described in the following section.



(a)

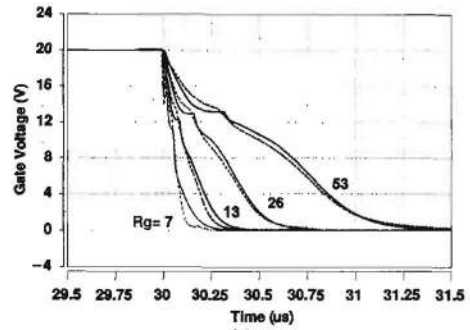


(b)

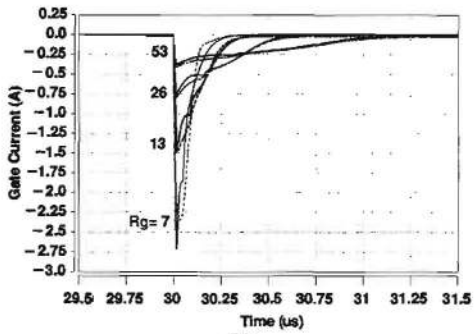
Fig. 1: Comparison of scaled measured (dashed) and simulated (solid) output characteristics at 25 °C (a) and at 125 °C (b) for a 5 A, 10 kV SiC power MOSFET.

III. Circuit Description

Fig. 5 is a block diagram of the new high-current, high-voltage-isolated gate drive circuit presented in this paper. The circuit consists of ground-referenced and high-voltage-isolated portions that are connected with three high-voltage-isolated, high frequency transformers. One transformer provides power to the high voltage portion of the circuit and the other two transformers transmit the gate drive signal. The input to the circuit requires a 5 V PWM signal, and this is processed to produce a 0 to 20 V high current replica of



(a)



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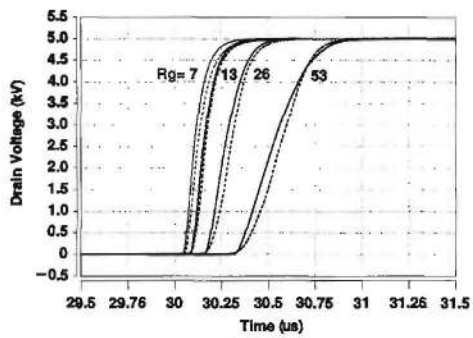

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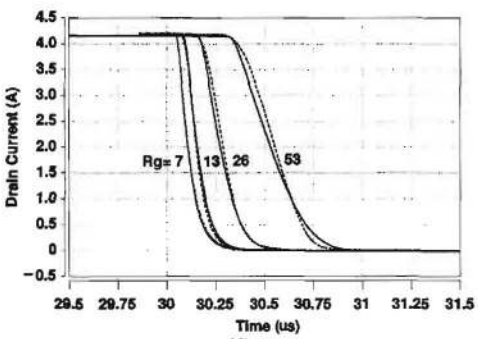

(d)

Fig. 2: Comparison of measured (dashed) and simulated (solid) resistive-load switching turn-off waveforms at 25 °C for a 5 A, 10 kV SiC MOSFET for various gate-drive resistances: (a) gate voltage, (b) gate current, (c) drain voltage, and (d) drain current.

the PWM signal to the SiC MOSFET gate. The circuit has no restrictions on duty cycle, and it can provide single pulses for laboratory characterization of the SiC devices as well as be able to drive these devices in a 20 kHz PWM application.

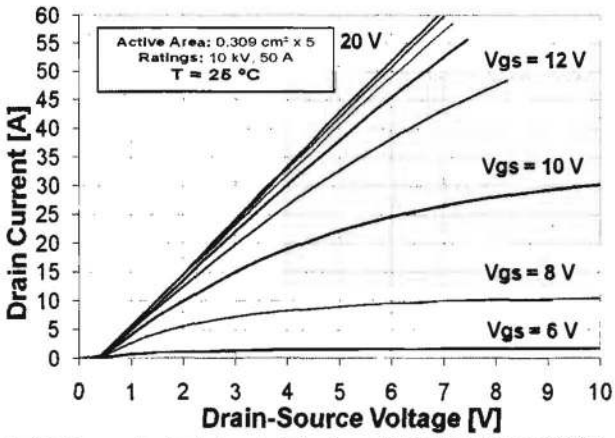

Fig. 3: Measured output characteristics for a 10 kV, 50 A SiC MOSFET at 25 °C.

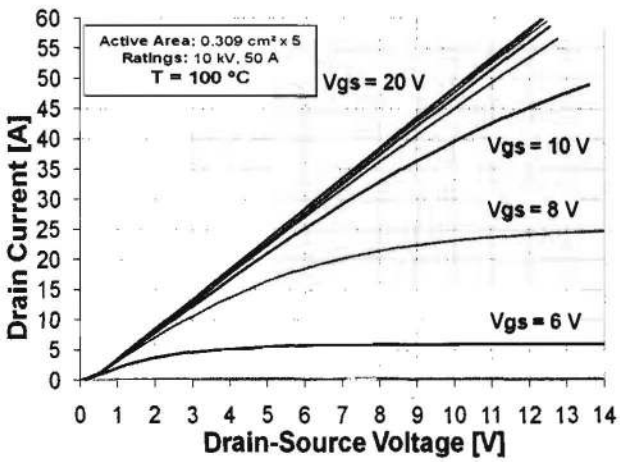

Fig. 4: Measured output characteristics for a 10 kV, 50 A SiC MOSFET at 100 °C.

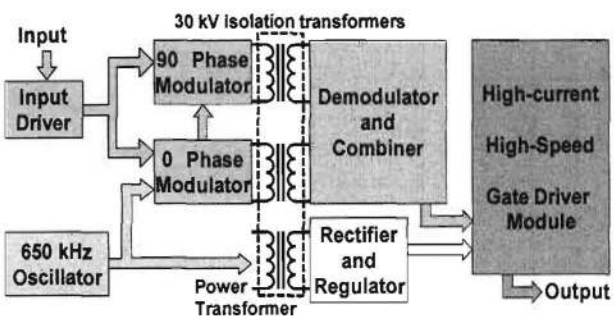

Fig. 5: Block diagram of the isolated gate drive system.

The signal-ground referenced portion of the circuit includes a 650 kHz oscillator that delivers a square-wave to drive the power transformer and also to drive a 0° phase modulator. An additional 90° phase modulator is supplied with a 90° phase-lagged 650 kHz signal from the 0° phase modulator. Each modulator is a full-bridge that obtains modulating power from the input via a power amplifier buffer. Each modulator produces a replica of the input PWM signal riding on a 650 kHz carrier, and these outputs are fed to separate isolation coupling transformers. The reason for having the two modulators operating 90° out-of-phase is that it greatly improves demodulator performance by eliminating the need for a filter network that would add delay and restrict the ability to transfer well-defined narrow PWM pulses.

In the demodulator and combiner block, the secondary voltages from the two isolation transformers with their different phases are individually rectified and combined. The purpose of the two phases is to have one phase delivering current during the time that the other phase is in a switching transition thus leaving no gaps in the demodulated output. With this scheme, the current ripple on the demodulator output is less than 20 %, which is low enough to prevent false turn-off of the gate driver chip. The rectifier and regulator block is straightforward, and provides operating power for the high-speed, high-current gate drive chip DEIC420 [9]. The gate drive chip is mounted on a small circuit board with carefully controlled power supply impedances. A detailed schematic and operating description of the new high-current, high-voltage-isolated gate drive circuit is given in the Appendix.

IV. Circuit Performance

This gate drive circuit is developed for 10 kV, 100 A SiC module high-side switches, and the switching frequency required is nominally 20 kHz. The 100 A modules will have a gate capacitance of roughly 80 nF and will require a total gate drive resistance of approximately 0.5 Ω (including the DEIC420 resistance and the balancing resistors within the module). The average power required to switch the gate with 20 V transitions can be very roughly approximated by the energy stored in the capacitor multiplied by twice the 20 kHz switching frequency, or 0.64 W. This is well within the power capability of the circuit as described in this paper. If switching above 20 kHz is required, the power capability of the rectifier and regulator section of the system would have to be increased.

System common-mode noise resulting from high-side switching with fast transitions is critically dependant on the parasitic capacitance between the system ground and the high-side switch and driver. For this reason, the transformers in the circuit of Fig. 5 need to be designed with minimal primary-to-secondary capacitance. Fig. 6 shows the winding technique used to fabricate each of the three transformers in Fig. 5. The windings consist of the required number of turns of # 26 Teflon-insulated wire inserted in PVC tubing. The cores are TX13/7.9/6.4-3E27 toroids. The measured capacitance of each transformer is about 1.7 pF for a total of approximately 5 pF from the high-voltage-isolated portion of the circuit to ground.

A sample transformer was tested to evaluate the voltage isolation capability. The test circuit is shown in Fig. 7. Two

different leakage currents are measured. In the first case, only the 26.8 kV DC voltage is applied. The measured leakage current is 0.5 nA. In the second test, the transformer is subjected to the 26.8 kV DC, and at the same time a 6.5 kV pulse waveform is added as shown in Fig. 7. The pulses are about 12 μs wide and at about 15.7 kHz rate. The measured leakage current under these conditions is 2.3 nA. It is not clear whether the additional leakage current is due to properties of the dielectric in the transformer or whether it is the result of ionization in the air around the circuit elements. In any case, this leakage is sufficiently low as to not cause problems in high-side switching applications.

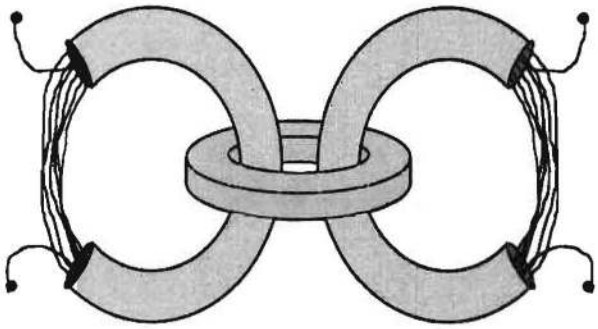

Fig. 6: Low-capacitance, high-voltage transformer construction.

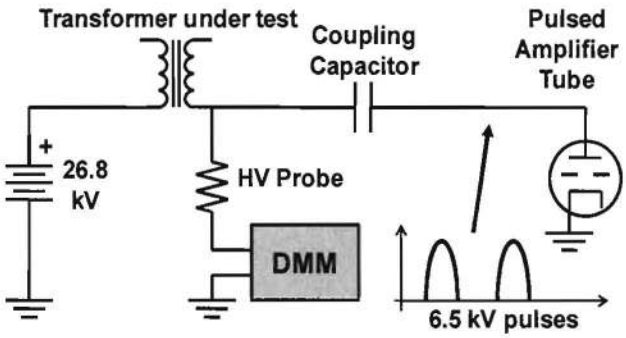

Fig. 7: Test circuit for measuring transformer leakage current.

V. Discussion of Results

Measured (dashed) and simulated (solid) waveforms are shown in Fig. 8 for the high-current, high-voltage-isolated gate driver presented in this paper with a 0.5 Ω and 80 nF series test load. The entire driver circuit itself is not simulated, but rather only the output portion including its internal output impedance, which is used to generate the gate waveforms before and after the test load. This load is similar to the gate driver requirements imposed by the 10 kV, 100 A half-bridge SiC MOSFET/JBS power module and drive shown in Fig. 9. The waveforms of Fig. 8 include the gate voltage at the output terminal of the gate driver (V_{DR1}), and the voltage at the junction of the 0.5 Ω and 80 nF capacitor (V_{G1}). Note that V_{DR1} and V_{G1} are defined in Fig. 9, however in that figure the 0.5 Ω resistor and the 80 nF capacitor actually represent the internal module MOSFET chip resistors and gate capacitances. This voltage corresponds to the MOSFET gate voltage internal to the module when the driver is connected to an actual module.

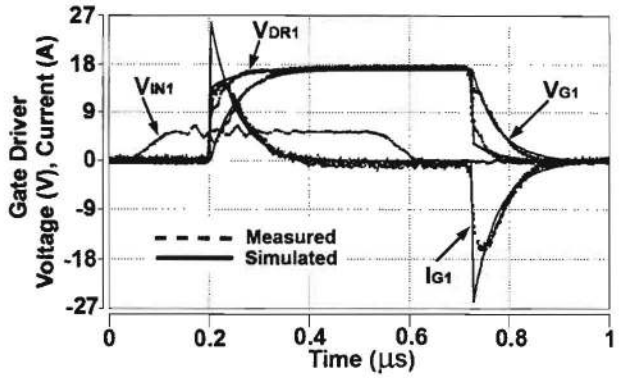

Fig. 8: Gate driver current and voltage simulated (solid) and measured (dashed) waveforms.

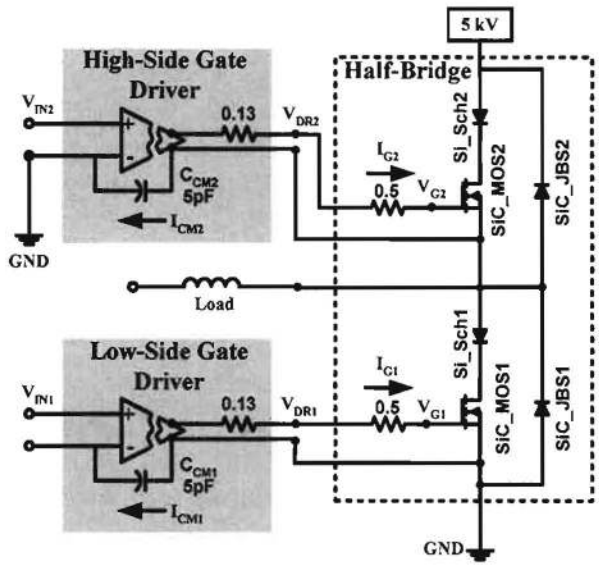

Fig. 9: Circuit topology of the half-bridge SiC power MOSFET module with series diodes to prevent reverse conduction in the MOSFETs.

Fig. 8 also shows the measured gate driver input voltage (V_{IN1}). The overall delay of the isolated gate drive system is about 120 ns. The major difference between the measured and simulated waveforms comes from a combination of the current being limited by parasitic inductance and the internal gate drive chip output devices.

Fig. 9 shows the SiC module with its connection to both upper and lower gate drivers similar to the driver described in this paper. This represents a typical application configuration. For the results of this paper, only one gate driver is used, as only one MOSFET is characterized at a time. The gate of an unused MOSFET is connected to its source for these device characterizations.

Simulated waveforms are presented in Fig. 10 for the low-side SiC MOSFET and the parasitic common-mode current coupled through the 5 pF capacitor (C_{CM2}) shown in Fig. 9. The waveforms are based on a physics-based model

of the 10 kV, 100 A half-bridge SiC MOSFET/JBS power module [5, 6] operating in an application circuit with an inductive load. Presented in the figure are waveforms for (a) zoomed-in turn-on and turn-off drain current (I_{DRAIN2}) and drain-to-source voltage (V_{DRAIN2}), (b) zoomed-in turn-on and turn-off gate current (I_{G1}) and gate-to-source voltage (V_{G2}) for the lower SiC MOSFET with A_{MOSFET} = 3.09 cm^2 and the upper SiC JBS diode with A_{JBS} = 2.0 cm^2, and (c) the common-mode current (I_{CM1}) passing through C_{CM1}.

The waveforms of Fig. 10 indicate the fast turn-on and turn-off switching speeds of typically less than 100 ns of the SiC MOSFET in the module are achieved. As mentioned previously, the modules characterized in this work are devices consisting of five MOSFETs per switch, and are similarly scaled in terms of the diode chip count (total diode area). For the 50 A module measured in this work, the area of the insulating direct-bond-copper (DBC) layers and the area of the diodes are larger than the optimal areas used for the simulated waveforms of Fig. 10. Thus the switching transition times shown in this paper will likely be increased for the 100 A modules of the future with more optimal area ratios.

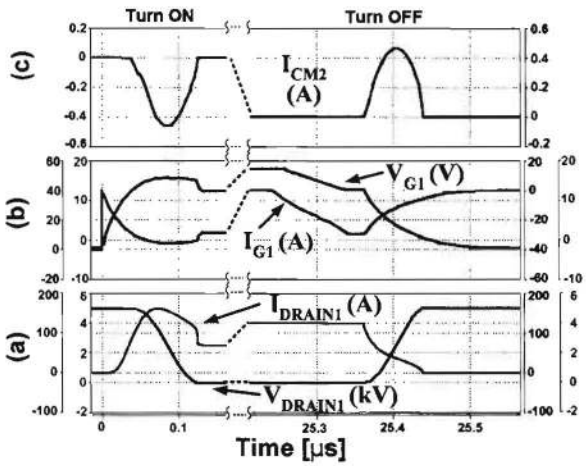

Fig. 10: Simulated waveforms for the low-side SiC MOSFET in the 100 A, 10 kV half-bridge power module: (a) zoomed-in turn-on and turn-off drain current and drain-to-source voltage, (b) zoomed-in turn-on and turn-off gate current and gate-to-source voltage, and (c) the common-mode current through C_{CM2}.

Fig. 11 shows the drain leakage current as (a) linear scale and (b) semi-log scale characteristics for the high-side MOSFET in the 50 A, 10 kV SiC MOSFET/JBS half-bridge power module as shown in Fig. 9 at Vgs = 0 V at 25 °C and 100 °C. The measurements are repeated three times for 25 °C and twice for 100 °C. Fig. 12 shows the gate-source voltage turn-off waveforms for 5 kV and multiple currents for an inductive load with R_G = 0.13 Ω.

Fig. 13 shows measured inductive load turn-off current and voltage waveforms for different load currents up to the continuous current rating of the module. In this case the source of the high-side MOSFET is shorted to the drain of the high-side MOSFET and the inductor is applied with an external clamp diode to effectively measure the low-side MOSFET as a discrete transistor. The external clamp diode with a 5 kV clamp supply voltage is used so that the drain current can be measured directly with an external current probe.

Fig. 14 shows the measured low-side MOSFET inductive load turn-off drain voltage and source current waveforms for different gate resistors. In this case the drain of the low-side MOSFET is connected to the inductive load and the drain of the high-side MOSFET is connected to the 5 kV clamp supply so that the module internal SiC JBS antiparallel diode is used as the voltage clamp. The figure demonstrates that a gate resistor value of less than 1.1 Ω only results in a turn off delay whereas larger gate resistances increase the voltage and current transition times and thus increase turn-off losses. The voltage rate of rise is different between Figs. 13 and 14 because the capacitances of the high-side MOSFET components and the DBC must be charged as the voltage rises in the case of Fig. 14.

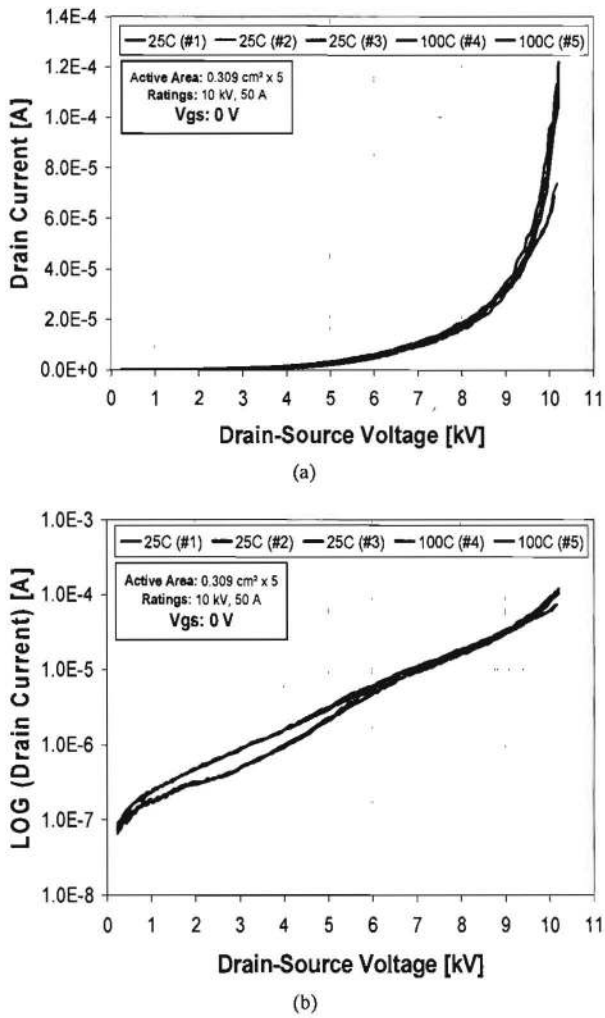

Fig. 11: Drain leakage current (a) linear scale and (b) simi-log scale characteristics for high-side MOSFET in the 50 A, 10 kV SiC MOSFET/JBS half-bridge power module as shown in Fig. 9 at Vgs = 0 V at 25 °C and 100 °C.

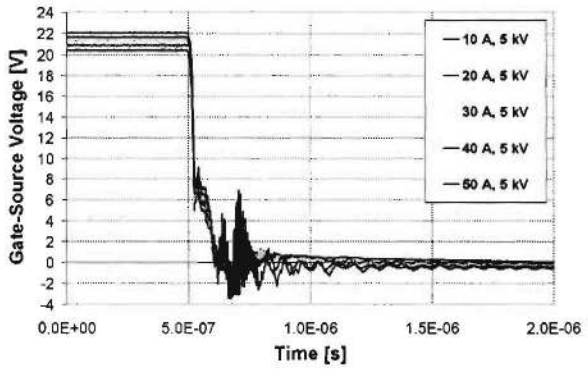

Fig. 12: Gate-source voltage waveforms at 5 kV (10 A, 20 A, 30 A, 40 A, and 50 A) for the inductive load turn-off switching with $R_G = 0.13\ \Omega$.

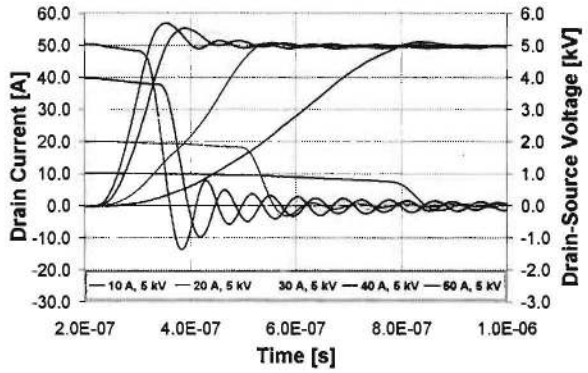

Fig. 13: Measured inductive load turn-off for the 50 A, 10 kV SiC MOSFET/JBS half-bridge power module at 25 °C.

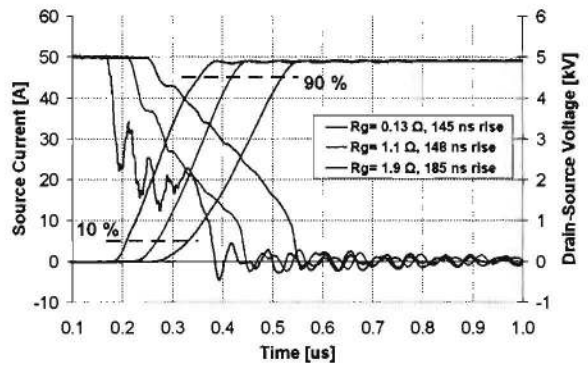

Fig. 14: Measured gate resistance dependence inductive load turn-off for the 50 A, 10 kV SiC MOSFET/JBS half-bridge power module at 25 °C.

VI. Conclusions

A new high-current, high-voltage-isolated gate drive circuit for 100 A, 10 kV SiC half-bridge modules is presented. The new gate drive circuit has the 30 kV voltage isolation required for the 13.8 kV, 2.75 MVA SSPS application. Measured and simulated results demonstrate that the gate drive circuit enables a gate resistance of less than 0.5 Ω as required to achieve 100 ns switching for 100 A, 10 kV SiC MOSFET/JBS modules. The low parasitic coupling capacitance of only 5 pF between the ground side and the floating drive side minimizes the common-mode EMI current. With the gate drive circuit prototype presented in this paper, tests can be performed on the modules being developed by the DARPA WBST-HPE Phase II and III programs thus demonstrating the ability of the modules to meet the requirements of the Phase III 13.8 kV, 2.75 MVA SSPS.

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Appendix

Fig. A1 is a detailed schematic of the new high-current, high-voltage-isolated gate drive circuit. A 650 kHz oscillator and buffer (Q1-Q4) delivers square-wave drive to the power transformer (T7) and also to a resonant tank consisting of L2 and the reflected gate capacitances of modulator transistors (Q6-Q9). The quality factor (Q) of the resonant network is reduced by the clamping diodes D3 and D4 so that a clamped sine-wave of controlled amplitude is delivered to the gates of Q6-Q9. Modulator transistors Q6-Q9 form a full-bridge that obtains its power from the inverting driver U1 (MIC4421), which is a gate-driver chip. In this scheme, the voltage that supplies the bridge is a replica of the PWM input via Q4 and the U1. The amplitude of the PWM signal feeding the bridge is close to the DC supply voltage of 12 V. This circuit block is shown as the 0° phase modulator in Fig. 3 and the bridge delivers a 12 V PWM signal riding on a 650 kHz carrier to the isolation transformer (T4). Another circuit block in Fig. 3 is shown as the 90° phase modulator. This modulator works just like the 0° phase modulator except that the 650 kHz carrier signal is delayed by 90° by the clamped resonant network consisting of L1 and the parasitic gate capacitances of modulator transistors Q10-Q13. In the demodulator and combiner block, the secondary voltages from the two isolation transformers with their different phases are individually rectified and combined. Buffer transistor Q14 drives collector power from the rectifiers, and has a small storage capacitor C7.

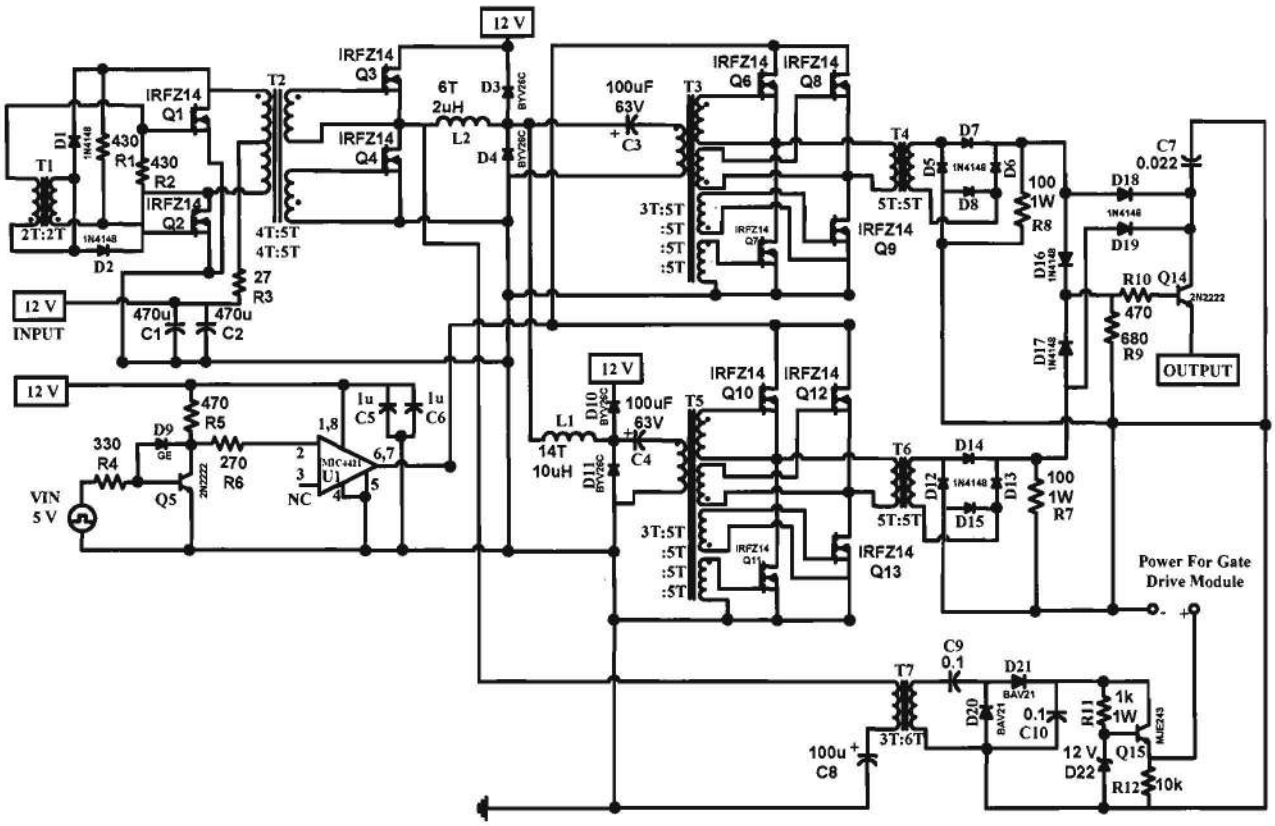

Fig. A1: A detailed schematic of the isolated gate-driver system.

This transistor is needed to drive the 50 Ω input impedance of the gate-driver chip input termination network. The 100 Ω, 1 W resistors R7 and R8 are loads that are used to overcome leakage inductance in the isolation transformers. The purpose of the two phases is to have one phase delivering current during the time that the other phase is in a switching transition, thus in principle there are no gaps in the demodulated output. Without the load resistors, the current in one phase would not overcome the leakage inductance until after the other phase actually entered a switching transition period, and this would cause a gap in the demodulator output. If the buffer transistor was not used, these 100 Ω resistors would need to have much lower values and much more power would be wasted. With this scheme, the current ripple on the demodulator output is less than 20 %, which is low enough to prevent false turn-off of the gate driver chip. The rectifier and regulator block is straightforward. The voltage doubler configuration requires fewer turns on the secondary power transformer T7, thus reducing capacitance. The zener diode D22 can be selected to obtain the desired switching voltage for the high-side switch by adjusting the supply voltage of the gate-driver chip.

Although the application for this gate drive circuit calls for 20 kHz, it is interesting to explore its capability and limits for higher switching frequencies. As previously discussed, the carrier frequency is 650 kHz. If the input PWM frequency is 650 kHz, the circuit does not work. Otherwise, PWM frequencies either above or below this frequency can be transferred. If the PWM frequency is an odd harmonic or odd sub harmonic of 650 kHz, the output of the demodulator can have additional ripple. There is little point in addressing frequencies above 650 kHz because the application of this circuit will likely be restricted to much lower frequencies. The 3rd sub harmonic occurs at about 216 kHz, and if this PWM frequency is applied the demodulator output ripple is about 30 %, and the gate-driver chip could possibly have false turn-off events. The 5th sub harmonic occurs at about 130 kHz, and the ripple is about the same as the contribution from the phase switching previously discussed and there is adequate immunity from false turn-off events. Because of the square wave carrier, even-order sub harmonics do not cause problems. Also, sub harmonics of higher order than the 5th are not readily visible on the demodulated output. Therefore, this is a robust system for all PWM frequencies below 216 kHz.