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PAPERS

High voltage low quiescent current LDO with self-regulation impedance buffer

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To improve the whole characteristic of the LDO, a low quiescent current structure of high voltage LDO with self-regulation impedance buffer and bandgap amplifier is presented in this paper. With the bandgap amplifier proposed, the function of voltage reference and error amplifier can be achieved simultaneously, which can efficiently reduce the consumption. The load capacitor can be as small as 0.47 μF by using the self-regulation impedance buffer and current buffer compensation scheme. The LDO has been implemented in a 0.18 μm process with die size 0.03 mm^2. Without the load, the consumption quiescent current of the LDO is 1 μA. Experimental result shows that the overshoot and undershoot of line transient response are less than 30 mV/V. The load regulation is about 0.1A, and line regulation is about 0.07 mV/V at no load condition.

K e y w o r d s: LDO, self-regulation, buffer, bandgap, load capacitor

1 Introduction

With the improving demands of the green power IC (integrated circuit), the LDO (low-dropout regulator) with its low power consumption and stable output voltage gets a lot of applications [1-3]. During the design process, low dropout voltage, low consumption, adequate output current and the fast-transient response are four main issues which should be focused [4,5]. The traditional LDO consists of the EA (error amplifier), the power MOS, the feedback resistor network and the bandgap voltage reference circuit. The low quiescent current will restrict the transient response of LDO, and then slow down the transient response speed [6]. It leads to a substantial overshoot or undershoot, even makes the device misoperation or the load damaged. Zero-tracking is proved to be an effective compensation scheme [7-9]. The internal zero position can be changed with the variation of the output pole. But the structure and more transistors are required. It leads to a larger die size and more power consumption. PCA (programmable capacitor array) is also suffered from more die size and high cost [10]. Reference [11] employed the structure called super-source-follower that can decrease the buffer output impedance greatly without much tail current [12], but the problem is the negative feedback loop cannot be stable in all cases, especially when driving a capacitive load [13]. FVF (flipped voltage follower) is also a good way to enhance the transient response but more transistors and current will be consumed [14].

In order to reduce the chip die size and the power consumption for enhance transient response, a novel bandgap amplifier with current buffer compensation and self-regulation buffer is proposed to realize a compact LDO [15]. The current buffer compensation can reduce 60% size of the on-chip frequency compensation capacitor without influencing the stability. The output stage of the LDO uses auto adjusting buffer, which can improve the response speed.

2 The structure of the proposed LDO

In this section, the stability of the proposed LDO will be discussed by the loop-gain transfer function $H(s)$ of the regulation loop. Small-signal block diagram of the proposed LDO with current-buffer is shown in Fig. 1.

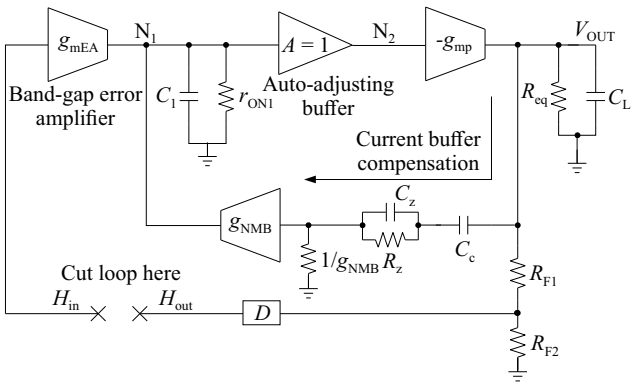

Fig. 1. Small-signal block diagram of the proposed LDO

In Fig. 1, g_{mEA}, g_{NMB} and g_{mp} are the transconductance of bandgap amplifier, current buffer stage

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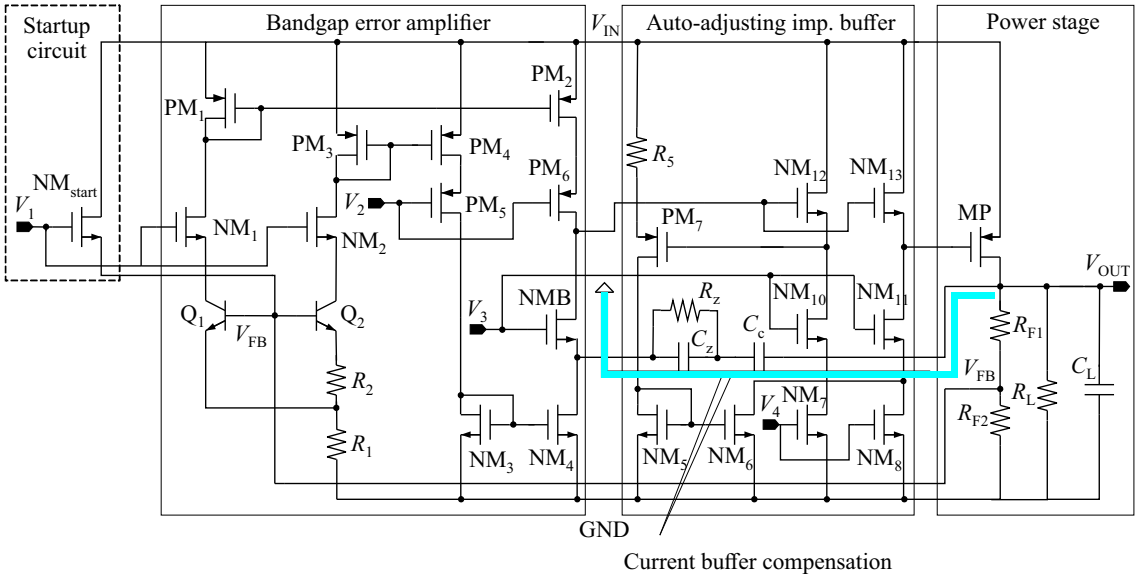

Fig. 2. Schematic of the proposed LDO

NMB and power MOS M_{p}, respectively. R_{eq} is the output impedance of power MOS, and F is the feedback factor, then

$$H_{\mathrm{out}} = -\left[g_{\mathrm{mEA}}H_{\mathrm{in}} + \frac{V_{\mathrm{out}}}{1/g_{\mathrm{NMB}} + (R.z||\frac{1}{sC_{\mathrm{Z}}}) + \frac{1}{sC_{\mathrm{C}}}}\right] \times \times \left(r_{\mathrm{OM}}||sC_1\right) g_{\mathrm{mp}} \left(R_{\mathrm{eq}}||\frac{1}{sC_{\mathrm{L}}}\right) F. \quad (1)$$

Here, $C_{\mathrm{L}}, C_{\mathrm{C}}, C_{\mathrm{Z}} >> C_1$, $F = R_{\mathrm{F2}}/(R_{\mathrm{F1}} + R_{\mathrm{F2}})$ and $g_{\mathrm{mp}} \propto \sqrt{I_{\mathrm{load}}}$, $R_{\mathrm{eq}} \propto 1/\sqrt{I_{\mathrm{load}}}$.

Based on above, the loop-gain transfer function of the proposed LDO is given as

$$H(s) = \frac{H_{\mathrm{out}}}{H_{\mathrm{in}}} \approx -\frac{F g_{\mathrm{m1}} r_{\mathrm{ON1}} g_{\mathrm{mp}} R_{\mathrm{eq}} \left(1 + \frac{sC_{\mathrm{C}}}{g_{\mathrm{NMB}}}\right)(1 + sR_{\mathrm{Z}}C_{\mathrm{Z}})}{as^4 + bs^3 + cs^2 + ds + 1}. \quad (2)$$

When the load current $I_{\mathrm{load}} = 0$, current flowing through the power MOS MP is very small, thus g_{mp} is so small, the transfer function $H(s)$ can be approximated by

$$H(s) \approx -\frac{F g_{\mathrm{m1}} r_{\mathrm{ON1}} g_{\mathrm{mp}} R_{eq}}{(sC_{\mathrm{L}}R_{\mathrm{eq}} + 1)(sr_{\mathrm{ON1}}C_1 + 1)}, \quad (3)$$

with two poles: $p_1 = -1/(C_L R_{\mathrm{eq}})$, $p_2 = -1/(r_{\mathrm{ON1}}C_1)$, the value of C_1 is so small that p_2 is out of the UGB (unit gain bandwidth). So, there is only one pole p_1 in the range of the UGB, and the loop can achieve good phase margin under $I_{\mathrm{load}} = 0$.

When the load current increases sharply, g_{mp} gets relatively large, and the equivalent output resistance in output stage, R_{eq} is quite small. Then the transfer function of H(s) is approximated as

$$H(s) \approx -\frac{F g_{\mathrm{mEA}} r_{\mathrm{ON1}} g_{\mathrm{mp}} R_{\mathrm{eq}}}{(sR_{\mathrm{eq}} r_{\mathrm{ON1}} g_{\mathrm{mp}} C_{\mathrm{c}} + 1)(s\frac{C_1 C_{\mathrm{L}}}{g_{\mathrm{mp}} C_{\mathrm{c}}} + 1)}. \quad (4)$$

According to the transfer function in (4), there are also two poles

$$\begin{cases} p_1 = \dfrac{1}{R_{\mathrm{eq}} r_{\mathrm{ON1}} g_{\mathrm{mp}} C_{\mathrm{c}}} \\ p_2 = \dfrac{g_{\mathrm{mp}} C_{\mathrm{c}}}{C_1 C_{\mathrm{L}}} \propto \dfrac{C_{\mathrm{c}}}{C_1 C_{\mathrm{L}}} \sqrt{I_{\mathrm{load}}} \end{cases}.$$

Because of the range of g_{mp} is large, p_1 is the dominant pole and p_2 is the non-dominant pole. Since C_1 is small, p_2 locates at high frequency. Furthermore, the unit gain frequency can be expressed as

$$\omega_0 = \frac{1 + D g_{\mathrm{mEA}} g_{\mathrm{mp}} r_{\mathrm{ON1}} R_{\mathrm{eq}}}{R_{\mathrm{eq}} r_{\mathrm{ON1}} g_{\mathrm{mp}} C_{\mathrm{c}} + \dfrac{C_1 C_{\mathrm{L}}}{g_{\mathrm{mp}} C_{\mathrm{c}}}} \approx \frac{D g_{\mathrm{mEA}}}{C_{\mathrm{c}}}. \quad (5)$$

Because the value of ω_0 is independent of the load current, $\frac{g_{\mathrm{mp}} C_{\mathrm{C}}}{C_1 C_{\mathrm{L}}} >> \frac{g_{\mathrm{m1}}}{C_{\mathrm{C}}}$. There is also a pole in the range of UGB. Good phase margin can be guaranteed. In addition, p_2 increases with the load current, implying a better phase margin with the load current increased.

3 The implementation of the proposed LDO

In order to control the quiescent current and reduce the compensation capacitor, the proposed LDO with bandgap error amplifier (BGEA) and current buffer scheme is presented. At the same time, the output stage of the proposed LDO using the self-regulation buffer, so it is called BGEA LDO. This scheme can resolve the trade-off among the quiescent current, the chip die size and the transient response. The traditional LDO usually uses separate voltage reference and EA. In this paper, the proposed LDO with bandgap amplifier structure is shown in Fig. 2. It consists of the startup circuit, the BGEA, the self-regulation impedance buffer and the power MOS MP.

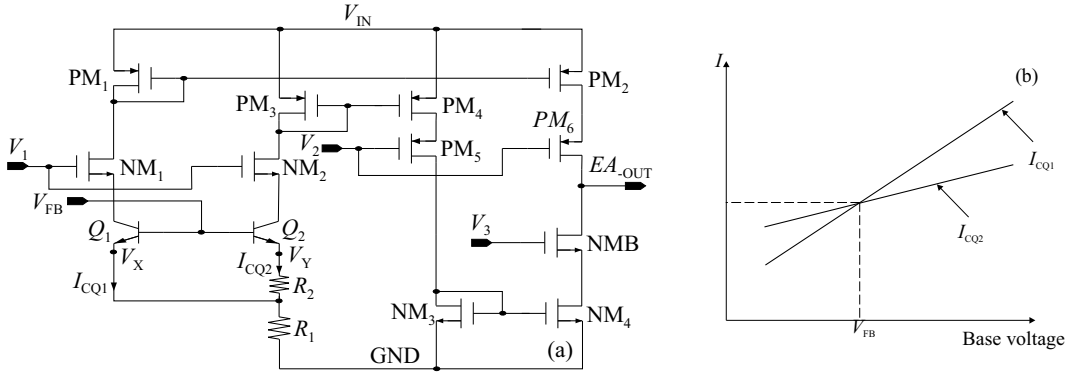

Fig. 3. (a) – the structure of BGEA, (b) – the relationship of Q_1 and Q_2 varies with V_{FB}

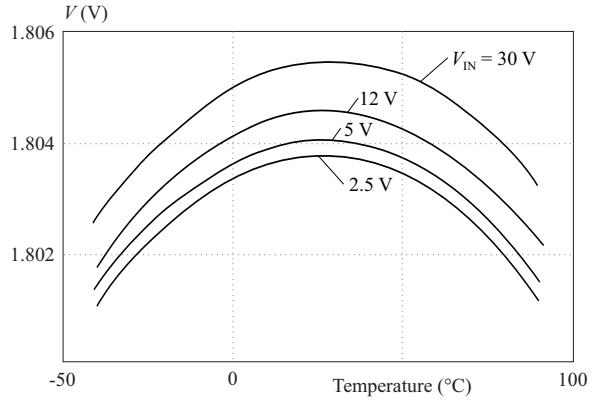

Fig. 4. V_{OUT} varies with temperature under different supply voltage

3.1 The structure of the bandgap error amplifier

In Fig. 3(a) is the Bandgap error amplifier (BGEA), it is performed by the feedback voltage V_{FB}, Fig. 3(b) is the curve of collector current relationships of Q_1 and Q_2 varying with V_{FB}. I_{CQ1} and I_{CQ2} are the collector current of Q_1 and Q_2 , V_X and V_Y are the emitter voltage of Q_1 and Q_2 , g_{mQ1} and g_{mQ2} are trans-conductance of Q_1 and Q_2 and the ratio of collector current I_{CQ1} and I_{CQ2} is m: 1, so

$$I_{CQ1} = \frac{g_{mQ1} V_{FB}}{1 + g_{mQ1}(1 + \frac{1}{m})R_1}, \tag{6}$$

$$I_{CQ2} = \frac{g_{mQ2} V_{FB}}{1 + g_{mQ2}\left[(1+m)R_1 + R_2\right]}, \tag{7}$$

where, G_{m1} and G_{m2} are defined as the equivalent trans-conductance of Q_1 and Q_2, respectively:

$$G_{m1} = \frac{\partial I_{CQ1}}{\partial V_{FB}} = \frac{g_{mQ1}}{1 + g_{mQ1}\left(1 + \frac{1}{m}\right)R_1} \approx \frac{1}{\left(1 + \frac{1}{m}\right)R_1}, \tag{8}$$

$$G_{m2} = \frac{\partial I_{CQ2}}{\partial V_{FB}} = \frac{g_{mQ2}}{1 + g_{mQ2}\left[(1+m)R_1 + R_2\right]} \approx \frac{1}{(1+m)R_1 + R_2}. \tag{9}$$

Set $m \geq 1$, it is easy to obtain $G_{m1} > G_{m2}$ and $I_{CQ1} \geq I_{CQ2}$. When the base voltage V_{FB} gets higher, both currents get bigger, because of faster variation rate of I_{CQ1} . Hence the current variation flow through PM_2 is larger than the current flow through NM_4, then the output of BGEA gets higher and so does the gate voltage of Power MOS MP. So the feedback loop of the circuit is negative. The base voltage can be fixed at V_{FB} and the V_{OUT} regulation is accomplished. Set $(W/L)_{PM1} : (W/L)_{PM2} = 1 : 1$ and $(W/L)_{NM3} : (W/L)_{NM4} = 1 : 1$, the trans-conductance g_{mEA} and the output impedance r_{ON1} are

$$g_{mEA} = \frac{\Delta I_{EA}}{\Delta V_{FB}} = \frac{G_{m1}\Delta V_{FB} - G_{m2}\Delta V_{FB}}{\Delta V_{FB}} = G_{m1} - G_{m2}, \tag{10}$$

$$r_{ON1} = (g_{mNMB} r_{ONMB} r_{ONM4}) \,||\, (g_{mPM6} r_{OPM6} r_{OPM2}). \tag{11}$$

So the gain of BGEA can be expressed as

$$G = g_{mEA} r_{ON1}. \tag{12}$$

For the requirement of low quiescent current, currents flow through the branch of PM1 and PM3 are only around several hundred nano-amperes, the output impedance r_{ON1} of BGEA is about several hundreds of MΩ. The value of g_{mEA} is small, as impedance r_{ON1} is large enough, so the gain BGEA is large enough to guarantee the accuracy of output voltage. As described above, $I_{CQ1} : I_{CQ2} = m$, $m \geq 1$, the size of Q_2 is n times than Q_1, the voltage V_{FB} and V_{OUT} can be expressed as

$$V_{FB} = V_{BEQ2} + \left[1 + \frac{(1+m)R_1}{R_2}\right] V_T \ln(mn), \tag{13}$$

$$V_{OUT} = \left(1 + \frac{R_{F1}}{R_{F2}}\right)\{V_{BEQ2} + \left[1 + \frac{(1+m)R_1}{R_2}\right] V_T \ln(mn)\}, \tag{14}$$

where, V_{BEQ2} is negative temperature dependent, the term in (square) brackets is a positive temperature dependent term, so V_{FB} and V_{OUT} can be set to reach a zero temperature dependence.

Figure 4 gives the simulation results of V_{OUT} varying with temperature under different supply voltage. From the figure, just about 1.804 V at $V_{\mathrm{IN}} = 5\,\mathrm{V}$, the temperature coefficient is about only 18 ppm, the line regulation is about 0.07 mV/V at no load condition.

3.2 Self-regulation impedance buffer

In many proposed works, source-follower buffer is used to separate large output impedance of EA from large parasitic capacitor of the power MOS. Fig. 5(a) shows the self-regulation impedance buffer circuit.

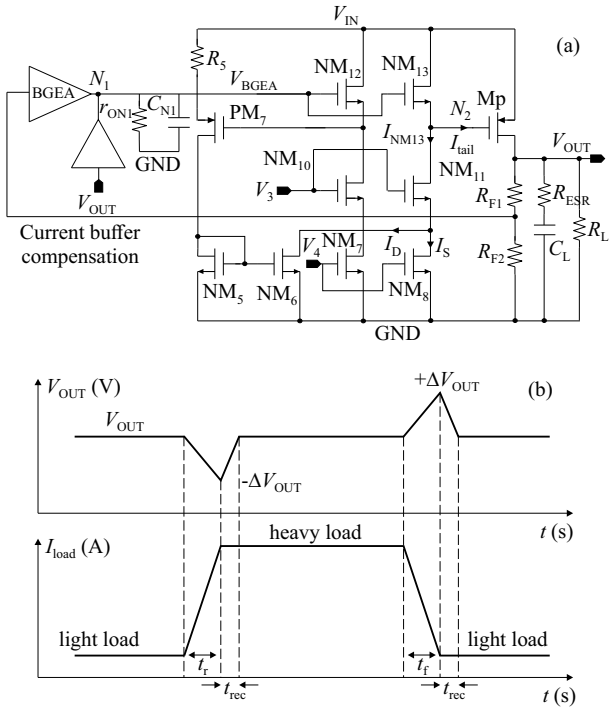

Fig. 5. (a) – the self-regulation buffer circuit and, (b) – the variation of V_{OUT} with load transient response

The threshold of the power PMOS MP is higher than that of the NMOS NM13, MP can be turned off completely. I_{NM13} is the bias current of the output stage in the self-regulation buffer circuit. I_{tail} is the charging or discharging current during the transient response. I_{D} is the dynamic bias current of the self-regulation buffer. I_{S} is the static bias current of the output stage. As $(W/L)_{\mathrm{NM5}} : (W/L)_{\mathrm{NM6}} = 1:1$, when V_{OUT} is regulated at a constant voltage

$$I_{\mathrm{tail}} = I_{\mathrm{NM13}} - \big(I_{\mathrm{D}} + I_{\mathrm{S}}\big) = 0\,. \tag{15}$$

The trans-conductance and output impedance of self-regulation impedance buffer circuit are

$$g_{\mathrm{mB}} = \frac{\Delta I_{\mathrm{tail}}}{\Delta V_{\mathrm{BGEA}}} = \frac{\Delta I_{\mathrm{NM13}} - \Delta I_{\mathrm{D}}}{\Delta V_{\mathrm{BGEA}}} = g_{\mathrm{mNM13}} + \frac{g_{\mathrm{mPM7}}}{1 + g_{\mathrm{mPM7}} R_5}\,, \tag{16}$$

$$r_{\mathrm{ON2}} = \frac{1}{g_{\mathrm{mNM13}}} \| \left[g_{\mathrm{mNM11}} r_{\mathrm{ONM11}} \big(r_{\mathrm{ONM8}} \| r_{\mathrm{ONM6}} \right] \approx \frac{1}{g_{\mathrm{mNM13}}}\,, \tag{17}$$

where,

$$g_{\mathrm{mNM13}} = \sqrt{2\mu_{\mathrm{n}} C_{\mathrm{ox}} \Big(\frac{W}{L}\Big)_{\mathrm{NM13}} \big(I_{\mathrm{D}} + I_{\mathrm{S}}\big)}\,. \tag{18}$$

The variation ΔV_{OUT} during the load transient response in Fig. 5(b), ΔI_{tail} is the charging or discharging current of the power PMOS MP, C_{L} is the output capacitance.

The load transient response is

$$\Delta V_{\mathrm{OUT}} = -\Delta I_{\mathrm{MP}} \big(R_{\mathrm{ESR}} + \frac{t_{\mathrm{rec}}}{C_{\mathrm{L}}} \big)\,, \tag{19}$$

while the recovery time can be estimated as

$$t_{\mathrm{rec}} < \Big[C_{\mathrm{L}} \frac{1 + \dfrac{R_{\mathrm{F1}}}{R_{\mathrm{F2}}}}{g_{\mathrm{mMP}} g_{\mathrm{mEA}} r_{\mathrm{ON1}}} - R_{\mathrm{ESR}} \Big]\,. \tag{20}$$

Hence, the self-regulation buffer can speed up the recovery time. The pole generated at N_2 node is

$$p_3 = -\frac{g_{\mathrm{mNM13}}}{C_{\mathrm{pra}}}\,. \tag{21}$$

As the value of r_{ON1} and C_{pra} are quite small, the pole p_3 is out of UGB. It can be concluded that p_3 has no influence on the stability of the proposed LDO.

4 Experimental results

The proposed LDO has been implemented in a 0.18 m CMOS process. Fig. 6 and Fig. 7 show the simulation results of loop gain transfer function of the proposed LDO for no load and full load, respectively.

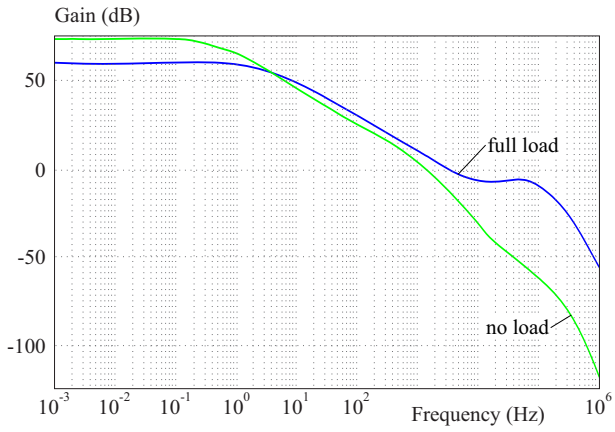

Fig. 6. Gain simulation under no load and full load 50 ma

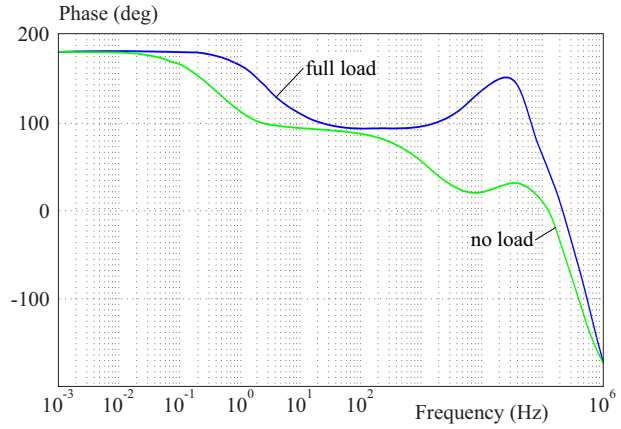

Fig. 7. Phase simulation under no load and full load 50 ma

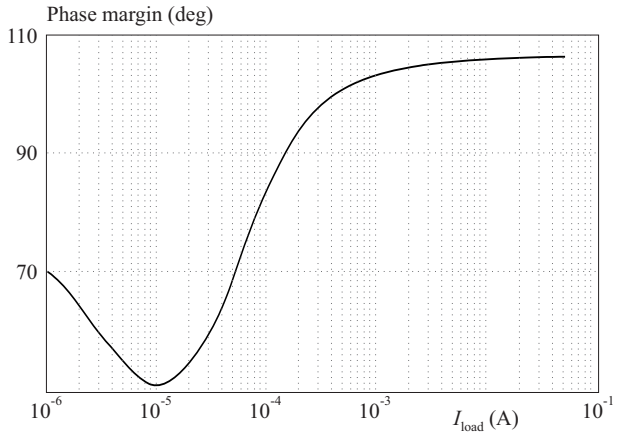

Fig. 8. Phase margin under different load current

From the Fig. 6, the load current in the no load and the full load cases, the open loop gain reached 74 dB and 58 dB, respectively. In Fig. 7, the load current in no load and the full load cases, the phase margin is 52 deg and 105 deg, respectively. In order to represent the phase margin more completely, the simulation results of the circuit at different load currents are shown in Fig. 8.

The simulation results show that the phase margin is always greater than 51 deg in the current range from 1 μA to 50 mA, which also verifies the stability of the system

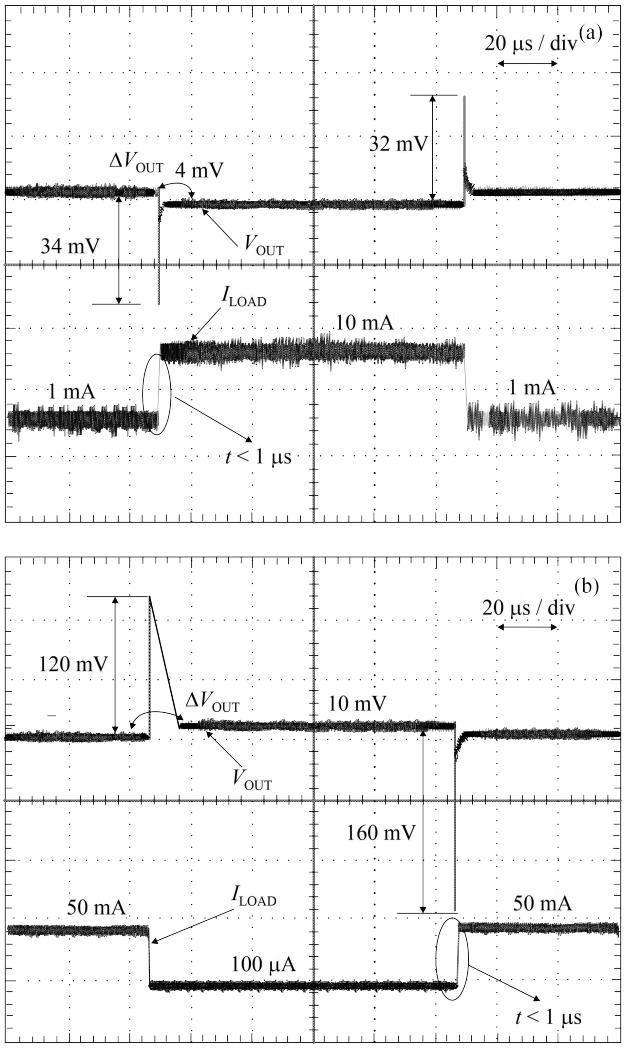

Fig. 9. The measurement result of the line transient response, $V_{\text{out}} = 1.8$ V

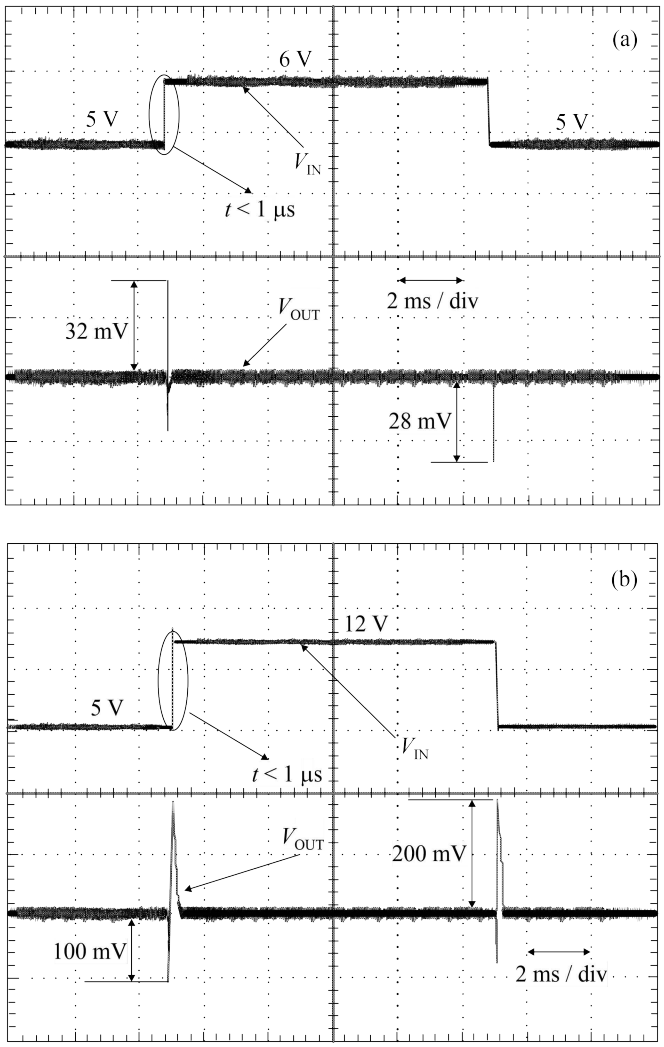

Fig. 10. The measurement result of the load transient response, $V_{\text{out}} = 1.8$ V

at full load current. Therefore, the LDO is stable with the proposed compensation scheme. To verify transient response of the circuit structure, line and load transient response are also measured. The measurement results are shown in Fig. 9 and Fig. 10.

Figure 9 shows the output voltage variation in line transient response from 5 V to 6 and from 5 V to 12 V in 1 μs with 10 mA load current, respectively. The overshoot voltage is 32 mV and the undershoot voltage is 28 mV.

Figure 10 gives the measured load transient response for a step load change from 1 mA to 10 mA and from 0.1 mA to 50 mA within 1 μs. The overshoot voltage is 32 mV and the undershoot voltage is 34 mV. It takes 10 μs for output to return to its normal value, the variation ΔV_{OUT} is about 4 mV to 10 mV, the load regulation is about 0.1%/A. A comparison of some other proposed LDO is given in Tab. 1. From the table the LDO presented here realize the minimum quiescent current, chip die size and small off-chip capacitor.

Table 1. 1 Comparison with previous reported LDOs

Reference	[6]	[14]	[15]	This work
Technology (μm)	0.35	0.13	0.13	0.18
Supply voltage (V)	3.3	1.2	1.25	5
Output voltage (V)	2.9	1	1	1.8
Load current: I_{Lmax} (mA)	100	50	100	50
Quiescent current: I_{q} (μA)	55	42	0.7	9.5
Load transient (mV) (I_{load}-rising)	90	140	76	32
Load transient (mV) (I_{load}-falling)	160	80	198	34
Load regulation (mV)	-	10	10	4
Line regulation (mV)	-	30	16.6	10
C_{L}(pF)	100	400	10^6	0.47×10^6
Year	2016	2019	2020	2023

5 Conclusions

This paper presents a novel structure of LDO using the self-regulation impedance buffer which can improve transient response. Compared with the traditional LDO, the proposed LDO consume 1A quiescent current in the no load condition and 10 μA quiescent current even in the full load. Meanwhile the LDO can realize good stability under full range of load current using the current buffer compensation. The circuit can realize as large as 50 mA load current with input voltage range between 2.5 V and 30 V.

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