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High-Voltage n-Channel IGBTs on Free-Standing 4H-SiC Epilayers

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High-Voltage n-Channel IGBTs on Free-Standing 4H-SiC Epilayers

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Abstract—In this paper, we describe a process for fabricating high-voltage n-channel double-diffused metal–oxide–semiconductor insulated gate bipolar transistors (IGBTs) on free-standing 4H silicon carbide (SiC) epilayers. In this process, all critical layers are epitaxially grown in a continuous sequence. The substrate is then removed, and device fabrication takes place on the carbon face of a free-standing epilayer having a total thickness of about 180 μm. For a drift layer with doping and thickness values capable of blocking 20 kV, the n-channel IGBT carries 27.3-A/cm^2 current at a power dissipation of 300 W/cm^2, with a differential ON-resistance of 177 m$\Omega \cdot$ cm^2. To our knowledge, this is the first detailed report of device fabrication on free-standing SiC epilayers.

Index Terms—Free-standing epilayer, high voltage, insulated gate bipolar transistor (IGBT), silicon carbide (SiC).

I. INTRODUCTION

THE RECENT emphasis on clean renewable energy and more efficient energy utilization has lead to renewed interest in distributed energy sources, hybrid electric vehicles, and intelligent power distribution grids, all of which require power semiconductor devices. In many of these applications, operating voltages are sufficiently high that complex multilevel converters are required if silicon power devices are used. Silicon carbide (SiC) devices are capable of operating at higher voltages than silicon, eliminating the need for multilevel circuits in many applications.

Since the early 1990s, the SiC power MOSFET has been the primary focus of research, and significant progress has been made. By 2004, the blocking voltage of SiC power MOSFETs had reached 10 kV, with specific ON-resistances as low as 123 m$\Omega \cdot$ cm^2 [1]. However, the drift region resistance of MOSFETs increases as the square of the blocking voltage, and at high voltages, this resistance begins to limit the range of applications that can be addressed. As blocking voltages increase, the SiC insulated gate bipolar transistor (IGBT) becomes an attractive choice to replace the SiC MOSFET, particularly in low-frequency switching applications [2].

In principle, n-channel IGBTs are preferred over p-channel IGBTs for their higher performance [2], but n-channel IGBTs require p-type substrates, which introduce a high resistance (0.8–1.0 $\Omega \cdot$ cm^2) in series with the device. The first SiC n-IGBTs were reported in 1996 [3], but their performance was inferior to MOSFETs of that day because of the high substrate resistance. Recently, a 13-kV n-IGBT has been reported by Cree, Inc. [4], [5], but their paper does not discuss removal of the substrate and provides no details about the formation of the p$^+$ collector region. To solve this problem, we have developed a novel inverted-growth process that, in principle, could allow all critical epilayers to be grown in a continuous sequence on an original growth substrate ($\sim$400 μm), which is subsequently removed by polishing. Continuous epigrowth has been shown to minimize basal plane dislocations that form at interrupted-growth interfaces and nucleate stacking faults during operation [6], [7]. In our process, device fabrication takes place on a free-standing epilayer with a total thickness of about 180 μm. The thick p$^+$ substrate is replaced by a thin p$^+$ epilayer, and the collector resistance is reduced by almost two orders of magnitude. The process is demonstrated by fabricating n-IGBTs on epilayers with doping and thickness values capable of blocking 20 kV. To our knowledge, this is the first detailed report of SiC devices fabricated on free-standing SiC epilayers.

II. DEVICE DESIGN AND FABRICATION

Fig. 1 shows a schematic cross section of the fabricated device. The junction field-effect transistor (JFET) region width W_J is selected based on the MEDICI simulations shown in Fig. 2. As the JFET width is reduced, the forward voltage increases due to the increasing resistance of the narrow JFET region. As shown, for W_J greater than 12 μm, the forward voltage drop V_F is relatively constant; thus, we select $W_J = 12$ μm for these devices.

The epitaxial growth process is illustrated in Fig. 3. Starting wafers are 75 mm n$^+$ (8° off-axis) 4H-SiC substrates purchased from Cree, Inc. First, a low-basal-plane-defect (LBPD) template layer and a standard 1-μm n$^+$ buffer layer are grown on the Si-face. Then, three layers are grown in succession: a 200-μm 2 $\times$ 10^{14} cm^{-3} n$^-$ drift layer, a 0.2-μm 1 $\times$ 10^{18} cm^{-3} n$^+$ nonpunchthrough buffer layer, and a 3-μm 1 $\times$ 10^{19} cm^{-3} p$^+$ collector layer. This inverted-growth procedure makes it possible to continuously grow all critical layers, minimizing the introduction of basal plane dislocations during growth (however, continuous growth was not used for the
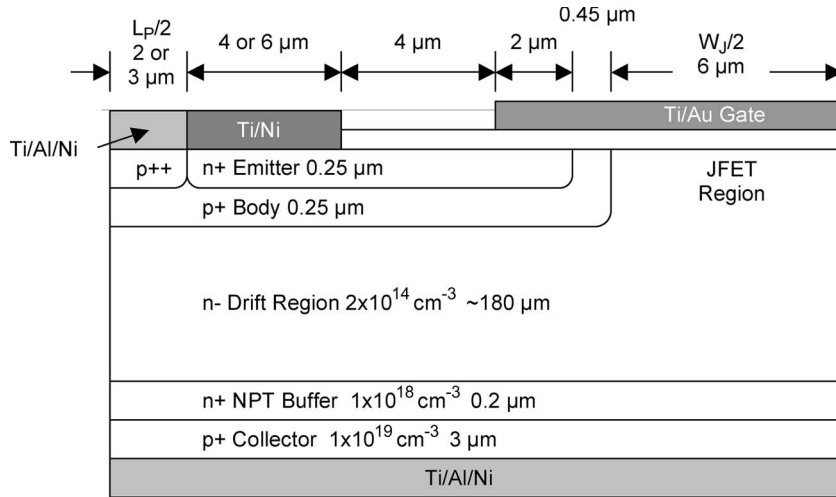
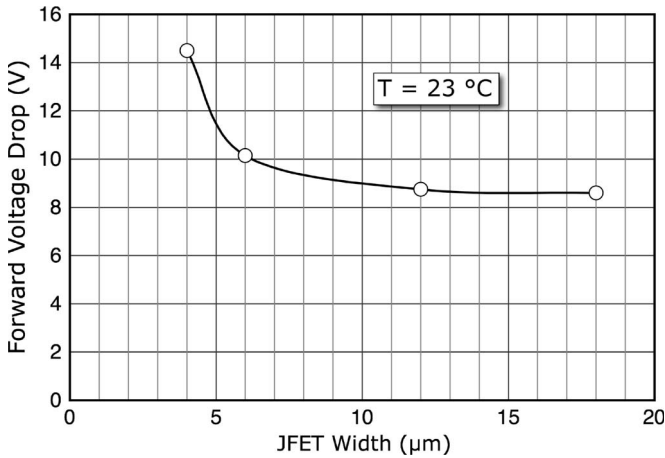Fig. 1.   Schematic cross section of one cell of the fabricated device.

Fig. 2.   Forward voltage drop of the IGBT as a function of the JFET width W_J, obtained from MEDICI simulations at $V_G = 20$ V and $J_C = 100$ A/cm^2.

Fig. 3.   Inverted-growth process. Epigrowth takes place on the Si-face of an n$^+$ 4H-SiC substrate. In principle, all layers can be grown in a continuous manner, minimizing basal plane dislocations that can nucleate stacking faults. After growth, the substrate, LPBD template, and n$^+$ buffer layer are removed by polishing, and device fabrication takes place on the carbon face of the free-standing epilayers.

devices reported here). The ambipolar lifetimes in the drift layer of two small pieces from one wafer are measured by microwave photoconductivity decay and time-resolved photoluminescence and are found to be greater than 1 μs over large portions of the wafer. The n$^+$ substrate, LBPD layer, and n$^+$ buffer layer are then removed by polishing at NovaSiC, and the wafer is inverted, with the p$^+$ collector at the bottom and the n$^-$ blocking layer at the top. Devices are fabricated on the top surface (carbon face) of the n$^-$ drift layer, as illustrated in Fig. 3.

To produce a short-channel MOSFET, we use the self-aligned technique of Matin et $al.$ [8], slightly adapted for the carbon face of SiC. First, 100 nm of silicon nitride is deposited by low-pressure chemical vapor deposition (LPCVD) at 825 °C to prevent the SiC from being oxidized in a later step. Then, a 1.5-μm polysilicon layer is deposited by LPCVD at 600 °C and patterned by reactive ion etching in SF$_6$ using a Ti/Ni mask. This polysilicon layer serves as the mask for the p-well implantation. The p-well is formed by a retrograde implantation of Al at 650 °C with (doses/energies) of $2.7 \times 10^{12}/90$, $3.1 \times$
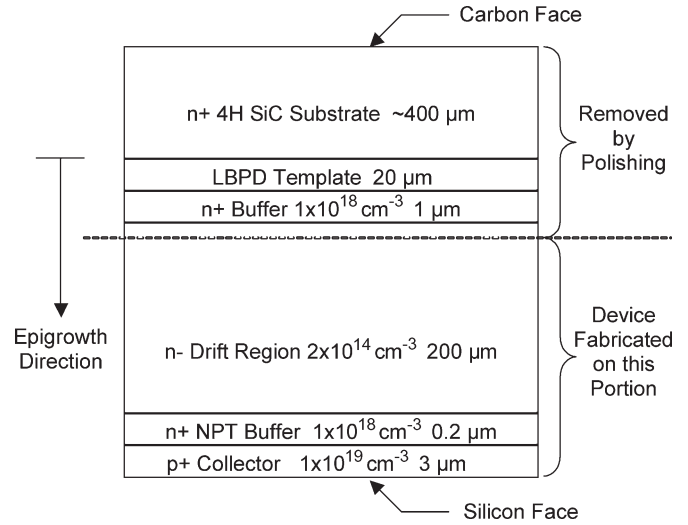
$10^{12}/140$, $5.6 \times 10^{13}/360$ (cm^{-2}/keV), respectively. This is followed by a shallow implantation of nitrogen at 650 °C with a dose of 8.8×10^{12} cm^{-2} and energy of 45 keV to reduce the threshold voltage. After the p-well and threshold-adjust implants, Ti/Ni is stripped, and the sample receives a 9-h wet oxidation at 1000 °C, which horizontally expands the polysilicon by about 0.45 μm [8]. The expanded oxidized polysilicon and a separate optical Ti/Au p$^+$ block mask are used to define the n$^+$ emitter implantation. To form the emitter, nitrogen is implanted at 650 °C with (doses/energies) of ($9.5 \times 10^{14}/50$, $1.4 \times 10^{15}/90$, $2.0 \times 10^{15}/150$) (cm^{-2}/keV). The MOS channel length is controlled by the horizontal expansion of the polysilicon implant mask and is around 0.45 μm. After removing all layers from the SiC top surface, a Ti/Au layer is deposited, patterned, and used as the mask for the
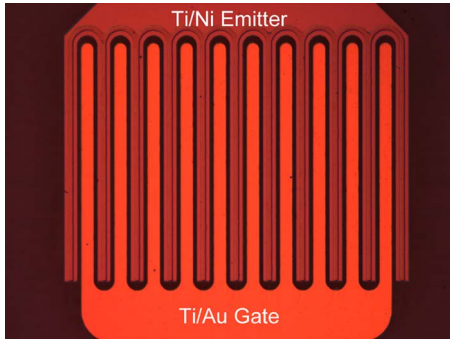
Fig. 4. Completed device. This device has ten fingers, with an active area of 3.4×10^{-4} cm^2.

Fig. 5. ON-state characteristics of an n-channel IGBT with an active area of 1.48×10^{-3} cm^2, measured at room temperature. The gate voltage ranges from 0 to 20 V in 1-V intervals. Two simulations are also shown: one with the actual n$^+$ and p$^+$ contact resistivities obtained from TLM measurements on the device wafer, and one with contact resistivities that can normally be obtained on 4H-SiC. Both simulations assume an ambipolar lifetime of 1 μs and $V_G = 20$ V (oxide field of 4 MV/cm). The dashed lines show the specific ON-resistance of the n$^-$ drift layer if no conductivity modulation was present (0.577 $\Omega \cdot$ cm^2) and the actual differential ON-resistance of the entire IGBT (0.177 $\Omega \cdot$ cm^2), demonstrating that significant conductivity modulation is occurring.

p$^+$ body-contact implantation. The body contact is formed by implanting Al at 650 °C with (doses/energies) of $(1.0 \times 10^{14}/40, 2.0 \times 10^{14}/100, 4.0 \times 10^{14}/180)$ (cm^{-2}/keV). All the implants are annealed in Ar for 30 min at 1600 °C under a graphite cap.

Following the implant anneal, the sample is oxidized in a pyrogenic system at 1100 °C for 20 min to form the gate oxide. A NO postoxidation anneal is then performed at 1175 °C for 70 min to reduce the interface trap density and improve the mobility [9]. The oxide thickness is around 45 nm after the NO anneal. We use a lower oxidation temperature and a shorter oxidation time on the carbon face because the oxidation rate is about ten times faster than on the silicon face.

Ohmic contacts are formed by depositing (33-nm Ti/ 167-nm Al/50-nm Ni) as the p$^+$ body contact and (33-nm Ti/ 167-nm Al/~100-nm Ni) on the back side as the p$^+$ collector contact. These metals are annealed in vacuum to form ohmic contacts. The target temperature for the p$^+$ contact anneal was 1000 °C, but the actual temperature reached during anneal is not precisely known due to equipment problems during annealing. However, as will be discussed in the next section, the annealed contacts are ohmic, suggesting that the peak temperature is well above 800 °C.

Emitter ohmic contacts and gates in these devices are formed using a modified fabrication sequence. In preliminary processing runs, we had observed high oxide leakage, thought to be caused by surface roughness from the implant anneals, which were uncapped in those runs. In this processing run, we wanted to preserve the option of subsequently depositing a thick low-temperature oxide (LTO) on top of the thermal oxide if the thermal oxide proved to be leaky. For this reason, we deposited a metal gate that could easily be removed to allow LTO deposition, if needed. Accordingly, (50-nm Ti/100-nm Ni) and (50-nm Ti/100-nm Au) are deposited and patterned as the n$^+$ emitter contact and the gate, respectively, and the emitter contacts are not annealed (previous experiments [10] had shown that unannealed Ti/Ni forms a low-resistance ohmic contact to a heavily doped n$^+$ material). Because the implants were annealed under a graphite cap in this run, surface roughness was minimal, and probe testing indicated that the thermal gate oxides were not leaky. As a result, LTO deposition was not needed, and the devices were ready for characterization. Fig. 4 is a photograph of the finished device.
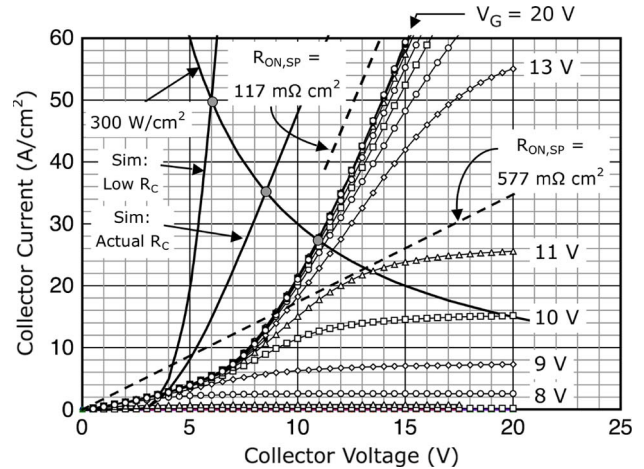
III. DEVICE CHARACTERIZATION

Fig. 5 shows the ON-state characteristics of an n-channel IGBT at room temperature. At a gate voltage of 20 V (oxide field of 4 MV/cm), the collector current J_{300} at the 300-W/cm^2 power limit is 27.3 A/cm^2. The figure also shows two MEDICI simulations of the IGBT. The first uses resistivities for the n$^+$ and p$^+$ contacts derived from TLM measurements on the actual devices (1.2×10^{-2} and 1.9×10^{-2} $\Omega \cdot$ cm^2, respectively), and the second uses resistivities that can typically be obtained on 4H-SiC (5×10^{-4} and 5×10^{-3} $\Omega \cdot$ cm^2, respectively). Both simulations assume an ambipolar lifetime of 1 μs and a gate voltage of 20 V, corresponding to an oxide field of 4 MV/cm. At the 300-W/cm^2 power limit, the J_{300} current density for the simulated device with low contact resistivities is 50 A/cm^2, the J_{300} for the device with contact resistivities of the actual device is 35 A/cm^2, and the J_{300} of the actual device is 27.3 A/cm^2.

The dashed lines in Fig. 5 correspond to the specific ON-resistance of the 180-μm n$^-$ drift layer *without* conductivity modulation (577 m$\Omega \cdot$ cm^2) and the differential ON-resistance of the actual device at $V_G = 20$ V (177 m$\Omega \cdot$ cm^2). Since the resistance of the entire device is 3× lower than the resistance of an unmodulated drift region, it is clear that substantial conductivity modulation is taking place. We also note that the differential resistance of the actual device at $V_G = 20$ V is the same as predicted by the simulations, suggesting that the assumed lifetime of 1 μs is reasonable. A possible explanation for the lateral voltage shift of the actual device is that the p$^+$ collector contact on the back side of the device may not be fully ohmic (note that this contact cannot be measured by TLM structures on the test chip). At low collector currents, the differential resistance of the p$^+$ back contact appears to
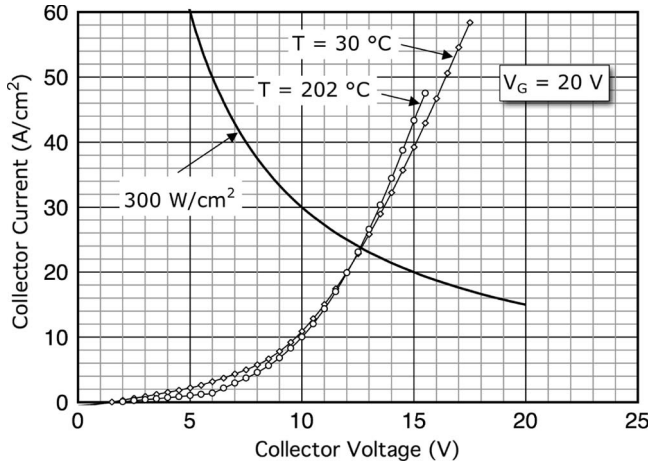
Fig. 6. ON-state characteristics of an n-channel IGBT at 30 °C and 202 °C. $V_G = 20$ V in both cases. The I–V characteristics and J_{300} are essentially unchanged at elevated temperatures due to the increase in lifetime with temperature, which compensates for the decrease in mobility.

be high, shifting the current–voltage (I–V) characteristic of the measured device to the right compared with the simulations. This results in a lower J_{300} than predicted by the simulations.

Fig. 6 shows the ON-state characteristics of an n-IGBT at 30 °C and 202 °C. The gate voltage is 20 V in both cases. As shown, J_{300} at elevated temperatures is essentially unchanged from its room-temperature value. In an IGBT, the current density depends on the ambipolar diffusion length, i.e., the square root of the ambipolar diffusion coefficient times the ambipolar lifetime. Although the ambipolar diffusion coefficient decreases with temperature, the ambipolar lifetime increases by almost the same factor, leaving the ambipolar diffusion length virtually unchanged. This is in contrast to the MOSFET, where the ON-resistance depends on the electron mobility in the drift region, which decreases with temperature, leading to much higher ON-resistances. The temperature dependence is important because, when the devices are operated at the package limit of 300 W/cm^2, the junction temperatures will be much higher than ambient.

The fabricated IGBTs exhibit several problems, some of which may be associated with processing on the carbon face of the epilayers. As already mentioned, the contact resistivities for both n$^+$ and p$^+$ ohmic contacts are high and clearly limit performance. We believe that the high resistances are due to specific processing problems on these devices and are not inherent in fabrication on the carbon face. In addition, a small gate leakage current is observed in some devices. Separate measurements of the emitter, body, and collector currents indicate that when the gate is biased at 20 V and all other contacts grounded, about 90% of the gate leakage current passes through the oxide over the n$^+$ emitter region, 9.8% through the oxide over the n$^-$ JFET region, and about 0.2% through the oxide over the p$^+$ body region. Measurements at Vanderbilt University [11] indicate that thermal oxides on the carbon face of SiC have a lower breakdown field ($\sim$5.5 V/cm) than oxides on the silicon face ($\sim$10 MV/cm). The breakdown field may be even lower for oxides on implanted regions. To investigate this, we measured

oxides on MOS capacitors over the n$^+$ emitter implants, p-type body implants, and n$^-$ JFET regions on the same wafer as the IGBTs. The breakdown field of the oxide over n$^+$ regions is around 2.7 MV/cm (corresponding to a gate bias of 12 V), and over the p-type body and n$^-$ JFET regions, the breakdown field is slightly above 4 MV/cm. The reduced breakdown strength of oxides on the carbon face is an issue that needs to be addressed in future device work.

The n$^-$ drift layer has doping (2×10^{14} cm^{-3}) and thickness (180 μm) values designed to give a theoretical parallel-plane breakdown voltage of 25 kV. With proper edge terminations, it should be possible to achieve 80% of this value, or 20 kV, in actual devices. Since none of the test devices had edge terminations, we did not attempt to measure the blocking voltage on these devices.

IV. CONCLUSION

n-Channel double-diffused MOS IGBTs with 180-μm drift layers capable of blocking 20 kV have been designed and fabricated on the carbon face of 4H SiC free-standing epilayers. The devices show good conductivity modulation, and the collector current at 300 W/cm^2 is 27.3 A/cm^2. To our knowledge, this is the first detailed report of device fabrication on free-standing SiC epilayers.

ACKNOWLEDGMENT

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