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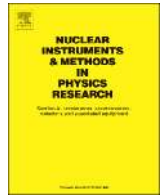
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High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments [☆]



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ABSTRACT

High-voltage particle detectors in commercial CMOS technologies are a detector family that allows implementation of low-cost, thin and radiation-tolerant detectors with a high time resolution. In the R/D phase of the development, a radiation tolerance of 10^{15} n_{eq}/cm², nearly 100% detection efficiency and a spatial resolution of about 3 μm were demonstrated. Since 2011 the HV detectors have first applications: the technology is presently the main option for the pixel detector of the planned Mu3e experiment at PSI (Switzerland). Several prototype sensors have been designed in a standard 180 nm HV CMOS process and successfully tested. Thanks to its high radiation tolerance, the HV detectors are also seen at CERN as a promising alternative to the standard options for ATLAS upgrade and CLIC. In order to test the concept, within ATLAS upgrade R/D, we are currently exploring an active pixel detector demonstrator HV2FE14; also implemented in the 180 nm HV process.

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1. Introduction: high-voltage pixel detectors—development in the early phase

High-voltage pixel detectors in commercial CMOS technologies are a detector family that allows implementation of low-cost, thin and radiation-tolerant detectors with a high time resolution. The unique property of these detectors is that the pixel electronics,

based on p- and n-channel transistors (CMOS-electronics), are embedded inside a single deep n-well that acts as a charge-collection electrode, as shown in Fig. 1. This n-well isolates the low-voltage devices from the p-type substrate. Since the pixel-transistors do not “see” the substrate potential, the substrate can be biased with a high negative voltage without damaging the transistors. In this way the depletion zone is formed in the space around the n-well. The n-well is acting as a potential minimum for electrons and the charge collection occurs by drift.

A pixel n-well plays two roles, it is the signal collection electrode and the substrate for the transistors. Since it forms a diode with embedded signal processing we refer to such a device as a “smart” diode and to the pixel array as a “smart diode array” (SDA).

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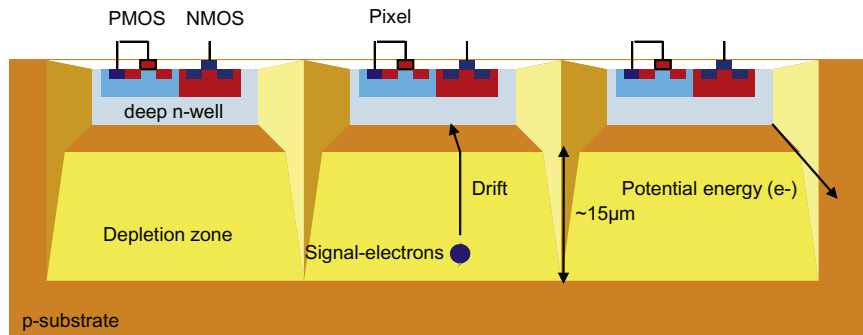


Fig. 1. Three high-voltage pixels. The pixel electronics of every pixel are enclosed by a deep n-well.

The high-voltage pixel detectors (or SDAs) can be implemented in any CMOS technology that has an n-well which encloses the low-voltage devices and a low enough substrate doping. Maximizing of the depleted region size improves the performances of the detector. A large depleted region leads to a decreased detector capacitance, decreased noise, and increased signal amplitude – hence the best results can be achieved in the high-voltage technologies since they use lowly doped substrates and n-wells.

The majority of the sensors, we have designed so far, were implemented in the AMS 350 nm HVCMOS-process. The typical reverse bias voltage in this technology is 60–100 V and the depleted region has a thickness of 15 μm . The substrate resistance is about 20 $\Omega\text{ cm}$.

The main advantages of SDAs are the use of standard technologies, which allows low-cost fabrication of large area sensors, a fast charge collection (we estimate ~ 200 ps) due to a high voltage across a small depletion region and a high radiation tolerance of at least 10^{15} $n_{\text{eq}}/\text{cm}^2$ for non-ionizing- and 60 MRad for ionizing effects [1]. Finally, since the charge collection occurs at the surface of the detector, we expect that thinning is possible without a significant charge loss. First measurements on thinned samples will be performed soon.

The detector development has been conducted in three main directions:

- (1) Simple integrating pixels with pulsed reset and rolling shutter readout (possible applications: International Linear Collider, transmission electron microscopy, etc.).
- (2) Pixels with complex CMOS-based pixel electronics (possible applications: LHC-experiments, etc.).
- (3) Capacitive coupled hybrid detectors based on a pixel sensor implemented as a smart diode array.

All these detectors have been implemented in the AMS 350 nm HVCMOS process. The results of the R/D project phase have been published in Refs. [1–6]. The capacitive coupled pixel detectors – CCPDs have been described in Refs. [7,8]. CCPDs are rather unusual detector structure. They are based on a pixel sensor implemented as an SDA. The pixel electronics contain a charge sensitive amplifier. The voltage output of the amplifier is connected to a transmitting electrode implemented in the last metal layer. A readout chip is flipped and glued onto the sensor so that the transmitting electrodes and the input pads of the readout channels form capacitors. In this way, the voltage signals can be transmitted from the sensor to the readout chip by means of AC coupling. Since there is no need for bump-bonding, the detector is cheaper and easier to produce than in the case of the standard, bump-bonded implementation. CCPDs are thus a large-volume, low-cost and thanks to possible thinning a low-mass alternative to the standard bump-bonded hybrid detectors.

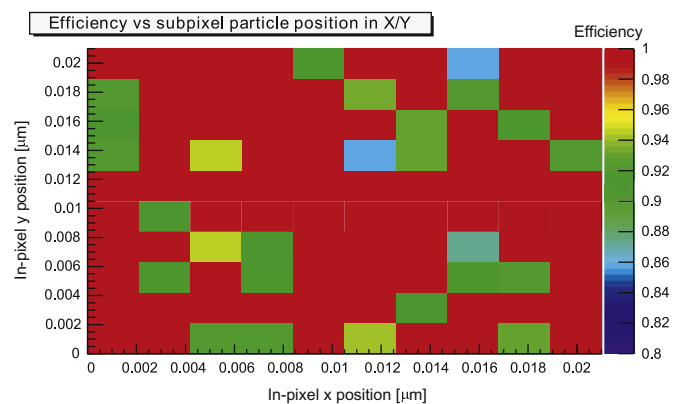


Fig. 2. Test-beam measurement. Efficiency vs. the in-pixel position of the fitted hit. No signs of a pixel-position dependent inefficiency were observed.

In order to test the detectors we have performed beam tests, irradiations, and used the test – injection circuits based on small capacitors for simple laboratory tests.

Figs. 2 and 3 show as an example the results obtained at the latest CERN SpS beam test using the Eudet telescope. The device under test (DUT) was a rolling shutter integrating detector with 21 μm –pixels. Detector efficiency has been measured by searching for the particle signals near the points where the tracks obtained by fitting of the telescope data intersect the DUT-plane. Missing DUT-signals count as inefficiency. Nearly 98%–detection efficiency has been measured, Fig. 2. The imperfect efficiency can be explained by the fact that during the rolling-shutter readout one pixel row (out of 64) is always inactive. Fig. 2 shows the efficiency as function of the in-pixel position of the fitted hit. No signs of a pixel-position dependent inefficiency were observed. A spatial resolution of almost 3 μm (after correction for the telescope resolution) has been measured, Fig. 3 (upper figure). The seed-pixel signal to noise ratio (SNR) is measured to be about 27, Fig. 3 (lower figure). The most probable cluster signal is 2000 e and the average pixel noise is 44 e.

Irradiations up to 10^{15} $n_{\text{eq}}/\text{cm}^2$ (protons), 10^{14} $n_{\text{eq}}/\text{cm}^2$ (neutrons) and 60 MRad (x-rays) have been performed with encouraging results. The irradiated sensors are still working with somewhat increased noise due to increased leakage currents. After irradiation with protons, a high signal to noise ratio has been measured for high energy beta-particles, even at nearly room temperatures (10 $^{\circ}\text{C}$). The irradiation results have been published in Ref. [1].

Several variants of CCPD detectors have been tested as well. Excellent signal to noise ratios of up to 60 have been measured using radioactive beta sources.

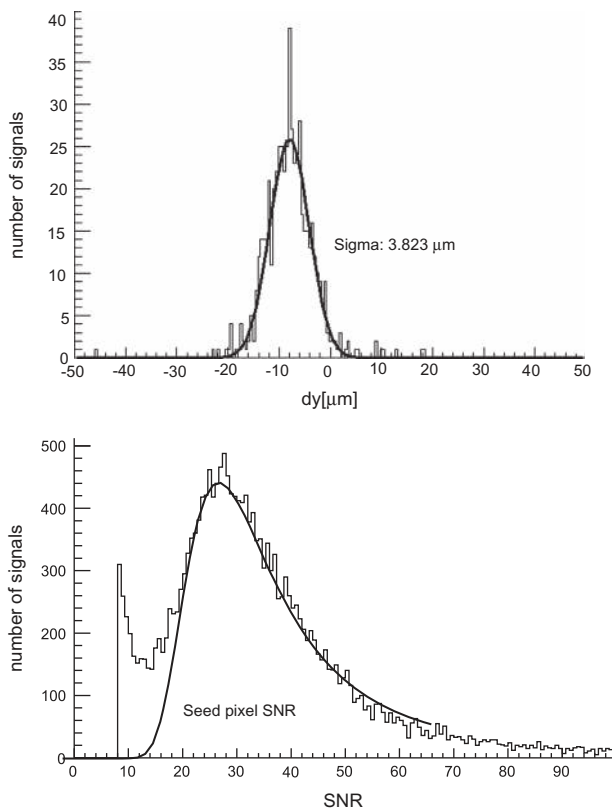


Fig. 3. Test-beam measurement. Upper figure: spatial resolution – the telescope resolution of $2.3 \mu\text{m}$ is not subtracted. Lower figure: seed pixel SNR.

2. Developments for the Mu3e and ATLAS experiments

The high-voltage CMOS sensors have first applications:

- (1) The Mu3e experiment at Paul Scherrer Institute (PSI) (Switzerland). For this application we have proposed a monolithic CMOS pixel detector that contains the high-voltage pixels with in-pixel charge sensitive amplifiers. We have designed three test chips in a 180 nm high-voltage technology.
- (2) SDAs are one of the technology options for the ATLAS and CLIC at CERN. For these applications, we are developing the smart sensors based on the high-voltage pixels that will be readout by the existing readout ASICs.

Common for both applications is the use of the simplified pixel electronics that do not contain the digital hit processing. The digital-processing tasks, like the hit signal buffering or the generation of time stamps, are dislocated from the pixel matrix. The pixel electronics are based on a charge-sensitive amplifier and optionally a comparator and a pixel-address generator. The amplifier output-pulse or the address-information are sent as analog signals to the digital processing block placed outside the pixel matrix. In the case of Mu3e detector, the digital block is placed on the sensor chip periphery. In the case of ATLAS/CLIC applications the pixel address is transmitted to a separated readout chip, like FE-I4, TimePix or a strip-readout chip.

3. Mu3e

The aim of the Mu3e experiment at PSI is the search for decay $\mu^+ \rightarrow e^+ e^- e^+$ [12]. This lepton flavor violating decay is unobservable in the Standard Model (SM), with a branching ratio (BR) of less than 10^{-50} . However, the decay can be enhanced to BR 10^{-12} in

certain models beyond the SM. The two main difficulties in the search for the decay are the low electron energy $< 53 \text{ MeV}$ leading to a large multiple scattering effect and a high background from muon decays that generate electrons, neutrinos and photons. The design challenges are:

- Muon-decay rates $> 10^9/\text{s}$.
- Hit rates $\sim 50 \text{ MHz}/\text{cm}^2$ (3 kHz/pixel).
- Momentum resolution $\leq 0.5 \text{ MeV}/c^2$.
- Vertex resolution $\sim 100 \mu\text{m}$.
- Low material budget $\sim 10^{-3} X_0$.
- Time resolution $< 1 \text{ ns}$. (to be achieved with scintillating fiber detectors).

To fulfil these requirements we are proposing the following pixel detector structure:

- Four layers with $80 \mu\text{m} \times 80 \mu\text{m}$ pixels.
- Time stamping with $< 100 \text{ ns}$ resolution is required to reduce the number of tracks in an image.
- Sensors should be thinned to $50 \mu\text{m}$ or less.
- Triggerless readout.
- Power consumption $\sim 200 \text{ mW}/\text{cm}^2$, cooling with helium gas.
- Total area: 1.9 m^2 , 275 million pixels.

High-voltage pixel detectors are a suitable choice for the Mu3e experiment. They can be produced thin, have relatively low production cost per unit area. The use of CMOS circuits makes the implementation of the continuously active pixels with a high time resolution relatively easy. Also, in contrast to the monolithic technologies based on diffusion that favor small pixels, SDA pixels can be relatively large, since the collection electrodes (n-wells) have a small capacitance per unit area.

The pixel detector will consist of high-voltage sensor-modules with two different geometries: $1 \text{ cm} \times 2 \text{ cm}$ and $2 \text{ cm} \times 2 \text{ cm}$. The modules will be thinned to $50 \mu\text{m}$ and glued onto a self supporting kapton structure carrying metal lines (see Fig. 4). The wire bonding will be done along the longer module edge through the holes in the kapton.

3.1. Sensor structure

As already mentioned in the introduction, the sensor pixels of the proposed module will contain only simple CMOS electronics based on a charge sensitive amplifier and a unity gain output buffer – source follower. Every pixel will have a direct connection to its digital processing unit (DPU) placed on the chip periphery. The connections will be implemented as metal lines in the third, fourth and fifth metal layer. The digital processing units contain the circuits for signal detection and time measurement, they perform comparison with threshold, store a time stamp when a hit is detected and send the data according to the defined priority.

To test the concept, we have designed three sensor prototypes in a 180 nm HV technology. Two of them (MuPixel1 and 2) have been tested. These chips have smaller pixel size and a simplified DPU structure. The latest prototype (MuPixel3) has a near to final pixel size and the full-featured DPU structure. This chip is still in production (November 2012).

Placing of DPUs on the chip periphery, outside of pixels, is not an “elegant” solution; it leads to a certain insensitive area and requires a lot of metal connections. However, this approach simplifies the pixel design, it allows us to make simpler in-pixel electronics that introduces a smaller detector capacitance. In this way signal to noise ratio and power consumption can be optimized. Further, the separation of the analog and the digital parts avoids crosstalk of the digital signals to the noise-susceptible

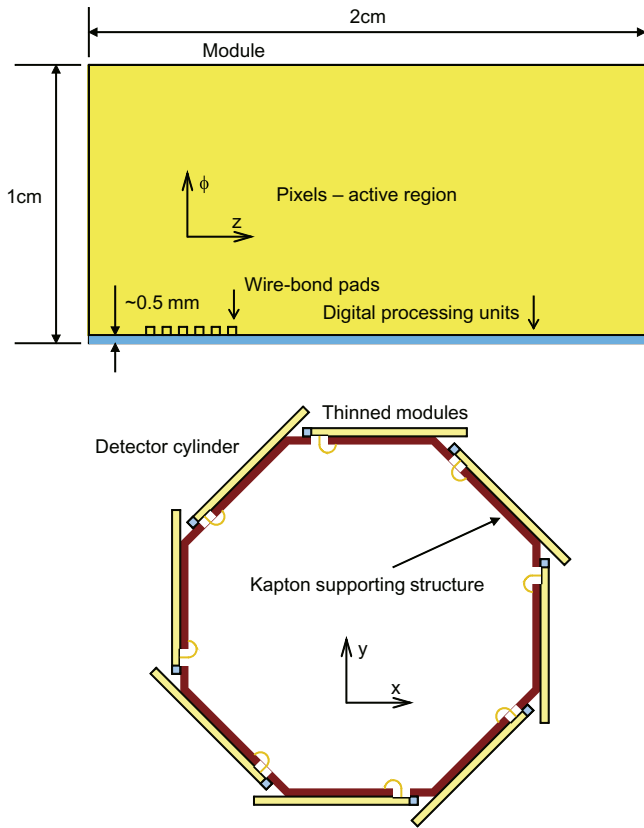


Fig. 4. Mu3e detector modules mounted on the self supporting kapton structure.

charge sensitive amplifiers. Fig. 5 shows the layout of the pixel (size $92\ \mu\text{m} \times 80\ \mu\text{m}$) and as comparison the layout of the DPU (size only $46\ \mu\text{m} \times 7\ \mu\text{m}$) as implemented in MuPixel3 chip. Although it contains more complicated circuits than the pixel itself, the DPU occupies 20 times smaller area. The periphery of the detector module will contain the DPUs (one for every pixel), relatively simple digital readout circuits and IO/power pads. Among all these circuits, DPUs will cover the largest space. Therefore we estimate that the periphery, which is not particle-sensitive, will cover only 5–10% of the total detector area. Three metal layers that are available for routing of the pixel signals have $0.7\ \mu\text{m}$ -pitch each, which enables the transfer of all required signals to the periphery.

The block schematics of the pixel electronics are shown in Fig. 6. The n-well is biased using a highly resistive element R, based on a PMOS. The connection between the n-well and the input of the charge sensitive amplifier A is established by capacitor C). The feedback capacitor Cf connects the output of the amplifier and the n-well. The signal detection is based on the following principle: the signal charge Q_s (electrons) are collected by the positively biased n-well. This leads to a small voltage drop in the n-well (equals $Q_s/C_{\text{nwell}} \sim Q_s/100\ \text{fF}$) that is detected by the amplifier. The charge Q_s is then “absorbed” by the feedback capacitance Cf and the amplified signal at the output of the amplifier equals $Q_s/C_f \sim Q_s/1\ \text{fF}$. The purpose of the DC feedback is to clear Cf after the signal amplification. Finally the original n-well voltage is restored by the bias element R. The power consumption of one pixel is about $7\ \mu\text{W}$.

Fig. 6 also shows the drawing of the “smart” n-well surrounded by the diffusion guard ring. In order to decrease detector capacitance and improve SNR we have designed the n-well significantly smaller than the pixel. This will lead to un-depleted zones between the pixels. The charge generated in these regions will be (partially) collected by diffusion. P+ diffusion guard rings

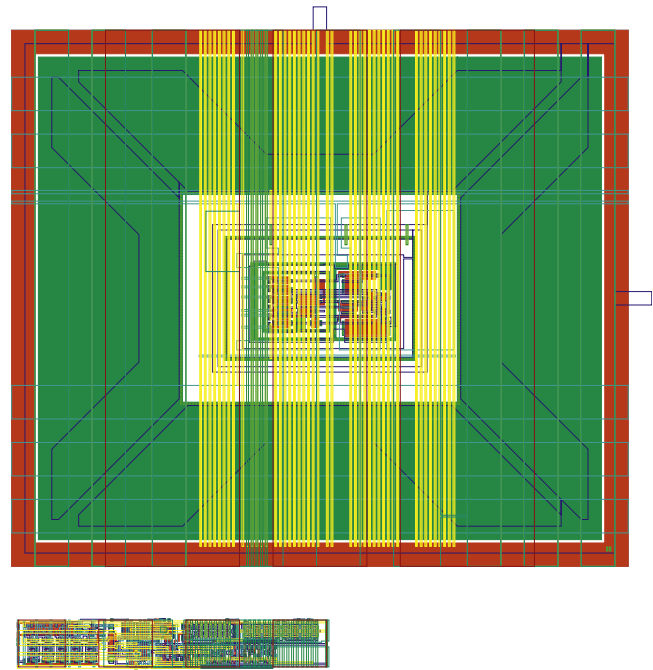


Fig. 5. Layout of the pixel (upper figure) and the DPU (lower figure) as implemented in MuPixel3 chip.

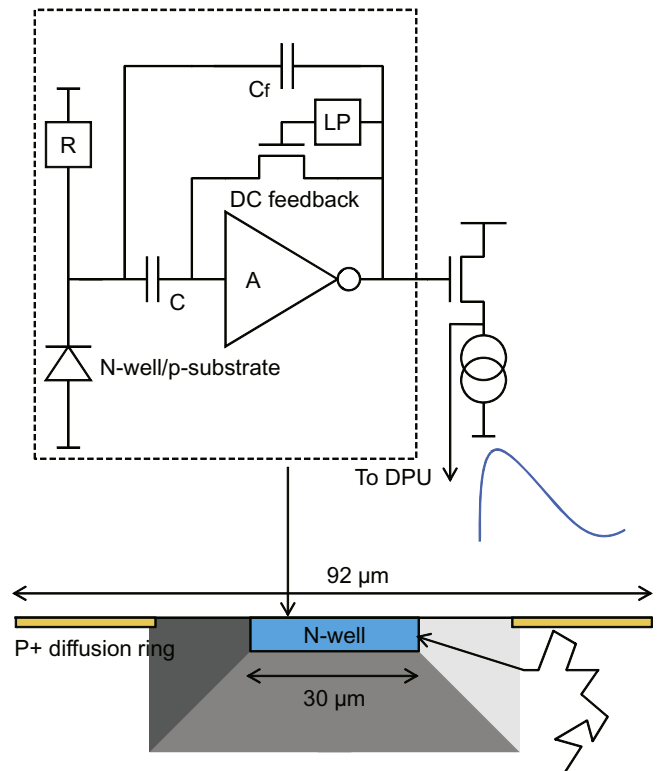


Fig. 6. Block schematics of the pixel electronics as implemented in MuPixel3 chip.

should prevent the recombination of the signal electrons at the bulk-field-oxide interface. We will investigate the possible signal losses and increase the size of the n-well in the final design.

3.2. Experimental results

The prototype chips MuPixel1 and 2 have been successfully tested with radioactive sources, using infra-red laser and LEDs, and

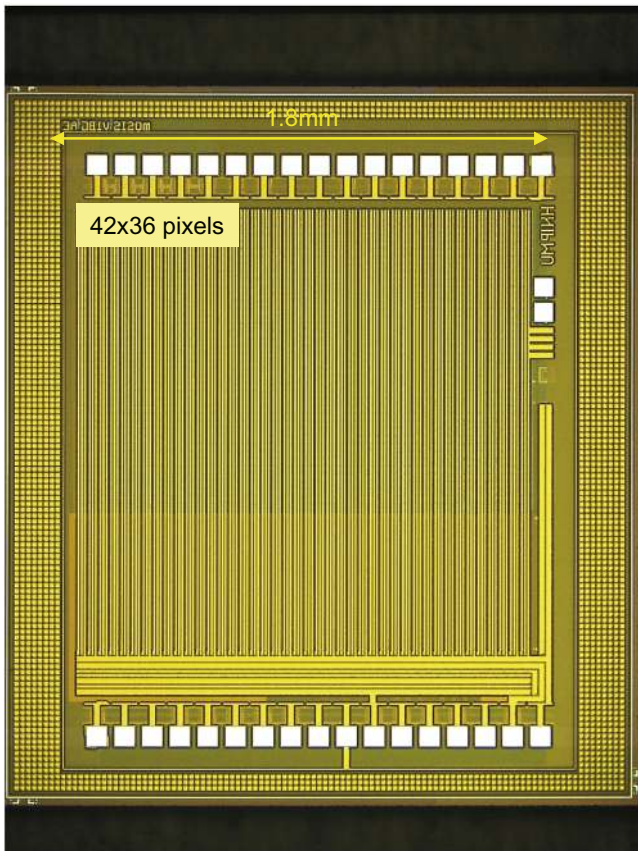


Fig. 7. Photo-micrograph of the MuPixel2 chip.

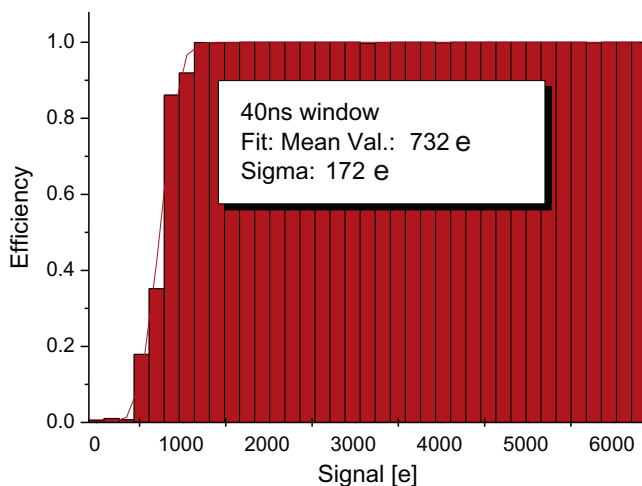


Fig. 8. MuPixel2 chip: in-time 40 ns detection efficiency of the whole pixel matrix vs. input signal amplitude.

by means of electrical test signals. Test beam measurements have been performed as well. Figs. 7 and 8 show the photo-micrograph of the MuPixel2 chip and a measurement result respectively. The detection efficiency of the whole pixel matrix has been measured applying the test injection pulses of variable amplitude. The window-logic has been adjusted to accept only the discriminator pulses that are coincident in time (within 40 ns) with the test pulses. Detection of signals above 1230 e with 40 ns time resolution is possible. We expect signals of about ~ 1800 e from minimum ionizing particles.

Preliminary infra-red laser measurements indicate that the charge collection time is shorter than 10 ns [6].

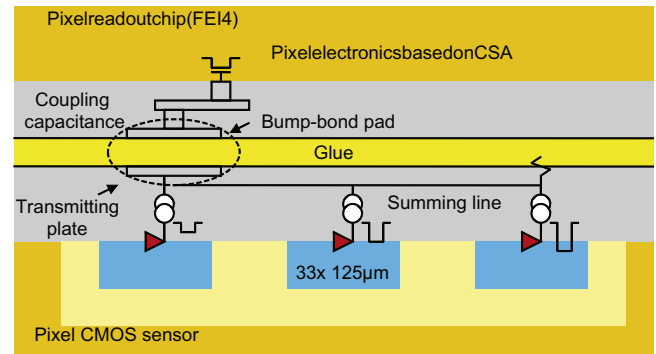


Fig. 9. CCPD readout concept for ATLAS: HV2FEI4 readout by the FE-I4 chip.

4. High-voltage pixel detectors for ATLAS and CLIC

To be able to fully exploit the advantages that SDA detectors offer while being able to use the existing readout ICs that enable complex pixel signal processing, we are proposing the use of “smart” sensors implemented in HV CMOS technologies instead of the classical diode-based detectors. The pixel electronics of a smart-sensor element are based on a charge-sensitive amplifier (similar to that of the MuPixel3 chip) and a comparator followed by a pixel-address generator. The address-information is sent as an analog signal to the readout chip. This can be for instance the FE-I4 chip in the case of ATLAS [9–11] or TimePix in the case of CLIC applications. The use of smart sensors for ATLAS and CLIC opens new possibilities. For instance, a capacitive coupling can be used for the signal transmission instead of bump-bonding. This can save material and costs. Another possibility is to increase the spatial resolution by coupling of many sensor pixels to a single readout channel.

In order to test the concept we are currently investigating a pixel detector demonstrator HV2FEI4 implemented in a 180 nm high-voltage CMOS process. This detector has a pixel pitch of $33 \mu\text{m} \times 125 \mu\text{m}$. A group of three detector pixels is coupled to one FE-I4 pixel readout channel. The contacts between the detector and the readout chip can be established either capacitively or by the classical bump-bonding. A strip-like readout is also possible, where a larger array of pixels is connected to one readout channel of a strip readout chip. Finally, the pixel signals can be measured in stand-alone mode using a test multiplexer.

The HV2FEI4 chip is described in detail in Ref. [6] and here briefly. The pixel electronics respond to a particle hit by generating a current pulse with a defined amplitude. The signals of three pixels are summed, converted to voltage and transmitted to the charge sensitive amplifier in the corresponding channel of the front-end chip using AC coupling. The AC coupling occurs between the transmitting plate on HV2FEI4 and the bump-bond pad on FE-I4. The FE-I4 and HVCMOS sensor are glued onto each other without bump bonding. Each of the pixels that couples to one front-end receiver has a unique signal amplitude, such that the pixel can be identified by examining the amplitude information generated in the front-end chip. The readout concept has been illustrated in Fig. 9.

4.1. Experimental results

We have tested HV2FEI4 chips in stand-alone operation and as an CCPD. Additionally, we have irradiated several chips (stand-alone readout) at the PS irradiation beam at CERN.

The purpose of the tests was to estimate the signal and noise, demonstrate the capacitive signal transmission, investigate the radiation hardness and show the increased spatial resolution by

decoding the analog pixel address from the time over threshold information of the FE-I4 chip.

The preliminary noise measurements have been done, in the test beam area, by sweeping in amplitude the test signal and measuring the discriminator response probability. We measure an equivalent noise charge (ENC) of about 110 e. We expect a MIP signal of about 1800 e. The noise is by factor two higher than simulated and this is probably the result of the non-ideal setup.

The CCPD module works. We were able to measure response to ionizing particles and perform the test injection measurements to estimate the coupling capacitance between HV2FEI4 and FE-I4 electrodes and to determine ENC. In order to measure the coupling capacitance, one of the transmitting plates is connected to the externally generated test pulse. The coupling capacitance is 0.82 fF which is relatively small, however high enough for the signal transmission. The measured ENC was about 170 e. There is no principal reason for the noise in CCPD-operation to be different than the noise in the stand-alone operation and we hope to improve this value with a better setup. The irradiation at PS (CERN) is still ongoing. We have irradiated the first set of chips to 435 Mrad. The measurement setup allows remote operation of the device under test and monitoring of the output signal of one pixel amplifier. Counting rate of a test pixel (placed at the edge of the matrix) has been measured during the irradiation. Preliminary results show that the particle-counting rate decreases by factor of two to three (depending of bias settings) from low doses to 350 Mrad. Beyond 350 Mrad the decrease of counting rate is steeper. The counting rate decrease can be assigned to the bulk damage. Such kind of damage reduces the amount of the charge collected by diffusion. The charge-signals that originate from distant particle hits are not collected. We also observe the increase of the detector leakage current and the noise. The high noise can also influence the counting rate, since it prevents the operation of the detector under the optimal threshold setting. Additional studies of radiation hardness are planned.

5. Conclusions

High-voltage pixel detectors in commercial CMOS technologies are a detector family that allows implementation of low-cost, thin and radiation-tolerant detectors with a high time resolution. In the initial phase of the development a high signal to noise ratio, nearly perfect detection efficiency and a radiation tolerance

of $10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ have been shown. The high-voltage detectors have the first application at the Mu3e experiment at PSI. The HV CMOS detectors are also seen as an option for ATLAS-upgrade and CLIC. For Mu3e we are proposing a monolithic pixel detector with continuous readout. Three prototype sensors have been designed in a standard 180 nm HV CMOS process. Experimental results are encouraging. The latest prototype has a structure very close to the final one, and after the tests are accomplished we will design a large scale detector within a wafer production run. The proposed detector structure for ATLAS and CLIC is a smart sensor based on HV-CMOS technology that is readout with an external pixel- or strip-readout chip. The advantages with respect to the existing detectors are: no need for bump-bond connection between the sensor and readout chip (capacitive coupling can be used); better mechanical stability and less material; the use of commercial technologies with low production cost per 8-in. wafer; increased spatial resolution with the existing front-end chip and the possibility of sensor-thinning without signal loss. We have designed a small prototype HV2FEI4 to test the concept. First results show that the detector works as a capacitively coupled pixel sensor and has a high radiation tolerance.

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