5-2016

High Voltage Point of Load Converter for Data Center Power Supplies

Yutian Cui
University of Tennessee - Knoxville, ycui7@vols.utk.edu

To the Graduate Council:

I am submitting herewith a dissertation written by Yutian Cui entitled "High Voltage Point of Load Converter for Data Center Power Supplies." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

Leon M. Tolbert, Major Professor

We have read this dissertation and recommend its acceptance:

Fred Wang, Daniel J. Costinett, Andrew W. Wereszczak

Accepted for the Council:

Carolyn R. Hodges

Vice Provost and Dean of the Graduate School

(Original signatures are on file with official student records.)

High Voltage Point of Load Converter for

Data Center Power Supplies

A Dissertation Presented for the

Doctor of Philosophy

Degree

The University of Tennessee

Yutian Cui

May 2016

ACKNOWLEDGEMENT

First of all, I would like to take this opportunity to express my sincere gratitude and respect to my advisor, Dr. Leon M. Tolbert. He guided me into this research area and taught me how to do research with his broad vision, profound knowledge, and great patience. I feel blessed to have such a great advisor in my Ph.D studies, without his support, this dissertation would never been possible.

I would like to extend my gratitude to Dr. Fred Wang and Dr. Daniel J. Costinett, for their help and suggestions during the meetings as well as the discussion and feedback on this dissertation.

I would like to thank Dr. Andrew A. Wereszczak for serving on my committee and offering me great suggestions on my dissertation.

I would like to thank all the colleagues in the power electronics lab in the University of Tennessee, Knoxville. They are Dr. Shengnan Li, Dr. Bailu Xiao, Dr. Dong Jiang, Dr. Lijun Hang, Dr. Jingxin Wang, Dr. Wanjun Lei, Dr. Faete Filho, Dr. Mithat Can Kisacikoglu, Dr. Lakshmi Reddy Gopi Reddy, Dr. Zhuxian Xu, Dr. Fan Xu, Dr. Ben Guo, Dr. Zheyu Zhang, Dr. Jing Xue, Dr. Zhiqiang Wang, Dr. Jing Wang, Dr. Xiaojie Shi, Dr. Liu Yang, Dr. Weimin Zhang, Dr. Sheng Zheng, Mr. Bradford Trento, Mr. Yalong Li, Mr. Wenchao Cao, Mr. Yiwei Ma, Ms. Yang Xue, Mr. Bo Liu, Mr. Saeed Anwar, Mr. Edward Jones, Mr. Siyao Jiang, Mr. Yiqi Liu, Mr. Tong Wu, Mr. Shuoting Zhang, Mr. Chongwen Zhao, Ms. Ling Jiang, and Mr. Ren Ren. Special thanks to Mr. Fei Yang, for his encouragement during my darkest days.

Last but not least, I would like to thank my parents for their unconditional love and support. Without them, this work would never been possible.

ABSTRACT

With the increased cloud computing and digital information storage, the energy requirement of data centers where a large number of computer systems are housed keeps increasing. However, most of the data centers today are operated inefficiently, both economically and environmentally. Efforts including improving power delivery architecture, power conversion efficiency and thermal management have been made to increase the power delivery efficiency from grid to point of load.

In this dissertation, a new power delivery architecture, high voltage point of load (HV POL) architecture, has been proposed in order to improve power conversion and distribution efficiency for data center power supplies.

First, the conversion structure has been selected as input series and output parallel (ISOP) to fulfill the high ratio (400:1) conversion and mitigate the step down stress of a single converter. Also, with multiple output phases, interleaving control technique can be applied to increase equivalent switching frequency and allows smaller output inductor.

Then, two different types of converter topologies have been chosen for evaluation in the ISOP structure: phase shift full bridge (PSFB) and half bridge current doubler. High efficiency driven converter design and control method have been performed on both topologies. In PSFB, the impact of primary side MOSFETs' output junction capacitances on the converter's efficiency has been studied. For half bridge current doubler, a novel control method enabling soft switching over the entire load range with auxiliary circuit is proposed and verified in experiments.

A six phase ISOP connected half bridge current doubler converter was built and tested to realize the single stage 400 V to 1 V conversion. Adaptive voltage positioning (AVP) control is analyzed and performed on the ISOP system to meet the on-board power supply requirement. Also, the impact of mismatches in the ISOP connected modules are calculated and simulated for both static and dynamic performance, and it is shown that the ISOP system is relatively immune to circuit's mismatches. Therefore, the concept of using the single stage ISOP connected converter has been shown to be feasible as a high efficiency on-board power supply with good transient performance.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

1.1. Challenge of power supplies in data centers

The number and performance of microprocessors keeps increasing in computer systems, which require more transistors to be integrated in the microprocessors. The increase of transistors is expected to follow Moore's law [1], which predicted that the number of components used in the integrated circuit will be doubled every two years. Figure 1.1 shows the number of transistors used in Intel's microprocessors [1], indicating the rapid growth of transistor number.

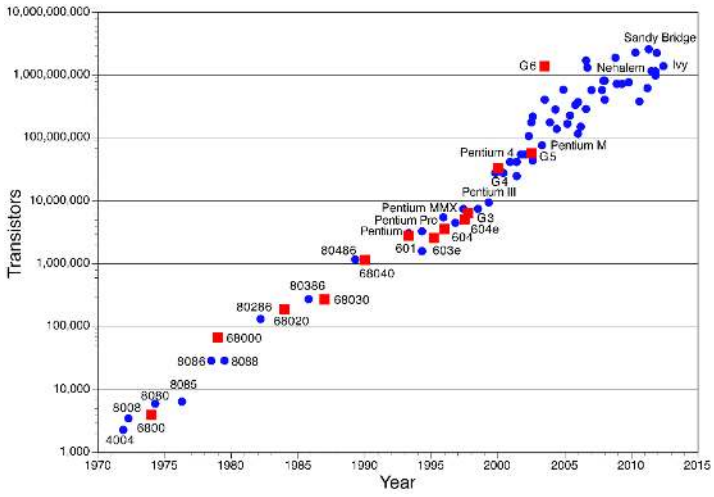


Figure 1.1. Number of transistors on Intel's microprocessors [1].

The fast increasing number of components in microprocessors challenges power supplies used in them. The power requirement is roughly proportional to the clock's frequency (f), the total lumped capacitances of the transistors (C), and the square of the core voltage (V_{cc}) [2][3], as indicated in (1-1), where AV is the activity factor [4] which indicates the actual frequency with respect to the clock's frequency.

$$P_{CPU} = AV \cdot f \cdot C \cdot V_{CC}^2 \tag{1-1}$$

The clock frequency keeps increasing in order to get a higher operation frequency. The total lumped capacitance is also growing larger with increased component number. Therefore, the power required by the central processing unit (CPU) keeps increasing. All the power consumed by the CPU eventually turns into heat, which challenges the thermal management of the CPU as well.

Several methods have been proposed to reduce power consumption by the CPU. One way is to reduce the core voltage $V_{cc.}$ As indicated in (1-1), the power consumption reduces greatly with reduced $V_{cc.}$ Figure 1.2 shows the core voltage and corresponding current, which clearly indicates that the core voltage is reducing over time [5][6]. However, with reduced core voltage, the current demand is increasing dramatically. With increased current and reduced voltage, it makes the voltage conversion ratio keeps increasing from the grid to the CPU, which further challenges the power supply used in data center.

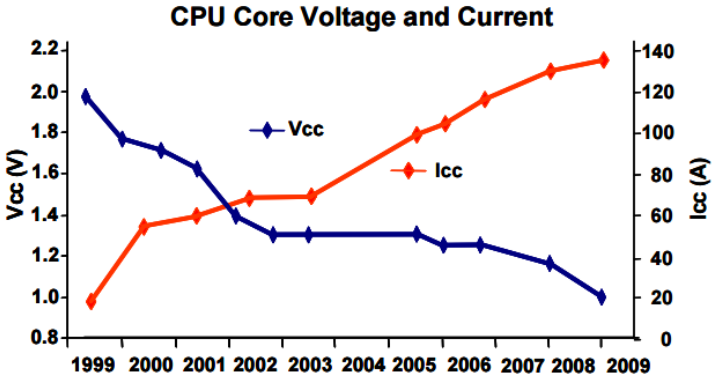


Figure 1.2. Roadmap of Intel microprocessors [5].

1.2. High efficiency power supplies

Based on earlier discussion, the energy used in data centers and processed by power supplies keeps increasing. Figure 1.3 shows the power used for data centers from 2010 to 2020

[7]. Based on the data, over 350 billion kW hours of electricity has been used for data centers in the year 2014.

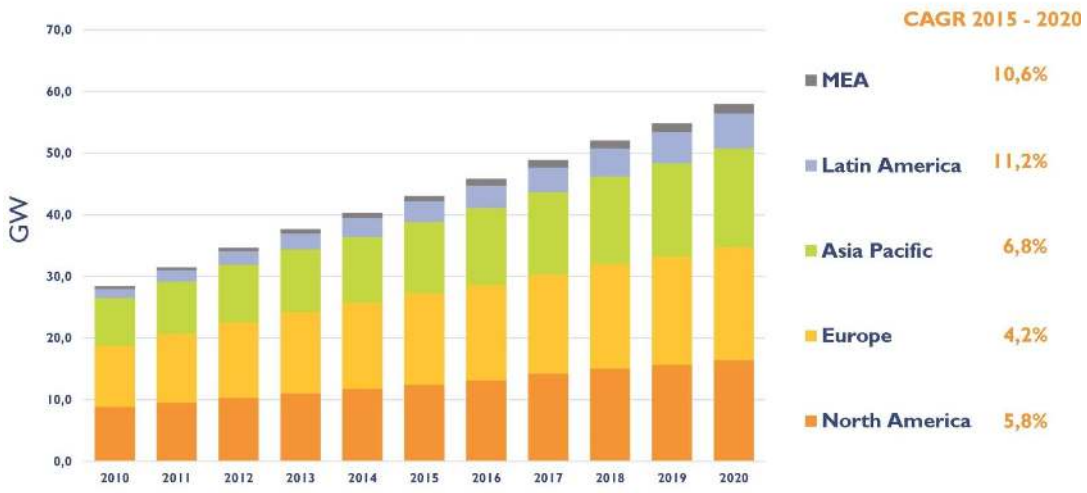


Figure 1.3. Data center installed based and spending [7].

In the meantime, most of power supplies used in data centers are operated inefficiently at this time. Combining the large electricity usage in the data centers, considerable amount of energy is lost during the power conversion and distribution process from grid voltage to the point of load. Figure 1.4 is the path of power flow in data centers [8][9]. Out of 405 W input power, 200 W is provided to the cooling system, and 205 W is processed by the power supplies. Only 100 W is usable to the microprocessors from 205 W at the beginning of the power supply chain, with the remainder lost during the power delivery process, such as with power supply unit (PSU), voltage regulator (VR), and also the fans and cooling system. The overall power delivery efficiency is roughly 50 % [9]. Combining the with 350 billion kW hours used in the year 2014 and assuming 40 % of the power is used for the cooling system in the data center (which is within the range defined in Figure 1.4), around 100 billion kW hours are lost in the power supplies.

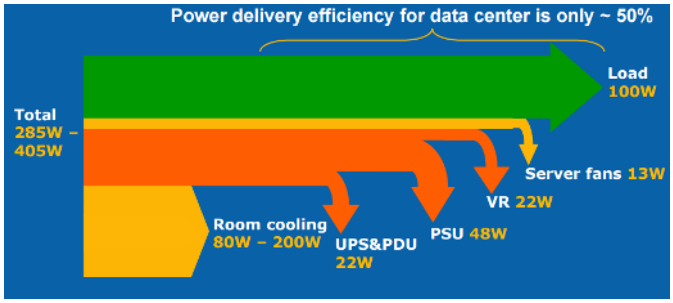


Figure 1.4. Power delivery for data centers [9].

Because of the low power delivery efficiency and large amount of electricity usage, with a 10% point loss reduction of power supplies, the electricity bill savings can be as much as $480 million per year, and the CO_2 production can be reduced as well. In the meantime, the power supplies losses reduce, the cooling requirement also decrease which would further reduce the energy used in the cooling system and reduce the energy usage for the data centers.

1.3. Motivation and strategy

Efficiency requirements for data center power supplies have been proposed by different information technology (IT) companies, such as Google [11], IBM [12], and Intel [13], with targeted efficiency above 85 %. Great efforts have been made to improve the efficiency of power supplies and reach the target, from different aspects.

1.3.1. Innovation of power supplies architecture

Figure 1.5 shows the conventional AC architecture, including a two-stage uninterruptable power supply (UPS) and a power delivery unit (PDU) which provides 208 V AC voltage to the rack. Inside the rack, another two-stage conversion in power supply unit (PSU) converts the 208 V AC to 12 V DC and feeds voltage regulators (VR) which further steps down the 12 V into 5 V, 3.3 V or 1 V depending on the load condition [8]. It is clear that the conventional AC architecture contains redundant power conversion stages, which leads to a low overall

efficiency. Therefore, removing unnecessary power conversion stages is one method to improve the system efficiency.

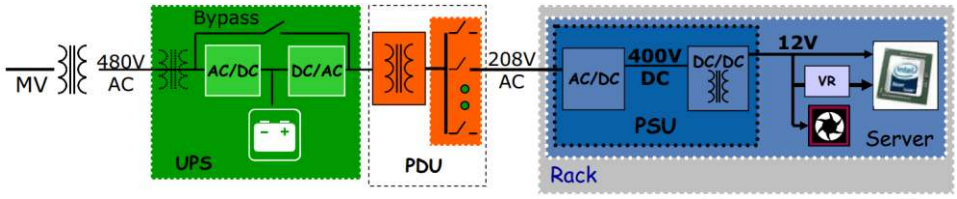


Figure 1.5. Conventional 208 V AC power delivery architecture [8].

Facility voltage DC architecture (shown in Figure 1.6) is proposed for better efficiency as the DC/AC conversion stage is removed from the UPS and the AC/DC stage is removed from the PSU. At first, 48 V DC distribution voltage was used. However, as discussed earlier, the current demand is large and keeps increasing, with 48 V distribution voltage, the distribution current limits the power rating for large data centers [8]. In order to increase power capability, a higher distribution voltage is used in data center. At this time, 350 V - 400 V distribution voltage is used for the high voltage DC (HVDC) architecture [8].

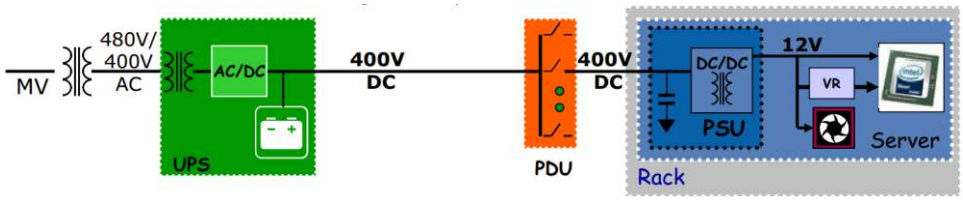


Figure 1.6. High voltage DC power deliver architecture [8].

1.3.2. Improved power converter efficiency

Besides implementation of less power conversion stages architecture, another method to improve system efficiency is to use high efficiency power converters within HVDC architectures.

(1) AC/DC stage in UPS

Different topologies can be used as the three phase rectifier, such as voltage source rectifier, Z-source rectifier [14], current source rectifier [15][16], and Delta rectifier [17]. Wide band gap (WBG) devices are also implemented to further improve the efficiency [15][16]. Commercial product efficiency of front end rectifier is 97 % [18]. University prototypes can reach higher efficiency, up to 99 % [15][16].

(2) DC/DC stage in PSU

Isolated DC/DC converter is used in PSU inside the rack. Mostly, resonant LLC converter [19], or pulse-width modulated converter [20] can be used as the DC/DC converter. The efficiency is up to 95 % with commercial products [21] and up to 96.5 % with research prototypes [22].

(3) Voltage regulator

Synchronous buck converter is usually used as the voltage regulator (VR). Because of transient requirement, multi-phase buck converter with interleaved gate signal is used. Commercial product's efficiency is around 88 % at 15 A output current and 600 kHz switching frequency [23] and around 86.5 % at 15 A output current and 1 MHz switching frequency [24].

As the efficiency of each stage in the HVDC architecture was discussed, it clearly shows that most of the loss during power delivery is within the PSU and VR. Therefore, in this proposal, rack level delivery from 400 V_{DC} to 1 V_{DC} is being studied.

1.4. Dissertation outline

According to the discussed strategy discussed above, the outline of this proposal is as follows:

Chapter 2 is the literature review of current power delivery architecture and converter topologies used within data center architectures. Also, device selection criteria, soft switching and input series and output paralleled converter control techniques are discussed.

Chapter 3 further studies the widely used intermediate bus architecture (IBA) with different bus voltage. Also, a high voltage point of load (HV POL) has been proposed, and a comparison between the proposed HV POL and IBA has been made.

Chapter 4 provides the design of a phase shift full bridge converter which is used in HV POL targeting high efficiency. The impact of the primary side MOSFETs' output junction capacitance on the converter's operation and efficiency has been studied thoroughly.

Chapter 5 discusses a half bridge current doubler circuit which is another converter topology used in HV POL. A load dependent soft switching technique has been proposed with auxiliary components that can achieve zero voltage switching (ZVS) for the entire load range.

Chapter 6 provides the implement of the proposed method to achieve the adaptive voltage positioning (AVP) which is a common requirement for on-board power supplies. The impact of mismatches among modules in the ISOP is simulated as well.

Chapter 7 summarizes the work that has been done in this dissertation and the significance of the work. Possible future work is also described.

2. Literature Review

This chapter provides a literature review of different methods to improve the power conversion and distribution efficiency in data centers from different aspects. First, different power supply architectures are summarized. Then, different methods for efficiency improvement of the pulse width modulated (PWM) DC/DC converter which can be used in the power supplies are discussed, including device selection and soft switching method. At last, the control methods to ensure stable operation of an input series output parallel (ISOP) connected system are summarized.

2.1 Data center power supply architecture

2.1.1 Intermediate bus architecture

Intermediate bus architecture (IBA) [8] is a widely used architecture at this time as shown in Figure 2.1 where 1.x V is between 1.0 V and 1.9 V based on load requirement. IBA includes two power conversion stages: intermediate bus converter (IBC) and a point of load (POL) converter. IBC is usually a resonant converter and performs as a DC voltage transformer (DCX) without regulation (Figure 2.2) [25][26][27]. POL is usually a multiphase synchronous buck converter which further steps down the bus voltage from unregulated 12 V to the required voltage with regulation (Figure 2.3) [28][29]. Interleaving control is applied to the multiphase buck converter with several advantages: 1) reduces both input and output current ripple; 2) faster transient response because a smaller inductor can be used; and 3) distribute power and heat evenly [6]. The conversion efficiency of the power supply chain from 400 V to 1 V is 83.1 % based on Vicor's products [21] at room temperature and under full load condition.

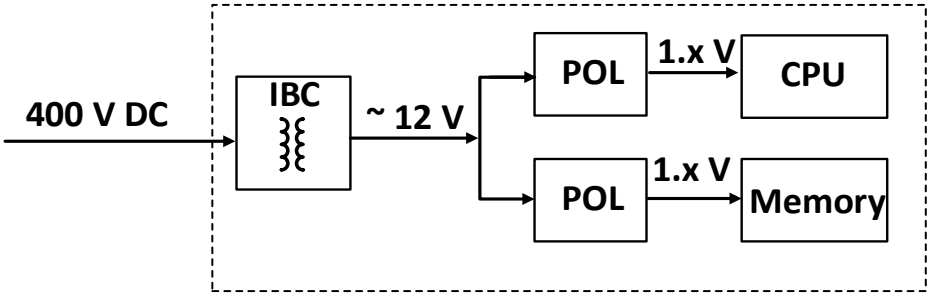


Figure 2.1. Intermediate bus architecture for data center power supplies.

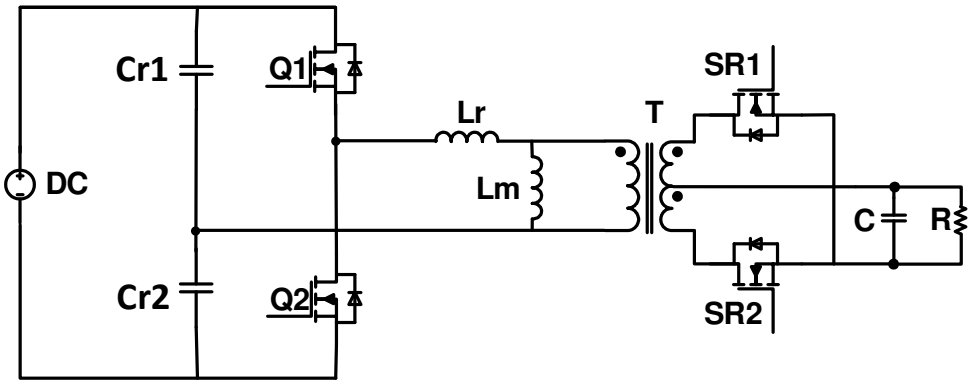


Figure 2.2. LLC resonant converter as IBC.

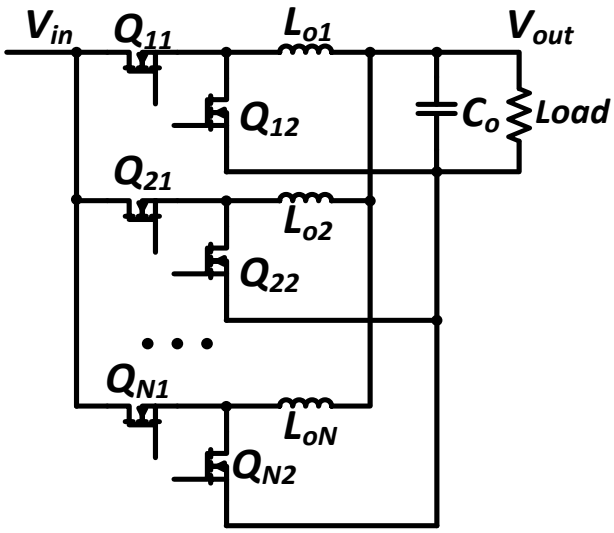


Figure 2.3. Synchronous buck converter as POL.

Some alternative converter topologies have been proposed to improve the efficiency in the POL stage and are discussed in the following section.

(1) Two-stage POL

To improve the efficiency of POL with 12 V input voltage, a two-stage POL is proposed as shown in Figure 2.4 [4][6][30]. The first stage steps down the 12 V bus voltage from IBC to a lower bus voltage, where a synchronous buck converter is implemented (shown in Figure 2.5). The second stage further steps down the 5 V bus voltage to the required voltage. For this stage, a multiphase buck converter, similar to conventional POL with lower voltage rating devices, can be implemented. Also, a switch capacitor converter, shown in Figure 2.6 is also proposed as the second stage in the two stage architecture [6]. To improve light load efficiency, the bus voltage between first and second stage is varied based on load condition. When load is light, the bus voltage is also low (3 V), and as the load increases, the bus voltage is between 3 V to 6 V.

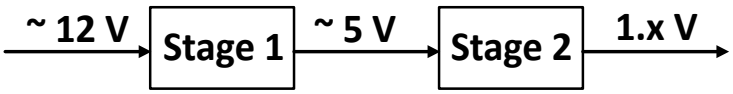


Figure 2.4. Two stage buck architecture.

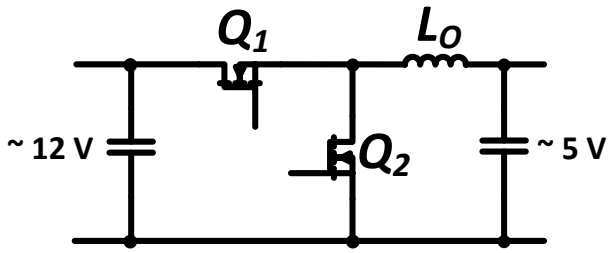


Figure 2.5. Buck converter as first stage in two stage POL in Figure 2.4.

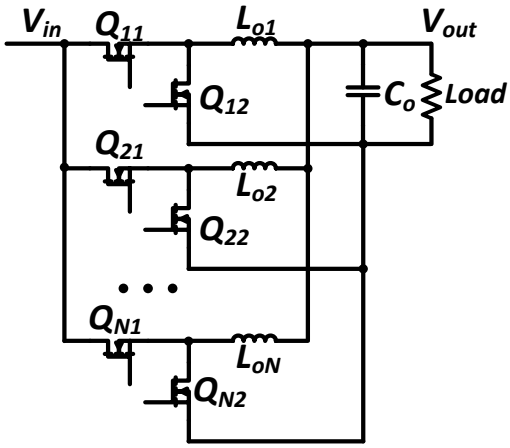


Figure 2.6. Multi-phase buck as second stage in two stage POL in Figure 2.4.

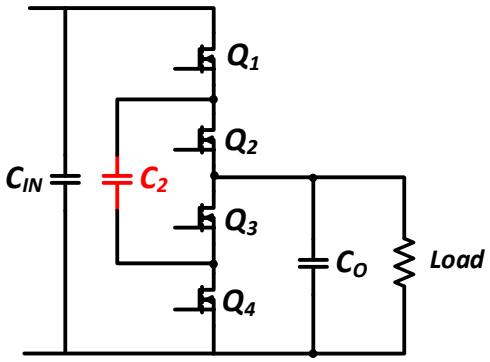


Figure 2.7. Switch capacitor as second stage in two stage POL in Figure 2.4.

(2) Sigma connected POL converter

Another alternative architecture within IBA of POL is sigma connected POL as shown in Figure 2.8 [6]. Instead of parallel connected multiphase phase buck converter, Sigma architecture is implemented with one resonant converter (DCX) and a buck converter with input series connection. DCX handles power transfer while buck converter fulfills voltage regulation of the POL. Also sigma architecture allows lower voltage rating devices for both DCX and buck converter because the series input connection.

The efficiency of Sigma architecture can be calculated as (2-1).

$$\eta_{Sigma} = \frac{P_{DCX}}{P_{Sigma}}\eta_{DCX} + \frac{P_{buck}}{P_{Sigma}}\eta_{buck} \tag{2-1}$$

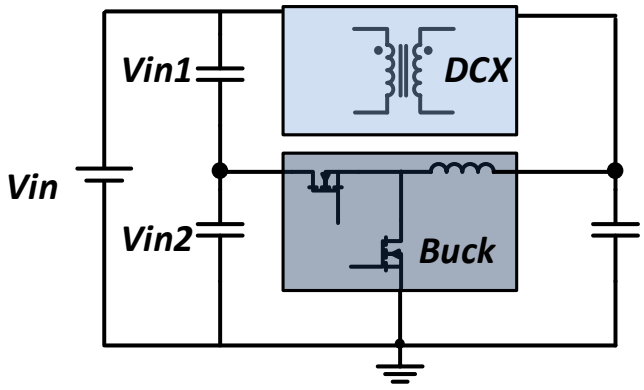


Figure 2.8. Sigma connected POL converter.

2.1.2 Factorized power architecture

Vicor proposed factorized power architecture (PFA) composed with bus converter module (BCM), pre-regulated module (PRM) and voltage transformation module (VTM) as shown in Figure 2.9 [21]. PRM is buck-boost type converter which can be soft switched over the entire operational range. VTM performs as the DC voltage transformer and requires no regulation capability. Since the VTM has no regulation capability, therefore, the transient performance dependents on PRM and is more complex than IBA. The power conversion efficiency of FPA from 400 V to 1 V based on Vicor's website is 81.7 % [21] at room temperature and under full load condition. However, the distribution losses of both IBA and FPA are not included in the efficiency calculation. In FPA, a higher voltage (48 V) is used for the on board distribution voltage compared with IBA (12 V); therefore, the distribution loss in FPA is 16 times smaller compared with IBA for the same dimension board and delivering the same amount of power.

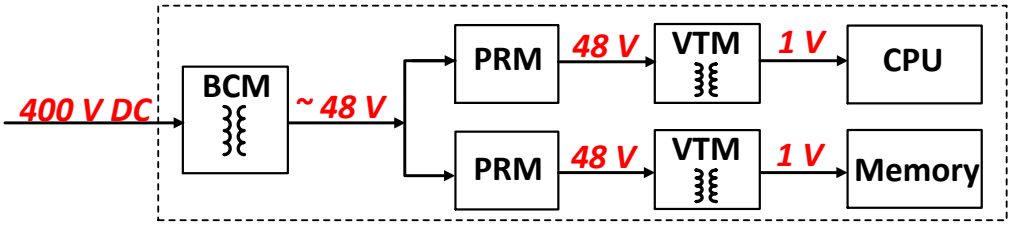


Figure 2.9. FPA architecture.

2.2 High efficiency PWM DC/DC converter

Losses in the PWM DC/DC converter include: active devices losses and passive components losses. Methods to achieve the low active device losses are reviewed in this section. First, device selection criteria have been reviewed. Next, to reduce switching loss, soft switching method can be implemented. Different soft switching methods are reviewed here.

2.2.1. Device selection

(1) Hard switching figure of merit (FOM)

Semiconductor losses in converter include three parts: conduction loss (P_{cond}), switching loss (P_{sw}), and gate driving loss (P_{gate}), all of which can be expressed as the following equations.

$$P_{cond} = R_{ds(on)} I_{rms}^2 \tag{2-2}$$

$$P_{sw} = \frac{1}{2} I_{don} V_{ds} (t_{ir} + t_{vf}) f_s + \frac{1}{2} I_{doff} V_{ds} (t_{if} + t_{vr}) f_s \tag{2-3}$$

$$P_{gate} = V_{gate} Q_g f_s \tag{2-4}$$

where $R_{ds(on)}$ is the on-state resistance of MOSFET, I_{rms} is the root mean-square (RMS) current in MOSFET, I_{don} and I_{doff} are the current value at turn on and turn off transient, V_{ds} is the voltage when MOSFET is off, t_{ir} and t_{vf} are current rising and voltage falling during turn on transient, t_{if} and t_{vr} are current falling and voltage rising during turn on transient, V_{gate} is the turn on gate voltage, Q_g is the gate charge of the MOSFET, and f_s is the switching frequency of the MOSFETs.

Turn on transient without considering parasitics in devices and the circuit is plotted in Figure 2.10 [31][32]. Based on [31], the charging and discharging time of the gate to drain capacitance (C_{gd} in Figure 2.11) is the dominant switching loss during each switching period, which means $t_{ir} \ll t_{vf}$ during turn on and $t_{if} \ll t_{vr}$ during turn off. Therefore, the switching loss of a power device can be simplified into (2-5).

$$P_{loss} \cong R_{ds(on)} I_{rms}^2 + I_d V_{ds} t_v f = \frac{R_{ds,sp} I_{rms}^2}{A} + \frac{I_d V_{ds} f Q_{dg,sp} A}{i_{g,avg}} \tag{2-5}$$

where $R_{ds,sp}$ and $Q_{dg,sp}$ are specific on-state resistance and specific gate to drain charge, t_v is the sum of voltage rise time and voltage fall time in turn off and turn on transient, and A is the effective area of MOSFET.

Based on [31], in order to get minimum loss, $\frac{dP}{dA} = 0$ is desired. Therefore, the figure of merit (FOM) can be expressed in (2-6).

$$\text{FOM} = \frac{1}{\sqrt{R_{ds,sp} Q_{dg,sp}}} = \frac{1}{\sqrt{R_{ds} Q_{dg}}} \tag{2-6}$$

In first quadrant, the square root function is monotonic; therefore, figure of merit in (2-7) is used to compare devices.

$$\text{FOM}_{HS} = \frac{1}{R_{ds} Q_{dg}} \tag{2-7}$$

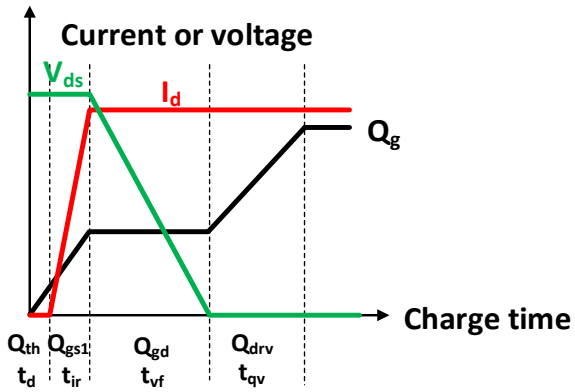


Figure 2.10. Voltage, current and gate charge during turn on transient.

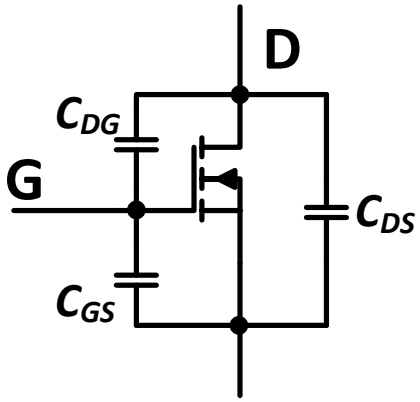


Figure 2.11. Equivalent MOSFET model with junction capacitances.

(2) Soft switching FOM

With soft switching technique, switching loss can be minimized in devices loss; therefore, the FOM derived in (2-7) is not accurate for device selection anymore. In ZVS switching, the output charge (Q_{oss}) in the MOSFET can be recovered and not dissipated as switching loss. However, Q_{oss} directly impacts the energy required to achieve soft switching. Based on this, soft switching figure of merit (FOM) has also been developed to select device in soft switching converters [33] as in (2-8).

$$\mathrm{FOM}_{SS} = \frac{1}{R_{ds,on} Q_{OSS}} \tag{2-8}$$

With hard and soft switching figure of merit defined, they can be used to evaluate devices in a power converter targeting low losses. The higher FOM, lower device losses or lower energy to achieve ZVS is expected.

2.2.2 Soft switching techniques of PWM converters

As discussed earlier, switching loss is one of the major losses in power semiconductor devices, and it increases linearly with switching frequency and becomes more significant under lighter load. For PWM converters, phase shift and asymmetrical control is widely used in order to archive zero voltage switching (ZVS), however, these methods depend on energy stored

within leakage inductance of the transformer to archive ZVS. Therefore, ZVS is lost as the load gets lighter. Also, increased leakage inductance leads to larger duty cycle loss which limits high frequency operation. Therefore, a number of methods have been proposed in order to achieve ZVS for a wider range without depending on the leakage inductance.

Figure 2.12 is the synchronous buck converter with junction capacitances (C_1 and C_2) of both devices (Q_1 and Q_2). Based on buck converter's operation, after the channel of Q_1 is turned off, the body diode of Q_2 starts to conduct the inductor current (i_L) which is in the direction from source to drain of Q_2. Therefore, Q_2 is turned on with zero voltage transition.

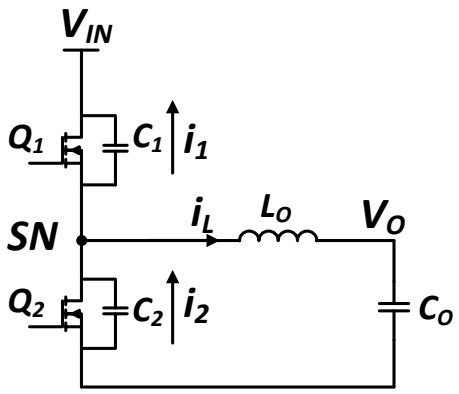


Figure 2.12. Synchronous buck converter with current direction of switches and inductor.

Similarly, in order to achieve soft switching of Q_1, before turn on of Q_1, the current of i_L direction at switch node (*SN*) should be the opposite of arrowed direction shown in Figure 2.12. As it is from load to source, it is called negative inductor current in the following section of this dissertation. Therefore, all the soft switching methods are implemented to generate negative inductor current before turning on Q_1.

A variety of soft switching methods have been proposed. Many of them are used in buck or buck derived circuits, which is the topology used in this dissertation. These methods have been

separated into two types, first one is no active components assist method and the second one is the active switches assist method.

One straightforward method to have negative inductor current is to reduce output inductance so that large current ripple will lead to a negative inductor current at the end of the freewheeling period [19][34][35], which is called quasi-square waveform (QSW) [19][34] as in Figure 2.13. Another benefit of QSW is that the two SR devices are turned off with channel conducting instead of body diode; therefore, the body diode reverse recovery is eliminated.

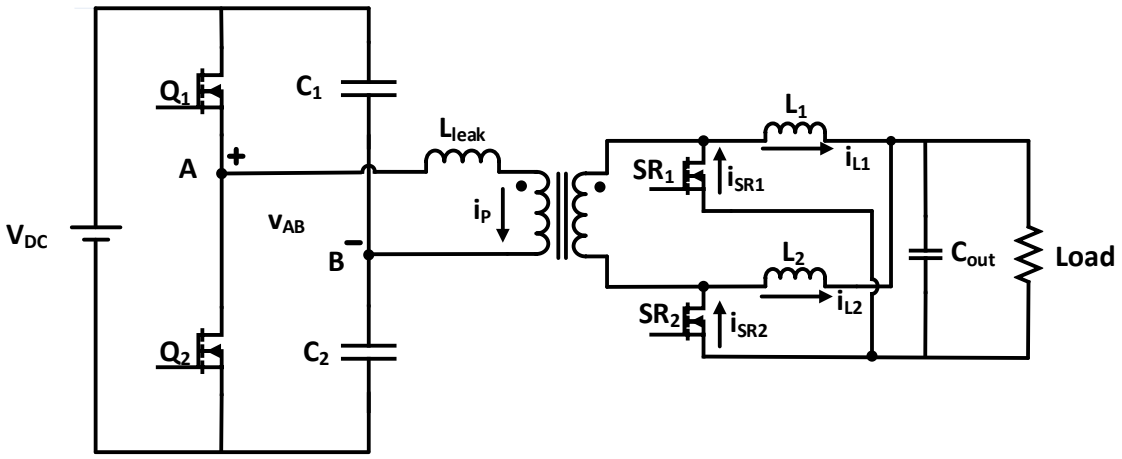


Figure 2.13. Half bridge current doubler converter.

The first drawback of QSW is that the reduced output inductance leads to an increased current ripple which will further lead to an increased RMS current and conduction loss in devices and transformer and an increased turn off loss for both primary and secondary side switches. Therefore, the QSW method has a tradeoff between conduction loss and primary side devices' switching loss. The other drawback is that the output inductance is designed to allow negative current under full load, therefore, as load current reduces, the negative current peak

will increase. As the SR devices is turning off with negative peak current, the turn off loss increases as load current reduces, which reduces the converter's light load efficiency.

In order to solve the increased turn off loss of Q_2, in [23], a clamping circuit is placed in parallel with the output inductor so the current is clamped at a desired value instead of keep increasing until Q_1 is turned on. In [36], an emulated diode rectification of synchronous rectifier is implemented, but it requires a zero current crossing detection to turn off the SR MOSFET, which increases the complexity of the circuit.

In order to solve the increased core loss of output inductor in QSW, other methods have been proposed with auxiliary components. Figure 2.14 shows the circuitry of two phase interleaved buck converter with one auxiliary inductor to assist soft switching [37][38][39]. In [37], non-synchronous buck converter (diodes are used as Q_{12} and Q_{22}), while the method proposed in [38] is working with synchronous buck converter when duty cycle is greater than 0.5. In [39], similar method has been applied to an input series and output paralleled phase shift full bridge converter. The main idea is that when Q_{11} or Q_{12} is on while the other one is off, the auxiliary inductor will be charged and discharged based on voltage direction. Therefore, the current value before Q_{11} and Q_{12} turns on is $(I_{LO} - I_{LS})$. To have the auxiliary inductor current greater than the output inductor current, the current at switch node will be in the opposite direction. The apparent drawback of this method is the auxiliary inductor loss as the auxiliary inductor is conducting continuously regardless of loading condition.

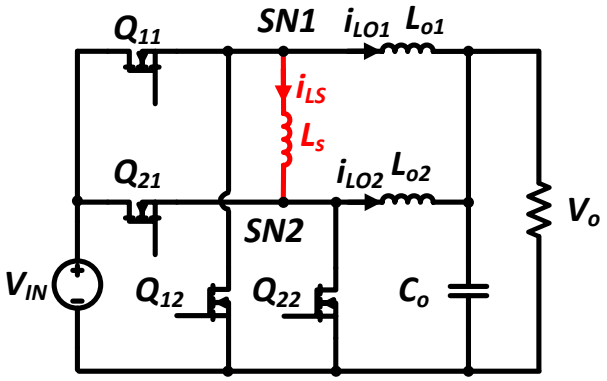


Figure 2.14. Inductor assist soft switching two phase buck converter [37][38].

Another way to realize ZVS is implementing a coupled inductor as shown in Figure 2.15 [40]-[43]. Soft turn on of the two switches (Q_1 and Q_2) can be achieved with an auxiliary circuit branch containing an additional winding of the output inductor (L_2), a smaller inductor (L_R), and a diode (D_a) in Figure 2.15. The basic idea is to provide anther power flow channel in addition to the output inductor so that the current through L_R will be negative before the turn on of S_1 as in Figure 2.16. Similar to previous methods, the magnitude of the negative current peak (i_{min}) keeps increasing as the load decreases; therefore, turn off loss of S_2 increases as load reduces. Also, the constant additional power loss in auxiliary branch limits the light load efficiency of the converter. In [43], this constant auxiliary loss is solved by reducing the resonant inductor so that the current in L_R will be discontinuous as D_a blocks any negative current. However, this method changes the zero voltage turn on of S_1 to zero current turn on, which means the energy stored in the output junction of capacitance of S_1 will be lost in the channel instead of being recovered.

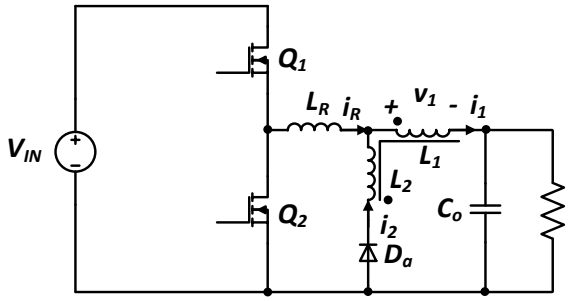


Figure 2.15. ZVS buck converter with coupled inductor [40].

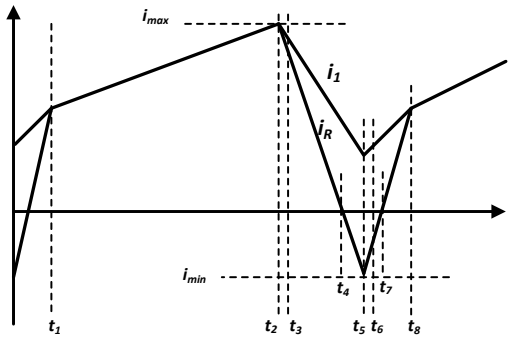


Figure 2.16. Waveforms of i_1 and i_R [40].

In [44]-[48], soft switching of main switch in a buck converter has been proposed with an auxiliary MOSFET, diode and inductor in parallel with output inductor as in Figure 2.17. In [44], this method is applied for a diode rectification buck converter which limits the duty cycle of the converter to be less than 0.5. In [45][46], by applying synchronous rectification, the duty cycle can be greater than 0.5, yet the operating principle is the same. Before the turn off of synchronous device S_2, the auxiliary switch S_a is turned on. Current in arrow direction will start to build up across the auxiliary inductor. As the inductor current across the output inductor L cannot change immediately, the current flowing through S_2, I_{s2}, starts to reduce while the current I_{sa} starts to increase. Based on KCL, the sum of I_{s2} and I_{sa} equals to I_O. The charging I_{sa} will continue until the current I_{s2} becomes negative. When S_2 is turned off with current flowing

though drain to source, the body diode conduction is prevented. Therefore, during the dead-time between S_2 turn off and S_1 turn on, resonance happens between the auxiliary inductor L_a and the snubber capacitor C_s. With enough energy stored in L_a, C_s can be fully discharged before the turn on of S_1. Therefore, soft switching turn on of S_1 can be achieved. The snubber capacitor is placed in parallel with main switch S_1 so that zero voltage turn off can be achieved for S_1 and S_2. The constant auxiliary circuit loss would also limit the light load efficiency of this method. In [47], a look up table (LUT) is implemented in digital controller to adjust the gate signal timing of auxiliary inductor to improve light load efficiency.

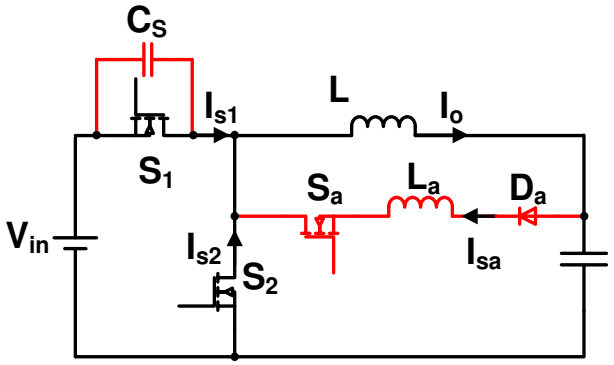


Figure 2.17 ZVT buck converter proposed in [45].

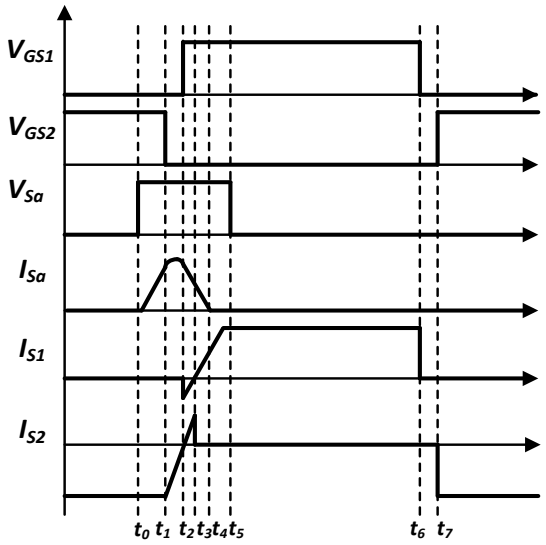


Figure 2.18. Theoretical waveforms of ZVT converter [45].

In addition to turn on loss reduction, different methods of turn off loss reduction have been proposed as well. A snubber capacitor is placed in parallel with either top switch or rectifier switch as C_s shown in Figure 2.17. During the turn off transient of S_1, the current flowing through S_1 is charging C_s, therefore, the voltage to be hard switched is $V_{Q1,HS}$ in Figure 2.19. The amount of required capacitance depends on the hard voltage $V_{Q1,HS}$ and peak inductor current. The larger the current or the lower the hard switch voltage, the larger the snubber capacitor needs to be. However, larger snubber capacitance limits high frequency operation and also increases the capacitance loss during the turn on process.

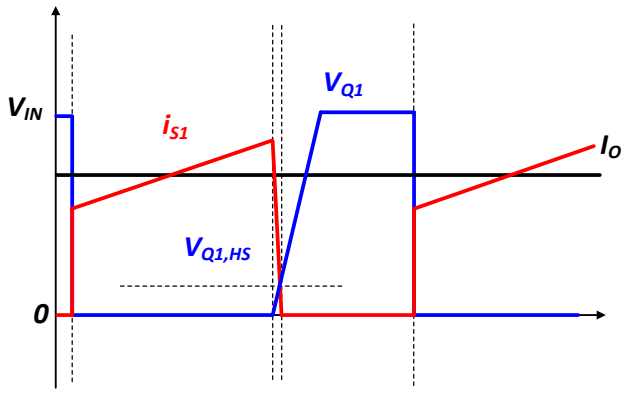


Figure 2.19. Turn off waveforms with snubber capacitor.

In [49], a quasi- resonant method with a LC resonant circuit has been proposed as in Figure 2.20 with the operation waveforms shown in Figure 2.21. When LC is selected, the resonant frequency is also fixed; therefore, quasi resonant converter is controlled with constant on time. In order to control duty cycle, the frequency is changed, so this is a frequency regulated converter. Frequency resonant converter complicates the output filter design, therefore, pulse width modulated converter with ZCS has been proposed [50][51] as shown in Figure 2.22 and the operational waveforms in Figure 2.23. By adding a MOSFET in series with resonant capacitor C_R, the resonance time can be controlled.

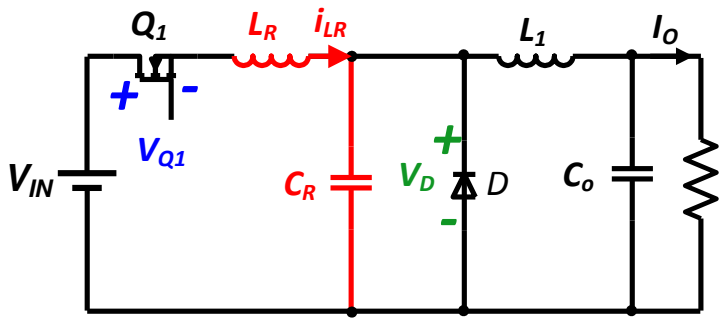


Figure 2.20. Quasi-resonant ZCS converter.

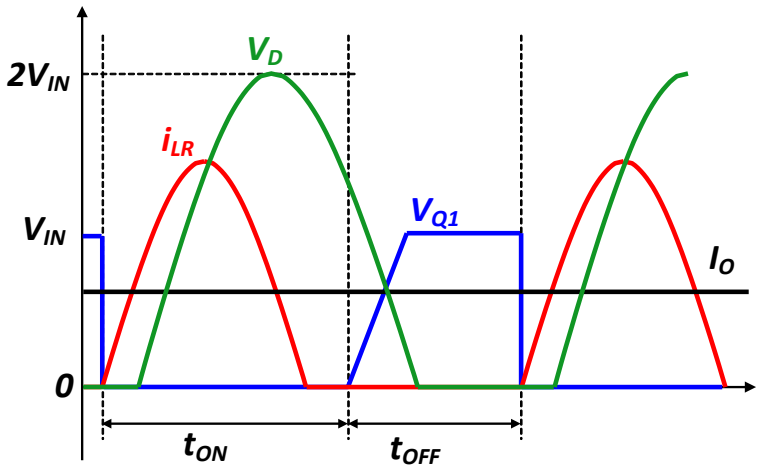


Figure 2.21. Operational waveforms of quasi-resonant converter.

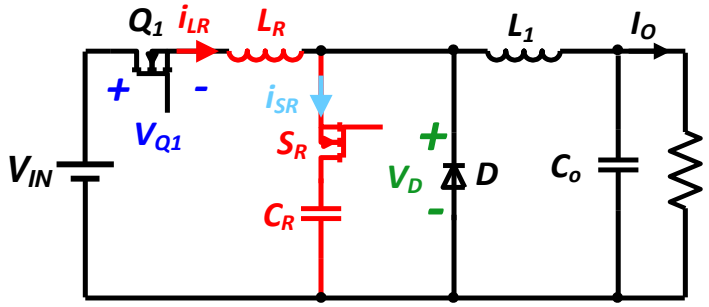


Figure 2.22. ZCS converter with pulse width modulation capability.

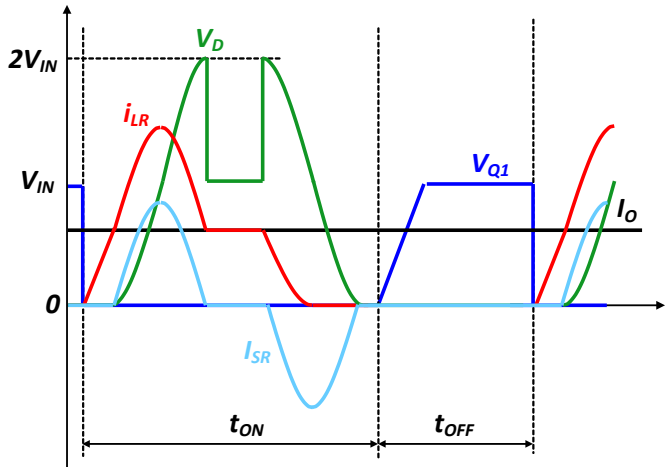


Figure 2.23. Operational waveforms of PWM ZCS converter.

However, the ZCS methods all require higher voltage rating SR devices and a higher resonant current, which will undermine the efficiency improvement by eliminating the turn off losses of the top MOSFET.

2.3 Control of input series and output parallel (ISOP) connected converter

For high input voltage low output voltage application, input series and output parallel (ISOP) connected converter has several advantages compared with single converter [52]: 1) Step down ratio is greatly reduced which leads to simpler converter design. 2) Lower switching frequency can be used compared with a single converter by interleaved gating signal. 3) Higher efficiency as a result of using low voltage rating devices in the circuit.

For input series and output paralleled converter as shown in Figure 2.24, one issue is to ensure input voltage and output current sharing and prevent converters from runaway (which means one phase takes the entire input voltage and output current). A number of methods have been proposed to achieve stable operation of ISOP connected converters. The methods can be divided into two categories: common duty cycle control and active control.

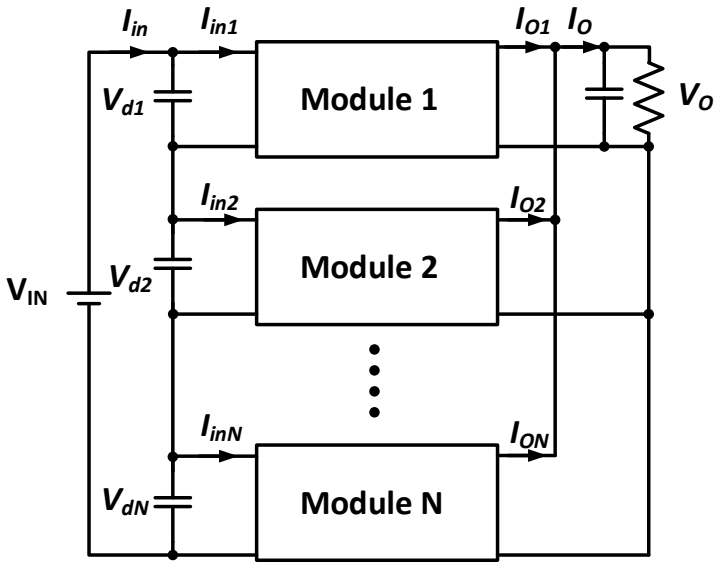


Figure 2.24. ISOP connected converters.

2.3.1 Common duty cycle control

Common duty cycle control is one of the simplest and most straightforward control method in the input-output connected converters, where all the converters are fed with the same duty cycle, and only time shift the gate signal for each individual converter (shown in Figure 2.25) [52]-[58]. The ramp signal (V_{ramp}) is phase shifted between one and another; therefore, the gate signal for each converter is also phase shifted and interleaved. Table 2.1 shows the stability of input-output connected converters with common duty cycle control with different transformer turns ratio [57] where the transformer turns ratio is n:1. For input series and output parallel connected converter, even with circuitry mismatch, such as transformer turns ratio difference, the common duty cycle control can prevent circuit from runaway where one converter in the ISOP system carrying the entire input voltage and output current, which is called self-correcting mechanism [57]. For example, in ISOP connected converter, the output voltage has to be equal. When the duty cycle is also the same, which means the average rectifier voltage is also the

same. Converter with higher turns ratio will withstand higher input voltage automatically. Assuming ISOP connected converters' efficiency is comparable with each other, converter with higher turns ratio will conduct higher output current as well [57]. In the meantime, clear shown in Table 2.1, IPOP and ISOS are not stable with common duty cycle control; therefore, active control is required for them.

However, when mismatches (like transformer turns ratio, device turn on time, parasitic inductances and etc.) exist in the circuit, even sharing of input voltage and output current is lost. Converter with higher turns ratio carries slightly lower input voltage and output current [52][56][57]. Other studies also show that with common duty cycle control, runaway can be eliminated for both steady state and transient with mismatches in transformer turns ratio and leakage inductance [52]. The magnitude of difference in input voltage and output current sharing relies on how well matched each module is.

Table 2.1. Suitability of common ratio cycle scheme [57].

Mode	Stability	Output current	Output voltage	Input current	Input voltage
IPOP	Unstable	Converter with **'n' lower** carries **entire** load current	Equal due to parallel connection	Converter with l**ower 'n'** carries **entire** current	Equal due to parallel connection
IPOS	Stable	Equal due to series connection	Converter with **lower 'n'** carries slightly **higher** voltage	Converter with **lower 'n'** carries slightly **higher** current	Equal due to parallel connection
ISOP	Stable	Converter with **lower 'n'** carries slightly **lower** current	Equal due to parallel connection	Equal due to series connection	Converter with **lower 'n'** carries slightly **lower** voltage
ISOS	Unstable	Equal due to series connection	Converter with **higher 'n'** carries **entire** voltage	Equal due to series connection	Converter with **higher 'n'** carries **entire** voltage

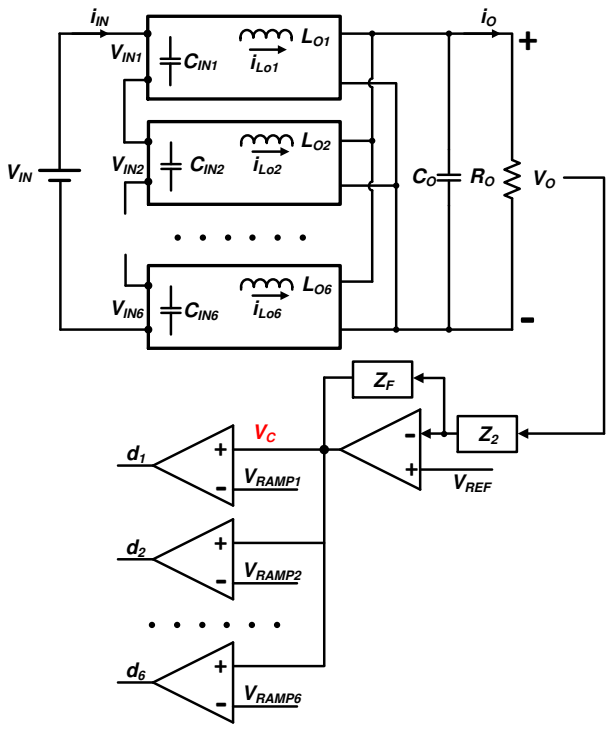


Figure 2.25. Common duty cycle control.

2.3.2 Active control

In order to make sure each module has even input voltage sharing (IVS) and output current sharing (OCS) with mismatch presented in the circuit, active control is required. Different methods of active IVS and OCS have been proposed.

One of the most widely used active sharing methods contains an input voltage feed-forward loop [59][60][61][62] in addition to the converter outer voltage and inner current loop. In [59], the input voltage is added to the reference voltage of the converter's output voltage and due to the positive output voltage gradient characteristic, IVS can be obtained. In [60], a common duty cycle is generated with the outer voltage feedback loop, and the duty cycle is further modified with input voltage sharing regulating (IVSR) loop for the first *m-1* modules, and the m^{th} module is modified with the entire error signals from the other modules. Similarly, in [61], within the

inner current loop, a common current reference is generated with the common outer voltage loop and adjusted with the input voltage sharing loop. In [62], a charge control technique used in addition with input voltage feedforward loop.

However, even though those methods can achieve an accurate input voltage and output current sharing among modules in an ISOP converter, they all required a complicated and dedicated input voltage sharing control loop, which increases circuit control complexity and reduces reliability.

2.4 Summary

In this chapter, a literature review on power supplies used in data centers at the rack level has been provided, including two of the most widely used architectures, IBA and FPA and some alternatives under IBA. The advantages and disadvantages of the architecture have been discussed as well.

Next, several high efficiency PWM DC/DC converters design and control methods are reviewed because they are essential parts of power delivery, including device selection criteria and soft switching technique. Figure of merit (FOM) of devices allows a simple yet effective way to select a device with possible low combination of losses (conduction and switching losses). Switching losses is one of the major contributions of device losses in PWM converters. The advantages and disadvantages of different soft switching methods have been discussed.

The last part in this chapter is the control method for the input series and output parallel (ISOP) connected converter to ensure stable operation. Two major methods have been categorized here: common duty cycle and active sharing method with pros and cons provided.

3. Alternative Power Supplies Architecture Design

Different types of power conversion architectures in power supplies have been discussed in the previous chapter. Besides power conversion losses, power distribution losses is non-negligible because of the continually increasing load current requirement in servers, which in turn makes the I^2R loss continue to increase for any given distribution voltage.

In this chapter, alternative power supply architectures with potential to improve efficiency are investigated. First, on-board distribution voltage's impact on efficiency has been studied where 400 V on-board distribution voltage is proposed to greatly reduce distribution losses.

Then, different bus voltages between IBC and POL in IBA have been investigated in order to determine how much efficiency gain can be obtained by varying the bus voltage within the IBA architecture.

At last, a single stage high voltage point of load (HV POL) architecture which converts 400 V to 1 V directly has been proposed to achieve high efficiency. Converter topologies have been selected for HV POL, and a comparison between HV POL and IBA is performed.

3.1 400 V on-board distribution voltage architecture

Based on the discussion in Chapter 1, the core voltage continues to decrease as the CPU core loss is proportional to the core voltage square [2][3]. With the low voltage and high current demands from the processor, on-board distribution losses ($P_{dis} = I_{dis}^2 \cdot R_{copper} = \frac{P}{V_{dis}^2} \cdot R_{copper}$) cannot be ignored with 12 V distribution voltage which is widely used in IBA [63].

A simple case study has been performed to indicate the considerable distribution losses under low distribution voltage. A 12 V and 400 V distribution voltage that handles 1600 W

power for multiple CPUs is studied as in Figure 3.1 and Figure 3.2, respectively. The size of the motherboard is selected as 0.305 m × 0.244 m, which is the standard Advanced Technology eXtended (ATX) size developed by Intel [64].

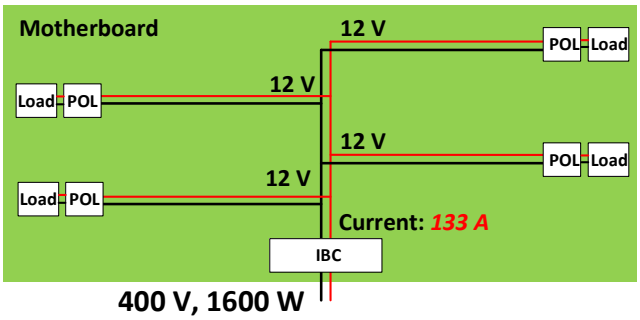


Figure 3.1. 12 V distribution voltage.

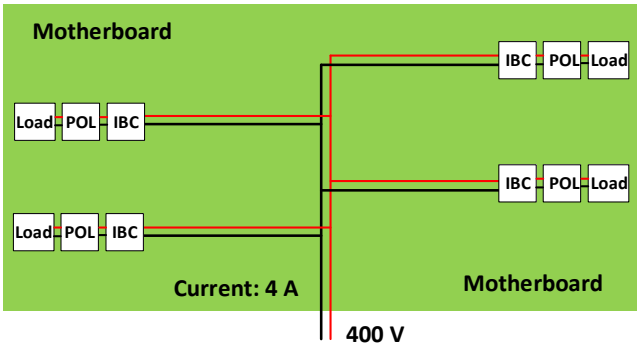


Figure 3.2. 400 V distribution voltage.

Table 3.1 shows the distribution loss of 12 V distribution voltage with different combinations of copper thickness and width, which indicates that the distribution loss is non-negligible. Even though distribution loss can easily be reduced by using thicker or wider copper, this will increase the cost the system. By increasing the distribution voltage from 12 V to 400 V, the distribution loss can reduce greatly as shown in Table 3.2 compared with losses listed in Table 3.1.

Table 3.1. Loss for 12 Vdc distribution on motherboard for 1600 W load.

Thickness \ Width	700 mils	1 inches	2 inches
0.5 oz	477.7 W	334.4 W	167.2 W
1 oz	238.9 W	167.2W	83.6 W

Table 3.2. Loss for 400 Vdc distribution on motherboard for 1600 W load.

Thickness \ Width	700 mils	1 inches	2 inches
0.5 oz	0.43 W	0.3 W	0.15 W
1 oz	0.21 W	0.15 W	0.075 W

To be fair, the drawback of high voltage on-board distribution voltage includes reliability and safety required by the system, which needs a more thorough design [63].

The following discussion is based on 400 V on-board distribution voltage, and distribution loss is reasonably ignored (less than 0.03 % of the load power) from the system's efficiency calculation.

3.2 Bus voltage optimization of intermediate bus architecture

As intermediate bus architecture (IBA) is the most widely used architecture at this time, a study has been performed on IBA when the bus voltage is treated as one variable. Figure 3.3 shows the structure of intermediate bus architecture (IBA) where the two stages are connected in series. For most current IBA, 12 V is selected as intermediate bus voltage because fans in servers usually are powered by 12 V; therefore, no further conversion is required for the fans. However, for all other loads in servers, a voltage regulator (VR) is required to further step down

12 V to a lower voltage (5 V, 3.3 V or 1 V), which is usually fulfilled by multi-phase synchronous buck converters.

In this section, only 1 V output voltage is considered. The overall efficiency from 400 V to 1 V is the combination of the two stages efficiency as shown in (3-1), where η is the overall efficiency, η_{IBC} is the IBC's efficiency and η_{POL} is the POL's efficiency. A selection of intermediate bus voltage is performed to achieve high overall system's efficiency as increasing the bus voltage favors IBC but worsens POL and vice versa. The bus converter is rated at 300 W which will be connected to power two POL converters each rated at 150 W for the following studies.

$$\eta = \eta_{IBC} * \eta_{POL} \tag{3-1}$$

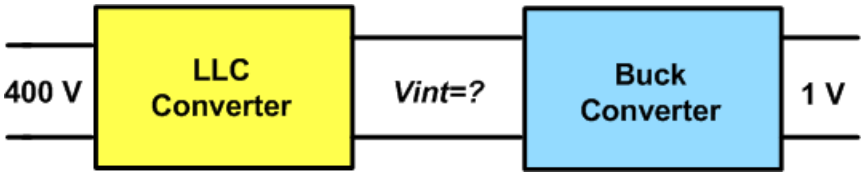


Figure 3.3. Intermediate bus architecture (IBA).

3.2.1. Bus converter efficiency with different bus voltage

LLC resonant converter shown in Figure 3.4 is selected here as for the IBC. The input voltage is 400 V and the output bus voltage is varied from 4 V to 24 V. The switching frequency of the bus converter is 1 MHz.

(1) Primary side device selection

Table 3.3 shows the primary side device comparison of 600 V MOSFET including both Si and GaN [22]. Devices listed in Table 3.3 [22] have comparable $R_{ds(on)}$, but it is clear that GaN FETs have lower output charge which lead to smaller RMS current though primary side devices

and transformer and also lower gate charge current. Therefore, 600 V GaN HEMT is selected as primary side devices in the LLC converter. Similar to the investigation of alternative architectures, replacing Si MOSFETs with GaN HEMTs in the IBC converter is an effective way to increase the converter's efficiency [22].

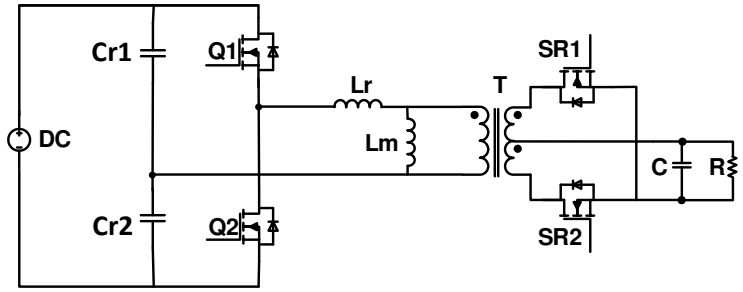


Figure 3.4. LLC resonant converter.

Table 3.3. Primary side device comparison for LLC converter [22].

Device	$R_{ds\ (on)}$ (Ω)	Output charge (nC)	Gate charge (nC)
TPH3006PS (GaN)	0.15	52	6.2
IPP60R165CP (Si)	0.15	105	39
FCH170N60 (Si)	0.15	91.2	42
AOT27S60 (Si)	0.14	106	26

(2) Transformer design

The transformer is the most lossy part among all the components in the LLC converter [22]. Different transformers have been designed based on the output voltage, and the summary in Table 3.4 includes copper thickness, core selection and the corresponding transformer turns ratio to step down the input voltage to designed output voltage. Lower output voltage from LLC converter means a higher transformer turns ratio. The losses of the transformer include both core

loss and winding loss. Skin effect and proximity effect are being considered in winding loss calculation [65] [66].

Table 3.4. Transformer design of different output voltage in LLC converter.

Output Voltage	Copper Thickness	Core Type	Turns ratio
24, 12, 10, 8V	Primary: 2 Oz	E22/6/16 PLT22/16/2.5	8, 16, 20, 24
6, 4 V	Secondary: 2 Oz	2 *E18/4/10 PLT18/10/2	32, 48

(3) Secondary side device selection

The secondary side MOSFETs of LLC resonant converter are being turned on with zero voltage across them and turned off with zero current [22]; therefore, switching loss is ignored for SR MOSFETs.

Table 3.5. Si SR devices selection for different output voltage.

Output voltage	Device voltage (V)	$R_{ds\ (on)}$ (Ω)	Q_g (nC)
4	25	1.0	31
6	25	1.0	31
8	30	1.3	20
10	40	1.2	19
12	40	1.2	19
24	80	2.5	15

The SR devices losses include conduction loss and gate driving loss, which can be represented by $R_{ds\ (on)}$ and Q_g in Table 3.5.

(4) IBC's efficiency

With devices selected and transformer designed in the above sections, the efficiency of the LLC converter can be calculated with different output voltage and plotted in Figure 3.5. Full load efficiency reduces with a decreased bus voltage as more output current is handled by the transformer and SR devices.

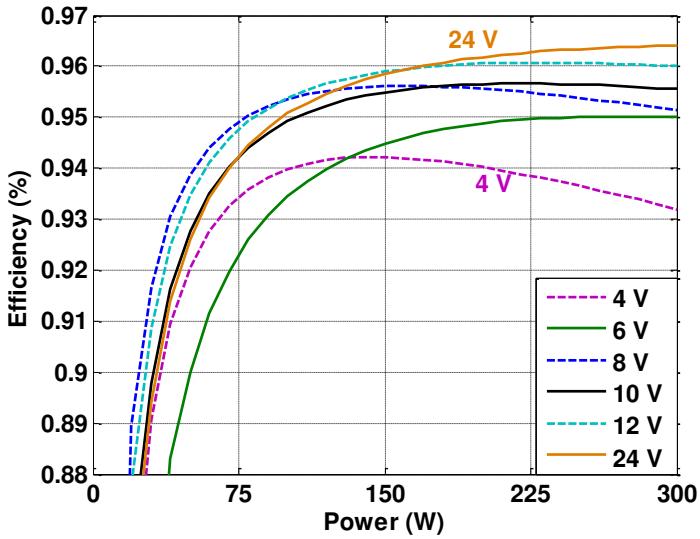


Figure 3.5. LLC efficiency at different bus voltages.

3.2.2. POL efficiency with different bus voltage

POL converter with five phase synchronous buck converter (shown in Figure 3.6) will be designed and discussed in this section. The switching frequency is 200 kHz for each phase, which makes the effective switching frequency 1.0 MHz. The output power is 150 W for all the cases. Table 3.6 summarizes devices selection for different input voltage with the large figure of merit (FOM) ($\frac{1}{R_{ds(on)} \cdot Q_{gd}}$) as discussed in Chapter 2. The same MOSFET is used for 6 V through 12 V, which is mainly because 25 V MOSFETs have more choices than 10 V though 20 V,

therefore, a better performance MOSFET at 25 V is actually available compared with lower voltage rating MOSFETs.

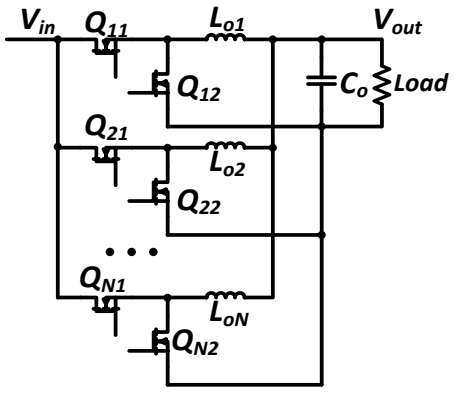


Figure 3.6. Multiphase synchronous buck converter.

Table 3.6. MOSFET selection for different output voltage in POL.

Input voltage (V)	Device voltage (V)	$R_{ds\ (on)}$ (Ω)	Q_{gd} (nC)
4	7	1.25	2
6	25	0.95	4.9
8	25	0.95	4.9
10	25	0.95	4.9
12	25	0.95	4.9
24	40	4	2.2

The losses of the synchronous buck converter mainly include the conduction loss of the two MOSFETs, switching loss of the main switch MOSFET (synchronous switch is being soft switched), reverse recovery loss of SR devices, gate driving loss of two MOSFETs, and the DCR and ESR loss of the inductor and capacitors. The switching losses of MOSFETs are calculated using the method in (2-3). Inductor is selected to have 30 % current ripple with the given input voltage and same output capacitor is used.

Figure 3.7 shows the efficiency of the buck converter for different output power with different input voltages. As the input voltage increasing, the efficiency reduces under the same load condition because of higher switching losses for the main switch and higher voltage rating devices need to be used.

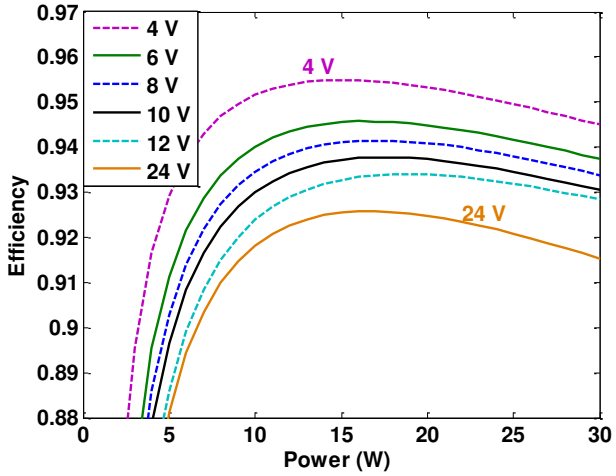


Figure 3.7. Buck efficiency at different bus voltage.

3.2.2 IBA efficiency with different bus voltage

With bus converter and POL converter efficiency calculated, the overall efficiency from 400 V to 1 V can be analyzed based on (3-1) and plotted in Figure 3.8.

It can be seen that 4 V bus voltage allows the highest light load efficiency yet worst full load efficiency as 4 V bus voltage complicates the transformer in the LLC converter. 24 V bus voltage provides limited efficiency over the whole range, therefore, it is not a good choice. 12 V, 10 V and 8 V offers comparable efficiency over the entire load range, yet 12 V has higher efficiency most of the time. 12 V bus offers slightly higher full load efficiency yet lower light load efficiency compared with 8 V bus voltage. Therefore, depending on load condition, 8 V and 12 V bus voltage can be selected correspondingly.

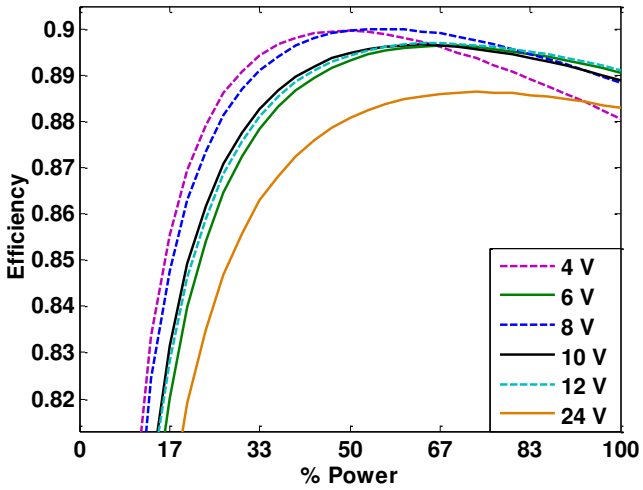


Figure 3.8. Overall system efficiency of IBA at different bus voltage.

Since 12 V is actually the bus voltage used most of the time in data center power supplies, which also means that changing the bus voltage, the efficiency gain would be quite limited. Other architecture is necessary to increase the system's efficiency.

3.3 HV POL Architecture

For the above architectures, despite the converter topology and distribution voltages difference, they all have several power stages connected in series. The overall efficiency from the 400 V entering the motherboard to the 1 V supplying the microprocessors becomes the product of each converter's efficiency, which will be lower than the lowest efficiency in the power supply chain. One reason for that is the on-board distribution voltage is different from the input voltage (400 V), which requires one or several power conversion to produce the on-board distribution voltage from the 400 V. However, by adopting the 400 V on-board distribution voltage, it is possible to convert 400 V to 1 V directly, saving one or more power conversion stages.

When it comes to actual losses in the converter, for LLC bus converter, the major losses are the transformer's winding loss and primary and secondary devices conduction loss [22]. Transformer winding loss is dominant because of the skin and proximity effect under high switching frequency which is usually implemented to shrink the volume of the bus converter.

400 V input voltage requires 600 V MOSFET with $R_{ds(on)}$ in the level of hundreds of mΩ [22]. 40 V MOSFET is selected since the nominal voltage is 24 V across SR in LLC, which has lower FOM compared with devices voltage rating at or below 25 V [6].

The dominant losses of POL are the top MOSFET switching loss [4][5][6]. The top MOSFETs in buck converter is switching at high voltage (~12 V) and high current (tens of A) and the switching loss cannot be reduced by paralleling of devices.

The overall loss breakdown for a 300 W IBA is illustrated in Figure 3.9. The losses of LLC and multiphase buck converter are obtained from the design in Section 3.2 with 12 V bus voltage. From Figure 3.9, it can be seen that the top MOSFETs in the multiphase buck converter are responsible for the dominant loss mechanism in the IBA. In order to improve the efficiency, the losses in the top MOSFETs need to be reduced.

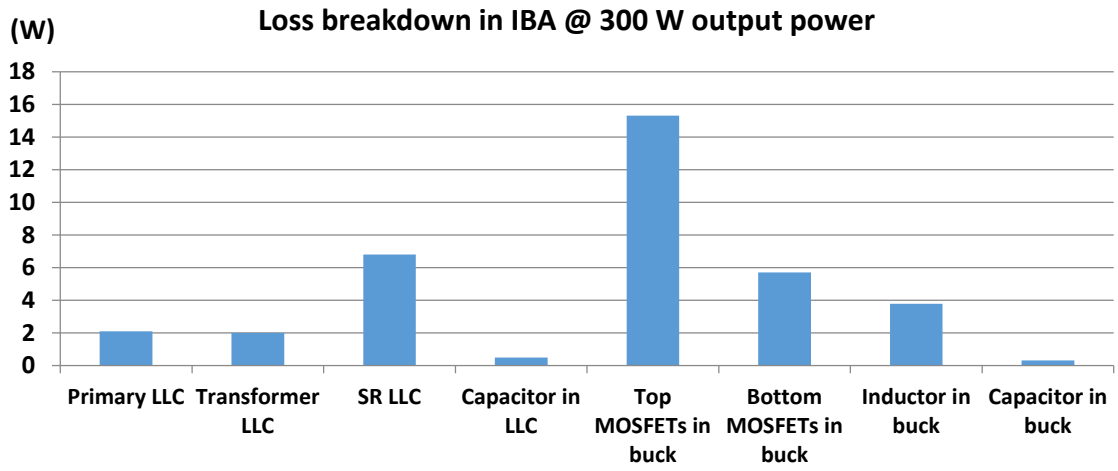


Figure 3.9. Loss breakdown of 300 W IBA.

A high voltage point of load (HV POL) architecture which converts 400 V directly to 1 V is proposed as an alternative architecture to improve the efficiency of the power supplies and the structure and topologies used in HV POL will be discussed in the following sections.

3.3.1 Structure of HV POL

Similar to the multiphase buck converter, instead of using one converter switched at high frequency, several converters with interleaved control signal allowing single converter to be switched at lower frequency is considered here. However, the input to output voltage ratio in HV POL is much larger (400:1) than POL (12:1); therefore, the converters in HV POL is input series and output parallel (ISOP) connected rather than input parallel and output parallel (IPOP) connected structure used in POL. Figure 3.10 shows the structure of ISOP connected HV POL. Six modules are used in the ISOP structure. The reasons to select six phases ISOP system include: 1) 100 V MOSFETs can be used with enough margin; 2) transformer turns ratio in each converter is limited to an acceptable number, and 3) the transformer AC skin depth equals 4 oz copper with the equivalent switching frequency become comparable with commercial products.

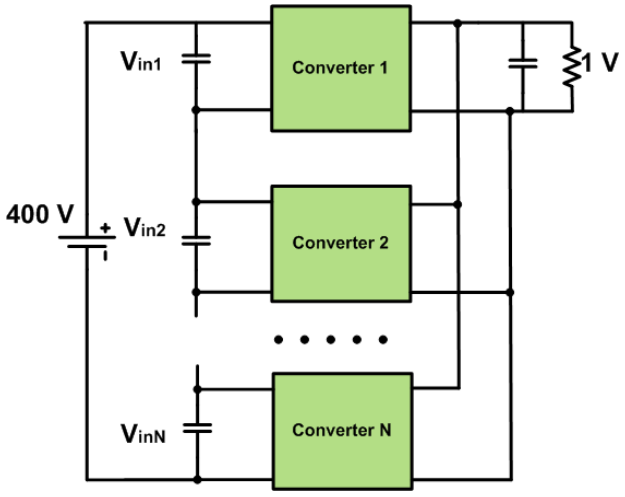


Figure 3.10. Structure of ISOP connected HV POL.

Multiphase structure allows interleaving control signal. With interleaved control, the inductor currents of different modules are not in phase with each other. When one inductor current is at the peak value the other might be at the minimum value, therefore, the output current is smaller compared with single inductor's current ripple as shown in Figure 3.11. Clearly indicated in Figure 3.11, the current ripple can be cancelled out with each other completely when the duty cycle equals to 0.5 for different phase number, which is the ideal case. However, the load or input voltage variation will change the duty cycle at the same time, which makes current ripple increase for all conditions. However, the current ripple is smaller when there are more phases involved for the same amount of duty cycle variation. For example, when the duty cycle changed from 0.5 to 0.6, the current ripple is increased to less than 0.1 for 12 phases and over 0.3 for two phases. Therefore, with more phases interleaved, the current ripple is limited to a smaller value regardless of duty cycle.

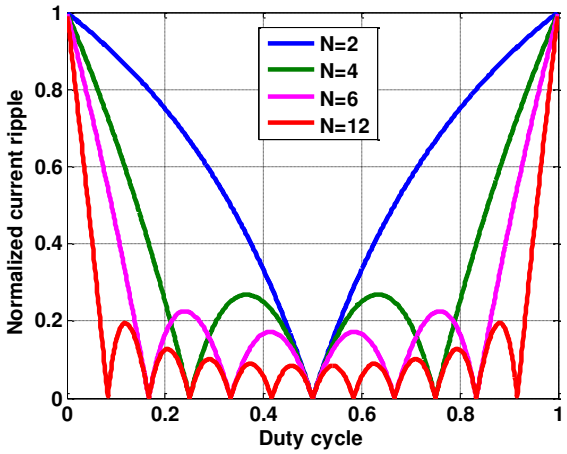


Figure 3.11. Ripple current cancellation with respect to interleaved phase number and duty cycle.

3.3.2 Topology selection for HV POL

After the structure is selected, the next step is to determine the converter topology in the HV POL. The requirements for HV POL include 1) isolation, 2) voltage transformation, and 3)

voltage regulation. The transformer realizes isolation and voltage transformation. Pulse width modulation (PWM) circuit is selected for HV POL for simple voltage regulation.

Figure 3.12 shows the two configurations for the primary side of the isolated converter, full bridge and half bridge, both of which are suitable and easy for voltage regulation. The major difference is that the voltage seen at the transformer primary side, which is $\pm V_{DC}$ for full bridge and $\pm \frac{1}{2}V_{DC}$ for half bridge. At the same time, the current stress of both primary side devices and transformer winding is roughly two times for the half bridge configuration compared with the full bridge configuration. The comparison is summarized in Table 3.7.

(a) Full bridge (b) Half bridge

Figure 3.12. Primary circuit configuration.

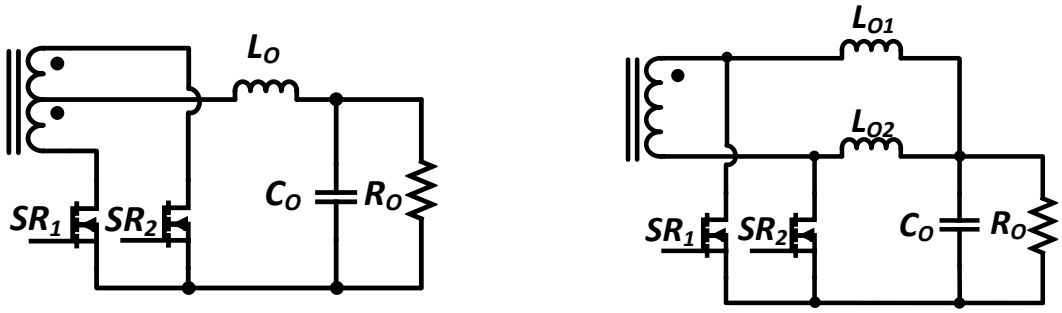
Table 3.7. Primary circuit comparison: half bridge compared with full bridge

	I_{RMS}	Number of FET	Transformer turns ratio
Full	1	4	N
Half	2	2	0.5N

Figure 3.13 shows the configuration for secondary side of the isolated converter, full wave and current doubler, both of which are good candidates for high output current application. Full wave rectification circuit is implemented with a center tapped transformer

and one output inductor, while current doubler requires a two winding transformer with two smaller output inductors. The inductor in full wave rectification sees twice the switching frequency current; therefore, a smaller value inductor can be used here with the cost of an extra transformer winding. Table 3.8 summarizes the comparison between the two secondary side topologies.

Two combination of primary and secondary structure are selected for further study, one is full bridge with full wave center tapped transformer (as shown in Figure 3.14), and the other one is half bridge with current doubler circuit (as shown in Figure 3.15).



(a) Full wave rectification (b) Current doubler rectification

Figure 3.13. Secondary circuit configuration.

Table 3.8. Secondary circuit comparison: full wave compared with current doubler

	Voltage rating	Number of FET	Sets of secondary side windings
Full wave	1	2	1
Current doubler	1	2	2

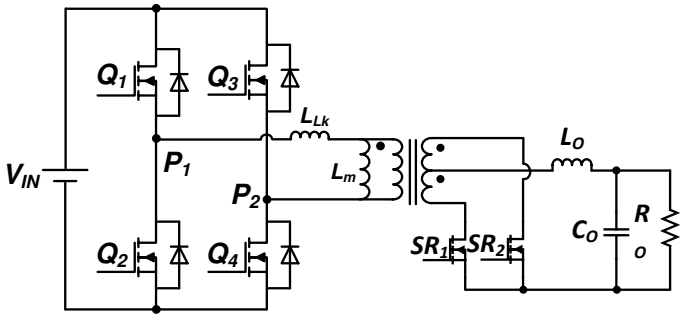


Figure 3.14. Full bridge with full wave rectification.

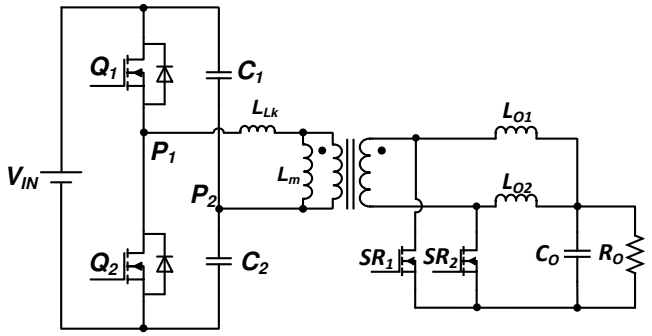


Figure 3.15. Half bridge with current doubler.

The reason for phase shift full bridge converter is that it has the potential to realize zero voltage switching (ZVS) with no extra cost. As for half bridge current doubler, it can achieve the same step down ratio under same duty cycle with lowest transformer turns ratio, which has the potential for easier transformer design. Also, current doubler structure allows current to circulate in the SR MOSFETs without flowing into the secondary side of the transformer, which helps to reduce the winding losses.

3.3.3 Comparison between IBA and HV POL

After converter structure and topology have been selected and designed, the losses and efficiency of HV POL can be calculated. Furthermore, it can be compared with IBA under the same input/output voltage and power condition (400 V/ 1 V and 400 W). For IBA architecture,

the bus converter is rated at 400 W while the POL is rated at 200 W. Therefore, one bus converter is connected with two POL converters with input parallel and output parallel (IPOP) connection. The HV POL is rated at 200 W with six half bridge current doubler circuit input series and output parallel connected. Two of the HV POL converters are IPOP connected to provide 400 W output power. The switching frequency for both synchronous buck converter in IBA and half bridge or full bridge in HV POL is 280 kHz.

Figure 3.16 shows the loss distribution of IBA and HV POL with both phase shift full bridge and half bridge current doubler. The comparison clearly shows that the overall loss of HV POL is smaller than IBA because the saving of top MOSFETs conduction and switching loss of POL. However, the transformer loss is larger in HV POL compared with IBA, mainly because it handles higher current. The output inductor for both IBA and HV POL is selected such that the output current ripple is the same. The overall volume of output inductor for HV POL is slightly higher compared with IBA. Therefore, there is a tradeoff between power density and efficiency.

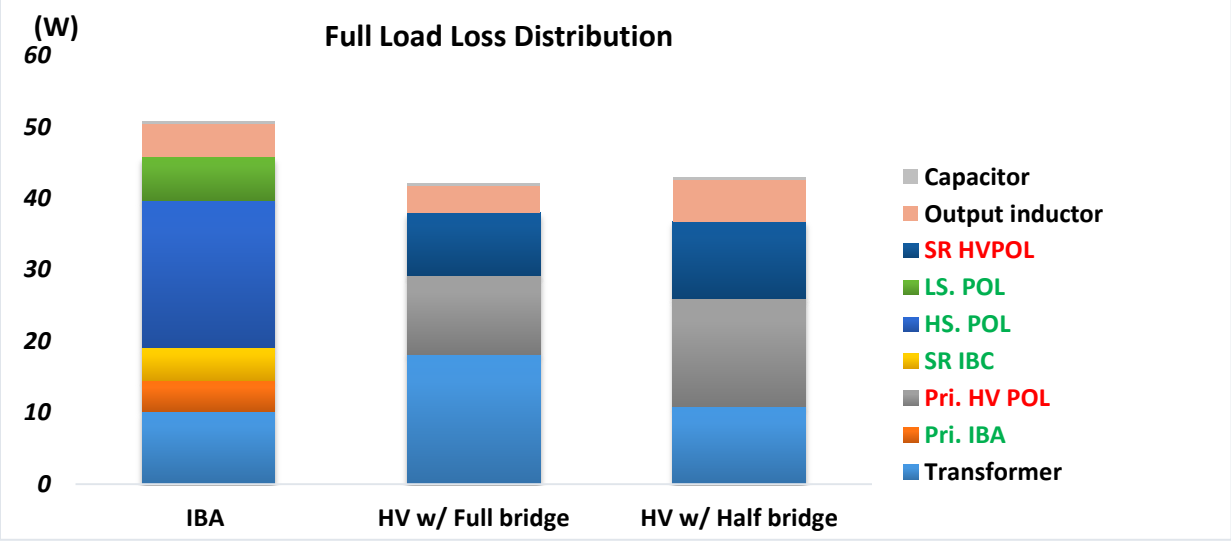


Figure 3.16. Comparison of loss distribution between IBA and HV POL.

3.4 Summary

In this chapter, alternative power delivery architectures have been studied in order to improve both power delivery and power conversion efficiency. First, the distribution losses with 12 V distribution voltage has been estimated, and because of the low core voltage and high current demand, distribution loss is quite large. Therefore, 400 V on-board distribution voltage has been selected to first reduce the distribution loss.

Then, the intermediate bus voltage of IBA has been studied in order to obtain high efficiency of the two stages (IBC and POL). Both IBC and POL have been designed and efficiency has been estimated respectively. Based on the analysis, bus voltage between 8 V to 12 V allows better efficiency over the expected load range.

In the last section, a high voltage point of load (HV POL) has been proposed which converts 400 V to 1 V with a single power conversion stage. Conversion structure and converter topology has been selected and a detailed comparison between HV POL and IBA has been conducted. Higher efficiency can be achieved for HV POL based on analysis.

4. Phase Shift Full Bridge DC/DC Converter in HVPOL

In this chapter, the design of the phase shift full bridge (PSFB) DC/DC converter with the specifications shown in Table 4.1 will be analyzed and discussed. Components including primary and secondary devices selection and planar transformer design will be discussed.

First, different transformer winding structures are designed, and corresponding leakage inductance and AC resistance are calculated considering the fact that a center tapped transformer with two secondary side windings are used in PSFB converter. The experimental measurement and verification is also provided.

Then, the detailed PSFB converter operation process is illustrated highlighting the impact of primary side devices' output junction capacitances on the transformer's current and converter's efficiency and verified in experiments.

A 89.1 % full load efficiency and 91.2 % peak efficiency can be achieved for the PSFB converter in experiments, which is given at the end of this chapter.

Table 4.1. Specifications of a single PSFB converter used in HV POL converter.

Power rating	33 W
Input voltage	66 V
Output voltage	0.98 V – 1.02 V (1 V nominal)
Output voltage ripple	10 mV peak to peak
Operating temperature	50 °C

4.1 Transformer design

The transformer in the phase shift full bridge (PSFB) DC/DC converter performs not only the isolation and voltage step-down, but also helps the zero voltage switching (ZVS) of primary side MOSFETs by making use of the leakage inductance of the transformer. Therefore, the key

factors that determine the performance of both the transformer and converters are: 1) turns ratio, 2) core loss, 3) AC winding loss, and 4) leakage inductance, which will all be discussed as follows.

4.1.1 Transformer turns ratio selection

The transformer in a PSFB converter should be designed for the worst case, which is the lowest input voltage and highest output current. The minimum input voltage of PSFB is decided by the holdup requirement. Hold-up time is required for the on-board power supply, which means when the AC main input power is off, the energy storage capacitor (C_H in Figure 4.1) can deliver power to the load for a short period of time (usually 10-20 *msec*) [71].

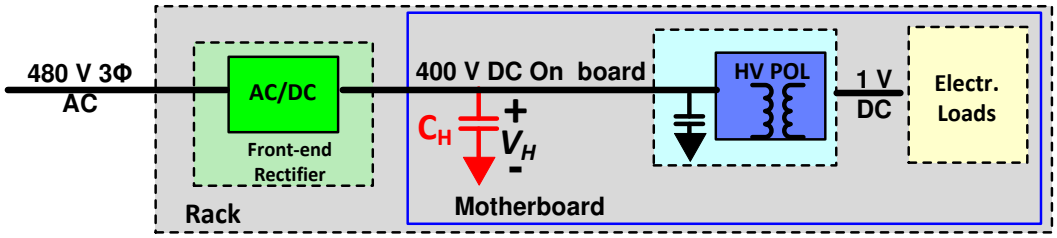


Figure 4.1. Indication of hold up capacitor.

Figure 4.2 shows the voltage waveform of the energy-storage capacitor, where $V_{H,nm}$ is the normal voltage across the energy-storage capacitor, $V_{H,min}$ is the minimum allowable bus voltage for HVPOL and t_h is the required hold-up time.

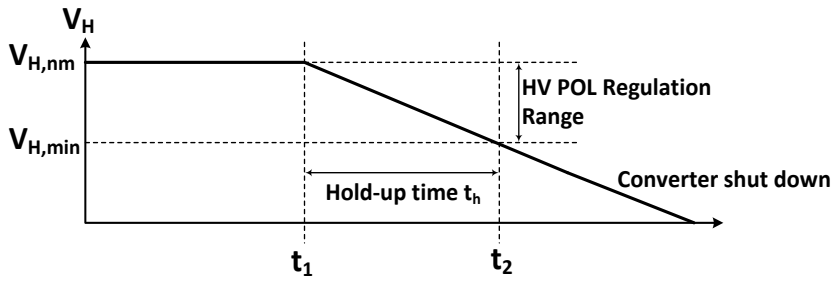


Figure 4.2. Voltage waveform of hold-up capacitor.

The relationship between the minimum voltage $V_{H,min}$ and the value of the energy-storage capacitor C_H can be derived and expressed in (4-1), where P_{out} and η_{HVPOL} is the output power and efficiency of the HVPOL converter. The value of C_H is positively related to the minimum allowable voltage $V_{H,min}$, which means for a lower $V_{H,min}$, smaller C_H can be used. This energy-storage capacitor is usually bulky; therefore, with a smaller $V_{H,min,}$ the power density of the system can be increased by using smaller $C_{H.}$

$$C_H = \frac{2t_H}{\eta_{HVPOL}(V_{H,nm}^2 - V_{H,min}^2)} \tag{4-1}$$

Figure 4.3 shows the utilization of the energy storage capacitance calculated as (4-2) with respect to the ratio of the $V_{H,min}$ and $V_{H,nm}$. Usually, $V_{H,min}$ is selected as 80%-90% of the normal operation voltage $V_{H,nm,}$ which means only a small percentage of energy stored in C_H is used during the hold-up time [71]. To increase the utilization and reduce the weight and volume of C_H, $V_{H,min}$ is selected as half (200 V) of the normal operation voltage, which is 400 V in the HVPOL. Therefore, a smaller hold up capacitor with more energy being utilized can be used compared to the capacitor designed with 80% voltage up voltage which is widely used today [71]. Therefore, the transformer is designed with 200 V input voltage and 33 A output current.

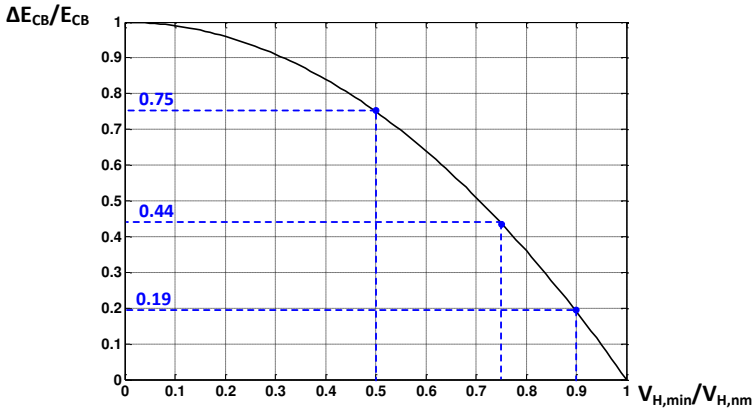


Figure 4.3. Normalized delivered energy from hold up capacitor during hold-up time as a function of hold-up voltage.

$$\frac{\Delta E_{CB}}{E_{CB}} = 1 - \left(\frac{V_{H,min}}{V_{H,nm}}\right)^2 \tag{4-2}$$

For the phase shift full bridge converter, duty cycle loss is induced into the circuit because of the leakage inductance from the transformer as shown in Figure 4.4. The effective duty cycle of the converter seen from output to input side can be expressed as in (4-3), and the duty cycle loss linearly increases with the leakage inductance. Therefore, the relationship between maximum turns ratio and the leakage inductance is derived in (4-4), and the corresponding values are plotted in Figure 4.4. With a larger leakage inductance, the transformer is required to have a lower turns ratio to make up the duty cycle loss of leakage inductance.

$$D_{eff} = D_{max} - D_{loss} = D_{max} - \frac{4L_{leak}f_s I_{out}}{nV_{in,min}} \tag{4-3}$$

$$n = 0.5 \times \left[\frac{V_{in,min}D_{max}}{V_{out}} + \sqrt{\left(\frac{V_{in,min}D_{max}}{V_{out}}\right)^2 + 4L_{leak}f_s I_{out}}\right] \tag{4-4}$$

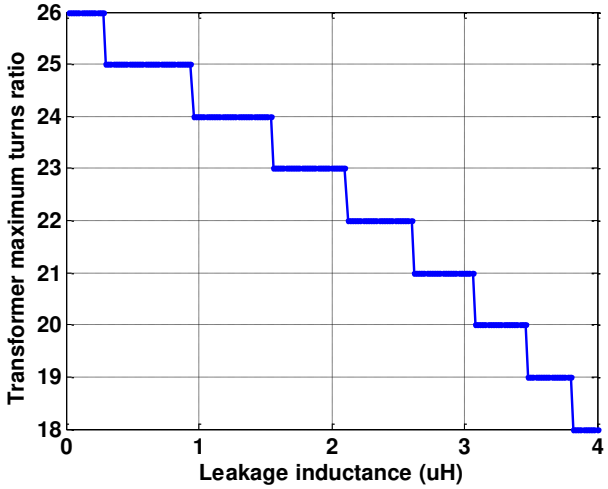


Figure 4.4. Relationship between leakage inductance and transformer turns ratio.

The turns ratio of the transformer is selected to be 24:1 because the targeted leakage inductance from the transformer is lower than 1.5 μH.

4.1.2 Transformer core selection

To maintain a less than 25 ℃ temperature rise of the transformer, a total 12 layers of PCB (4 layers for primary side and 8 layers for secondary side) is selected be used to fulfill to 24:1 turns ratio with center tapped secondary side winding. Therefore, the minimum height of the core should be greater than 100 mil. However, the commercially available planar cores do not meet the requirement. Therefore, to solve the problem, two cores are selected with primary side series and secondary side parallel structure as shown in Figure 4.5. The effective area of the core is calculated as (4-5). Two planar cores E/PLT core E 14/3.5/5 and PLT 14/5/1.5 is selected. After primary side series and secondary side parallel connection, the window is large enough to fit the transformer PCB windings.

$$A_C \geq \frac{DV_{in}}{2nB_{max}f_s} \tag{4-5}$$

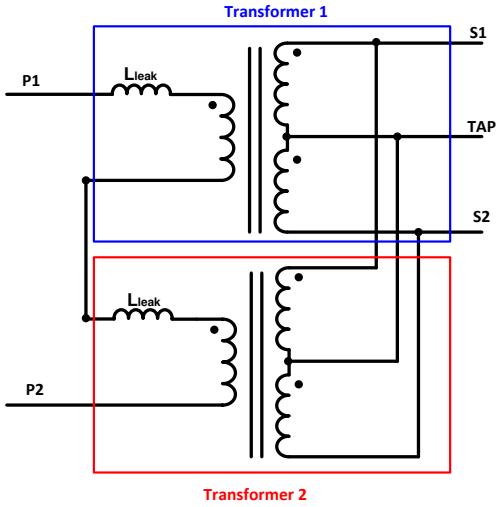


Figure 4.5. ISOP connected transformer.

As the voltage across the transformer is not sinusoidal, therefore, the Steinmetz equation cannot be directly applied, a modification from [65] is used to calculate the core loss of the transformer as in (4-6).

$$P_{core} = 2^{2\alpha-1} \cdot K \cdot f_{sw}^{\alpha} \cdot B_{sqm}^{\beta} \cdot D^{\beta-\alpha+1} \cdot V_{core} \ \ (mW/cm^3) \tag{4-6}$$

where α, β, and K are the parameters of the core based on Steinmetz equation and are usually provided by core vendors, and B_{sqm} is the peak to peak flux density when the converter's duty cycle is 0.5 ($B_{sqm} = \frac{V_{in}T_s}{4nA_e}$) with A_e being effective area of the core.

4.1.3 Transformer winding structure

Two parameters are essential for transformer design: (1) AC winding resistance which determines the winding loss, and (2) leakage inductance which greatly impacts the soft switching performance of primary side devices. Three different transformer structures are designed and evaluated in terms of AC winding resistance and leakage inductance in the following section.

(1) AC resistance

Because of eddy current effect, winding losses of the transformer increase significantly with the current frequency. The eddy current effect mainly includes skin effect and proximity effect, which will be discussed here. The ratio of AC resistance to DC resistance under sinusoidal excitation can be expressed as (4-7) [65][66], where $\xi = h/\delta$, h is the thickness of the copper, and δ is the skin depth of the conductor.

$$\frac{R_{AC}}{R_{DC}} = \frac{\xi}{2} \frac{sinh\xi + sin\xi}{cosh\xi - cos\xi} \tag{4-7}$$

Considering Dowell's assumption, the AC resistance of the *m-th* layer in the transformer can be expressed as (4-8) [65][66].

$$\frac{R_{AC,m}}{R_{DC,m}} = \frac{\xi}{2} \left[\frac{sinh\xi + sin\xi}{cosh\xi - cos\xi} + (2m-1)^2 \frac{sinh\xi - sin\xi}{cosh\xi + cos\xi} \right] \tag{4-8}$$

where m can be calculated as a ratio in (4-9)

$$m = \frac{F(h)}{F(h)-F(0)} \tag{4-9}$$

where *F(h)* and *F(0)*are the magnetomotive force (MMF) at the limits of a layer which will be illustrated later in this section.

Based on this analysis, the minimum AC can be calculated for different values of *m* and plotted in Figure 4.6. It is clearly shown that the AC resistance increases dramatically with the increased *m*.

However, the current through transformer primary winding of the PSFB converter is not sinusoidal, which means high frequency harmonics exist. As the eddy effect is strongly related to current frequency, resistance under each frequency needs to be calculated separately. The overall transformer winding loss will be the sum of winding loss under each frequency as in (4-10). Based on this, the equivalent AC resistance can be derived in (4-11), which is the effective resistance seen at the terminal of the transformer.

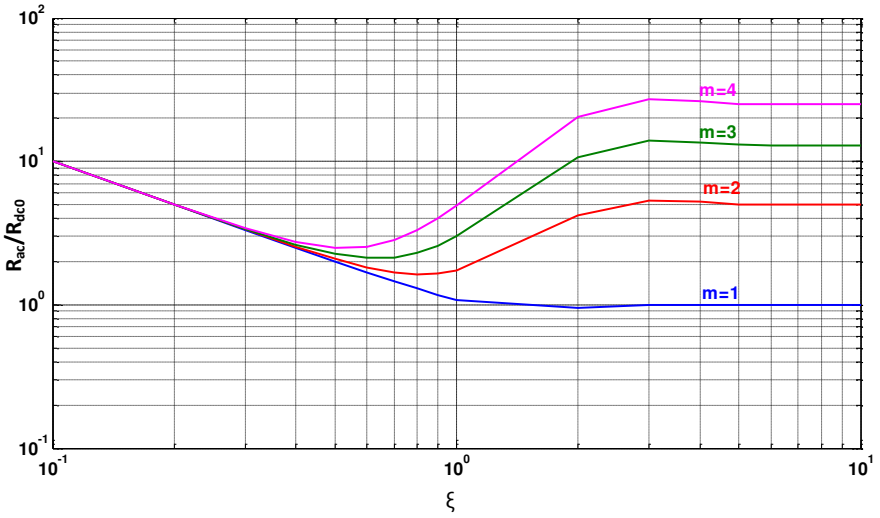


Figure 4.6. AC resistance relative to DC resistance in a layers with ξ=1.

$$P_{winding} = I_{RMS}^2 R_{eq} = \left(I_1^2 + I_3^2 + I_5^2 + \cdots + I_{2n-1}^2\right) * R_{eff} = \left(I_1^2 R_1 + I_3^2 R_3 + I_5^2 R_5 + \cdots + I_{2n-1}^2 R_{2n-1}\right) \quad (4\text{-}10)$$

$$R_{eq} = \frac{\left(I_1^2 R_1 + I_3^2 R_3 + I_5^2 R_5 + \cdots + I_{2n-1}^2 R_{2n-1}\right)}{I_{RMS}^2} \quad (4\text{-}11)$$

(2) Leakage inductance

Because of the imperfectness of coupling between primary and secondary side winding, leakage inductance does exist in every transformer design, and it is inevitable. However, in phase shift full bridge converter, this leakage inductance is a desired feature, as the energy stored in the leakage inductance will discharge the primary side device before it receives gate turn on signal, thus zero voltage switching (ZVS) can be achieved.

The leakage inductance can be calculated and estimated by the energy stored in it, which can be expressed as (4-12).

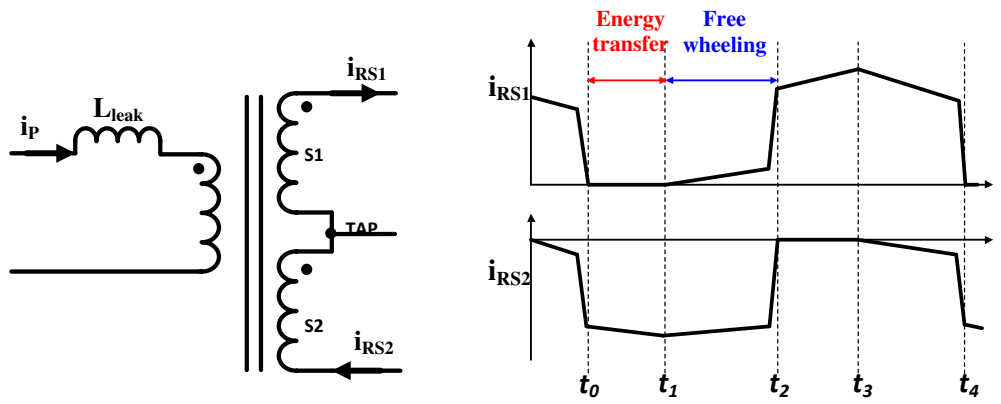
$$E_{lk} = \frac{\mu_0}{2} \sum \int_0^h H^2 \, l_w b_w dx = \frac{1}{2} L_{lk} I^2 \quad (4\text{-}12)$$

where l_w is the length of each turn, b_w is the width of each turn, and h is the thickness of each layer. The field strength H is related to the number of ampere turns with the flux path [65][66].

With the method of calculating AC resistance and leakage inductance introduced above, different winding structures can be evaluated in terms of AC winding resistance and leakage inductance.

(3) Winding structure comparison

The center tapped transformer with two secondary side windings is used in the phase shift full bridge converter, based on the operating principle of a phase shift full bridge converter, the two secondary side windings do not conduct current at the same time. During energy transfer period, only one of the secondary side windings is conducting. During the freewheeling period, both secondary side windings are conducting as shown in Figure 4.7.



(a) current direction (b) current waveforms

Figure 4.7. Secondary side current of center tapped transformer in a phase shift full bridge converter.

To simplify the following AC resistance calculation, an assumption has been made that is during the freewheeling period, only one set of secondary side transformer windings is conducting which is a common assumption for the analysis of phase shift full bridge converter with synchronous rectification [67][68]. Based on this assumption, the calculation for transformer AC resistance can be greatly simplified. Figure 4.8 is the secondary side current distribution assuming at a given time, only one set of secondary side winding is conducting and also square current waveform is assumed here. In the analysis, DC distribution is omitted as it does not impact the MMF of the transformer and will be considered as DC losses alone [69].

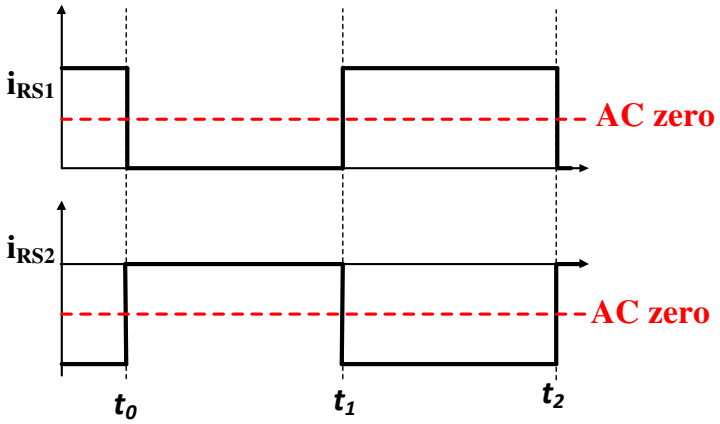


Figure 4.8. AC current of secondary side winding in PSFB converter.

Three different transformer winding structures for the center tapped transformer will be evaluated in the following sections in terms of AC resistance and leakage inductance.

a. Interleaved structure:

Figure 4.9 shows the structure of interleaved winding together with the magnetomotive force (MMF) of all the layers including conduction layers and insulator layers, the leakage inductance would be the same as in (4-13).

$$E_{lk} = \frac{\mu_0}{2} l_w b_w [2 \int_0^{h_P} \left(\frac{\frac{1}{2}I}{b_w} \frac{x}{h_P} \right)^2 dx + 4 \int_0^{h_S} \left(\frac{\frac{1}{2}I}{b_w} \frac{x}{h_S} \right)^2 dx + 4 \left(\frac{\frac{1}{2}I}{b_w} \right)^2 (h_\Delta)] \qquad (4\text{-}13)$$

where h_p, h_s and h_Δ is the thickness of primary side winding, secondary side winding, and insulation layer, respectively.

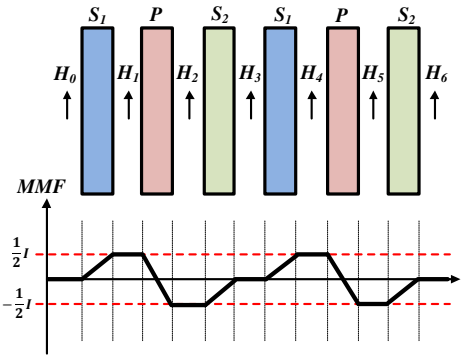


Figure 4.9. Interleaved winding structure.

b. Non-Interleaved structure:

Figure 4.10 shows the structure of the non-interleaved winding together with the MMF of all the layers including conduction layers and insulator layers. (4-14) calculates the leakage inductance.

$$E_{lk} = \frac{\mu_0}{2} l_w b_w [4 \int_0^{h_s} \left(\frac{\frac{1}{2}I}{b_w} \frac{x}{h_P}\right)^2 dx + 2 \int_0^{h_P} \left(\frac{I}{b_w} \frac{x}{h_P}\right)^2 + \left(\frac{I}{b_w}\right)^2 (h_\Delta) + \left(\frac{\frac{1}{2}I}{b_w}\right)^2 (h_\Delta) + 2\left(\frac{I}{b_w}\right)^2 (h_\Delta) + \left(\frac{\frac{3}{2}I}{b_w}\right)^2 (h_\Delta) +$$

$$\left(\frac{2I}{b_w}\right)^2 (h_\Delta) + \left(\frac{\frac{1}{2}I}{b_w}\right)^2 (h_S) + \left(\frac{I}{b_w}\right)^2 (h_S) + \left(\frac{\frac{3}{2}I}{b_w}\right)^2 (h_S) + \left(\frac{I}{b_w}\right)^2 (h_p)] \quad (4\text{-}14)$$

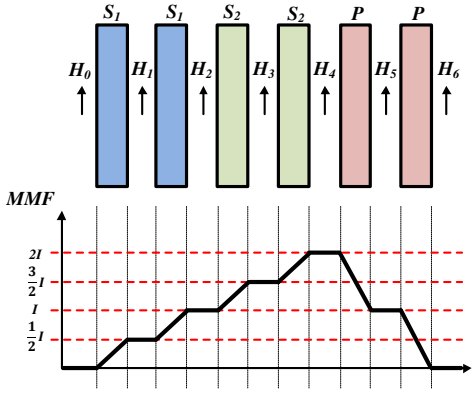


Figure 4.10. Non-interleaved winding structure.

c. Half-Interleaved structure:

Figure 4.11 shows the structure of the half-interleaved winding together with the MMF of all the layers including conduction layers and insulator layers. The leakage inductance can be calculated in (4-16).

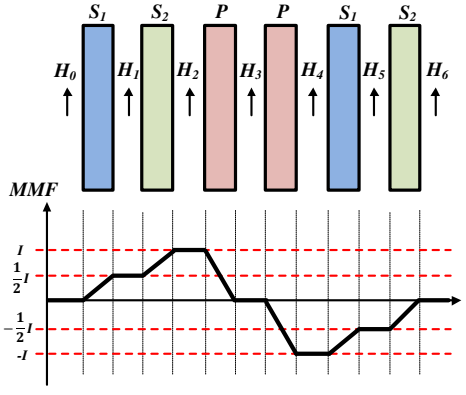


Figure 4.11. Half-interleaved winding structure.

$$E_{lk} = \frac{\mu_0}{2} l_w b_w [4 \int_0^{h_s} \left(\frac{\frac{1}{2}I}{b_w} \frac{x}{h_P}\right)^2 dx + 2 \int_0^{h_P} \left(\frac{I}{b_w} \frac{x}{h_P}\right)^2 + 2\left(\frac{I}{b_w}\right)^2 (h_\Delta) + 2\left(\frac{\frac{1}{2}I}{b_w}\right)^2 (h_\Delta) + \left(\frac{2I}{b_w}\right)^2 (h_\Delta) + 2\left(\frac{\frac{1}{2}I}{b_w}\right)^2 (h_S)]$$

(4-16)

The comparison of leakage inductance and AC resistance among the above three winding structures is summarized in Table 4.2.

Table 4.2. Transformer AC resistance and leakage inductance comparison among different structures.

Winding Design	Interleaved	Non-Interleaved	Half -Interleaved
$R_{ac,P}$ (mΩ)	376	672	398
$R_{ac,S}$ (mΩ)	0.51	0.81	0.59
L_{lk} (nH)	405	1866	748

After comparison, transformer winding structure 3, the half interleaved structure is selected here as it has similar resistance and higher leakage inductance compared with the interleaved structure and also much lower AC resistance compared with the non-interleaved case.

(4) Measurement and experimental verification

Both the leakage inductance and the equivalent AC winding resistance can be verified by measurement or by testing waveforms.

a. Leakage inductance measurement

Both interleaved and half interleaved transformers are built in prototype and their inductances have been measured separately using an impedance analyzer. Table 4.3 shows the measured leakage inductance for both of the two structures in comparison with the calculated results. The leakage inductance is measured at 280 kHz excitation frequency. The measurement

verifies that the half interleaved transformer has over 50 % higher leakage inductance, which is similar to the trend in calculation.

Table 4.3. Leakage inductance comparison between calculation and measurement.

Winding Design	Interleaved	Half - Interleaved
L_{lk} (nH) in calculation	405	748
L_{lk} (nH) in measurement	440	732

b. Equivalent AC resistance verification

Unlike the leakage inductance, which is not very sensitive to frequency, the equivalent AC resistance is the sum of AC resistance under different harmonic frequencies; therefore, it is not feasible and accurate to measure it directly using an impedance analyzer with a fixed frequency. However, based on the operational principle of PSFB converter, it is possible to calculate the AC resistance from transformer through freewheeling interval. During this interval, Q_2 and Q_4 or Q_1 and Q_3 are conducting, with the transformer being shorted; the equivalent circuit is shown in Figure 4.12.

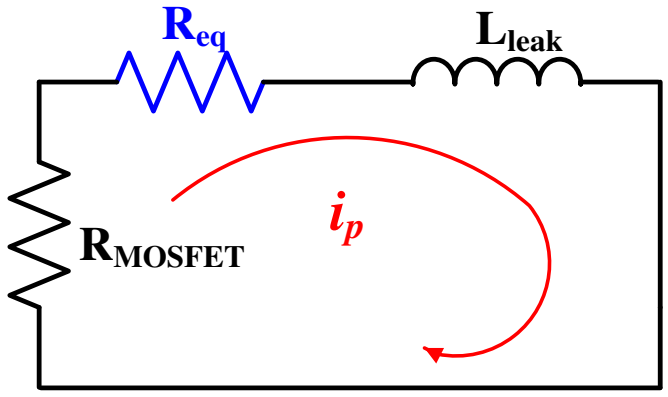


Figure 4.12. Equivalent circuit used to calculate R_{eq}.

As illustrated in Figure 4.12, it is a *RL* circuit, with the value of leakage inductance and device $R_{ds(on)}$ available in hand, it is fairly easy to calculate the equivalent AC winding resistance as expressed in (4-17). The leakage inductance used in (4-17) is larger than the value measured directly with the impedance analyzer with consideration of stray inductance on the printed circuit board and even the package inductance of secondary side devices [70]. The L_{leak} is 1.146 μH with consideration of the stray inductance on the printed circuit board under testing.

$$R_{eq} = \frac{-\ln\left(\frac{I_p(t_3)}{I_p(t_2)}\right)L_{leak}}{(t_3 - t_2)} - 2R_{MOSFET} \tag{4-17}$$

where $I_p(t_2)$ is the inductor current value at the beginning of the freewheeling period, $I_p(t_3)$ is the inductor current value at the end of the freewheeling period, (t_3-t_2) is the duration of freewheeling period, and R_{MOSFET} is the lumped resistance of all conducting MOSFETs during the freewheeling period, including both primary devices' resistance and secondary devices' resistance reflected to the primary side.

Figure 4.13 and Figure 4.14 are the experimental waveforms to verify the AC winding resistance for two different primary side devices. Two PSFB converter prototypes are built with different primary side devices and all other components including the transformer are the same. The on-state resistance of the primary MOSFETs is 110 mΩ in converter number 1 and 5.6 mΩ in converter 2. Based on (4-18), the AC resistance of the transformer for converter with different primary side device is 0.619 Ω.

The calculated AC resistance reflected to the primary side when both S_1 and S_2 are *ON* in Table 4.3 is 0.552 Ω, which means the error is around 10 %. There are several reasons for this difference in measurement and calculation:

i. The resistance from the board and connecting wires also add to the primary side loop which is not considered in (4-17) and should be subtracted from the equivalent AC resistance.

ii. The AC current in testing has some oscillation which induces high frequency harmonics into the current. The AC resistance is strongly positively dependent on the percentage of high frequency components in the current; therefore, the resistances calculated from the testing waveforms are higher than the calculated resistance.

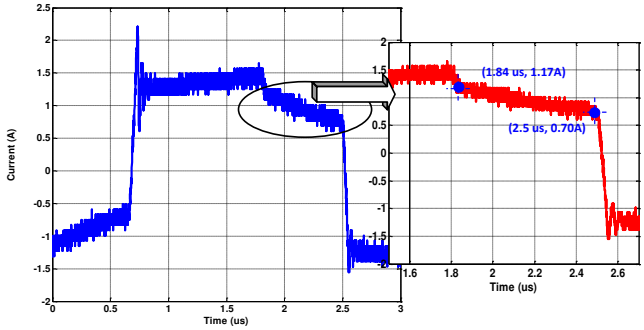


Figure 4.13. AC winding resistance verification of primary device #1 ($R_{ds(on)}$=*110 m*Ω).

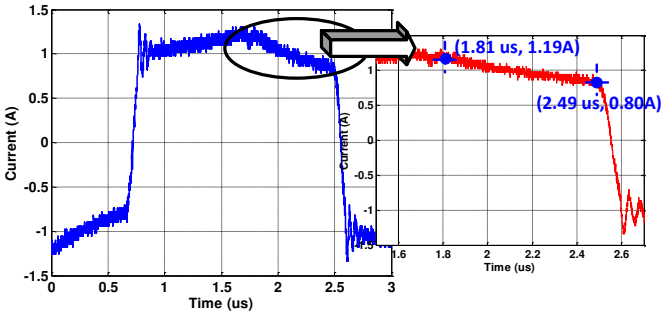


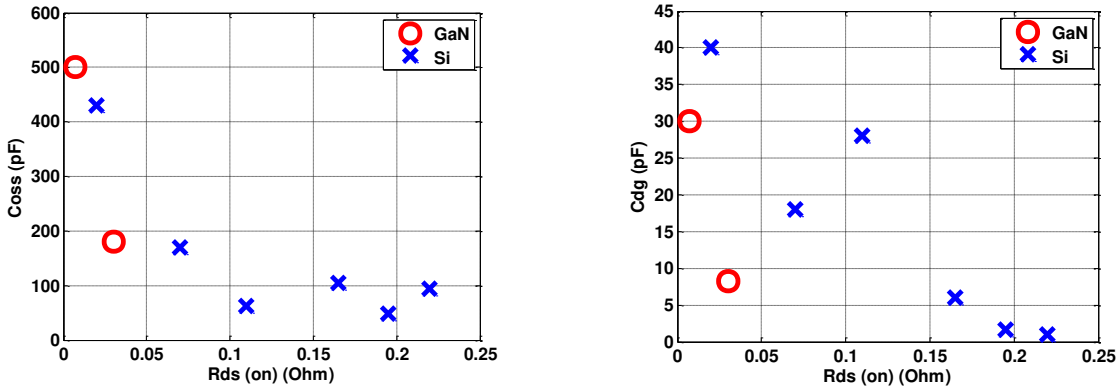
Figure 4.14. AC winding resistance verification of primary device #2 ($R_{ds(on)}$=*5.6m*Ω).

4.2 Primary side device selection

In this section, the selection of primary side MOSFET is discussed in detail based on a detailed analysis on converter's operational principles.

4.2.1 Device figure of merit comparison

Based on device figure of merit (FOM) discussed in Chapter 2, both hard and soft switching FOM has been calculated and plotted in Figure 4.15 with six Si MOSFETs and two GaN FETs rated at 100 V. The devices which are closer to the origin have a lower FOM which means a lower loss under the same operation conditions. GaN devices have lower FOM for both hard and soft switching condition compared with Si devices.



(a) Soft switching FOM (b) Hard switching FOM

Figure 4.15. FOM of 100 V MOSFETs.

To evaluate the theory, two different devices with similar Q_{gd} are selected, so that their switching losses under the same current and voltage condition are comparable with each other. Table 4.4 lists the specifications for the two selected devices, the GaN FET has lower $R_{ds(on)}$ but higher C_{oss}, and the Si MOSFET has higher $R_{ds(on)}$ but lower $C_{oss.}$

Table 4.4. Key parameters of two primary MOSFETs.

Device	$R_{ds(on)}$ (mΩ)	$C_{oss(energy)}$ (pF)	$C_{oss(charge)}$ (pF)	Q_{gd} (nC)
GaN	5.6	510.1	631.2	22
Si	110	29.4	47.5	20

4.2.2 Operation principle of PSFB converter considering output junction capacitance

To address the impact of the output junction capacitance, the basic theory of the phase shift full bridge converter will be discussed with emphasis of primary side MOSFETs' output junction capacitance's influence on the RMS current through both primary side and secondary side. Figure 4.16 is the operation waveform of the phase shift full bridge converter which can be divided into 12 intervals for each period. Because of symmetry, only t_0 though t_5 will be discussed here. Current values for primary and secondary side at each time are marked in Figure 4.16 [74].

a. Interval 1: t_0-t_1

During this time interval, energy is transferred from primary side to secondary side. The primary side current can be expressed as follows:

$$i_p(t) = I_{p0} + \frac{\left({}^{V_{in}}/_{n} - V_{out}\right)}{L_{out}}(t - t_0) \tag{4-18}$$

$$I_{p0} = \frac{1}{n}\left(I_{out\_t0} - \frac{{}^{1}/_{n}V_{in} - V_{out}}{L_{out}} D_{eff} T_s\right) \tag{4-19}$$

where I_{out_t0} is the output current value at time t_0. Based on the output current value, I_{out_t0} can be expressed as follows:

$$I_{out\_t0} = -\frac{(1-\frac{nV_{out}}{V_{in}})T_s}{2L_{out}} + \sqrt{I_{out}^2 - \frac{1}{12}\frac{V_{out}^2(1-\frac{nV_{out}}{V_{in}})^2 T_S^2}{L_{out}^2}} \tag{4-20}$$

$$D_{eff} = {}^{nV_{out}}/_{V_{in}} \tag{4-21}$$

b. Interval 2: t_1-t_2

During this time, the leading leg starts commutation (Q_4 turns off). The output junction capacitance has significant impact on the current waveform during this interval [74]. This

interval can be further divided into two sub intervals, and the primary side current can be calculated correspondingly.

i. v_{AB} reduces to zero $t \in t_1$-t_{1a}

During this time, the voltage across the transformer primary side winding reduces to zero. Because the output inductance L_{out} is involved, the current discharges Q_4 and charging Q_3 can be considered as constant. Therefore, the time for this interval can be calculated as $t_{1a} - t_1 = \frac{2C_P V_{in}}{I_1}$, where C_p is the charge equivalent capacitance of primary side MOSFETs.

$$i_p(t) = \frac{C'_{SR}}{2C_P + C'_{SR}} I_1 cos\omega_1 (t - t_1) + \frac{C'_{SR}}{2C_P + C'_{SR}} I_1 \tag{4-22}$$

$$v_{LM}(t) = V_{in} + \frac{1}{(2C_P + C'_{SR})\omega_1} I_1 cos\omega_1 (t - t_1) - \frac{1}{2C_P + C'_{SR}} I_1 (t - t_1) \tag{4-23}$$

$$\omega_1 = \sqrt{\frac{2C_P + C'_{SR}}{2C_P C'_{SR} L_K}} \tag{4-24}$$

$$L_K = L_{leak} + \frac{L_{lk\_SR}}{2} N^2 \tag{4-25}$$

$$C'_{SR} = \frac{4 * C_{SR}}{N^2} \tag{4-26}$$

In the equations, L_{leak} is the leakage inductance of the transformer on the primary side; L_{lk_SR} is the sum of the leakage inductance of the transformer on the SR side and the stray inductance of the SR devices. At the end of this interval, voltage across Q_3 is reduced to zero so it can be turned on under ZVS. There is still voltage across the magnetizing inductance L_m. For the secondary side, junction capacitance of SR_1 starts to be discharged and has not reached zero yet.

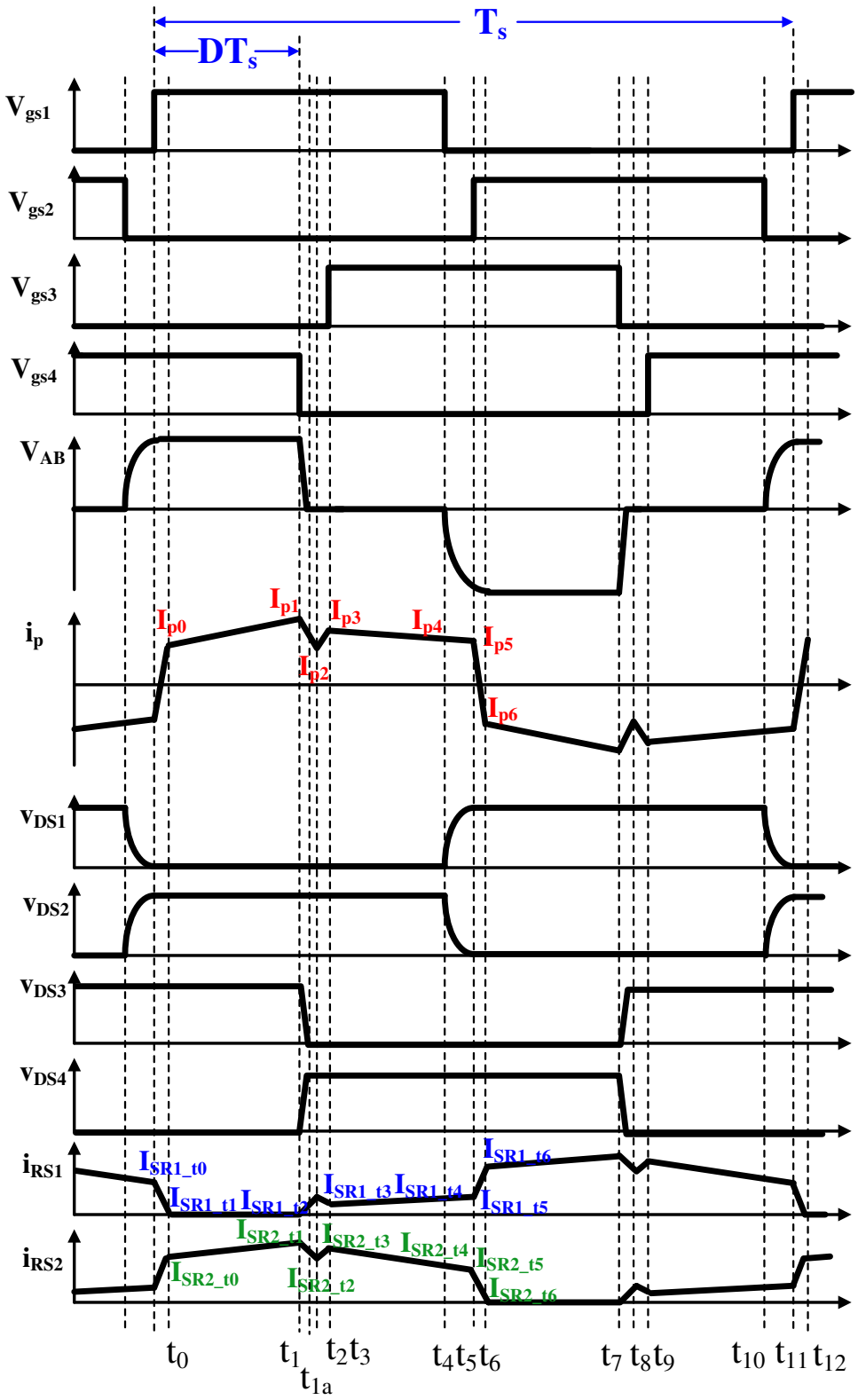


Figure 4.16. Operational waveforms of phase shift full bridge converter.

ii. v_{Lm} reduces to zero $t \in t_{1a}$-t_2

During this sub interval, voltage across L_m will be further reduced to reach zero and voltage across SR_1 will also reduce to zero [74].

$$i_p(t) = I_1 + \left(I_p(t_{1a}) - I_1\right)\cos\left(\omega_2(t - t_{1a})\right) - \frac{V_{Lm}(t_{1a})}{Z_2}\sin(\omega_2(t - t_{1a})) \tag{4-28}$$

$$\omega_2 = \frac{1}{\sqrt{L_K C'_{SR}}} \tag{4-29}$$

$$Z_2 = \sqrt{\frac{L_K}{C'_{SR}}} \tag{4-30}$$

$$t_{12} = arctan\left(\frac{V_{Lm}(t_{1a})}{(I_{p1} - I_p(t_{1a}))Z_2}\right)/\omega_2 \tag{4-31}$$

Since the time interval is short, therefore, the current during this interval is approximated as a linear function shown in (4-32) where $\Delta i_{P1} = I_{p2} - I_{p1}$ as shown in Figure 4.17.

$$i_p(t) = \frac{\Delta i_{P1}}{\Delta t_1}(t - t_1) + I_{p1} \tag{4-32}$$

Based on the analysis, Δi_{p1} is 0.43 A for Si (smaller C_{oss}) and 0.02 A for GaN (larger C_{oss}), which indicates a smaller output junction capacitance leads to a greater current reduction during leading leg commutation and a lower current value to begin freewheeling period.

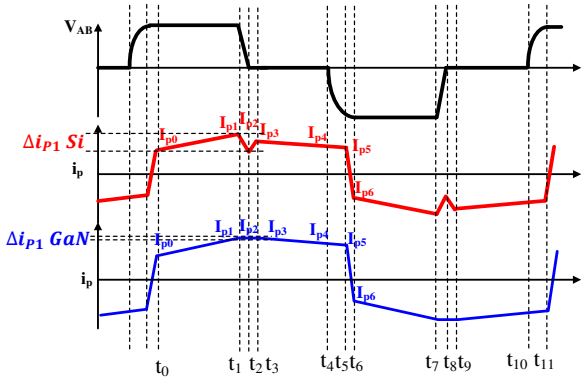


Figure 4.17. Current step down for both Si and GaN during interval 2.

c. Interval 3: t_2-t_3

If at time t_2, Q_3 and SR_1 are still in OFF state, then current flows through the body diode of Q_3 and SR_1. During this time interval, since body diodes of SR_1 and Q_3 conduct, a positive voltage is applied across L_{leak}, therefore, i_p starts to ramp up based on (4-33):

$$i_p(t) = \frac{v_{L_{leak}}}{L_{leak}}(t - t_2) + I_{p2} \tag{4-33}$$

The voltage across the leakage inductance (L_{leak}) can be expressed as (4-34), where V_{F_SR} is the forward voltage drop of the SRs' body diode and V_{F_P} is the forward voltage drop of the primary MOSFETs' body diode. The current during this time interval is expressed in (4-35).

$$V_{L_{leak}} = \frac{(nV_{F\_SR}+V_{F\_P})L_{leak}}{n^2\left(L_{lk_{SR1}}+L_{lk_{SR2}}\right)+L_{leak}} \tag{4-34}$$

$$i_p(t) = \frac{nV_{F\_SR}+V_{F\_P}}{(n^2\left(L_{lk_{SR1}}+L_{lk_{SR2}}\right)+L_{leak})}(t - t_2) + I_{p2} \tag{4-35}$$

d. Interval 4: t_3-t_4

This enters the freewheeling period of the phase shift full bridge converter. During this time interval, the transformer is shorted. On the primary side, the equivalent circuit is a RL circuit. The current i_p can be expressed as (4-36), where R_p is the lumped resistance on the primary side, which includes the MOSFETs on-state resistance $R_{ds(on)}$ and transformer winding resistance $R_{winding}$.

$$i_p(t) = I_{p3}e^{-\frac{Rp}{Lleak}(t-t_3)} \tag{4-36}$$

e. Interval 5: t_4-t_5

At time t_4, Q_1 turns off. Current starts to charge Q_1 and discharge Q_2. Because both SR_1 and SR_2 are still conducting, there is no reflection of the output inductor from the secondary side to

the primary side. Resonance occurs between the leakage inductance and the two output capacitances of Q_1 and Q_2. i_p can be expressed as:

$$i_p(t) = I_{p4} cos\omega_3 (t - t_4) \tag{4-37}$$

$$\omega_3 = \frac{1}{\sqrt{2L_{leak}C_P}} \tag{4-38}$$

Therefore, it can be seen that for the lagging leg, the energy required is purely provided by the leakage inductance and strongly dependent on the current value at t_4 (I_{p4}). The dead time required is a quarter of the resonant period as:

$$t_{d\_l} = \frac{2\pi\sqrt{2L_{leak}C_P}}{4} \tag{4-39}$$

The requirement of soft switching for the lagging leg switches can be expressed as:

$$\frac{1}{2} L_{leak} I_{P4}^2 \geq C_P V_{in}^2 \tag{4-40}$$

f. Interval 6: t_5-t_6

At time t_5, voltage across Q_1 is charged to V_{in} and Q_2 is discharge to zero. If Q_2 is turned on after t_5, it is turned on under ZVS condition. The current on primary side during this time can be expressed as:

$$i_p(t) = I_{p5} - \frac{V_{DC}}{L_K}(t - t_5) \tag{4-41}$$

The current value at the end of this period is the same as I_{p0}.

Based on the above analysis, the current RMS value of the primary side winding for 33 A output current is 1.11 A for Si and 1.36 A for GaN; this difference is mainly caused by current step-down difference during interval 2 as shown in Figure 4.16 where the freewheeling current

(from I_{p3} to I_{p4}) is smaller for Si than GaN. This indicates that a smaller output junction helps to reduce the freewheeling current naturally, which is desirable.

4.2.3 Primary side device loss analysis

For primary side devices, the losses include conduction loss, switching losses including turn off loss and turn on loss when soft switching is lost, and gate driving loss. These three losses will be discussed in the following sub-section.

(1) Switching loss

The output inductor is involved in the leading leg commutation, therefore, leading leg (Q_3 and Q_4) can achieve zero turn on through almost the entire load range. Turn off loss is simulated in Saber with two customized models based on data sheet specifications.

For the lagging leg, when (4-40) cannot be satisfied, the MOSFETs enter partial soft switching region as shown in Figure 4.18. The left voltage across the MOSFET ($V_{dsp,sw}$ in Figure 4.18) will be hard switched.

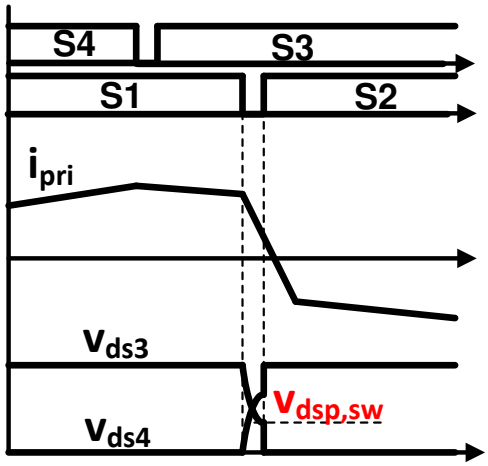


Figure 4.18. Partial soft switching of primary MOSFETs.

The switching loss can be calculated in (4-42).

$$P_{pri\_sw} = 2V_{dsp,SW}I_{p5}t_{on}f_s + 2V_{ds}I_{p5}t_{off1}f_s + 2V_{ds}I_{p2}t_{off2}f_s \tag{4-42}$$

where t_{on} is the turn on time of partial hard switched lagging leg MOSFETs and t_{off1} and t_{off2} is the turn off time for lagging and leading leg MOSFETs, respectively.

(2) Conduction loss

Based on the operation analysis in Section 4.2.2, the current RMS value on primary side can be expressed as (4-43), therefore, the conduction loss can be calculated in (4-44).

$$I_{pri_{RMS}} = \sqrt{\frac{1}{2T_S}\int_0^{T_S/2}\left(i_p(t_0) + \frac{(i_p(t_1) - i_p(t_0))t}{DT_S}\right)^2 dt} + \sqrt{\frac{1}{2T_S}\int_0^{T_S/2}\left(i_p(t_3) + \frac{(i_p(t_4) - i_p(t_3))t}{(1-2D)T_S}\right)^2 dt}$$

$$= \sqrt{2D}\sqrt{\frac{1}{3}(I_{P0}^2 + I_{P0}I_{P1} + I_{P1}^2)} + \sqrt{1-2D}\sqrt{\frac{1}{3}(I_{P3}^2 + I_{P3}I_{P4} + I_{P4}^2)} \tag{4-43}$$

$$P_{pri\_cond} = 4I_{pri\_RMS}^2 R_{pri} \tag{4-44}$$

(3) Gate driving losses

The gate driving loss of primary MOSFETs can be described as:

$$P_{pri\_g} = 4Q_{g\_pri}f_s \tag{4-45}$$

where Q_{g_pri} is the gate charge of primary side MOSFETs.

Therefore, the overall primary side MOSFETs losses are:

$$P_{pri} = P_{pri\_cond} + P_{pri\_sw} + P_{pri\_g} \tag{4-46}$$

4.3 Secondary side device selection

Based on waveforms shown in Figure 4.14, SR devices have the same soft switching region as the leading leg devices; therefore, turn on loss can be ignored. In the meantime, SR

MOSFETs are turned off with zero current condition; therefore, turn off loss can also be ignored. SRs MOSFETs' losses mainly include conduction loss and gate driving loss, which can be calculated as follows:

$$P_{SR\_cond} = \sqrt{2} n I_{pri\_RMS} R_{ds\_sr} \tag{4-48}$$

$$P_{SR\_g} = 2 Q_{g\_SR} f_s \tag{4-49}$$

$$P_{SR} = P_{SR\_cond} + P_{g\_SR} \tag{4-50}$$

4.4 Output inductor selection

The current ripple on the output inductor can be expressed as (4-51).

$$\Delta I_{L_{out}} = \frac{\left(\frac{V_{in}}{n} - V_{out}\right)}{L_{out}} D T_s \tag{4-51}$$

Since the system is being interleave controlled, therefore, the overall current ripple can be cancelled with each other as shown in Figure 3.11.

Each full bridge converter can be considered as two interleaved buck converter. With six full bridge converters interleaved, it is equivalent to a 12 phase interleaved buck converter. As ripple current can be cancelled greatly with 12 phases, a lower value of output inductance can be selected. If the converter is designed to operate under continuous conduction mode (CCM) when the load current is greater than 5 A, the output inductance is around 230 nH. Therefore, inductor model 1170-231 with a DC resistance of 0.25 mΩ from Coilcraft is selected.

The inductor loss of the output inductor can be calculated as (4-51) where core loss is obtained from the manufacturer's website.

$$P_L = P_{DCR} + P_{core} = I_{out} \sqrt{1 + \frac{1}{12} \left(\frac{\Delta i_L}{I_{out}}\right)^2 R_{L\_DCR}} + P_{core} \tag{4-51}$$

With major losses including MOSFETs' loss, transformer loss, inductor loss and capacitor ESR losses calculated, the efficiency is obtained and plotted in Figure 4.19.

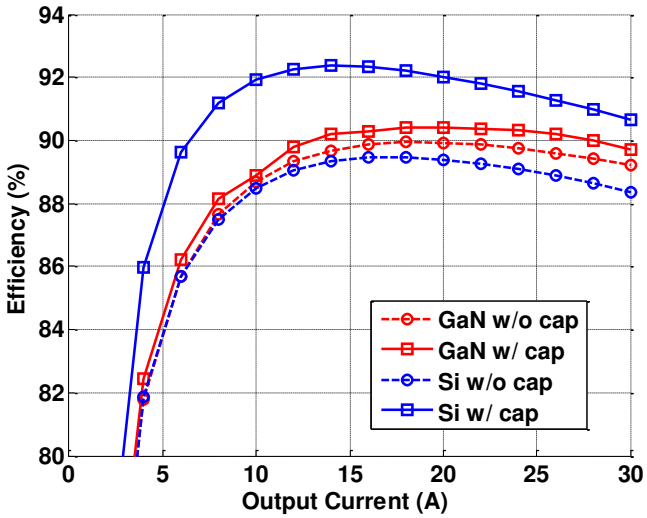


Figure 4.19. Estimated PSFB converter efficiency with Si and GaN devices.

It can be seen that GaN offers higher efficiency compared with the Si MOSFET since RMS value of the current is the same and GaN has a much lower R_{dson} without considering the current drop caused by C_{oss}. However, when considering the output junction capacitance, the reduction of the RMS current though devices and transformer makes the Si converter more efficient than the GaN converter, even though GaN has lower R_{dson} and comparable switching loss. Therefore, it is necessary to consider the impact of output junction capacitance when selecting devices as it not only affect the resonant intervals' performance, but also current RMS value during the freewheeling period.

However, the selection of 100 V GaN FETs is limited compared with the number of available Si devices. Therefore, to have a fair comparison between the performance of Si and GaN FETs, an assumption of more voltage and current rating devices being available is assumed which means $R_{ds(on)}$, C_{oss}, C_{dg} and Q_g changes continually. Both the hard switching

FOM and soft switching FOM keeps unchanged for both Si and GaN cases. Full load efficiency is calculated with respect to the output junction capacitances for Si and GaN cases and is shown in Figure 4.20, which indicates GaN FETs offer higher efficiency over a wide range of output junction capacitances. The two available GaN FETs and the selected Si devices are marked in Figure 4.21 as well.

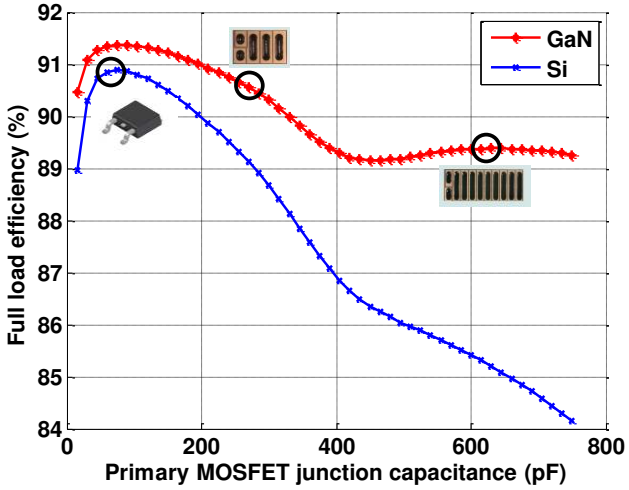


Figure 4.20. Estimated PSFB converter full load efficiency with respect to output junction capacitance.

4.5 Experimental verification

Prototypes of both Si and GaN based converters have been built. Figure 4.21 and Figure 4.22 are the experimental lagging leg waveforms for both Si and GaN based converter under full load which indicates that both devices are being partially hard switched.

Figure 4.23 shows comparison between Si and GaN converter's transformer current under the same loading condition. It clearly shows the current step down during the leading leg transient, which verifies the above analysis. However, by reducing the RMS current on the primary side, the current magnitude at the lagging leg transient is also reduced, which means

the energy stored in the leakage inductance ($\frac{1}{2}L_{leak}I_{P4}^2$ in Figure 4.23) in also reduced. Therefore, the soft switching capability is sacrificed.

Efficiency of both Si and GaN converter is also measured over a wide load range and is shown in Figure 4.24. It can be seen that the Si converter has a higher efficiency compared with the GaN converter even under heavy load, which is the same as estimated efficiency with consideration of output junction capacitance.

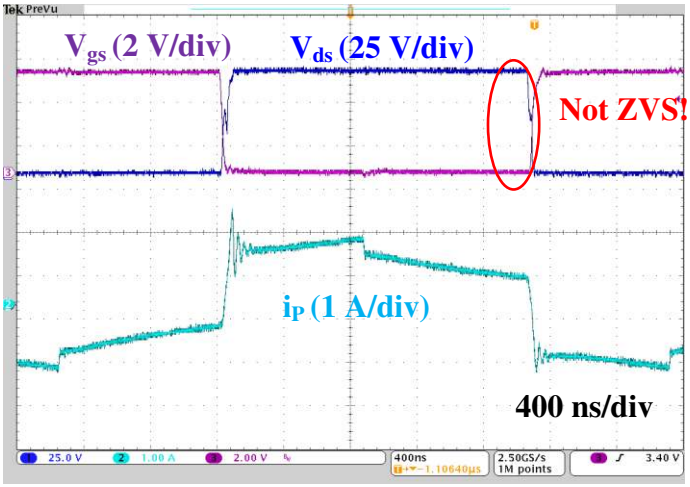


Figure 4.21. Testing lagging leg waveforms under full load for Si converter.

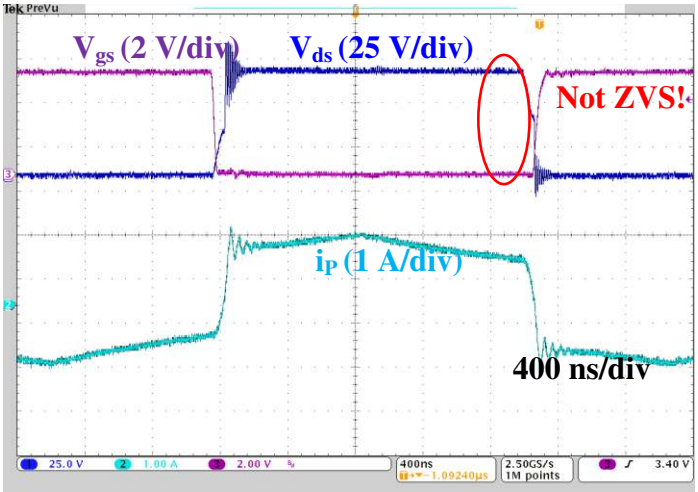


Figure 4.22. Testing transformer voltage and current waveforms under full load for GaN converter.

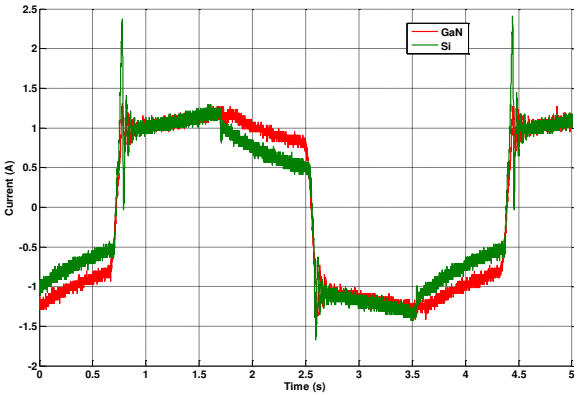


Figure 4.23. Transformer primary side current comparison between Si and GaN.

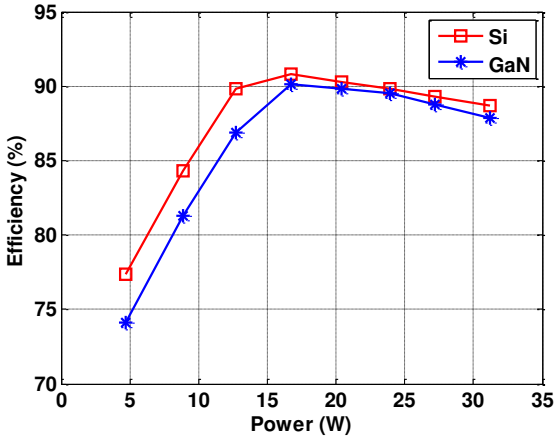


Figure 4.24. Measured efficiency of Si and GaN based converter.

4.6 Summary

In this chapter, the design of one phase shift full bridge (PSFB) DC/DC converter out of the six phases input series and output parallel (ISOP) connected system is performed.

First, the transformer of the PSFB is designed in terms of transformer turns ratio, core selection and winding structure design. The leakage inductance and AC resistance are either measured using an impedance analyzer or verified through testing waveforms to verify the calculation with consideration of high order harmonics in the current.

Then, by a detailed analysis of the PSFB operational principle, the significance of the output junction capacitance of primary side MOSFETs on the whole converter's efficiency is revealed. Two prototypes with significant different output junction capacitances are built and tested, which validated the impact of output junction capacitance on the converter's operation waveforms and efficiency. The experimental testing result shows that the designed converter can reach 89.1 % full load efficiency and 91.2 % peak efficiency.

5. Load Dependent Soft Switching Method for Half Bridge Current Doubler Converter in HV POL

As mentioned in Chapter 3, a half bridge current doubler converter (shown in Figure 5.1) is also being investigated here. In this chapter, first, two conventional control methods for half bridge current converter, symmetrical and asymmetrical control, are analyzed based on the application requirement. Symmetrical control offers higher efficiency compared with asymmetrical control; therefore, it is selected as the control method. Even though GaN FETs have the potential to improve the efficiency, Si MOSFETs are selected in the HV POL with half bridge current doubler so that any efficiency benefit would come from the proposed architecture rather than using better devices. Also, the cost of the HV POL is lower with Si compared with GaN FETs.

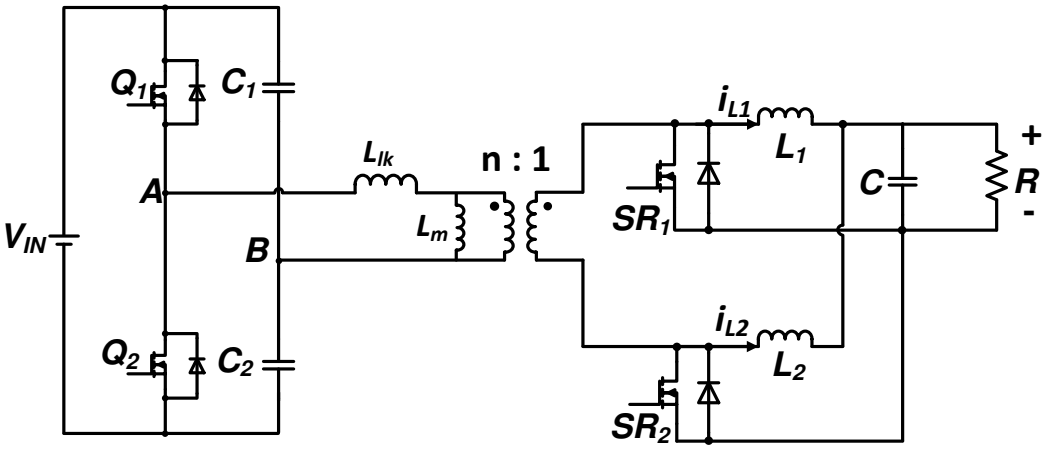


Figure 5.1. Half bridge with current doubler converter.

Yet, the major drawback of symmetrical control is the hard switching of the primary side devices. To further improve the efficiency, a novel control method is proposed so that the half bridge current doubler can achieve zero voltage turn on of primary MOSFETs for the entire

load range with the auxiliary components. The proposed method can adjust itself based on the loading condition of the converter automatically with commercial controller ICs. Experimental efficiency of a hardware prototype is provided to show that the proposed method can increase the converter's efficiency in both heavy and light load conditions.

5.1 Control of half bridge current doubler

5.1.1 Asymmetrical control

For a half bridge circuit, two types of control method are widely used. One is the asymmetrical control method as shown in Figure 5.2. In this case, Q_1 and Q_2 are controlled complementarily [75][76]. During the dead time between turning off SR devices and turning on primary devices, leakage inductance L_{lk} will charge and discharge the two junction capacitances of primary MOSFETs, therefore, zero voltage turn on can be achieved similar to the phase shift full bridge converter when the load is heavy and current in L_{lk} is large enough.

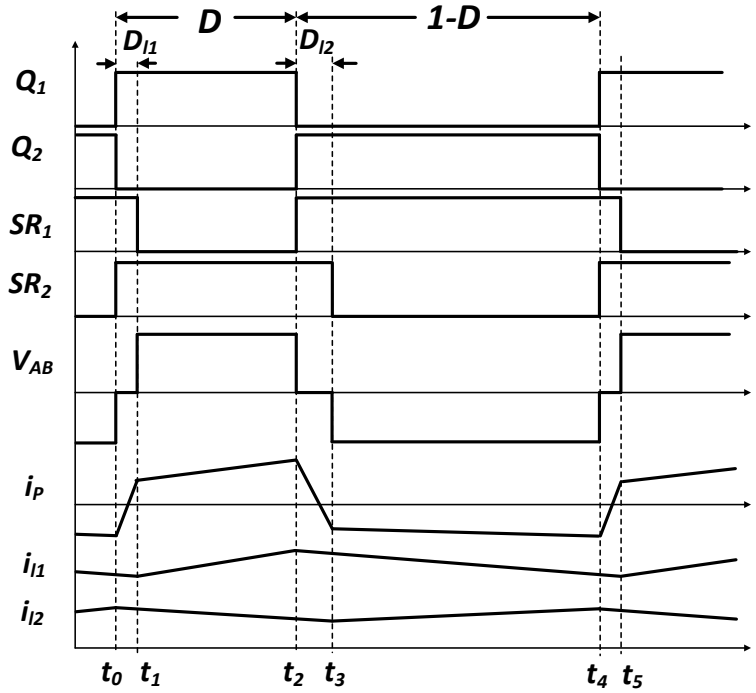


Figure 5.2. Operation waveform of asymmetrical control.

However, as indicated in Figure 5.2, L_{lk} will cause duty cycle loss (calculated in (5-1) and (5-2)) in the converter, further causing the RMS current in the transformer and devices to increase, which will reduce the benefit of saving switching losses. Also, asymmetrical control will stress the two primary side devices differently; one device (Q_1) will suffer both higher RMS current and being harder to achieve soft switching. Therefore, there will be a conflict of how large the leakage inductance should be: as increasing it, Q_1 will have more conducting loss, yet reducing it, soft switching might be lost even under full load.

$$D_{loss1} = \frac{I_O}{n}\frac{L_{lk}}{DV_{in}T_s} \tag{5-1}$$

$$D_{loss2} = \frac{I_O}{n}\frac{L_{lk}}{(1-D)V_{in}T_s} \tag{5-2}$$

$$V_{out} = \frac{(D-D_{loss1})(1-D-D_{loss2})V_{in}}{n} \tag{5-3}$$

5.1.2 Symmetrical control

Another control method widely used in half bridge converter is symmetrical control, where Q_1 and Q_2 are controlled with $\pi/2$ phase difference as shown in Figure 5.3 [77][78]. The half bridge converter now becomes an interleaved isolated buck converter with two sets of switches (Q_1/SR_1 and Q_2/SR_2).

The input and output voltage relationship is described in (5-4).

$$V_{out} = \frac{(D-D_{loss})V_{in}}{2n} \tag{5-4}$$

where D_{loss} can be calculated as in (5-5):

$$D_{loss} = \frac{I_O}{2n}\frac{L_{lk}}{DV_{in}T_s} \tag{5-5}$$

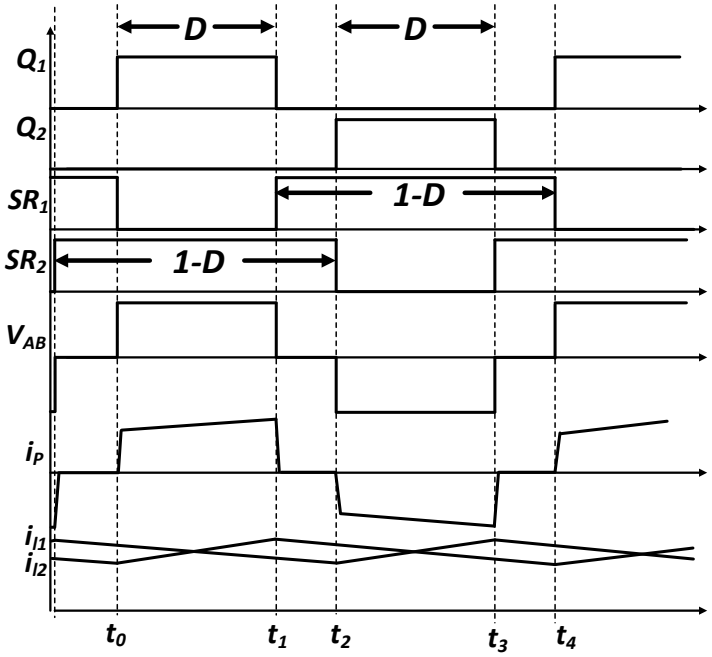


Figure 5.3. Operation waveforms of symmetrical control of converter.

When both of the primary MOSFETs are off, the output inductor currents (i_{L1} and i_{L2}) are freewheeling through the SR devices without flowing into the transformer, which reduces the winding loss of the transformer. The major drawback of the symmetrical controlled half bridge converter is that Q_1 and Q_2 are being hard switched for the entire load range. Unlike the asymmetrical controlled half bridge where leakage inductance helps to achieve soft switching, in symmetrical control, the leakage inductance causes oscillation with devices' output junction capacitances when both devices are off and cannot reduce switching losses; therefore, for symmetrical control, the smaller the leakage inductance is, the lower the losses are.

5.1.3 Comparison between two control methods

For both asymmetrical and symmetrical control methods, the current RMS value increases as the transformer leakage inductance increases as shown in Figure 5.4. For different leakage inductances, the symmetrical control always offers a lower RMS current, both in the transformer winding and devices.

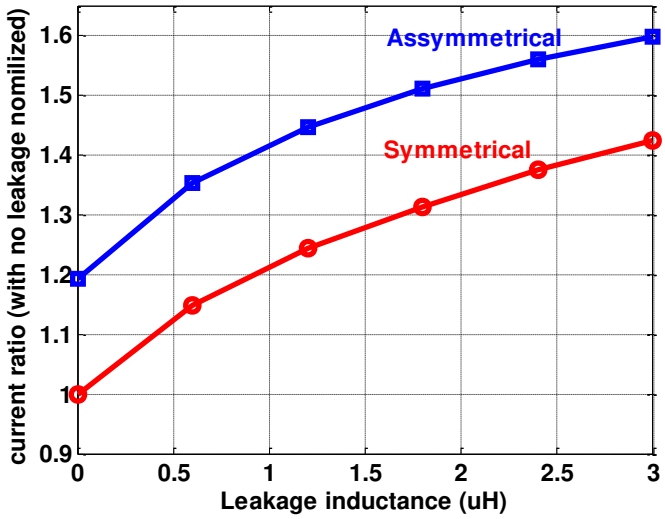


Figure 5.4. Transformer current comparison between asymmetrical and symmetrical control.

The converters' efficiency is further estimated for different leakage inductances with asymmetrical control and 0.1 μH leakage inductance for symmetrical controls. 500 nH output inductances and 6:1 turns ratio transformer is used for both control scheme. Based on analysis, symmetrical control provides higher efficiency compared with asymmetrical control. Therefore, symmetrical control is selected here for the following discussion.

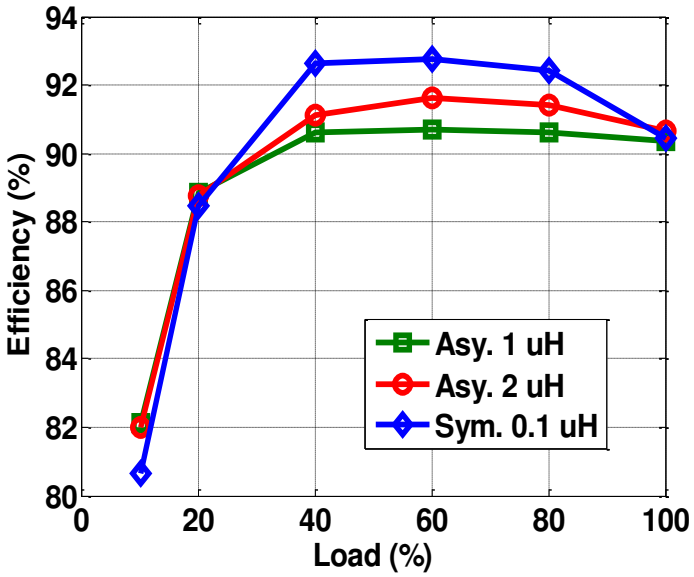


Figure 5.5. Efficiency comparison between asymmetrical and symmetrical control.

5.2 Operation principle of proposed zero voltage switching half bridge current doubler

Even though symmetrical controlled half bridge offers higher efficiency, in order to further improve the efficiency, a load dependent zero voltage switching (ZVS) method shown in Figure 5.6 has been proposed. Besides the power stage of a conventional half bridge current doubler, the proposed circuit also contains an auxiliary circuit, which includes series connected MOSFETs (S_a and S_b), a diode (D_a), and an inductor (L_a). The capacitances in parallel with the devices are the junction capacitances drawn explicitly and are not extra discrete components which will be used to explain how the proposed method works in the following sections.

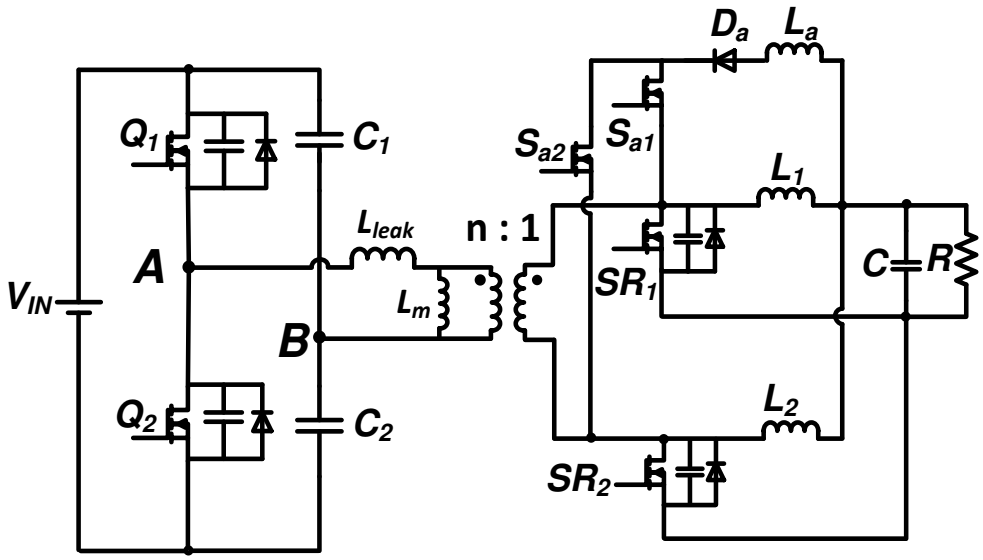


Figure 5.6. Proposed zero voltage switching circuit for half bridge current doubler.

Figure 5.7 illustrates the theoretical operation waveforms of the converter's major components. The operation of the load dependent soft switching half bridge current doubler can be divided into 12 intervals as t_0 through t_{11} in Figure 5.7. Because the half bridge converter is a symmetrical converter, only the first six intervals (t_0 through t_5) will be discussed here to indicate how the proposed method works. The magnetizing inductance L_m in the transformer as

shown in Figure 5.6 is designed to have a large value so that the magnetizing current in the transformer can be greatly reduced. Therefore, the magnetizing inductance and current is ignored from the following discussion to simplify the analysis.

The detailed operation principle will be discussed for each interval. Only the switching losses of MOSFETs in the converter are discussed, as the conduction losses and gate driving losses of the power stage MOSFETs are the same as conventional half bridge current doubler. The auxiliary components losses will be discussed in Section 5.3.

a. Interval 1: t_0 to t_1

Before t_0, two inductor currents i_{L1} and i_{L2} are freewheeling through SR_1 and SR_2 as in Figure 5.8. At time t_0, S_a is turned on, then a positive voltage is applied across L_a as indicated in Figure 5.9 and auxiliary current in the arrow direction shown in Figure 5.9 starts to build up. S_a is turned on with zero current switching (ZCS). Based on KCL, the sum of i_{SR1} and i_{Sa} is equal to the current i_{L1} at any given time; therefore, the current flowing through SR_1 is transferring to the auxiliary inductor L_a.

In order to achieve zero voltage switching of primary side devices and avoid reverse recovery loss of SRs' body diode, the current direction of i_{SR1} needs to be negative with respect to the current direction in Figure 5.9 when SR_1 is being turned off. The current flowing through the auxiliary inductor can be calculated as in (5-7), which clearly indicates the current in the auxiliary inductor depends not only on the inductance value but also the time when both SR_1 and S_{a1} are ON.

$$i_{sa} = \frac{V_o - V_{F\_D}}{L_a}(t - t_0) \tag{5-7}$$

where V_o is the output voltage and V_{F_D} the forward voltage drop of the auxiliary diode.

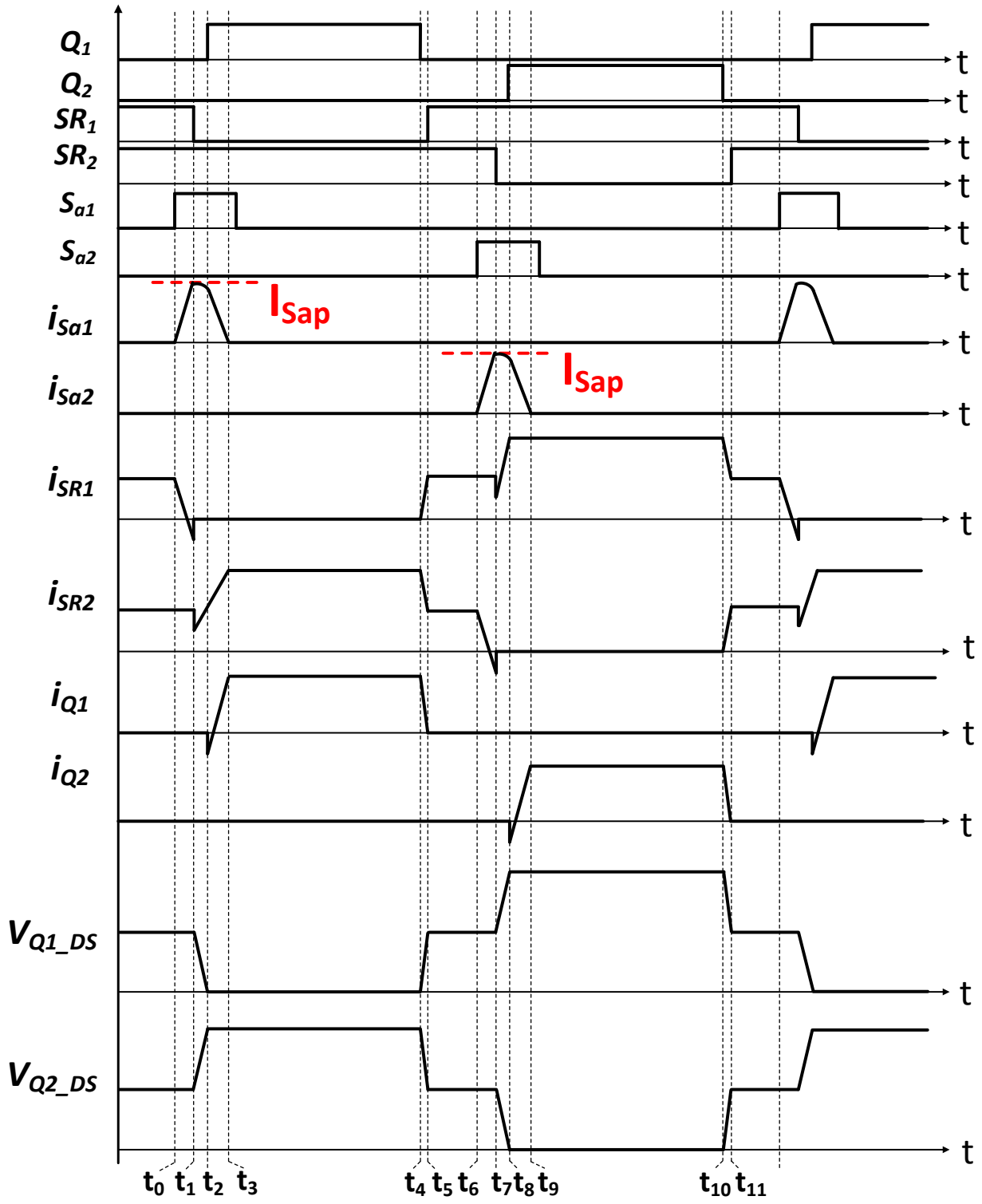


Figure 5.7. Operational waveform of proposed soft switching method for half bridge current doubler.

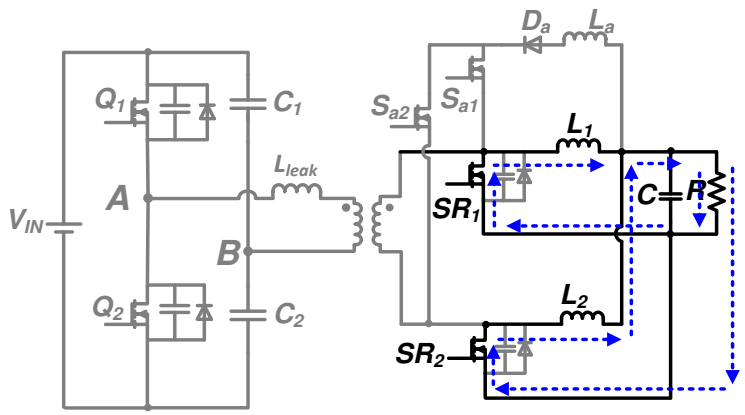


Figure 5.8. Equivalent circuit prior to t_0.

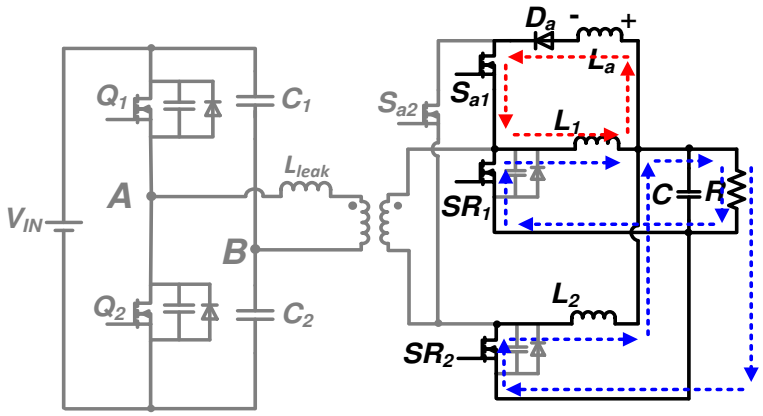


Figure 5.9. Equivalent circuit from $t_0 - t_1$.

b. Interval 2: t_1 to t_2

At time t_1, SR_1 is turned off with the equivalent circuit shown in Figure 5.10. As the current is flowing from drain to source when SR_1 is turned off, the body diode conduction of SR_1 is prohibited together with the reverse recovery current and loss. Yet, active turn off loss occurs in SR_1. The energy charging the output junction capacitance is taken out of the turn off loss of SR_1 as indicated in (5-8). By designing the difference between $(I_{sap} - \frac{1}{2}I_o)$ as small as possible, the actual turn off losses of SR devices are also kept at the minimum value.

$$P_{SRoff} = \frac{1}{2}V_{SR}\left(I_{sap} - \frac{1}{2}I_o\right)t_{off,sw}f_s - \frac{1}{2}V_{SR}^2 C_{SR} f_s \tag{5-8}$$

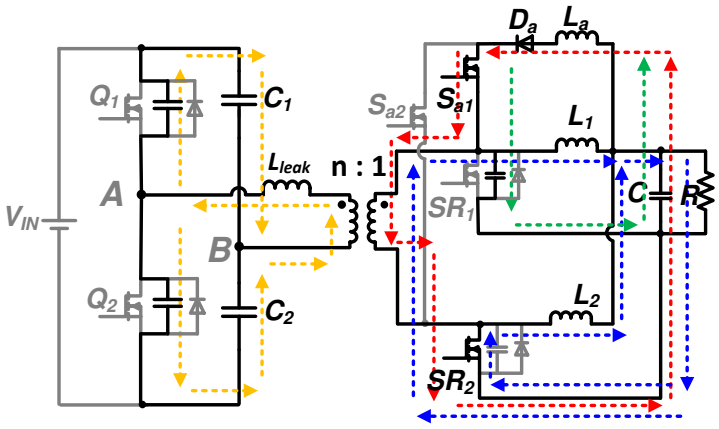


Figure 5.10. Equivalent circuit from $t_1 - t_2$.

At the instant SR_1 is turned off, the current in the auxiliary inductor is larger than the current in the output inductor. The difference between the two currents is forced to flow through the capacitances in the converter including SR_1, Q_1 and Q_2. The current and voltage relationship during this interval can be expressed as (5-9) to (5-12). As indicated in (5-11), a larger difference between I_{sap} and $\frac{1}{2}I_O$ leads to a faster discharging of voltage across Q_1, which means ZVS can be achieved for a shorter period of resonance.

$$\omega_o = \sqrt{\frac{1}{L_{eq}C_{eq}}} \tag{5-9}$$

$$Z_o = \sqrt{\frac{L_{eq}}{C_{eq}}} \tag{5-10}$$

$$v_{Q1\_DS} = V_{in} - V_o\left(n^2 + cos\omega_o(t-t_1)\right)\frac{Z_o - \omega_o L_a}{Z_o} - \frac{Z_o}{\omega_o^2 C_{SR} L_{leak} + \frac{C_{SR}}{C_{pri}} + 1}(I_{Sap} - \frac{1}{2}I_o)\sin\omega_o(t-t_1) \tag{5-11}$$

$$i_{La} = I_o + \frac{V_o}{Z_o}\sin\omega_o(t-t_1) + (I_{Sap} - \frac{1}{2}I_o)cos\omega_o(t-t_1) \tag{5-12}$$

where $L_{eq} = L_a + \frac{L_{leak}}{n^2}$, $C_{eq} = \frac{2n^2 C_{pri} C_{SR}}{C_{SR}+2n^2 C_{pri}}$ and C_{pri} is the junction capacitances of primary MOSFETs, C_{SR} is the junction capacitance of SR MOSFETs.

If Q_1's turn on signal still has not arrived when the voltage is discharged to zero, the body diode of Q_1 starts to conduct as shown in Figure 5.11, which is not preferred, as extra body diode conduction loss is being introduced [24] and efficiency is compromised.

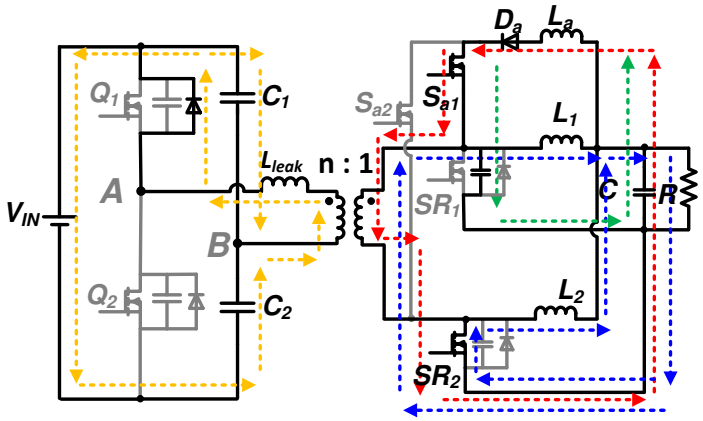


Figure 5.11. Primary body diode conduction between $t_1 - t_2$.

c. Interval 3: t_2 to t_3

At time t_2, Q_1 is turned on with zero voltage across it as shown in Figure 5.12. When Q_1 is conducting, a positive voltage is applied across the transformer while a negative voltage is applied across L_a (the direction is marked in Figure 5.12). Therefore, the current in the auxiliary inductor starts to reduce linearly as (5-13). When the current reaches zero, the diode D_a starts to block the voltage and stops conducting current. Clearly, S_a can be turned off with zero current through it. The time for the current to reduce to zero can be calculated based on (5-13) as well. At the same time when S_{a1} stops conduction, the current through Q_1 reaches the inductor current reflected to the primary side.

$$i_{sa} = I_{sat2} - \frac{\frac{V_{in}}{2n} - V_o - V_{Da}}{L_a}(t - t_1) \tag{5-13}$$

where I_{sat2} is current in auxiliary inductor at time t_2.

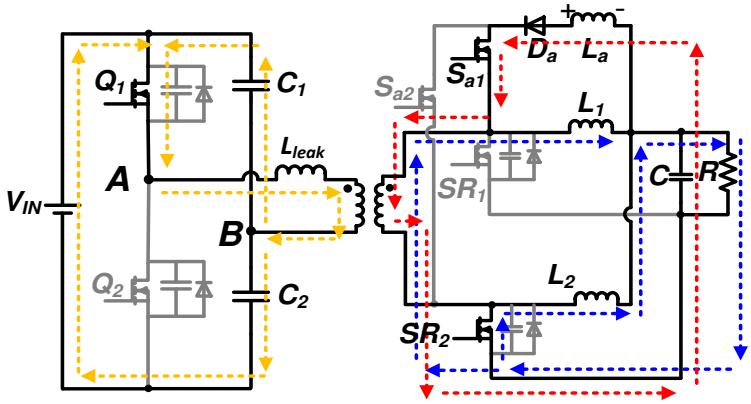


Figure 5.12. Equivalent circuit from $t_2 - t_3$.

d. Interval 4: t_3 to t_4

During this interval, the converter's operation is the same as the conventional half bridge current doubler as presented in Figure 5.13, and the energy is transferring from primary to secondary side. The duration of this interval can be calculated as in (5-14). Both inductors' currents are free-wheeling through SR_2. This interval is the same as conventional half bridge current doubler.

$$t = \left(\frac{2nV_o}{V_{in}}\right) \times T_s \tag{5-14}$$

e. Interval 4: t_4 to t_5

At time t_4, Q_1 is turned off as shown in Figure 5.14. The actual turn off loss can be calculated in (5-14) where the current charging the junction capacitances is not included in the turn off loss of Q_1 and is subtracted. For high input voltage low input current application here, the actual turn off losses of Q_1 and Q_2 are much smaller compared with VI product calculation

as in (5-14). Also, the actual turn off losses of Q_1 and Q_2 are smaller than the extra auxiliary components loss if the snubber capacitor was added in parallel with Q_1 and Q_2 to eliminate the turn off loss as in [45]-[47] for high input voltage low input current application.

$$P_{prioff} = \frac{1}{4} V_{in} I_{off} t_{off,sw} f_s - V_{in} Q_{oss} f_{sw} \tag{5-15}$$

where I_{off} is the current value of Q_1 is turned off and $t_{off,SW}$ is the turn off transition time which is found by Saber simulation.

The body diode of SR starts to conduct when the channel of Q_1 starts turning off.

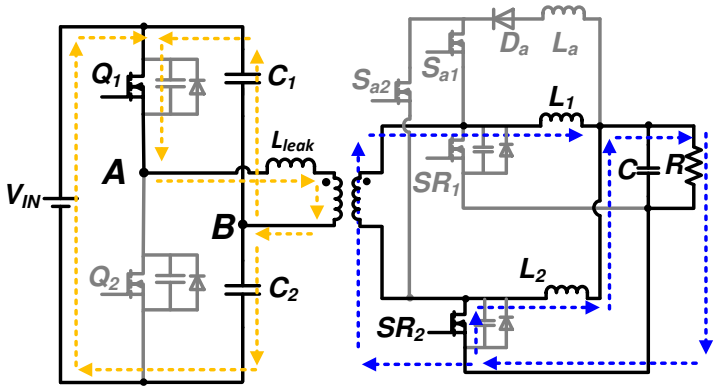


Figure 5.13. Equivalent circuit from $t_3 - t_4$.

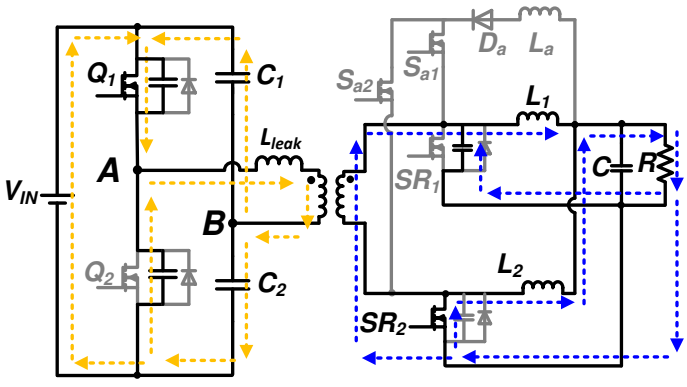


Figure 5.14. Equivalent circuit from $t_4 - t_5$.

f. Interval 4: t_5 to t_6

From time t_5, SR_1 is turned on with zero voltage across it. The converter enters the free-wheeling period, which is the same as the time interval before t_o and Q_2 and SR_2 will be switched for next half switching cycle. Because of symmetry of the half bridge current doubler operation, the rest of the switching intervals will not be discussed here.

Even though ZVS can be obtained and switching losses and reverses recovery losses are eliminated based on the discussion in this section, extra auxiliary components losses occur to the converter. In the next section, the auxiliary losses are analyzed and the method to improve light load efficiency is discussed.

5.3. Load dependent charging time analysis and controller design

5.3.1. Losses under constant charging time of auxiliary inductor

Based on earlier discussion, the intervals 1 and 2 are the key transitions to realize zero voltage turn on of primary MOSFETs. During interval 1, energy is stored in the auxiliary inductor, which is released to junction capacitances during interval 2. The current in the auxiliary inductor is discharged during interval 3. Energy losses will occur during the interval charging and discharging the auxiliary inductor, mainly conduction loss of auxiliary MOSFETs and diode which can be calculated as in (5-16) and (5-17), receptively. The auxiliary inductor (L_a) is an air core inductor formed with printed circuit board (PCB) traces which will be discussed in detail in Section 5.4.2, therefore, the conduction losses of L_a is ignored here.

$$P_{AUX\_M} = 2I_{RMS\_AUX}^2 R_{AUX\_M} \tag{5-16}$$

$$P_{AUX\_D} = 2I_{RMS\_AUX}^2 \times R_{AUX\_D} + 2I_{AVG\_AUX} \times V_{F\_D} \tag{5-17}$$

where I_{RMS_AUX} and I_{AVG_AUX} are the RMS and average value of auxiliary current, which can be further calculated in (5-18) and (5-19) and R_{AUX_M} is the on-state resistance of the auxiliary

MOSFETs and V_{F_D} and R_{AUX_M} are the forward voltage drop and resistance of the auxiliary diode. Usually the resonant duration is much shorter than the charging and discharging period, therefore, the current value is assumed to be constant from t_1 to t_2.

$$I_{RMS\_AUX} = \sqrt{\left(\frac{\boldsymbol{I_{Sap}^2}\left((\boldsymbol{t_3}-\boldsymbol{t_2})+3(\boldsymbol{t_2}-\boldsymbol{t_1})+(\boldsymbol{t_1}-\boldsymbol{t_0})\right)}{\boldsymbol{3T_s}}\right)} = \sqrt{\left(\frac{\boldsymbol{I_{Sap}^2}(t_c+3t_r+t_{dc})}{\boldsymbol{3T_s}}\right)} \tag{5-18}$$

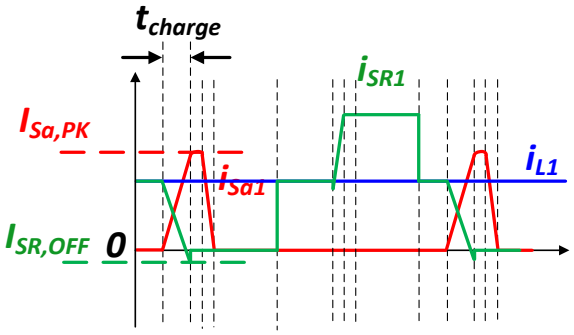
$$I_{AVG\_AUX} = \frac{I_{sap}\left((\boldsymbol{t_3}-\boldsymbol{t_2})+2(\boldsymbol{t_2}-\boldsymbol{t_1})+(\boldsymbol{t_1}-\boldsymbol{t_0})\right)}{2\boldsymbol{T_s}} = \frac{I_{sap}\left((t_c+2t_r+t_{dc})\right)}{2\boldsymbol{T_s}} \tag{5-19}$$

where t_c, t_r and t_{dc} are the charging time, resonance time and discharging time of the auxiliary inductor, which is the time duration from t_0 to t_1, t_1 to t_2, and t_2 to t_3 in Figure 5.7, respectively.

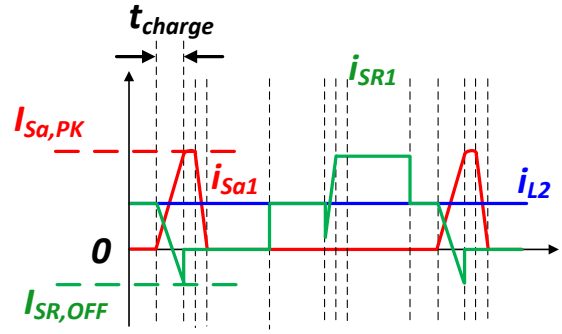
For the on-board power supplies, the electric loads demand high current (30 A) at low voltage (1 V), which means a considerable amount of current is flowing through the auxiliary components to achieve ZVS, making the losses in auxiliary components non-negligible. When the charging timing of the auxiliary inductor is determined and being fixed, the losses of auxiliary components are also fixed regardless of the loading condition of the converter. The constant auxiliary components' losses mean the percentage of the auxiliary components' losses increases as load decreases. Therefore, the light load efficiency is compromised by the constant charging time method.

In the meantime, the constant auxiliary components' loss is not the only factor that worsens the light load efficiency, the SR devices turn off losses also increase as load decreases. Figure 5.15 presents the theoretical current waveforms of the output inductor, SR device and auxiliary inductor with constant charging time of the auxiliary inductor. It clearly indicates that as load reduces, the SR devices are turned off with a larger current through them, resulting in an increased turn off loss when load is lighter as in (5-8).

At the same time, if a constant dead time is implemented in the converter, the conduction period of primary MOSFETs' body diode is longer as the load becomes lighter. As indicated in (5-11), a larger difference between I_{sap} and $\frac{1}{2}I_O$ leads to a faster discharging of junction capacitances. Therefore, the converter experiences an increased body diodes conduction loss as load reduces. Adjusting the dead time can solve this issue, but it increases the complexity of the controller.



(a) Heavy load



(b) Light load

Figure 5.15. SR waveforms under different load conditions with constant charging time method.

5.3.2. Proposed load dependent charging time method

The essential part to realize zero voltage switching of primary side MOSFETs is the resonance between MOSFET junction capacitances and auxiliary inductance between t_1 and t_2

discussed in the last section. In order to achieve ZVS, the energy stored in the auxiliary inductance must be equal or greater than the energy stored in the output junction capacitances of MOSFETs expressed in (5-20).

$$\frac{1}{2}L_{Sa}\left(I_{sap}-\frac{1}{2}I_O\right)^2 \geq \frac{1}{2}C_{pri}V_{in}^2 + C_{SR}V_{SR}^2 \tag{5-20}$$

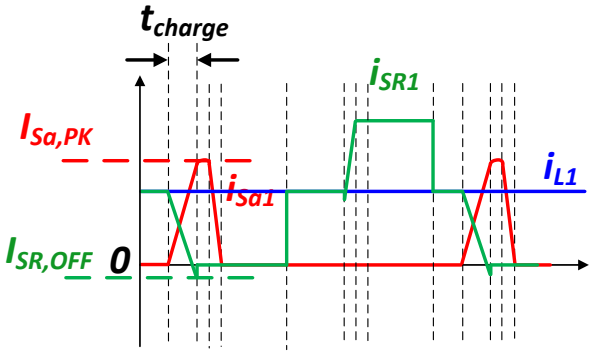
As (5-20) indicates, the energy stored in the auxiliary inductor is related to the difference between the auxiliary current and output current. Therefore, the optimal design with minimum auxiliary losses is that energy stored in the auxiliary inductor equals to the energy stored in the junction capacitances in all the load conditions. Therefore, the optimum design is to keep a constant$\left(I_{sap}-\frac{1}{2}I_O\right)$, which means when load current reduces, I_{sap} reduces correspondingly. For a given auxiliary inductance, it means a shorter charging time of the auxiliary inductor. The desired charging current and corresponding charging time can be calculated as in (5-21) and (5-22), which clearly indicates that to store the same amount of energy in the auxiliary inductor as in the junction capacitances, the charging current and charging time is related to the load condition.

$$I_{sap} = \sqrt{\frac{C_{pri}V_{in}^2 + 2C_{SR}V_{SR}^2}{L_{Sa}}} + \frac{1}{2}I_O \tag{5-21}$$

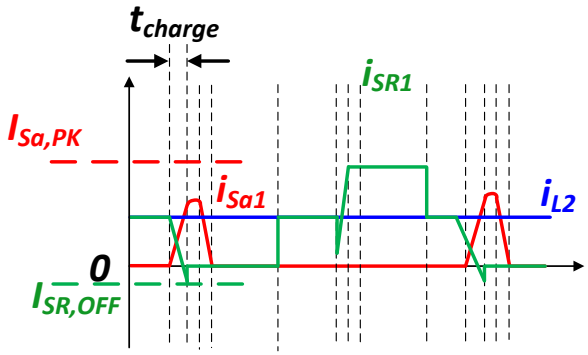
$$t_{charge} = \frac{L_{Sa}\left(\sqrt{\frac{C_{pri}V_{in}^2 + 2C_{SR}V_{SR}^2}{L_{Sa}}} + \frac{1}{2}I_O\right)}{V_o - V_{F\_D}} \tag{5-22}$$

Figure 5.16 is the theoretical current waveforms of output inductor, SR devices and auxiliary inductor with the proposed load dependent control. When the output inductor current reduces, the auxiliary MOSFET is triggered to turn on later, which means the auxiliary inductor is charged for a shorter period of time (t_{charge}). The difference between the auxiliary inductor

and output inductor current is constant regardless of the load. Therefore, the losses in the auxiliary circuit are reduced, the turn off loss of SR devices is not increasing, and the constant dead time can be used in the converter as the load reduces in the proposed method.



(a) Heavy load



(b) Light load

Figure 5.16. SR waveforms under different load conditions with load dependent charging time method.

After the necessity of adjusting the charging time being established, Figure 5.17 indicates the controller design of the load dependent ZVS method and Figure 5.18 illustrates the key waveforms of the controller. A commercial half bridge controller IC (UCC 28250) is used to generate the control signals Q_1, Q_2, SR_{1C} and SR_{2C}.

A large dead time between SR devices' turn off (SR_{1C} and SR_{2C} in Figure 5.17) and primary devices' turn on (Q_1 and Q_2 in Figure 5.17) is programmed on the controller IC so that

the falling edges of SR_{1C} and SR_{2C} can be used to generate gate signals for S_{a1} and S_{a2}. In order to consider the load condition, a comparator between inductor current (i_{L1} and i_{L2} in Figure 5.17) and the RC delayed falling edge (SR_{1C_D} and SR_{2C_D} in Figure 5.17) is used to generate the turn on signal for S_{a1} and S_{a2}. A larger load leads to a sooner cross over between SR_{1C_D} and I_{L1} (same for SR_{2C_D} and I_{L2}) which will trigger the comparator sooner to create a longer charging time of L_a.

The multivibrator is set to be rising edge triggering, therefore, the rising edge of the comparator (when I_{L1} becomes larger than SR_{1C_D} as t_1 in Figure 5.18) will trigger the multivibrator to turn on for a given time, the falling edge (when I_{L1} becomes smaller than SR_{1C_D} as between t_6 and t_7 in Figure 5.18) will not trigger the multivibrator. Also, a falling edge delay circuit is implemented so that SR_1 and SR_2 will have a suitable dead-time.

As indicated in Figure 5.17 and Figure 5.18, the inductor current or load current information is necessary to adjust the charging time of the auxiliary inductor. DCR current sensing method (shown in Figure 5.19), which is widely adopted for the on-board power supplies, is implemented for the half bridge current doubler [80][81][82]. The DCR is the DC equivalent resistance of the inductor, which is not added to the circuit as an extra sensing resistor. When $R_{CS}C_{CS} = L/DCR$ is satisfied, the voltage across the capacitor, C_{CS}, is proportional to the inductor current as (5-23). Then the signal is fed to an op amp to get larger signal and become the positive input to the comparator. Therefore, the current information can be obtained with no extra component losses.

$$v_{CS} = DCR * i_L \tag{5-23}$$

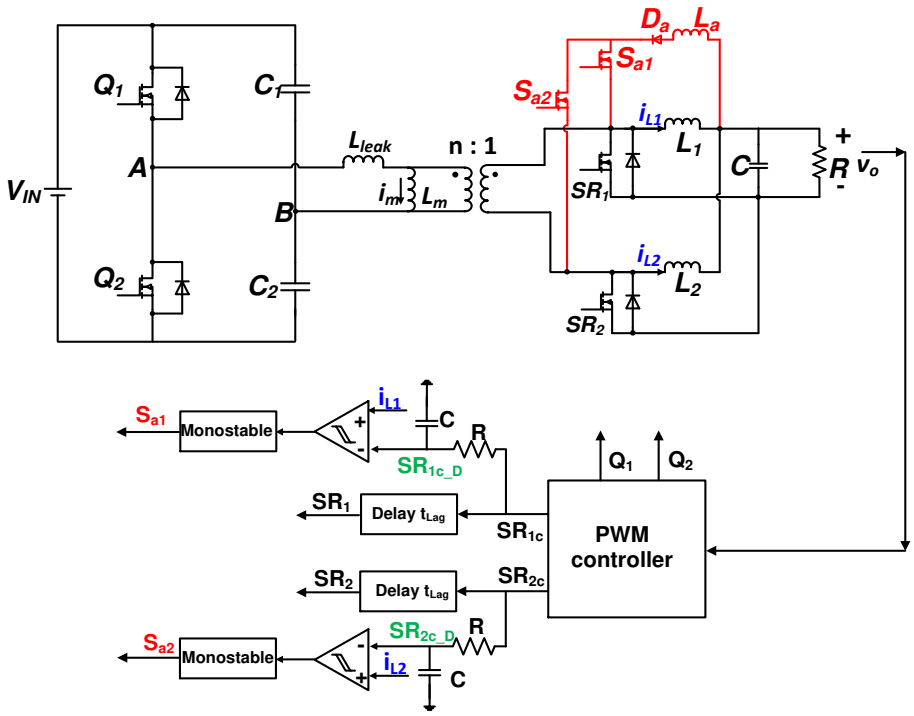


Figure 5.17. Control scheme of load dependent soft switching method.

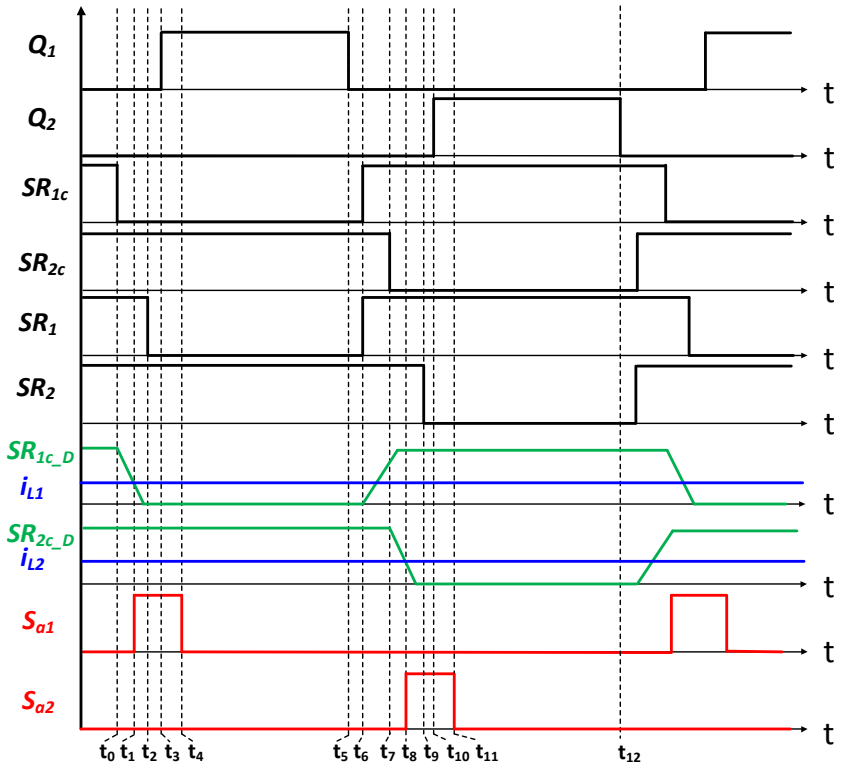


Figure 5.18. Gate signal sequence for load dependent soft switching half bridge current doubler.

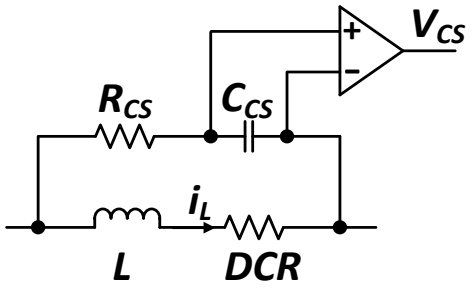


Figure 5.19. DCR current sensing of output inductor current.

Based on the discussion in this section, a load dependent zero voltage switching method is necessary to improve the light load efficiency, and the method to generate the desired gating sequence and sensing output inductor current is also covered. In the next section, a prototype is built to verify the proposed method.

5.4. Converter design for proposed method

5.4.1. Power stage design

A laboratory prototype has been designed and built to verify the proposed method. The system specifications of half bridge current doubler are listed in Table 5.1.

Table 5.1. Specification of half bridge current doubler.

Parameter	Value/ Part number
Input voltage	66 V
Output voltage	1 V
Output power	30 W
Output current	30 A
Switching frequency	280 kHz

The transformer is designed with printed circuit board winding at 6:1 primary to secondary turns ratio. The winding is designed with primary and secondary side interleaved as shown in Figure 5.20 [65][66] to reduce the leakage inductance in the half bridge current doubler which causes resonance with the junction capacitances. Non-gapped cores are used to obtain large magnetizing inductance to limit the magnetizing current as discussed in Section 5.2. Planar cores E/PLT core E 14/3.5/5 and PLT 14/5/1.5 are selected with 4 oz (140 µm) copper windings. The leakage inductance and AC resistance is 63 nH and 76 mΩ at switching frequency, respectively as presented in Figure 5.21.

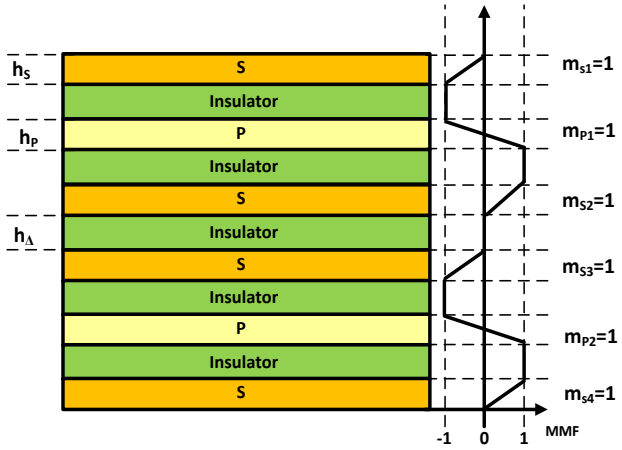


Figure 5.20. Interleaved winding structure.

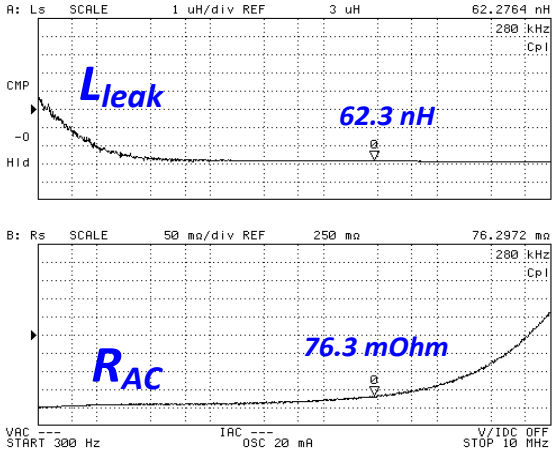


Figure 5.21. Measured transformer leakage inductance and AC resistance.

Other components including primary and secondary side MOSFETs, output inductors and capacitors used in the half bridge current doubler are listed in Table 5.2.

Table 5.2. Components in half bridge current doubler.

Components	Part number/ Value
Q_1 and Q_2	AON7296
SR_1 and SR_2	BSC010NE2LS
C_1 and C_2	4.7 µH
Output inductor	220 nH
Output capacitor	500 uH

5.4.2. Auxiliary circuit design

The auxiliary inductance together with the charging time (duration ($t_1 - t_0$) in Figure 5.7) determines the auxiliary current (I_{sap} in Figure 5.7) and then determines if energy stored in the auxiliary inductor ($\frac{1}{2}L_{Sa}\left(I_{sap}-\frac{1}{2}I_O\right)^2$) is enough to discharge the junction capacitances completely for the primary MOSFETs. Therefore, the value of the auxiliary inductance is not strictly defined because the charging time can be adjusted to accommodate the actual value of the auxiliary inductance in order to store enough energy.

Figure 5.22 shows the relationship of the auxiliary inductance and the ratio of I_{sap} to I_L in order to have enough energy stored. Then, the charging time can be calculated correspondingly as presented in (5-7). Since the auxiliary inductance is in the range of nH, an air core inductor from turns formed on a printed circuit board using traces as the turns is designed. The actual auxiliary inductance based on an impedance analyzer's measurement is 32 nH.

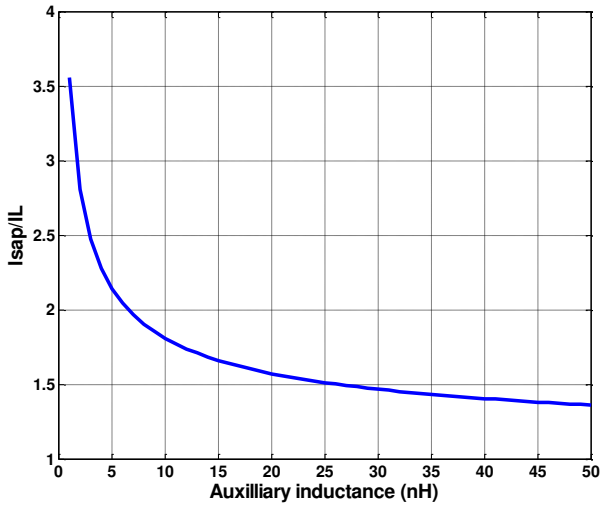


Figure 5.22. Relationship between auxiliary inductance and the ratio between desired auxiliary charging current and output inductor's current.

Unlike the buck converter, the leakage inductance (L_{leak}) is part of the resonant network in the half bridge; therefore, it impacts the ZVS behavior of the primary side devices. Figure 5.23 shows the equivalent circuit during the resonant period (t_2-t_1), and Figure 5.24 shows the relationship between the minimum duration of this interval (t_2-t_1) and the ratio of leakage inductance to the auxiliary inductance reflected to the primary side ($L_{leak} / n^2 L_a$) with zero leakage inductance being unity based on Saber simulation. As a high step down converter with large transformer turns ratio, the leakage inductance needs to be much larger compared with the auxiliary inductance to impact the resonance. Based on the prototype measured, $L_{leak} / n^2 L_a$ is less than 0.1, which means it has very limited impact on the resonance. Schottky diode DSS40-0008D and MOSFET BSZ036NE2L are selected as the auxiliary diode and MOSFET, respectively.

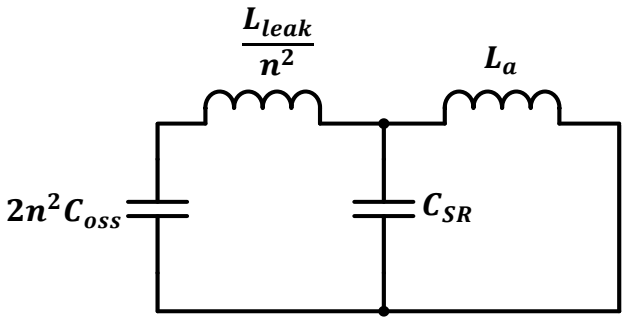


Figure 5.23. Equivalent resonant circuit during interval 2 (as in Figure 5.7).

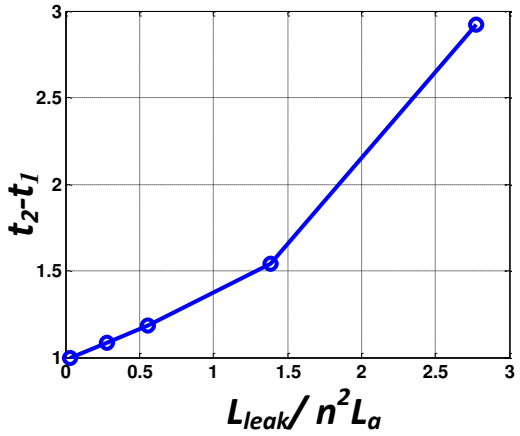


Figure 5.24. Relationship between the leakage inductance and resonance time (t_2-t_1) in Figure 5.7.

5.5. Experimental verification

Based on schematic of the proposed method in Figure 5.6, the gate of the auxiliary MOSFETs is connected to the drain of SR MOSFETs, which means a floating gate driver is required. However, as the specification indicates, the drain voltage of the SR MOSFETs is below 6 V, therefore, a 12 V driving voltage directly connected to ground is used in this paper. Even when the SR MOSFET is off, there is still enough gate voltage to keep the auxiliary MOSFETs on with a slightly higher $R_{ds(on)}$. The complexity of the gate driver circuit is greatly reduced.

Figure 5.25 through Figure 5.30 show the zero voltage switching (ZVS) of primary side MOSFETs under different load conditions with the proposed load dependent ZVS method as the drain to source voltage (V_{ds}) has been discharged to zero before the arrival of gate voltage (V_{gs}). Neither the MOSFETs' current nor the auxiliary inductor's current are measured in the experiments directly, mainly because measuring the currents would introduce extra inductance to the circuit. As the leakage inductance of the transformer is 60 nH and auxiliary inductance is around 30 nH, therefore, the measuring wire's inductance would make a difference. The charging time is indicated by the overlap between secondary side devices' (V_{gs_SR2}) and auxiliary devices' gate signal (V_{gs_sa2}) as the auxiliary inductor is only being charged when both of them are on. From the experimental results, it can be clearly seen that ZVS of primary side devices can be achieved over a wide load range, and the charging time is dependent on the load condition, which prevents charging the auxiliary inductor to an unnecessarily large value and increasing conduction loss of the auxiliary MOSFETs and diode and turn off loss of SR devices as in the constant charging time method.

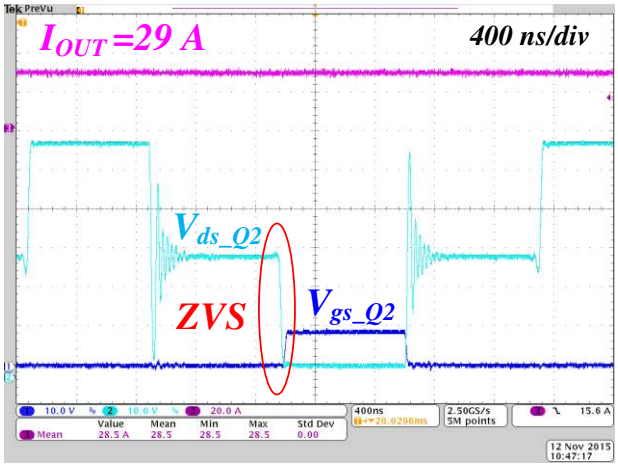


Figure 5.25. ZVS for primary device with 29 A load current.

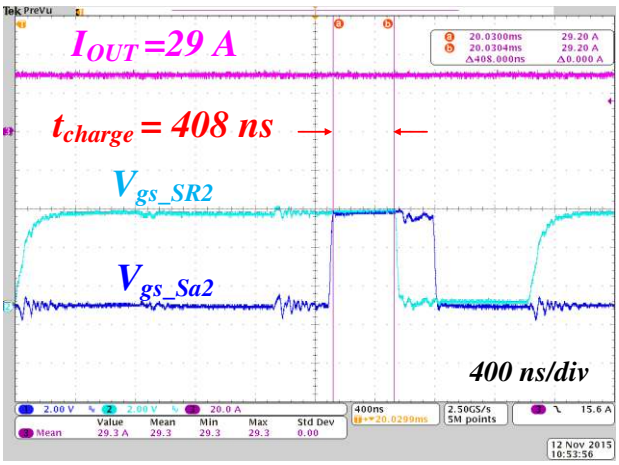


Figure 5.26. Charging time for auxiliary inductor with 29 A load current.

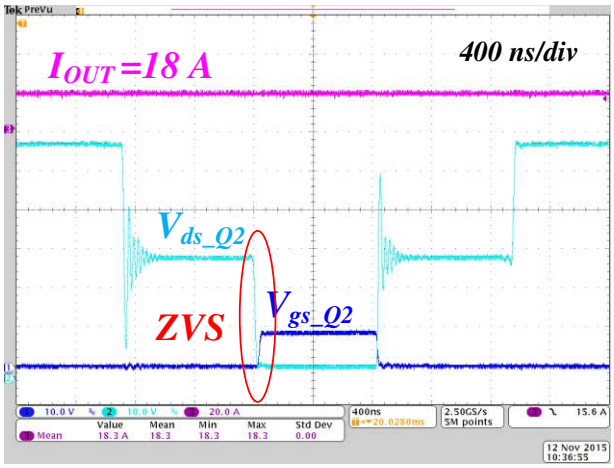


Figure 5.27. ZVS for primary device with 18 A load current.

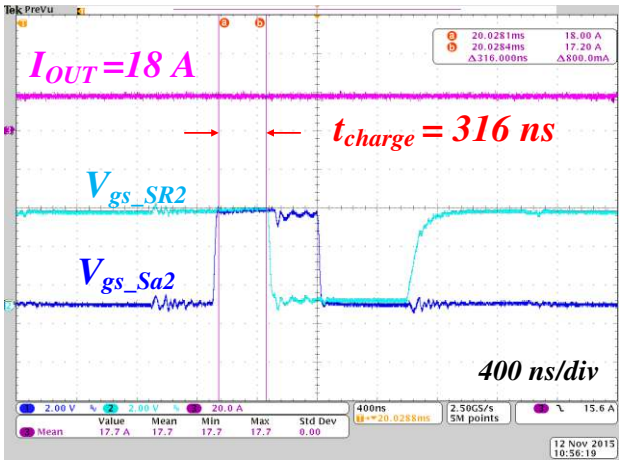


Figure 5.28. Charging time for auxiliary inductor with 18 A load current.

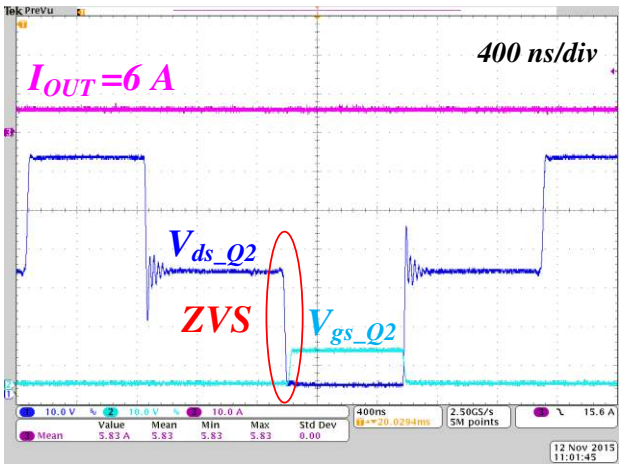


Figure 5.29. ZVS for primary device with 6 A load current.

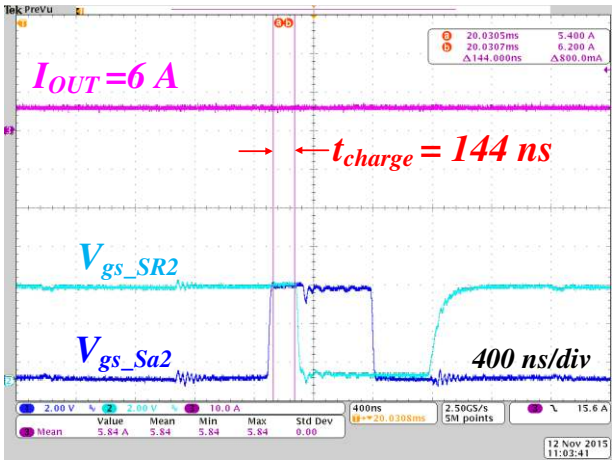


Figure 5.30. Charging time for auxiliary inductor with 6 A load current.

In the meantime, constant dead time is implemented in the controller for all the loading conditions. It can be seen the junction capacitances can be completely discharged and almost no body diode conduction of primary side MOSFET regardless of the load conditions as illustrated in Figure 5.25, Figure 5.27 and Figure 5.29.

Figure 5.31 illustrates the charging time of the auxiliary inductor under different load conditions based on experimental testing. The charging time reduces when load reduces as designed. One thing to notice is that in the experiments, it actually requires longer charging

time to achieve ZVS in all the load conditions, therefore, longer charging time is implemented in the experiment compared with analysis. However, this difference does not impact the load dependent operation; it simply means a larger I_{sap} is needed to obtain ZVS under all load conditions. The longer required charging time is because of the parasitics in the converter which are not being considered in calculation.

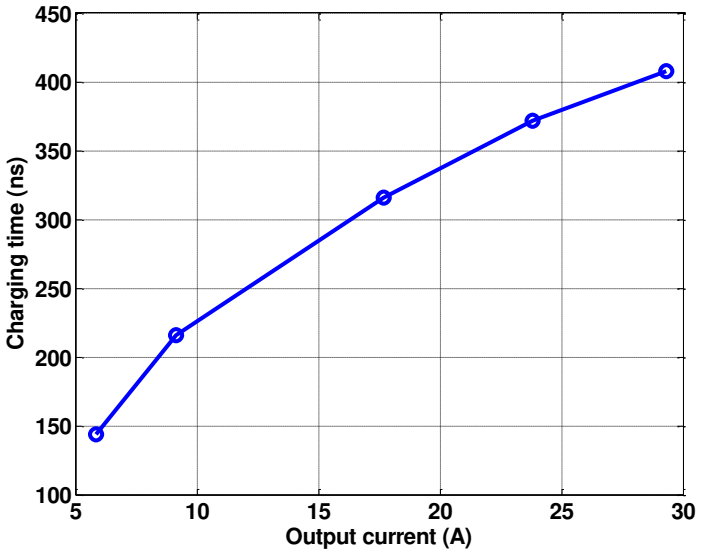


Figure 5.31. Experimental charging time under different load conditions.

Figure 5.32 shows the efficiency comparison among different control methods, including conventional hard switching, constant charging time of the auxiliary inductor which is obtained under full load condition and proposed load dependent charging method. Dead time between primary and secondary side devices is not being adjusted based on load condition for all three the cases. It clearly shows that the proposed method has higher efficiency compared with the other two methods in a wide load range. Even with conventional hard switching half bridge current doubler, the full load efficiency is over 88%, which is 3% point higher than the conventional architectures with state of the art products. Therefore, the architecture of HV POL

itself can improve the efficiency without advanced wide bandgap (WBG) devices or ZVS control techniques.

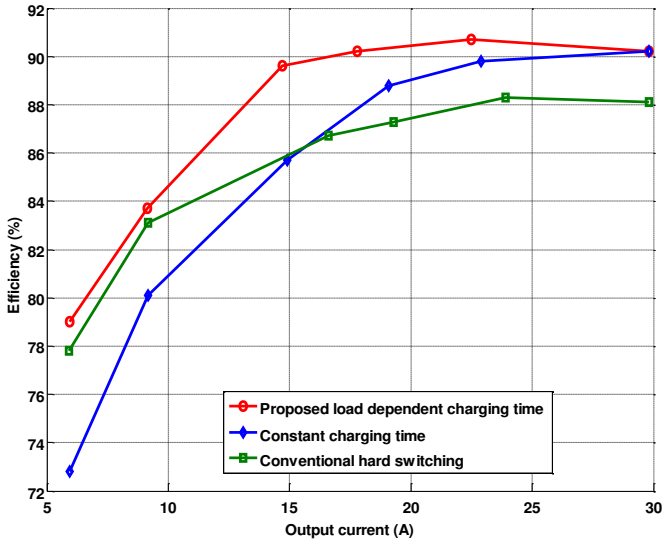
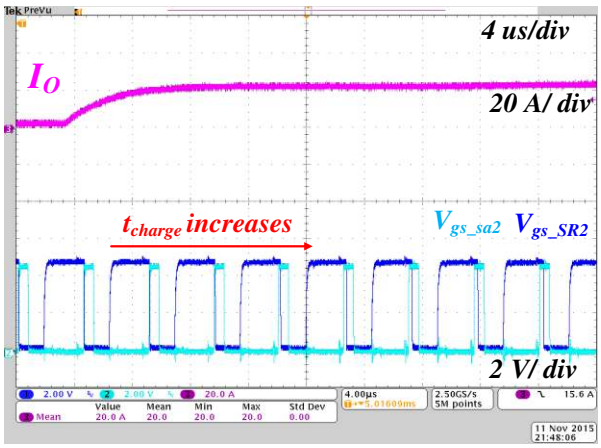
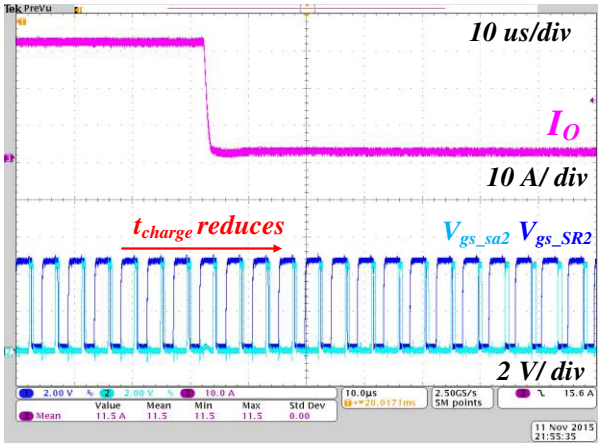


Figure 5.32. Experimental efficiency comparison among proposed load dependent charging time, constant charging time and conventional hard switching.

Figure 5.33 shows the transient performance of the proposed method when load changes. The time scale for load step up is 4 µs/ div and for load step down is 10 µs/ div. Charging time (t_{charge}) is indicated by the overlap of ON signal between the auxiliary MOSFET (V_{GS_Sa2}) and SR MOSFET (V_{GS_SR2}). It can be seen that the charging time changes with the load current changing automatically. It takes several switching cycles for the control to respond to the load change, mainly because inductor current is used for the load condition in the controller, which is not as fast as the output current to the load. However, after several switching cycles, the proposed method can adjust the charging time to a desired value and offers a higher efficiency compared with constant charging time method.



(a) Load stepping up



(b) Load stepping down

Figure 5.33. Transient of proposed load dependent charging method.

Based on the experimental results, the proposed load dependent zero voltage switching method can improve the efficiency of the half bridge current doubler compared with both hard switching and constant charging time method. Also, the proposed controller can adjust the charging time automatically when the load changes.

Even though the method is proposed for the half bridge current doubler in the HV POL converter in power supplies for data centers, the method can easily be applied to the synchronous buck converter (stepping 12 V down to 1 V) used in POL converter in the

conventional power supply architectures where the turn on loss is also a dominant loss of the converter.

The method can also be applied to converters not typically used in power supplies but also a PWM converter, such as boost, buck boost, SEPIC, Cuk and so on.

5.6. Cost analysis

Even though the efficiency of the proposed HV POL is higher compared with intermediate bus architecture (IBA), cost should also be considered in addition to efficiency. Therefore, in this section, the cost of IBA and HV POL is estimated. Figure 5.34 shows the cost for some components of a 400 W unit including four converters: conventional intermediate bus architecture (IBA), high voltage point of load converter (HV POL) with hard switching half bridge, HV POL with auxiliary circuit assisted soft switching half bridge converter and HV POL with full bridge converter discussed in Chapter 4. Items that are common to all the four converters and have same cost are not shown in Figure 5.34 and include: (1) bottom MOSFETs in POL and SR MOSFETs in all HV POL, (2) input and output capacitors.

The converters are assumed to be operated under full power all the time. For IBA, the MOSFETs marked as 400 V in Figure 5.34 are the primary MOSFETs which include two MOSFETs rated at 600 V. For HV POL, 400 V MOSFETs are the primary MOSFETs which includes 24 MOSFETs rated 100 V for half bridge and 48 MOSFETs also rated at 100 V for full bridge converter. The MOSFETs at 12 V in Figure 5.34 are only applicable for IBA, which includes the SR MOSFETs in IBC (4 MOSFETs rated at 40 V) and top MOSFETs in POL (24 MOSFETs rated at 25 V). The cost of the transformer only includes the core cost. Output inductors are selected to allow the same current ripple. Capacitor includes all caps in the

converters except the input and output caps at 400 V and 1 V, because the cost of these two caps is the same for all the topologies. All the gate drivers are included in the cost analysis. Auxiliary cost is only applicable to the soft switching half bridge current doubler which includes a Schottky diode and two MOSFETs. The prices of components are found on the Vendors website with a large purchasing amount. The cost of bottom switches in POL and secondary side MOSFETs in the three HV POL topologies are not included as the cost for them are the same. Under the above assumptions, the cost for IBA, HV POL with hard switching half bridge, HV POL with soft switching half bridge, and HV POL with full bridge is $17.7, $23.9, $ 25.7 and $25.9, respectively. The cost of IBA is based on the design in [83][85].

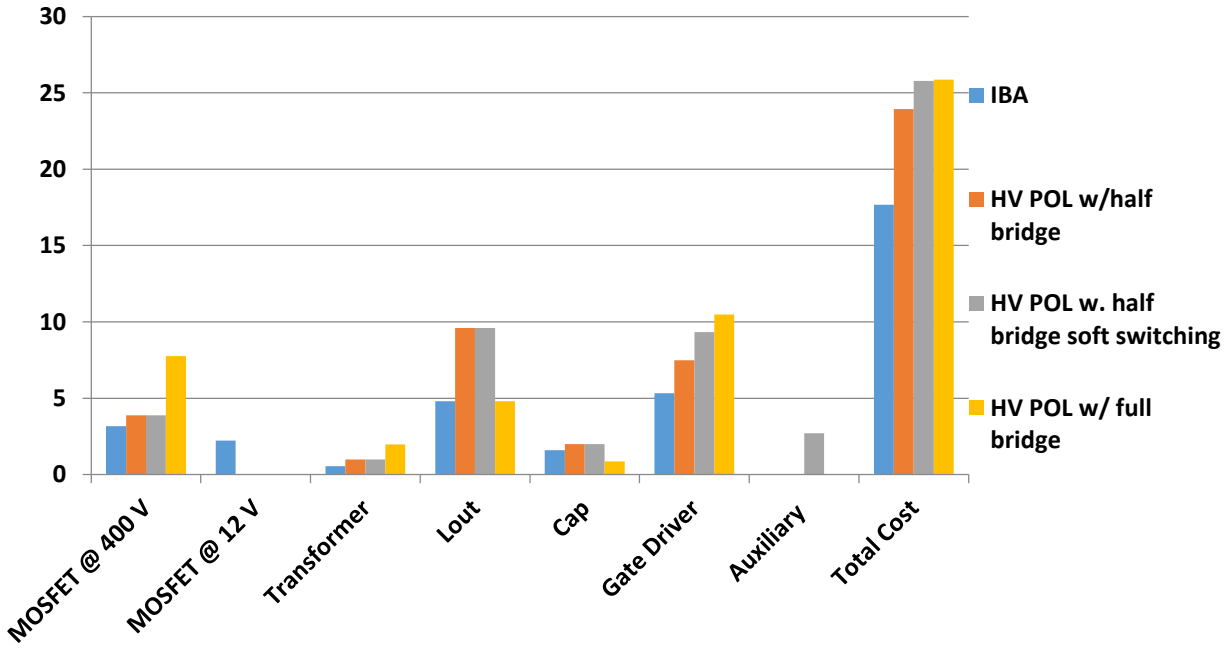


Figure 5.34. Cost comparison between IBA and HV POL.

Assuming a 100 MW data center operating at full load continuously for one yer, the cost reduction of electricity bill for HV POL for hard switching half bridge, soft switching half bridge and full bridge is $ 1.463 million, $ 2.294 million, and $ 1.92 million, respectively. The

average electricity was assumed to be 6.62 cent per kWh [83]. The efficiency of IBA is obtained based on the design in [84][85]. The cost of electricity bill reduction of a 400 W unit can be calculated as $ 5.85, $ 9.18 and $ 7.68, respectively. Combined with the cost increment for the components calculated above, the payback time of proposed HV POL for hard switching half bridge, soft switching half bridge and full bridge is 386 days, 318 days, and 390 days, respectively. Therefore, the extra cost of all the converter topologies within HV POL can be paid back for slightly over one year. For the soft switching half bridge current doubler, the cost can be paid back within one year. Therefore, the HV POL can save money if the operating time is over one year even though the converter is more expensive compared with IBA.

5.7. Summary

Half bridge current doubler is selected as the converter topology in an input series output parallel (ISOP) connected system used in the high voltage point of load converter (HV POL) for data center power supplies in order to improve the overall system efficiency from 400-V_{DC} to 1-V_{DC}. Based on loss analysis, symmetrical control is selected as it offers higher efficiency compared with asymmetrical control.

A control method has been proposed so that zero voltage switching (ZVS) of primary side MOSFETs can be achieved which eliminates the major drawback of symmetrical controlled half bridge converter being a hard switching converter. A load dependent ZVS method has further been proposed and analyzed to indicate the mechanisms which improve light load efficiency compared with constant charging time method in particular for the on-board power supply converters.

The converter design including device selection and transformer design together with the auxiliary components selection has been accomplished. A hardware prototype has been built to verify the proposed soft switching methods. Based on the experimental results, the proposed method can adjust the charging time of auxiliary inductor automatically based on load condition and thus higher efficiency is observed for the proposed method in comparison with conventional hard switching and constant charging time method. Therefore, the proposed soft switching method is an effective method to increase the entire load range efficiency.

6. Input Series Output Parallel Connected Half Bridge Current Doubler with Adaptive Voltage Positioning (AVP) Control

As discussed in earlier chapter, in order to fulfill 400 V to 1 V conversion, a six phase input side in series and output side in parallel (ISOP) connected converter is implemented. Based on the discussion in the earlier two chapters, a half bridge current doubler is selected because it has: (1) comparable efficiency with the phase shift full bridge converter, (2) lower devices count and smaller cores for the transformer, (3) smaller footprint and (4) lower cost.

In this chapter, the design and implementation of a six phase interleaved converter is performed. Adaptive voltage positioning (AVP) control is also analyzed for a half bridge current doubler to meet the strict voltage regulation requirement of the on-board power supply. The mismatches in the ISOP system have been analyzed and simulated. In the end, the experimental results are given to verify the feasibility of the proposed architecture.

Table 6.1 shows the specification of the system and the key components selection.

Table 6.1. Specification of ISOP system.

Parameter/ Components	Value
Input voltage (V)	66
Output current (A)	200
Switching frequency per phase (kHz)	280
Output inductor (nH)	220
Output capacitor (μF)	4700
ESR of output capacitor (mΩ)	0.8

6.1. Modeling of ISOP connected half bridge current doubler

In order to design AVP control, the transfer function of input series output parallel (ISOP) connected half bridge current doubler is derived in this section. First, the state space model and transfer function of single phase half bridge current doubler is analyzed. Then, the ISOP connected system is simplified into a single converter with proper scaling and is verified through simulation.

6.1.1. Modeling of single half bridge current doubler

The operation of a half bridge current doubler can be separated into three intervals ignoring the leakage inductance of the transformer and switching transition [86]. The state space equations are shown in (6-1) and (6-2). Based on state space analysis, the state variable *x,* input *u* and output *y* is defined as (6-3) through (6-6). All the variables are marked in Figure 6.1.

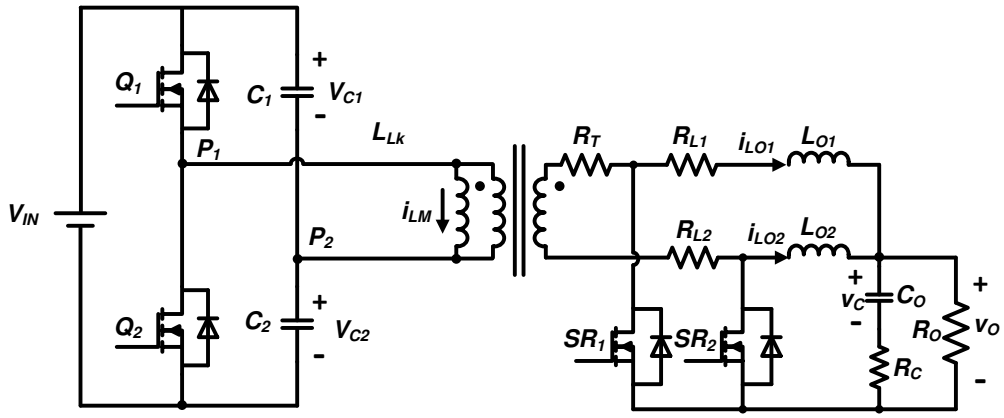


Figure 6.1. Half bridge current doubler with state space variables.

$$\dot{x} = A \cdot x + B \cdot u = f(x, u, d_1, d_2) \tag{6-1}$$

$$y = C \cdot x \tag{6-2}$$

$$x = [v_{C1} \quad i_{LO1} \quad i_{LO2} \quad v_c \quad i_{LM}]^T \tag{6-3}$$

$$u = V_{in} \tag{6-4}$$

$$y = V_O \tag{6-5}$$

$$\dot{x} = \left[\frac{dv_{C1}}{dt} \quad \frac{di_{LO1}}{dt} \quad \frac{di_{LO2}}{dt} \quad \frac{dv_c}{dt} \quad \frac{di_{LM}}{dt}\right]^T \tag{6-6}$$

1. Mode I: Q_1 is ON and Q_2 is OFF

During this interval, Q_1 is ON and Q_2 is OFF as shown in Figure 6.2. The state space equations during this time are expressed in (6-7) through (6-9). The primary MOSFETs' resistance is ignored from the discussion because the primary current is small, then the voltage drop on primary MOSFETs is also small.

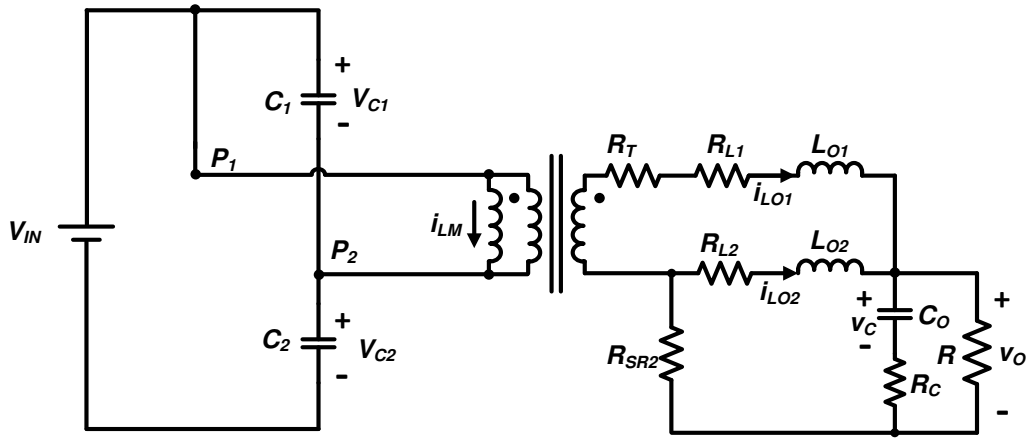


Figure 6.2. Mode I: Q_1 is ON and Q_2 is OFF.

$$A_1 = \begin{bmatrix} 0 & -\frac{1}{n(C_1+C_2)} & 0 & 0 & -\frac{1}{(C_1+C_2)} \\ \frac{1}{nL_1} & -\frac{R_T+R_{L1}+R_{SR2}+\frac{R\cdot R_C}{R+R_C}}{L_1} & -\frac{R_{SR2}+\frac{R\cdot R_C}{R+R_C}}{L_1} & -\frac{R}{L_1(R+R_C)} & 0 \\ 0 & -\frac{R_{SR2}+\frac{R\cdot R_C}{R+R_C}}{L_2} & -\frac{R_{L2}+R_{SR2}+\frac{R\cdot R_C}{R+R_C}}{L_2} & -\frac{R}{L_2(R+R_C)} & 0 \\ 0 & \frac{R}{C_O(R+R_C)} & \frac{R}{C_O(R+R_C)} & -\frac{1}{C_O(R+R_C)} & 0 \\ \frac{1}{L_M} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6-7}$$

$$B_1 = [0 \quad 0 \quad 0 \quad 0 \quad 0]^T \tag{6-8}$$

$$C_1 = \begin{bmatrix} 0 & \frac{R \cdot R_C}{R+R_C} & \frac{R \cdot R_C}{R+R_C} & \frac{R}{R+R_C} & 0 \end{bmatrix} \tag{6-9}$$

2. Mode II: Q_2 is ON and Q_1 is OFF

During this interval, Q_2 is ON and Q_1 is OFF as shown in Figure 6.3. The state space equations during this mode are expressed in (6-10) through (6-12).

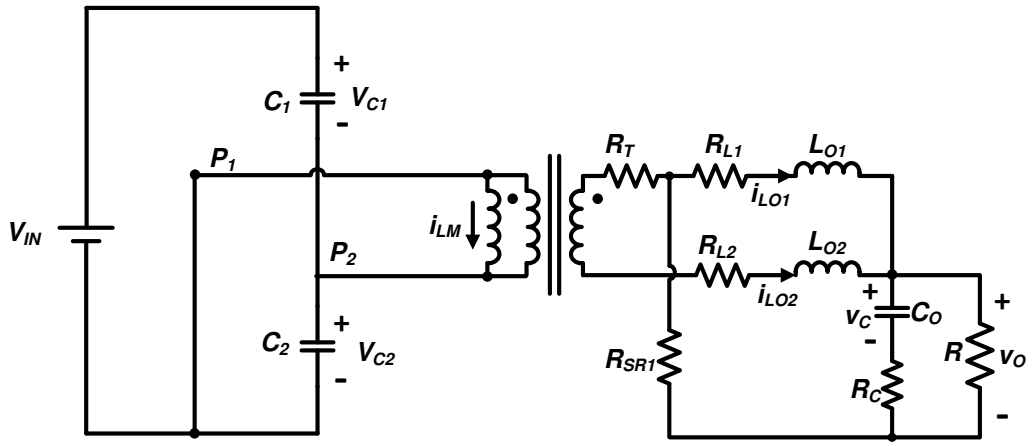


Figure 6.3. Mode II: Q_1 is OFF and Q_2 is ON.

$$A_2$$

$$= \begin{bmatrix} 0 & 0 & \frac{1}{n(C_1+C_2)} & 0 & -\frac{1}{(C_1+C_2)} \\ 0 & -\frac{R_{L1}+R_{SR1}+\frac{R \cdot R_C}{R+R_C}}{L_1} & -\frac{R_{SR1}+\frac{R \cdot R_C}{R+R_C}}{L_1} & -\frac{R}{L_1(R+R_C)} & 0 \\ -\frac{1}{nL_2} & -\frac{R_{SR1}+\frac{R \cdot R_C}{R+R_C}}{L_2} & -\frac{R_T+R_{L2}+R_{SR2}+\frac{R \cdot R_C}{R+R_C}}{L_2} & -\frac{R}{L_2(R+R_C)} & 0 \\ 0 & \frac{R}{C_O(R+R_C)} & \frac{R}{C_O(R+R_C)} & -\frac{1}{C_O(R+R_C)} & 0 \\ \frac{1}{L_M} & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6-10}$$

$$B_2 = [0 \quad 0 \quad \frac{1}{nL_2} \quad 0 \quad -\frac{1}{L_M}]^T \tag{6-11}$$

$$C_2 = \begin{bmatrix} 0 & \frac{R \cdot R_C}{R+R_C} & \frac{R \cdot R_C}{R+R_C} & \frac{R}{R+R_C} & 0 \end{bmatrix} \tag{6-12}$$

3. Mode III: Both Q_1 and Q_2 are OFF

During this interval, both Q_1 and Q_2 are OFF as shown in Figure 6.4. The state space equations during this mode are expressed in (6-13) through (6-15).

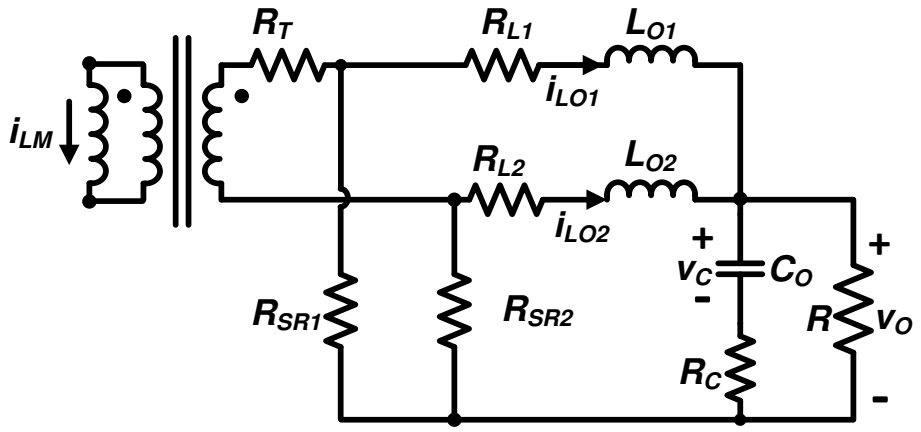


Figure 6.4. Mode III: Both Q_1 and Q_2 are OFF.

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{R_{L1} + R_{SR1} + \frac{R \cdot R_C}{R+R_C}}{L_1} & -\frac{R \cdot R_C}{L_1(R+R_C)} & -\frac{R}{L_1(R+R_C)} & -\frac{nR_{SR1}}{L_1} \\ 0 & -\frac{R \cdot R_C}{L_2(R+R_C)} & -\frac{R_{L2} + R_{SR2} + \frac{R \cdot R_C}{R+R_C}}{L_2} & -\frac{R}{L_2(R+R_C)} & -\frac{nR_{SR2}}{L_2} \\ 0 & \frac{R}{C_O(R+R_C)} & \frac{R}{C_O(R+R_C)} & -\frac{1}{C_O(R+R_C)} & 0 \\ 0 & -\frac{nR_{SR1}}{L_M} & \frac{nR_{SR2}}{L_M} & 0 & -\frac{n^2(R_T + R_{SR1} + R_{SR2})}{L_M} \end{bmatrix} \tag{6-13}$$

$$B_3 = [0 \quad 0 \quad 0 \quad 0 \quad 0]^T \tag{6-14}$$

$$C_3 = \begin{bmatrix} 0 & \frac{R \cdot R_C}{R+R_C} & \frac{R \cdot R_C}{R+R_C} & \frac{R}{R+R_C} & 0 \end{bmatrix} \tag{6-15}$$

An average state space model is expressed and shown in (6-16) and (6-17) with the switching period being T and duty cycle for Q_1 and Q_2 being d_1 and d_2, respectively based on the above analysis for each operation stage.

$$\dot{x} = A \cdot x + B \cdot u = f(x, u, d_1, d_2) \tag{6-16}$$

$$y = C \cdot x \tag{6-17}$$

where $A = d_1 A_1 + d_2 A_2 + (1 - d_1 - d_2) A_3$

$B = d_1 B_1 + d_2 B_2 + (1 - d_1 - d_2) B_3$

$$C = \begin{bmatrix} 0 & \frac{R \cdot R_C}{R + R_C} & \frac{R \cdot R_C}{R + R_C} & \frac{R}{R + R_C} & 0 \end{bmatrix}$$

In the small signal analysis: $x = X + \hat{x}$, $y = Y + \hat{y}$, $u = V_{in} + \hat{u}$, $d_1 = D_1 + \hat{d}_1$, $d_2 = D_2 + \hat{d}_2$, where *X, Y, V_{in}, D_1 and D_2* are steady state value, and $\hat{x}\ \hat{y}\ \hat{u}\ \hat{d}_1 \hat{d}_2$ is the small signal disturbance.

Based on the analysis, the duty cycle to output transfer function can be calculated as (6-18). Duty cycle to output transfer function of the single phase half bridge current doubler is plotted in Figure 6.5.

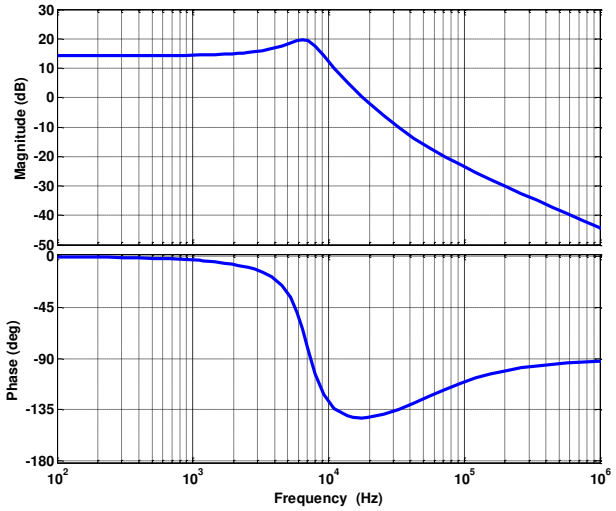


Figure 6.5. Bode plot of half bridge current doubler.

$$G_{vd}(s) = \frac{\hat{v}_O}{\hat{d}} = C(s \cdot I - A_{SS})^{-1}[(A_1 + A_2 - 2 \cdot A_3) \cdot X_{SS} + (B_1 + B_2 - 2 \cdot B_3) \cdot V_{in}] \quad (6\text{-}18)$$

6.1.2. Modeling of input series and output paralleled (ISOP) converter

With common duty cycle control of input series output paralleled (ISOP) converter as shown in Figure 6.6, only a single compensator is implemented in the system; therefore, it is possible to represent the ISOP converter with a single converter. Based on the analysis in [58], under the conditions that 1) all the cells are identical and 2) input capacitor is sufficiently large, the ISOP system can be represented by single converter.

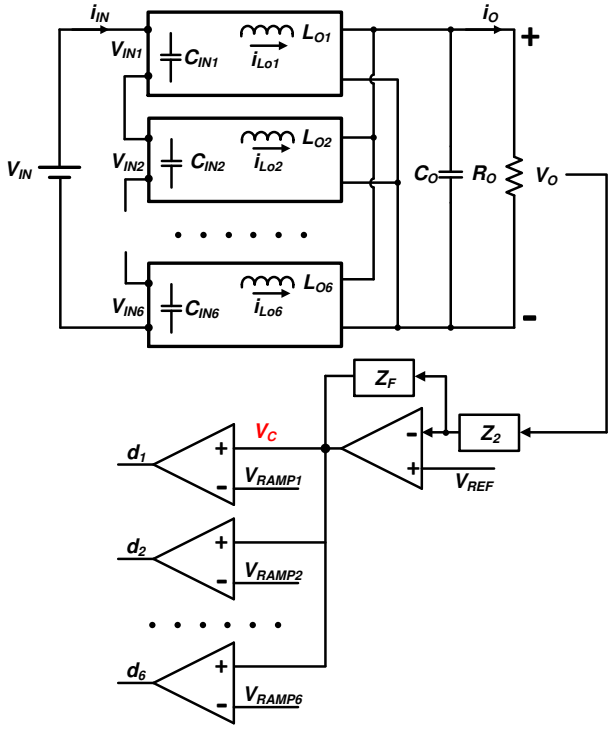


Figure 6.6. Control diagram of common duty cycle controlled ISOP converter.

Figures 6.7 and 6.8 are the Simplis simulation comparison between two phase interleaved half bridge converter transfer function and equivalent single phase half bridge current doubler after scaling. The input voltage of the single phase converter is ½ and the load is the same as two phase converter. With interleaving control, the output inductor of the single phase should

be ½ of the inductance as the inductance in the two phase converter and the switching frequency is two times the switching frequency of single converter [87]. As shown in Figure 6.7 and Figure 6.8, the two transfer function are almost the same except for a small variation at the switching frequency, which is not important in terms of regulating the output voltage because the control bandwidth is much lower than the switching frequency. Therefore, it is possible to design the compensator based on a single converter. The mismatches of components in the circuit will be discussed in a later part of this chapter.

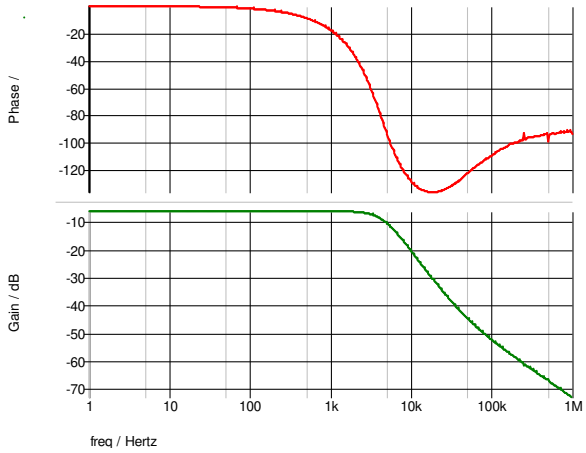


Figure 6.7. Bode plot of two phase interleaved half bridge current doubler.

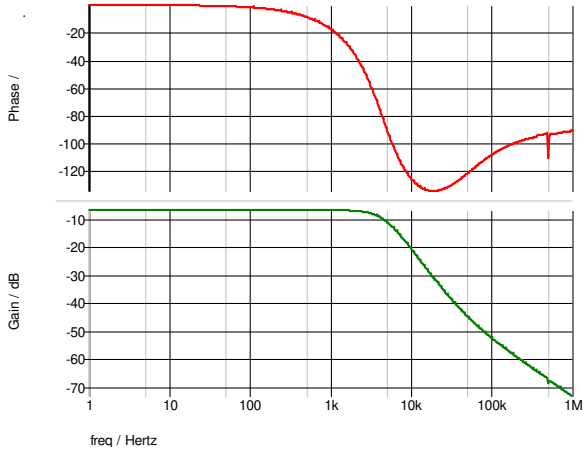


Figure 6.8. Bode plot of equivalent single phase half bridge current doubler.

6.2. Adaptive voltage positioning (AVP) control of half bridge current doubler

Adaptive positioning control (AVP) control as shown in Figure 6.9 is implemented for the on-board power supplies [88]-[92]. AVP control allows the voltage spikes to be the entire voltage tolerance window while the constant output voltage control only allows the voltage pulse being half of the voltage tolerance window. With the small voltage window for on-board power supply, AVP allows larger voltage pulse and simplifies the compensator design.

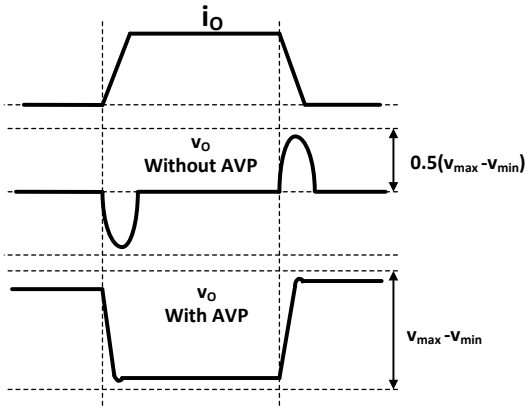


Figure 6.9. Transient with and without AVP control.

Based on the operation principle of AVP, the converter can be simplified with a constant voltage source (V_{max}) in series with a resistance (R) as shown in Figure 6.10. Therefore, controlling the converter with constant output impedance is the key feature to realize AVP [88].

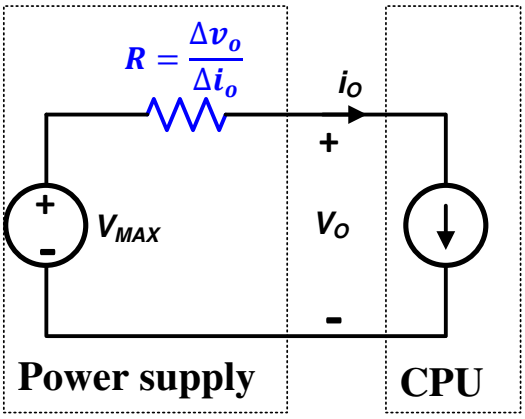


Figure 6.10. Equivalent circuit of POL converter.

Based on earlier discussion, the six phase ISOP system is simplified into a half bridge current doubler with scaling for compensator design. The control diagram is presented in Figure 6.11 [89]. A sum of the actual output voltage (V_o) and the droop voltage (V_{droop}= R_{droop}×I_O) is compared with a constant reference voltage (V_{ref}) to realize AVP control.

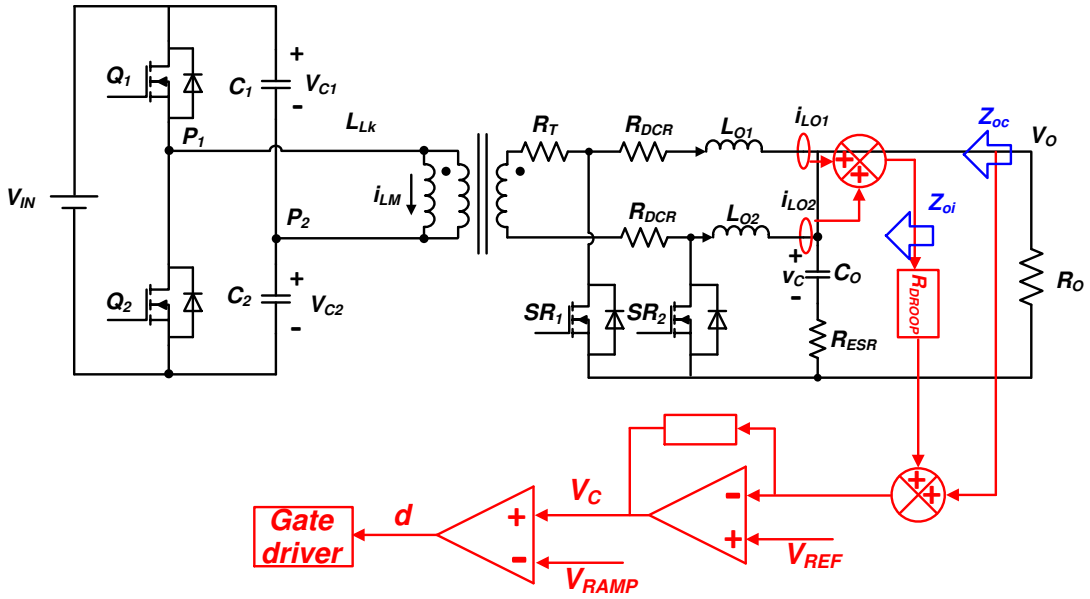


Figure 6.11. Implementation of AVP control of half bridge current doubler.

Based on the small signal analysis, the open loop output impedance of the half bridge current doubler is expressed as following:

$$Z_o = \frac{v_o(s)}{i_o(s)} = R_L \cdot \frac{\left(1+\frac{s}{\omega_{ESR}}\right)\cdot\left(1+\frac{s}{\omega_L}\right)}{\Delta} \tag{6-19}$$

where $\Delta = 1 + \frac{s}{Q\cdot\omega_o} + \frac{s^2}{\omega_o}$, $Q = \frac{1}{\omega_o}\cdot\frac{1}{R_C C_o + \frac{L_{O\_EQ}}{R_O}}$, $\omega_{ESR} = \frac{1}{R_{ESR}C_O}$, $\omega_L = \frac{R_L}{L_{O\_EQ}}$,

$\omega_O = \sqrt{\frac{R_O C_O}{L_{O\_EQ}C_O(C_O+R_O)}}$, and $L_{O\_EQ} = \frac{L_O}{N_{phase}}$.

The small signal control block diagram of AVP control shown in Figure 6.11 is illustrated in Figure 6.12. T_i and T_v are the loop gain functions and they are defined in (6-20) and (6-21) [89].

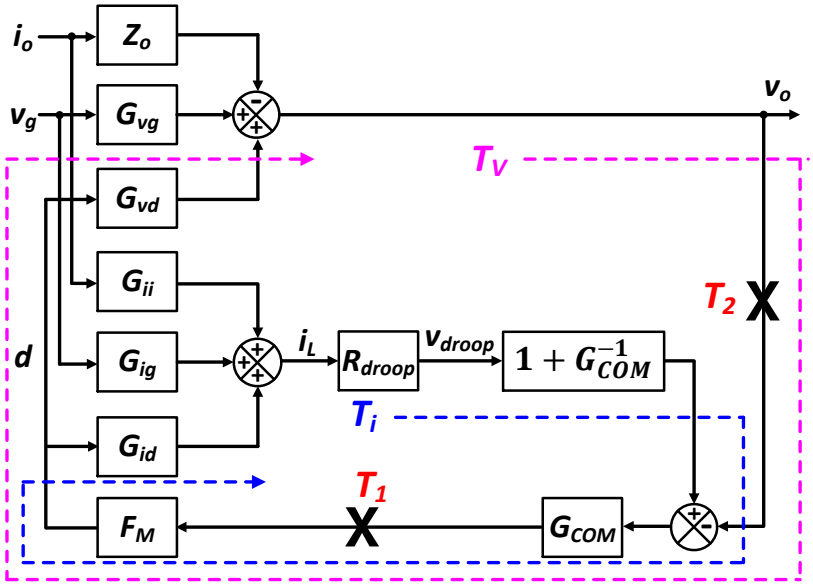


Figure 6.12. Small signal block diagram of closed loop half bridge current doubler.

$$T_v(s) \equiv F_m \cdot G_{vd}(s) \cdot G_{com}(s) \tag{6-20}$$

$$T_i(s) \equiv F_m \cdot G_{id}(s) \cdot R_{droop}(1 + G_{com}(s)) \tag{6-21}$$

The output impedance transfer function Z_{oi} is defined as current loop closed but voltage loop open is shown in Figure 6.11, where $G_{ii}(s)$ is the inductor current to load current transfer function and $G_{id}(s)$ is the inductor current to duty cycle transfer function, $G_{vd}(s)$ is the duty cycle to ouput voltage transfer function, $G_{ig}(s)$ is the input voltage to inductor current transfer function, $G_{COM}(s)$ is the compensator's gain, and F_m is the modulator's gain. With current loop closed, the output impedance is actually increased compared with the open loop output impedance Z_o.

$$Z_{oi}(s) = Z_o(s) + \frac{T_i(s)}{1+T_i(s)} \cdot \frac{G_{vd}(s) \cdot G_{ii}(s)}{G_{id}(s)} \tag{6-22}$$

Equation (6-23) shows the output impedance Z_{oc} (shown in Figure 6.11) with both voltage and current loop closed. Based on (6-23), $T_2(s)$ defined as $\frac{T_v(s)}{1+T_i(s)}$ (as shown in (6-24)) is the outer loop gain of the converter which determines the control bandwidth and phase margin of the HV POL. Therefore, to reach constant $Z_{oc}(s)$, $T_2(s)$ needs to be properly designed. Then, based on (6-18), (6-19) and (6-22), the desired compensator $G_{COM}(s)$ can be designed.

$$Z_{oc}(s) = \frac{(1+T_i(s))\cdot Z_{oi}(s)}{1+T_i(s)+F_m\cdot G_{vd}(s)\cdot G_{com}(s)} = \frac{Z_{oi}(s)}{\frac{1+T_i(s)+T_v(s)}{1+T_i(s)}} = \frac{Z_{oi}(s)}{1+\frac{T_v(s)}{1+T_i(s)}} = \frac{Z_{oi}(s)}{1+T_2(s)} \tag{6-23}$$

$$T_2(s) = \frac{T_v(s)}{1+T_i(s)} \tag{6-24}$$

At high frequency beyond the control bandwidth of the compensator, the output impedance cannot be controlled and eventually becomes the ESR of the output capacitor. In order to achieve constant output impedance over frequency range, the droop resistance in the control loop (R_{DROOP}) should be equal to the ESR of the output capacitor, R_{ESR}. Therefore, the output impedance will be controlled to be R_{ESR} for the entire frequency range. Figure 6.13 illustrates the theoretical relationship among Z_o Z_{oi} and Z_{oc} [88][89]. As Intel requires 0.8 mΩ output impedance [92], output capacitor with 0.8 mΩ ESR is selected.

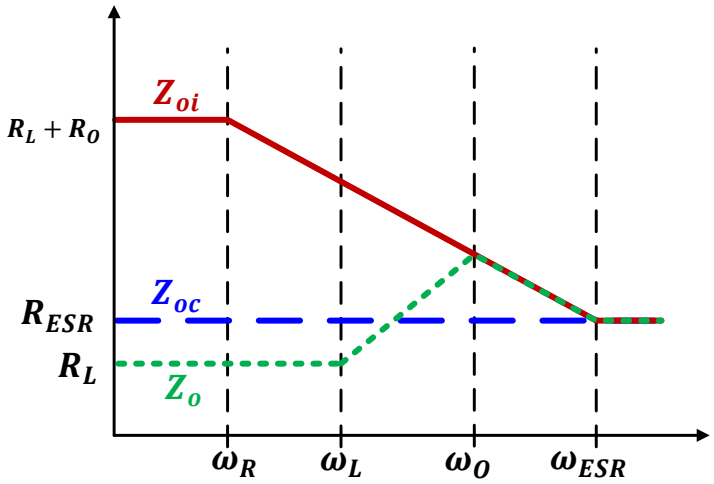


Figure 6.13. Comparison of Z_o, Z_{oi} and Z_{oc}.

Clearly shown in Figure 6.13, beyond the ESR frequency of the output capacitor ω_{ESR}, the open loop output impedance becomes R_{ESR} which means no compensation is required. Therefore, the bandwidth of $T_2(s)$ should be the ESR frequency of the output capacitance [88]. Also, under the following two assumptions, (1) $|T_i| \gg 1$ and (2) $|G_{COM}| \gg 1$ when $\omega < \omega_{ESR}$, T_2 can be approximated by (6-25) [89].

$$T_2 \cong \frac{R_o}{R_{esr}} \cdot \frac{1+\frac{s}{\omega_{esr}}}{1+\omega_R} \tag{6-25}$$

At the same time, Z_{oc} can be further simplified by (6-26) with $T_2(s)$ being simplified in (6-23).

$$Z_{oc} \cong R_{esr} \cdot G_{ii}(s) \tag{6-26}$$

From (6-26) it can be seen that in addition to the ESR of the output capacitor, the inductor current to output current transfer function (G_{ii}) also impacts the closed loop output impedance. As indicated in Figure 6.14, a larger inductance leads to a lower cutoff frequency (ω_0) of the output filter in the half bridge current doubler. As the control bandwidth is defined as f_{ESR}, which means at the desired control bandwidth, the compensator designed for larger output inductance needs to have larger gain compared with the converter with smaller output inductance, which leads to a larger duty cycle variation. In order to prevent the duty cycle saturation when load transient occurs, there would be a limitation on the maximum value of the output inductance as expressed in (6-27) [88].

$$L_{max} = \frac{V_{in}}{8n \cdot \Delta I_o \cdot f_c} \times \min(D, 1-D) \tag{6-27}$$

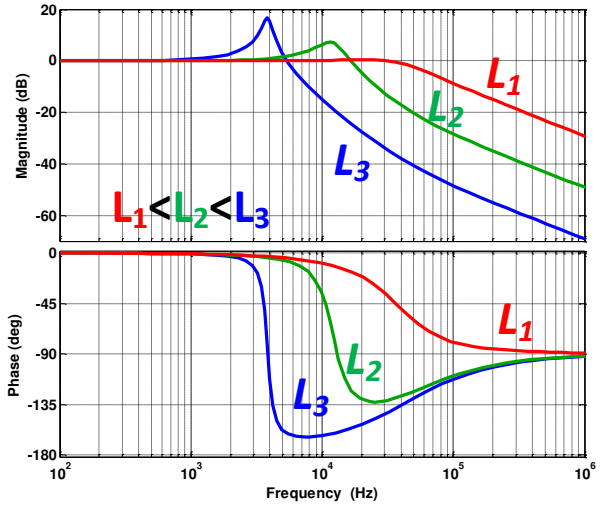


Figure 6.14. $G_{ii}(s)$ comparison with different output inductance.

Based on the above analysis, the desired compensator would have two requirements: (1) high gain at low frequency, (2) $T_2(s)$ crossover at ESR frequency. Therefore, a pole at origin is implemented in the compensator to have high gain at low frequency. A type III compensator is implemented and the outer loop transfer function T_2 is presented in Figure 6.15 with the crossover frequency of 42 kHz, which is the same as the f_{ESR} based on components selection in Table 6.1. The switching frequency of a single converter is 280 kHz and with interleaving among phases, 42 kHz control bandwidth can be easily obtained for the ISOP system.

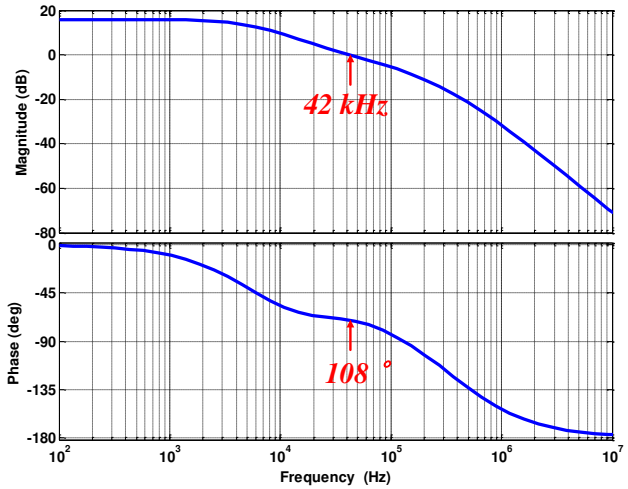


Figure 6.15. Outer loop gain $T_2(s)$.

The three impedances are also plotted in Figure 6.16 based on the designed compensator, from which we can see almost constant closed loop output impedance is achieved with slight variation around the cutoff frequency of the converter's output filter.

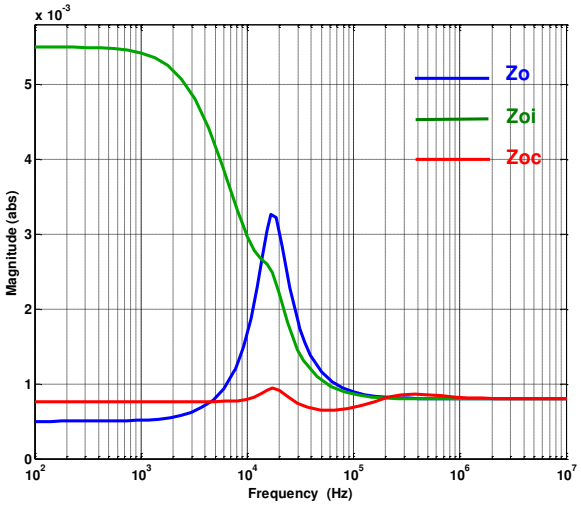


Figure 6.16. Analytical output impedance comparison among Z_o, Z_{oi} and Z_{oc}.

Based on the analysis in this section, it can be seen that the proposed HV POL can be controlled with constant output impedance, which is the key feature to meet the adaptive voltage positioning (AVP) requirement of the on-board power supply.

6.3. Common duty cycle control of ISOP converter with mismatches

Earlier discussions are all based on the assumption that the components in the input series output parallel (ISOP) connected system have identical values with common duty cycle control. However, mismatches are inevitable in reality. In this section, the impact of mismatches among modules is analyzed in two aspects, (1) the impact on current and voltage sharing among the modules and (2) the impact on output voltage regulation performance of the ISOP system considering the compensator is designed under the identical components assumption. For simplicity of analysis, two phase interleaved ISOP connected converter is analyzed here instead of six phases as presented in Figure 6.17. However, the same principle can be applied to the six

phases' case. Furthermore, any mismatch in the two phases ISOP system is more apparent compared with the same mismatch in a six phase ISOP system. Therefore, the impact of mismatch is most severe in two phase ISOP system which is discussed here.

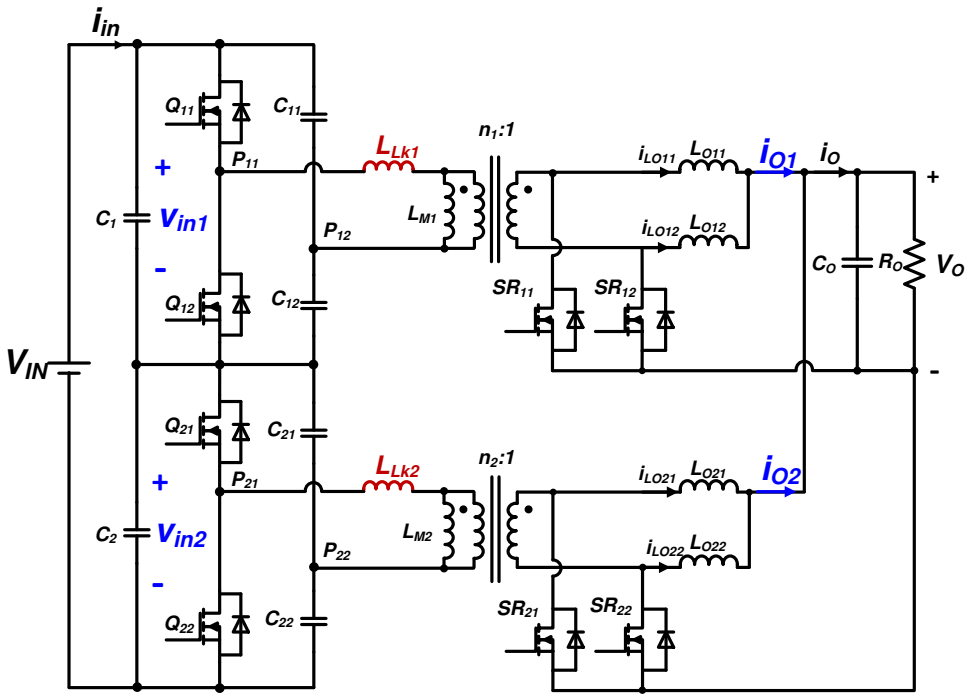


Figure 6.17. Two phase ISOP connected half bridge current doubler.

6.3.1. Sharing among phases with mismatches

As the two modules are ISOP connected, then the even sharing of input current and output voltage is enforced and (6-28) and (6-29) are satisfied under any circumstance assuming the two modules have comparable efficiency:

$$\frac{V_{in1}D_{eff1}}{n_1} = \frac{V_{in2}D_{eff1}}{n_2} = V_o \tag{6-28}$$

$$\frac{I_{O1}D_{eff1}}{n_1} = \frac{I_{O2}D_{eff2}}{n_2} = I_{in} \tag{6-29}$$

where n_1 and n_2 are the turns ratio of each converter, D_{eff1} and D_{eff2} are the effective duty cycle of each converter, V_{C1}, V_{C2} , I_{L1} and I_{L2} are the input voltage and output current for each converter as marked in Figure 6.17.

Also, the effective duty cycle can be calculated as (6-30) and (6-31). Even though the same duty cycle is applied to both converters, different leakage inductances will cause different duty cycle losses as they take different amount of time to be charged and discharged [19]. Therefore, different effective duty cycles are seen by the two converters, which will cause uneven sharing eventually.

$$D_{eff1} = D - \Delta D_1 = D - \frac{2I_O}{n_1}\frac{L_{lk1}}{DV_{in1}T_s} \tag{6-30}$$

$$D_{eff2} = D - \Delta D_2 = D - \frac{2I_O}{n_2}\frac{L_{lk2}}{DV_{in2}T_s} \tag{6-31}$$

Rewriting (6-28) and (6-29) with (6-30) and (6-31) plugged in, input voltage and output current of two modules can be expressed as:

$$\frac{V_{in1}}{V_{in2}} = \frac{I_{01}}{I_{o2}} = \frac{n_1\left(D-\frac{2I_O \quad L_{lk2}}{n_2 \, DV_{in2}T_s}\right)}{n_2\left(D-\frac{2I_O \quad L_{lk1}}{n_1 \, DV_{in1}T_s}\right)} \tag{6-32}$$

Based on (6-32), input voltage and output current sharing depends strongly on the following parameters in the circuit: transformer turns ratios (n_1 and n_2), leakage inductances (L_{lk1} and L_{lk2}). The effect of these elements will be discussed one by one in the following section. Based on (6-32), the input voltage and output current have the same sharing ratio; in the following discussion, only output current sharing will be discussed.

Besides steady state sharing, transient sharing is also important to ensure stable operation of the ISOP system. Therefore, current sharing between two phases during a load transient has been simulated with PSIM.

1. Transformer turns ratio mismatch

First, only the difference in transformers' turns ratio is considered, leakage inductance and output inductance are the same in the two converters. As in Figure 6.17, converter 1's turns ratio is 7:1 and converter 2's turns ratio is 6:1. This difference is set on purpose to show how turns ratio affects current sharing as in (6-30). Leakage inductance for both converters is 0.1 μH and the output inductor is 220 nH. From Figure 6.18, it can be seen that converter with a higher turns ratio carries higher current both in steady state and during transients.

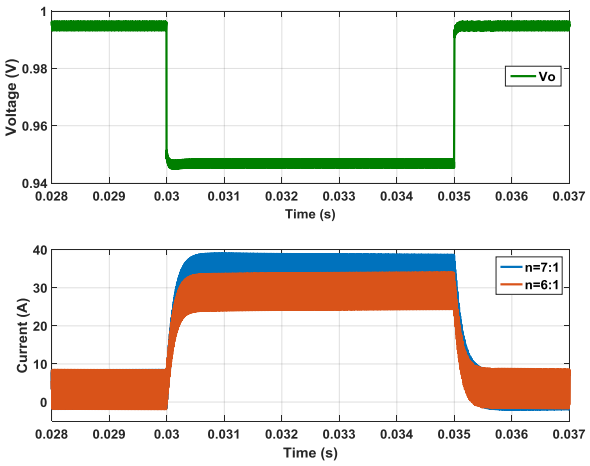


Figure 6.18. Output current sharing for different turns ratio.

However, for a planar transformer with printed circuit winding, it is almost impossible to have turns ratio mismatch between modules. Even if there is some mismatch, it is fairly easy to discover and eliminate by selecting transformer with the same turns ratio. Therefore, the mismatch caused by transformer turns ratio can be neglected.

2. Transformer leakage inductance mismatch

For different leakage inductances, the duty cycle losses on the two converters are different, therefore, the effective duty cycles are different on the two converter modules (the duty cycle

from the controller are the same for the two modules). Based on (6-28) and (6-29), the input voltage and output current will show some mismatch in the two converter modules. Unlike transformer turns ratio difference, leakage inductance difference exists in the transformer design and fabrication even with advanced transformer techniques and it also includes the connection between the transformer and the power stage, therefore, it is necessary to evaluate the effectiveness of common duty cycle control for the ISOP converters. Figure 6.19 shows the mismatch caused by leakage inductance alone (L_{lk1}=0.2 μH and L_{lk2}=0.1 μH) while other parameters are the same (n_1=n_2=6 and L_{O11}=L_{O12}=L_{O21}=L_{O22} =220 nH in Figure 6.17) in the ISOP system. The difference minor even for the large variation of leakage inductances as shown in Figure 6.19 in both steady state and during transient. Even though leakage inductance tends to be different between modules, its influence on current sharing is limited.

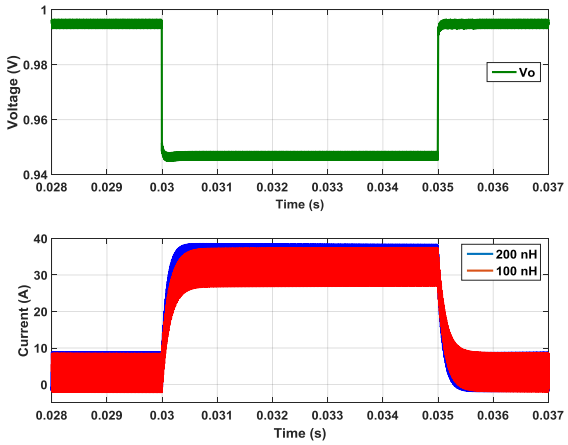


Figure 6.19. Output current sharing for different leakage inductance.

3. Output inductance mismatch

Even though the output inductor is not a factor impacting steady state current sharing in (32), the output inductor is a key element for transient performance of the ISOP system. Therefore, different output inductances have also be simulated to show the influence on current

sharing of the ISOP converter. The transformer turns ratio and leakage inductance is the same in the two modules, while L_{O11}=440 nH and L_{O12}=L_{O21}=L_{O22} =220 nH as in Figure 6.17. It clearly shows that the steady state average current sharing is the same with current ripples between the two modules being different. Current during transient is not even between the two modules. The converter with both output inductances being *220* nH has a faster transition with slight overshoot while the converter with one inductance being *440* nH experiences a slower transition without overshoot. The difference between the two modules is minor and current values of both modules are still within the designed margin even for the unrealistic large variation of output inductors.

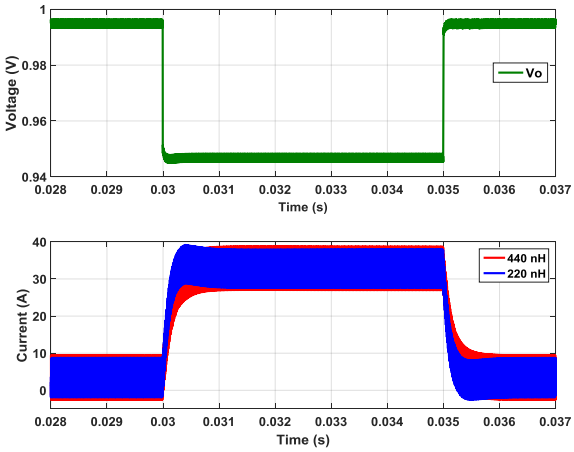


Figure 6.20. Output current sharing for different output inductance.

Based on simulation results, common duty cycle control of input series and output parallel (ISOP) connected converter is capable reaching steady state even with mismatches in the circuit.

6.3.2. Impact on output performance of ISOP system with mismatches

Besides the sharing among modules, the output transient performance might also be different with mismatched modules compared with identical modules when the same

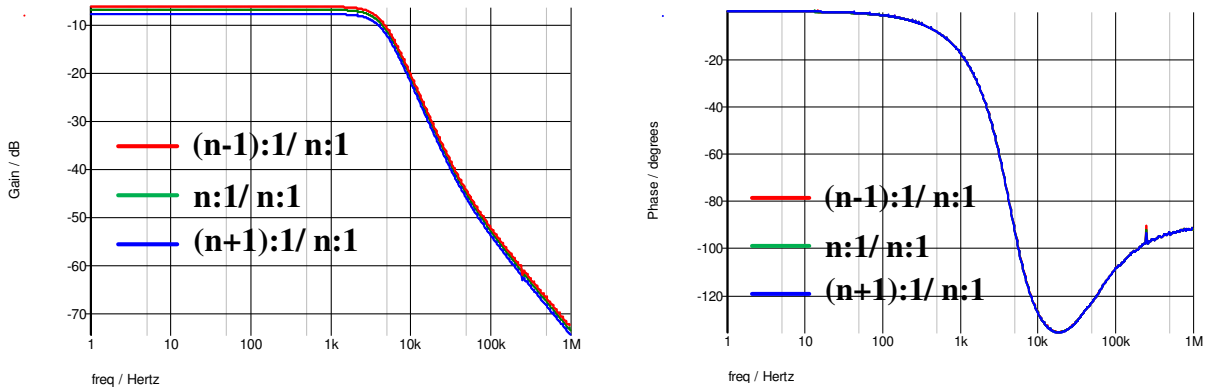
compensator is used. Because of the strict dynamic voltage regulation requirement of the on-board power supplies, the possible impact of mismatches among modules on the output voltage regulation is investigated here. The closed loop transfer function depends on both the power stage transfer function and the compensator's gain. The compensator here is to control the output voltage and is not designed to control the sharing among modules. Since the compensator stays the same with common duty cycle control, the amount of variation in the power stage transfer function of the ISOP system can represent the amount of variation in the closed loop transfer function with or without mismatches. If the power stage is hardly being impacted by the mismatches among modules, with the same compensator, the output voltage regulation performance will also be unaffected. The transfer function of the ISOP system with mismatched modules has also been simulated by Simplis software and compared with a system with the same parameters.

Similar to the earlier section, three mismatches are evaluated in the circuit: 1) transformer turns ratio, 2) leakage inductance, and 3) output inductor. Out of the two phases ISOP connected system; one module is operated with the designed values under all the conditions, and the other module with one parameter changing at a time. Therefore, the impact of the particular component can be clearly observed though simulation.

1. Transformer turns ratio mismatch

Figure 6.21 shows the transfer function from duty cycle to output voltage with different transformer turns ratio in the ISOP system. The green curve (in the middle) shows when the two modules have the same turns ratio, which is the condition for which the compensator is designed, while the blue is the one module with one less primary side turn and red with one more primary side turns. Based on Simplis simulation, it can be seen that the impact of the

transformer turns ratio on the ISOP system's transfer function is relatively minor and most of the difference is below the double pole frequency of the output filter which can easily be compensated by having a pole at the origin in the compensator. Therefore, the compensator designed with identical components in the two modules is capable to regulate the output voltage as desired even with the different transformer turns ratio in the ISOP system.

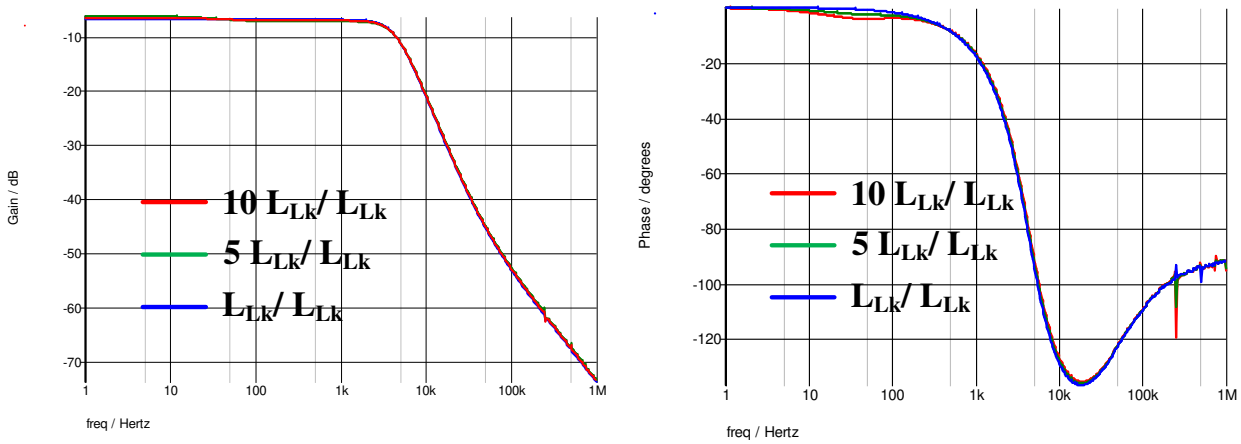


(a) Gain (b) Phase

Figure 6.21. ISOP system with unbalanced transformer turns ratios.

2. Transformer leakage inductance mismatch

Figure 6.22 show the transfer function from duty cycle to output voltage of the ISOP system with different leakage inductances between the two modules. The blue line in the plots is for both modules having the same leakage inductance, and the green line and red line is for one module to have five times and ten times larger leakage inductance compared with the other module, which is unrealistically large and is used here to observe the differences. Similar to transformer turns ratio, the difference is minor and most occurs before the double pole of the output filter. Therefore, with the origin pole in the compensator, the minor difference can be ignored from the closed loop transfer function, which also indicates the compensator designed works well even with different leakage inductances between two phases in the ISOP system.

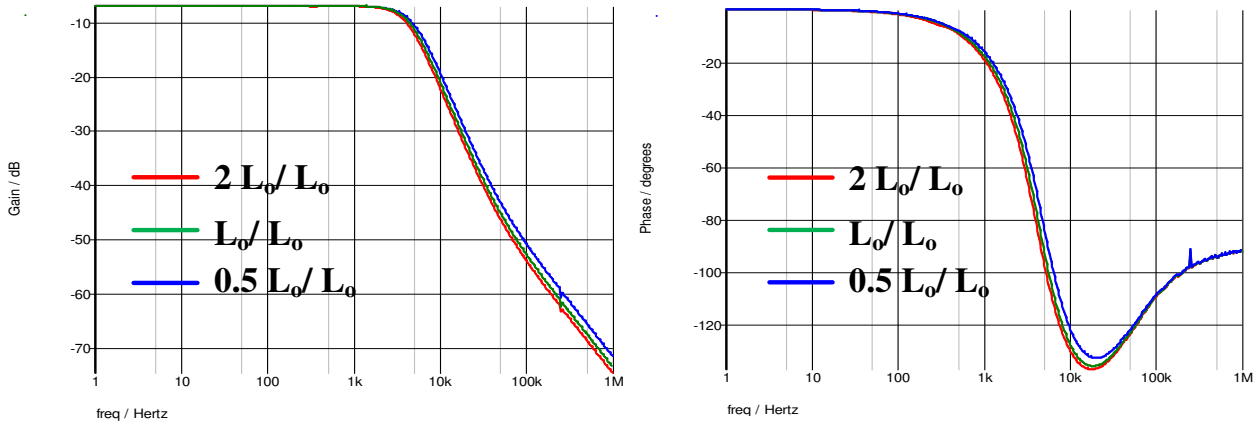


(a) Gain (b) Phase

Figure 6.22. ISOP system with unbalanced leakage inductance.

3. Output inductor mismatch

Figure 6.23 shows the transfer function from duty cycle to output voltage of the ISOP system with different output inductors. The green line is which all the four output inductors being the same in the two phase interleaved half bridge current doubler. The blue line is when one inductor out of the four is ½ of the rated value and the red line is when one inductor becomes 2 times of the rated value. Also, the difference simulated here is larger than the tolerance from the inductor vendor. The inductor used here has 10 % tolerance. The difference of transfer function when mismatches of output inductance exist is still minor (less than 5% for both gain and phase under the same frequency) even with unrealistically large mismatches in the ISOP. The difference will become even smaller with more phases adding to the ISOP system. Therefore, the compensator designed with identical inductors should still be valid even with different output inductance in the ISOP system.



(a) Gain (b) Phase

Figure 6.23. ISOP system with unbalanced output inductors.

Based on the above analysis, even though the mismatches among modules are inevitable, 1) the unbalance will not cause unstable operation of ISOP system and thus stable operation can be assured; 2) even though current sharing among phases in uneven, the factor that contributes most is the transformer turns ratio which is almost impossible to be different from one another, other mismatches have limited impact on current sharing; 3) all those mismatches has very limited influence on the ISOP system's transfer function; therefore, it is valid to design the whole system's compensator based on equivalent single phase circuit which is implemented here.

6.4. Experimental verification

The ISOP connected system is tested starting with one phase and gradually increased to six phases. The components such as MOSFET, inductor and transformer are not pre-selected so that they would have identical parameter, and, therefore, certain mismatches exist in the system, yet stable operation can be achieved with common duty cycle control.

Transient testing is also performed when load is changing between 10% and 100% of the rated output power. When more phases are added to the system, the load also becomes heavier correspondingly, therefore, the transfer function of the ISOP system is changing at the same time as shown in Figure 6.24 where the duty cycle to output transfer function is plotted from one all the way to six phases. During the process of adding more phases, the compensator is tuned to meet the AVP requirement.

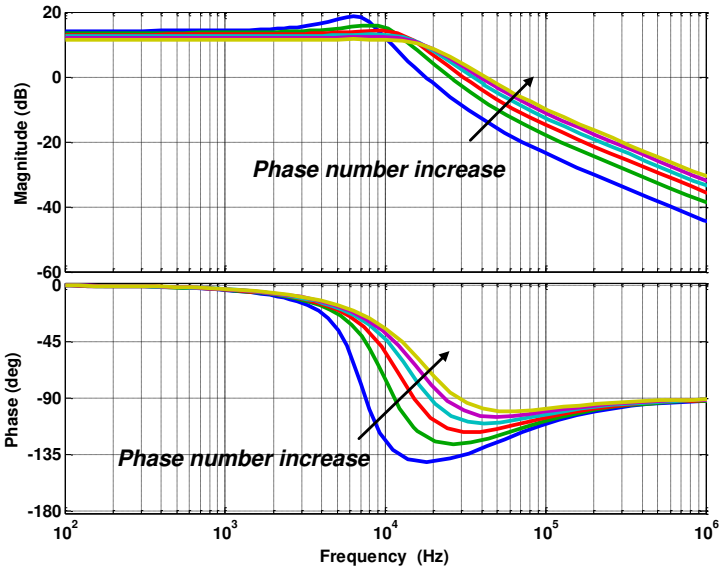


Figure 6.24. Transfer function of multiphase ISOP connected converter.

Even though, with ideal AVP control, no overshoot or undershoot would occur during the load transient, however, in reality, overshoot and undershoot will still occur and Intel has defined the requirement of overshoot as shown in Figure 6.25 [92]. When a load transient occurs, the overshoot should not exceed the maximum voltage (when no load is connected) for more than 25 µs.

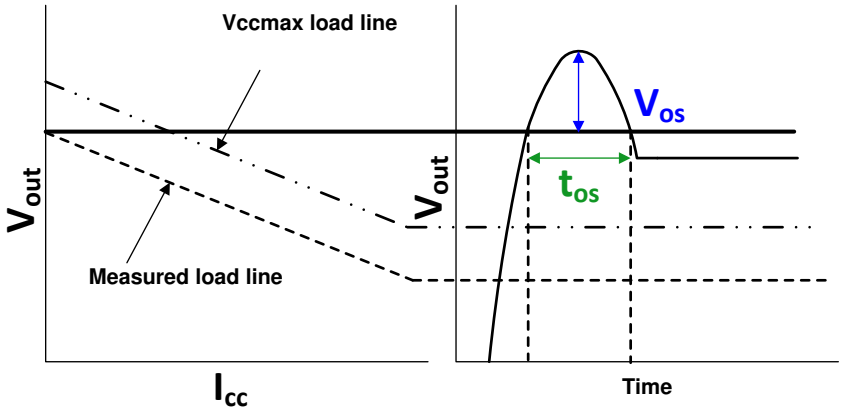


Figure 6.25. Overvoltage requirement during load transient.

Figure 6.26 and Figure 6.27 are the experimental results of six phases ISOP HV POL with 200 A output current, which is beyond the current requirement from Intel (100 A) [92]. A zoomed in transition when the load is charging from 100% to 10% is also given to show the output voltage meets the overshoot requirement. The overshoot time and voltage is based on the maximum voltage where no load is connected to the converter as V_{ccmax} in Figure 6.25. The voltage values without load in Figure 6.27 are obtained by adding the voltage change between 0% and 10% load to the voltage values with 10% load. Therefore, the baseline in the zoomed in waveforms which is the blackline in Figure 6.27 are higher than the voltage level with 10% load. Based in Figure 6.27, decent dynamic response with AVP control of multiphase ISOP connected half bridge current doubler can be achieved. One reason for the overshoot voltage during load stepping down transient is the parasitics (like ESL in the output capacitor, the parasitics resistance and inductance between the converter and load) in the converter. During the analysis of output impedance as discussed in Section 6.2, there is variation of output impedance over frequency even though the the stray resistance and inductance is not being considered. With extra parasitics in the actual test set up, the peak of the output resistance will be increased compared with the results shown in Figure 6.16.

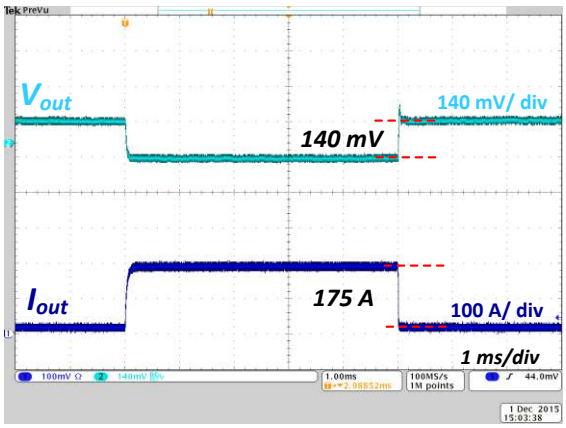


Figure 6.26. Output voltage and current transient between 10% and 100% load with six ISOP phases.

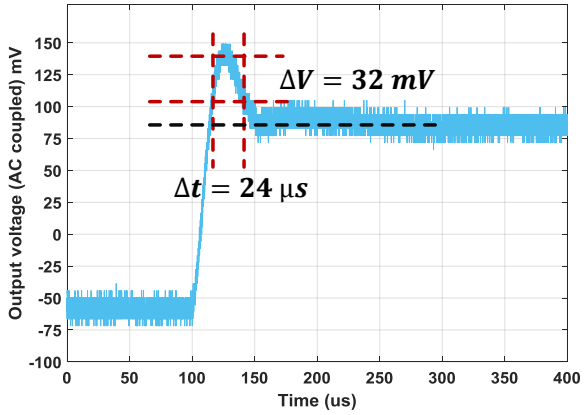


Figure 6.27. Zoomed in overshoot voltage during load stepping down with six ISOP phases.

Based on the experimental results, it shows that the single power stage power conversion architecture with the input series output parallel connected half bridge current doubler is capable to achieve adaptive voltage positioning control. At the same time, the ISOP system does not require extra tuning of converters to assure stable operation, which simplifies the system design. Combined with discussion in Chapter 5, the single power stage also helps to increase the system efficiency. Therefore, single power stage HV POL is capable of meeting on-board power supply requirement with higher efficiency compared with conventional architecture.

6.5. Summary

In this chapter, the six phase input series and output parallel (ISOP) connected half bridge current doubler to realize high voltage point of load (HV POL) with adaptive voltage positioning (AVP) is built in prototype and tested.

First, the transfer function of the ISOP system is derived based on state space model and properly scaling the components and frequency. Second, the compensator to realize adaptive voltage positioning control on a half bridge current doubler is analyzed. Constant output impedance can be obtained with a conventional type III compensator. Third, the impact of mismatches among circuit modules is performed on both current and voltage sharing among modules and the accuracy of designed compensator is verified under identical components assumption. Based on simulation results, the ISOP system is not sensitive to circuitry mismatches and stable operation can be obtained with large mismatches. In the end, the experimental results are given to prove that the proposed architecture is capable to meet the on-board power supplies requirement with a higher efficiency compared with state of the art products.

7. Conclusion and Future Work

7.1. Conclusions

7.1.1. Summary of the work

In this dissertation, an alternative power supply architecture for data centers is proposed in order to increase the efficiency and to reduce energy cost from the high voltage DC (HVDC) distribution voltage to the electric load on the motherboard.

Various power supplies architectures are available in the market, however, all of which contains several power stages in series. The overall efficiency of the power supply system becomes the product of each stage's efficiency. Even though, a single stage's efficiency may be decent (> 90 %), the overall system efficiency is limited.

In order to achieve higher efficiency, in this dissertation, a single stage power supply architecture is proposed converting from 400 V to 1 V directly with the capability of isolation, regulation and voltage transformation, which is named high voltage point of load (HV POL) architecture. Input series and output parallel (ISOP) connected structure is implemented with interleaving control so that 1) single converter can be designed with a lower transformer turns ratio which helps to reduce winding loss, 2) higher equivalent switching frequency can be achieved with the potential for higher control bandwidth.

Within the structure of input series and output parallel structure, two converter topologies are considered, phase shift full bridge converter and half bridge current doubler. For the phase shift full bridge converter, hardware prototypes are built with both Si and GaN devices targeting higher efficiency. The impact of primary side MOSFET's junction capacitances on the

phase shift full bridge converter's operation and efficiency is analyzed and verified through experiments. The full load efficiency of the proposed method can reach 89.1%.

In chapter 5, a half bridge current doubler is also implemented for the proposed HV POL. Both symmetrical and asymmetrical control is evaluated based on the requirement specifications. Simulation and analysis shows that the symmetrical control has better efficiency even though asymmetrical control allows zero voltage switching (ZVS) of the primary side devices under heavy load condition, yet it means higher RMS current and larger duty cycle loss. A load dependent soft switching method for primary side devices is proposed with the help of an auxiliary circuit including an air-core inductor, a diode, and two active switches which allow ZVS for the entire load range without adding current stress to the power stage devices. A prototype has been built and the proposed method is verified through experiments. It shows that the proposed soft switching method provides higher efficiency compared with both conventional hard switching and constant charging time soft switching proposed in the literature. The full load efficiency of the proposed method is above 90 %, which is about 4 % higher than the power supplies architecture available on the market.

In chapter 6, the six phase input series output parallel connected half bridge current doubler is designed and built. Adaptive voltage positioning (AVP) is the key feature of on-board power supplies, therefore, the compensator design of half bridge current doubler is analyzed in detailed to meet the AVP requirement. Also, the mismatches among the ISOP connected system is simulated in PSIM and Simplis, which indicates that with common duty cycle control, mismatches are allowed in the system to reach stable operation and to ensure the accuracy of the compensator even though the compensator is designed with identical modules. The ISOP structure is not sensitive to mismatches in the system of the half bridge current

doubler, which is favoring the system since mismatches are inevitable in reality. In the end, the hardware prototype testing results are giving from one phase to six phases. The experimental results indicate that the proposed architecture is capable to behave as the on-board power supply modules.

7.1.2. Contributions

The contributions of this work are summarized as follows:

1. A single stage power supply architecture is proposed to improve the power supply efficiency from 400 V to 1 V directly, expecting to reduce power delivery and power conversion losses at the same time. The full load efficiency at room temperature of proposed HV POL with both full bridge and half bridge is over 3% point higher compared with commercial products.

2. The impact of output junction capacitance of primary side MOSFETs in the phase shift full bridge converter on the transformer current and converter's efficiency is analyzed and verified in experiment. In order to design a high efficiency converter, the impact of the output junction capacitance needs to be considered.

3. A load dependent soft switching method is proposed for half bridge current doubler which allows higher efficiency compared with conventional hard switching in a wide load range. The proposed method can achieve ZVS for the entire load range and the current stress in the auxiliary components reduces as load reduces.

4. Adaptive voltage positioning control has been successfully applied to half bridge current doubler topology with input series output parallel structure (ISOP) with large dynamic current change (175 A). Therefore, the proposed HV POL is feasible for onboard power supplies with higher efficiency.

7.2. Future work

The following areas can be considered as future work in order to more fully develop a HV POL converter.

1. At this time, Oscon capacitor is used for transient testing because the control bandwidth is limited by switching frequency. The ESR of the Oscon capacitor is much larger than the ceramic capacitor, which means the ESR zero ($\frac{1}{2\pi C \times ESR}$) of the Oscon capacitor is at much lower frequency than the ESR zero of ceramic capacitor with same ESR. Therefore, the control bandwidth can be much lower with Oscon capacitor compared with ceramic capacitor. Table 7.1 shows an example [89]. However, the drawback of Oscon capacitor compared with ceramic capacitor is the size. In order to improve the power density of proposed HV POL, replacing the Oscon capacitor with ceramic capacitor is an effective way. In order to allow ceramic capacitor, the switching frequency of proposed HV POL needs to be increased. Assuming the control bandwidth is 1/6 of switching frequency, the converter in the proposed HV POL needs to be switched at 550 kHz to allow the ceramic capacitor listed in Table 7.1.

Table 7.1. Comparison between Oscon and ceramic capacitors

Capacitor type	Capacitance (μF)	ESR (mΩ)	ESR frequency (Hz)
Oscon	9840 (820x12)	1 (12/12)	16.17 k
Ceramic	200 (100x2)	0.75(1.5/2)	1.1 M

2. With increased switching frequency, the switching loss, gate driving loss and reverse recovery loss will increase linearly, which will jeopardize the converter's efficiency. Replacing currently used Si MOSFETs with wide bandgap power devices, such as GaN, can allow the converter to maintain high efficiency even with higher switching frequency.

3. In the ISOP connected system, a current sensor is implemented for each inductor; therefore, twelve current sensors in total are required to get accurate current information, which increases the cost and complexity of the whole system. Multiple current sensing is also required for the multiphase buck converter in the conventional IBA architecture. The ISOP connected system ensures even sharing of input current; therefore, there is only one current value at the input side of ISOP, which allows one current sensing of the input current rather than 12 current sensing at the output side. Therefore, input current sensing is a effective method is reduce the number of current sensors.

Reference

[1] Intel: Moore's law will continue through 7 nm chips.
Available online: http://www.overclock.net/t/1542835/pc-world-intel-moores-law-will-continue-through-7nm-chips

[2] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," *IEEE Journal of Solid State Circuits*, vol. 32, no. 8, pp. 1210-1216 August 1997.

[3] S. Saewong and R. Raikumar, "Practical voltage scaling for fixed-priority RT-systems," *Ninth IEEE Real-Time and Embedded Technology and Application Symposium,* May 2003, pp. 106-115.

[4] Jai Wei, "High frequency high-efficiency voltage regulators for future microprocessors," Ph.D. Dissertation, Virginia Tech, 2004.

[5] Kisun Lee, "Advanced control schemes for voltage regulators," Ph. D. Dissertation, Virginia Tech, 2008.

[6] Julu Sun, "Investigation of Alternative Power Architectures for CPU Voltage Regulators," Ph. D. Dissertation, Virginia Tech, 2008.

[7] Yole Development, "New Technologies and Architecture for Efficient Data Center", July 2015.

[8] A. Pratt, P. Kumar, T. V. Aldridge, "Evaluation of 400V DC distribution in telco and data centers to improve energy efficiency," *29th IEEE international Telecommunications Energy Conference,* Sept. 30 2007-Oct. 4, 2007, pp. 32-39.

[9] A. Pratt, P. Kumar, K. Bross, T. Aldridge, "Powering compute platforms in high efficiency data centers," *IBM Technology Symposium*, 2006.

[10] G. Warkozek, E. Drayer, V. Debusschere, S. Bacha, "A new approach to model energy consumption of servers in data centers," in *Proc. Int. Conf. Ind. Tech ,* 2012, pp. 211-216.

[11] U. Hoelzle, B. Weihl, "High-efficiency power supplies for home computers and servers," from Google website.
http://static.googleusercontent.com/external_content/untrusted_dlcp/services.google.com/en/us/blog_resources/PSU_white_paper.pdf

[12] J. Janick, "IBM Systems and Technology Update," *IBM Technology Symposium*, 2007.

[13] "Power Pod Design Specification," Intel Document No. 10956.

[14] F. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504-510, Mar/Apr 2003.

[15] A. Stupar, T. Friedli, J. Minibock, and J.W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V DC distribution systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1732-1744, April 2012.

[16] F. Xu, B. Guo, L. M. Tolbert, F. Wang, and B. J. Blalock, "An all-SiC three-phase buck rectifier for high-efficiency data center power supplies," *IEEE Transactions on Industry Applications*, vol. 49, no. 6, pp. 2662-2673, Nov./Dec. 2013.

[17] R. Greul, S. D. Round, J. W. Kolar, "The Delta-rectifier: analysis, control and operation," *IEEE Transactions on Power Electronic*, vol.21, no.6, pp.1637-1648, Nov. 2006.

[18] Emerson AC-DC Power supplies.
http://www.emersonnetworkpower.com/documentation/enus/brands/netsure/documents/netsure-4015 system.pdf

[19] Bo Yang, "Topology investigation of front end DC/DC power conversion for distributed power system," Ph. D. Dissertation, Virginia Tech, 2003.

[20] D. Li, X. Ruan, "Comparison of three front-end DC-DC converters for 1200w server power supply," *IEEE Power Electronics Specialists Conference*, 16-16 June 2005, pp. 394-398.

[21] Vicor DC-DC converters. http://www.vicorpower.com/

[22] W. Zhang, Z Xu, Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, "Evaluation of 600 V cascode GaN HEMT in device characterization and all-GaN-based LLC resonant converter," *IEEE Energy Conversion Congress and Exposition (ECCE),* 15-19 Sept. 2013, pp. 3571-3578.

[23] ZVS buck regulator from Picor: http://cdn.vicorpower.com/documents/datasheets/Picor/ds_pi34xx-00.pdf

[24] David Reusch, "High frequency, high power density integrated point of load and bus converters," Ph. D. Dissertation, Virginia Tech, 2012.

[25] H. Chen, X. Wu, "LLC resonant DC transformer (DCX) with parallel PWM output tight regulation," *IEEE Energy Conversion Congress and Exposition (ECCE),* pp. 4742-4747, 14-18 Sept. 2014.

[26] B. Yang, F. C. Lee, A. J. Zhang, G. Huang, "LLC resonant converter for front end DC/DC conversion," *IEEE Applied Power Electronics Conference (APEC)*, pp.1108-1112, 2002.

[27] Y. Ren, M. Xu, J. Sun, F. C. Lee, "A family of high power density unregulated bus converters," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1045-1054, Sept. 2005.

[28] F. C. Lee, Q. Li, "High-frequency integrated point-of-load converters: overview," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4127-4136, Sept. 2013.

[29] W. Zhang, Y. Su, M. Mu, D. J. Gilham, Q. Li, F. C. Lee, "High-density integration of high-frequency high-current point-of-load (POL) modules with planar inductors," *IEEE Transactions on Power Electronics,* vol. 30, no. 3, pp. 1421-1431, March 2015.

[30] Y. Ren, "High frequency, high efficiency two-stage approach for future microprocessors" Ph.D. Dissertation, Virginia Tech, 2005.

[31] A. Q. Huang, "New unipolar switching power device figures of merit," *IEEE Electron Device Letters*, vol.25, no.5, pp.298-301, May 2004.

[32] Y. Ying, "Device selection criteria---based on loss modeling and figure of merit", Master Thesis, Virginia Tech, 2008.

[33] D. Reusch, J. Strydom, "Evaluation of Gallium Nitride transistors in high frequency resonant and soft-switching DC–DC converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5151-5158, Sept. 2015.

[34] X. Zhou, M. Donati, L. Amoroso, F. C. Lee, "Improved light-load efficiency for synchronous rectifier voltage regulator module," *IEEE Transactions on Power Electronics*, vol. 15, no. 5, pp. 826-834, Sep 2000.

[35] X. Zhou, P. Wong, P. Xu, F. C. Lee, A. Q. Huang, "Investigation of candidate VRM topologies for future microprocessors," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1172-1182, Nov 2000.

[36] J. Wang, S. Wu, G. Jane, "A novel control scheme of synchronous buck converter for ZVS in light-load condition," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3265-3273, Nov. 2011.

[37] C. S. Moo, Y. J. Chen. H. L. Cheng, Y. Ch. Hsieh, "Twin-buck converter with zero-voltage transition," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2366-2371, June 2011.

[38] S. S. Broussev, N. T. Tchamov, "Two-phase self-assisted zero-voltage switching DC–DC converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 3, pp. 157-161, March 2013.

[39] Z. Guo, D. Sha, X. Liao, J. Luo, " Input-series-output-parallel phase-shift full-bridge derived dc–dc converters with auxiliary LC networks to achieve wide zero-voltage switching range," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5081-5086, Oct. 2014.

[40] Y. Zhang, P. C. Sen, "A new soft-switching technique for buck, boost, and buck-boost converters," *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1775-1782, Nov.-Dec. 2003.

[41] H. L. Do, "Zero-voltage-switching synchronous buck converter with a coupled inductor," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 8, pp. 3440-3447, Aug. 2011.

[42] S. S. Lee, " Step-down converter with efficient ZVS operation with load variation," *IEEE Transactions on Power Electronics,* vol. 61, no. 1, pp. 591 – 597, Nov. 2013.

[43] L. Jiang, C. C. Mi, S. Li, C. Yin, J. Li "An improved soft-switching buck converter with coupled inductor," *IEEE Transactions on Power Electronics,* vol. 28, no. 11, pp. 4885 – 4891, Nov. 2013.

[44] N. P. Filho, L. Carlos, L. C. de Freitas, "A novel family of DC-DC PWM converters using the self-resonance principle," *Power Electronics Specialists Conference,* 20-25 Jun 1994, pp.1385-1391.

[45] E. Adib, H. Farzanehfard, "Zero-voltage-transition PWM converters with synchronous rectifier," *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 105-110, Jan. 2010.

[46] M. R. Mohammadi, H. Farzanehfard, "Analysis of diode reverse recovery effect on the improvement of soft-switching range in zero-voltage-transition bidirectional converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 3, pp. 1471-1479, March 2015.

[47] J. Lee, D. Yu, J. Kim, Y. Kim, S. Shin, D. Jung, Y. Jung, C. Won, "Auxiliary switch control of a bidirectional soft-switching DC/DC converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5446-5457, Dec. 2013.

[48] J. Yang, H. Do, "Soft-switching bidirectional DC-DC converter using a lossless active snubber," *IEEE Transaction Circuits and System I, Reguler Papers*, vol. 61, no. 5, pp. 1588-1596, May 2014.

[49] F. C. Lee, "High frequency quasi-resonant converter technologies," *Proceedings of the IEEE*, vol. 76, no. 4, pp. 377-390, Apr 1988.

[50] I. Barbi, J. C. Bolacell, D. C. Martins, F. B. Libano, "Buck quasi-resonant converter operating at constant frequency: analysis, design and experimentation," *Power Electronics Specialists Conference,* 26-29 Jun 1989, pp. 873-880.

[51] Y. C. Chuang, "High-efficiency ZCS buck converter for rechargeable batteries," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 7, pp. 2463-2472, July 2010.

[52] J. Shi, J. Luo, X. He, "Common-duty-ratio control of input-series output-parallel connected phase-shift full-bridge DC–DC converter modules," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3318-3329, Nov. 2011.

[53] B. R. Lin, C. Chao, "Soft-switching converter with two series half-bridge legs to reduce voltage stress of active switches," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2214-2224, June 2013.

[54] H. Wu, P. Xu, W. Liu, Y. Xing, "Series-input interleaved forward converter with a shared switching leg for wide input voltage range applications," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 5029-5039, Nov. 2013.

[55] T. Qian, B. Lehman, "Coupled input-series and output-parallel dual interleaved flyback converter for high input voltage application," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 88-95, Jan. 2008.

[56] Y. Huang, C. K. Tse, X. Ruan, "General control considerations for input-series connected DC/DC converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 6, pp. 1286-1296, June 2009.

[57] R. Giri, V. Choudhary, R. Ayyanar, N. Mohan, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," *IEEE Transactions on Industry Applications*, vol. 42, no. 4, pp. 1101-1111, July-Aug. 2006.

[58] Q. Hu, R. Zane, "LED driver circuit with series-input-connected converter cells operating in continuous conduction mode," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 574-582, March 2010.

[59] X. Ruan, W. Chen, L. Cheng, C. K. Tse, H. Yan, T. Zhang, "Control strategy for input-series–output-parallel converters," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 4, pp. 1174-1185, April 2009.

[60] W. Chen, G. Wang, X. Ruan, W. Jiang, W. Gu, "Wireless input-voltage-sharing control strategy for input-series output-parallel (ISOP) system based on positive output-voltage gradient method," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 11, pp. 6022-6030, Nov. 2014.

[61] V. Choudhary, E. Ledezma, R. Ayyanar, R. M. Button, "Fault tolerant circuit topology and control method for input-series and output-parallel modular DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 402-411, Jan. 2008.

[62] R. Ayyanar, R. Giri, N. Mohan," Active input-voltage and load-current sharing in input-series and output-parallel connected modular DC-DC converters using dynamic input-voltage reference scheme," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1462-1473, Nov. 2004.

[63] M. Andres, A. Bieswanger, F. Bosco, G.F. Goth, H. Hering, W. Kostenko, T. B. Mathias, T. Pohl, H. Wen, "IBM zEnterprise energy management," *IBM Journal of Research and Development* , vol. 56, no. 1.2, pp. 12:1-12:13, Jan.-Feb. 2012.

[64] ATX motherboard size, 2012. Available: https://en.wikipedia.org/wiki/ATX

[65] O. Ziwei, O. C. Thomsen, M. A. E. Andersen, "Optimal design and tradeoff analysis of planar transformer in high-power DC–DC converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2800-2810, July 2012.

[66] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proceeding of*

Institution of Electrical Engineering, vol. 113, no. 8, pp. 1387 -1394, 1966.

[67] H. Lei, J. Guo, X. Jing, N. Mi, R. Chung, S. Luo, "Design considerations for secondary side synchronous rectifier MOSFETs in Phase Shifted Full Bridge Converter," *Applied Power Electronics Conference and Exposition (APEC)*, 17-21 March 2013, pp. 526-531.

[68] Application note, "Phase shift full bridge, zero voltage transition design consideration", Texas Instruments.

[69] J. P. Vandelac, P. D. Ziogas, "A novel approach for minimizing high-frequency transformer copper losses," *IEEE Transactions on Power Electronics*, vol. 3, no. 3, pp. 266-277, July 1988.

[70] M. Pavier, A. Woodworth, A. Sawle, R. Monterio, C. Black, J. Chiu, "Understanding the effect of power MOSFET package parasitics on VRM Circuit efficiency at frequencies above 1MHz", *presented in Power Conversion and Intelligent Motion (PCIM) Europe*, 2003.

[71] J. Yungtaek, M. M. Jovanovic, D. L. Dillman, "Hold-up time extension Circuit with integrated magnetics," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 394-400, March 2006.

[72] Application note, "Design of planar power transformers", Ferroxcube.

[73] B. Chen, Y. Lai, "Switching control technique of phase shift controlled full bridge converter to improve efficiency under light load and standyby conditions without additional auxiliary components," *IEEE Transactions on Industrial Electronics*, vol. 25, no. 4, pp. 1001-1012, April 2010.

[74] C. Yan, H. Wu, J. Zeng, J. Ting, J. Tan, " A precise ZVS range calculation method for full bridge converter," *IEEE Power Specialist Conference*, pp. 1832-1836, 2003.

[75] Y. C. Hung, F. S. Shyu, C. J. Lin, Y. S. Lai, "Design and implementation of symmetrical half-bridge DC-DC converter," *Power Electronic and Drive System,* 2003, pp. 338-342.

[76] Y. Panov, M. M. Jovanovic, "Design and performance evaluation of low-voltage/high-current DC/DC on-board modules," *IEEE Transactions on Power Electronics,* vol. 16, no. 1, pp. 26-33, Jan. 2001.

[77] J. H. Liang, P. C. Wang, K. C. Huang, C. L. Chen, Y. H. Leu, T. M. Chen, "Design optimization for asymmetrical half-bridge converters," *Proc*edding *Applied Power Electronics Conference and Exposition,* 2001, pp. 697-702.

[78] I. O. Lee, G. W. Moon, "A new asymmetrical half-bridge converter with zero dc-offset current in transformer," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2297-2306, May 2013.

[79] UCC 28250 http://www.ti.com/product/ucc28250

[80] Y. Dong, M. Xu, F. C. Lee, "DCR current sensing method for achieving adaptive voltage positioning (AVP) in voltage regulators with coupled inductors," *IEEE Power Electronics Specialists Conference (PESC),* 18-22 June 2006, pp.1-7.

[81] E. Dallago, M. Passoni, G. Sassone, "Lossless current sensing in low-voltage high-current DC/DC modular supplies," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 6, pp.1249-1252, Dec. 2000.

[82] H. Huang, C. Hsieh, J. Liao, K. Chen, "Adaptive droop resistance technique for adaptive voltage positioning in boost DC–DC converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1920-1932, July 2011.

[83] https://www.eia.gov/electricity/monthly/epm_table_grapher.cfm?t=epmt_5_6_a

[84] W. Zhang, “Energy efficient and power-dense DC-Dc converters in data center and electric vehicle applications using wide bandgap devices”, PhD Dissertation, University of Tennessee, 2015.

[85] L. L. Jenkins, “Optimization of high power gallium nitride based point of load converters for data center power supply chains”, PhD Dissertation, Auburn University, 2015.

[86] Liangbin Yao, “High current density low voltage isolated dc-dc converters with fast transient response”, Ph.D dissertation, University of Central Florida, 2003.

[87] Pit-Leong Wong, “Performance improvement of multi-channel Interleaving voltage regulator modules with integrated coupling inductors,” Ph. D. dissertation, Virginia Tech, 2001.

[88] K. Yao, M. Xu, Y. Meng, F. C. Lee, “Design considerations for VRM transient response based on the output impedance,” *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1270-1277, Nov. 2003.

[89] M. Lee, D. Chen, K. Huang, C. Liu; B. Tai, “Modeling and design for a novel adaptive voltage positioning (AVP) scheme for multiphase VRMs,”, *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1733-1742, July 2008.

[90] S. Pan, P. K. Jain, “A new digital adaptive voltage positioning technique with dynamically varying voltage and current references,” *IEEE Transactions on Power Electronics*, vol.2 4, no. 11, pp. 2612-2624, Nov. 2009.

[91] S. Xu, F. Li, Y. Yao, S. Lu, W. Sun, “A high-frequency model for a PCM buck converter,” *EEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2304-2312, April 2015.

[92] Intel, “Voltage regulator down 11.1, power delivery design guideline”, Sep. 2009.

VITA

Yutian Cui was born in Xi'an, Shaanxi, China. She received her B.S. degree in electrical engineering from Xian Jiaotong University in Xi'an in 2009 and M.S. in electrical engineering from the University of Tennessee at Knoxville in 2011. She continued work towards Ph. D. under supervision of Dr. Leon M. Tolbert at the Center for Ultra-wide-area Resilient Energy Transmission Networks (CURENT). Her research focused on high efficient power converters for data center power supplies. She completed her Ph. D in electrical engineering in spring 2016.