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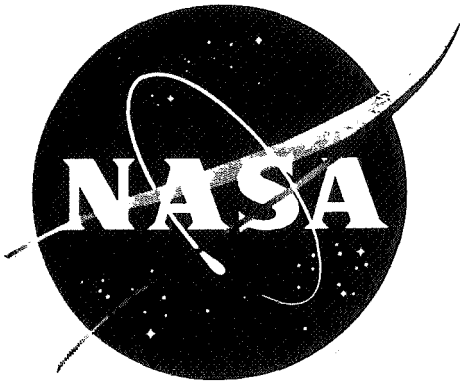

HIGH VOLTAGE SOLAR ARRAY ELECTRICAL CONFIGURATION STUDY

prepared by
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THE BOEING COMPANY

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA Lewis Research Center
Contract NAS3-8995
B. L. Sater, Project Manager

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FINAL REPORT

HIGH VOLTAGE SOLAR ARRAY ELECTRICAL CONFIGURATION STUDY

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NASA-LEWIS RESEARCH CENTER
CLEVELAND, OHIO

Contract NAS3-8995

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Spacecraft Technology Division

FOREWORD

The research described herein, which was conducted by The Boeing Company, Aerospace Systems Division, was performed under NASA Contract NAS3-8995. The work was done under the management of the NASA Project Manager, Mr. B. L. Sater, Spacecraft Technology Division NASA Lewis Research Center.

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ABSTRACT

This study was directed to increasing reliability and reducing the weight of high voltage solar-cell power systems for spacecraft. Conceptual designs of electrical configurations for a 15-kW, 2 to 16 kV, integrally regulated solar array were developed and evaluated for Earth orbit operation. Such an array could, for example, power ion thrustors on a satellite climbing to synchronous orbit, then power radio transmitting tubes. Concepts developed for integral power conditioning on the array are applicable to low voltage as well as high voltage solar arrays. The problems in developing these configurations, and the direction of work for solving these problems are defined.

Providing for radiation degradation of solar cells results in an initial solar-array power capability which is nearly twice the final 15 kW. A switching approach involving a slight additional weight in the proposed array permits this extra initial power to be used in secondary loads. Other switching reconfigures the array, from an arrangement where six different primary loads are powered at differing voltages, to a final configuration which supplies a single 16 kV load. Voltage or current is regulated to within 0.1% by low-dissipation digital switching techniques. The switches are optically linked to controls to isolate the high voltage from control circuits. Logic functions for array protection, regulation and reconfiguration are in a central computer. Both on-board and overriding ground control are provided. Mathematical reliability models show that an array can be configured to achieve an estimated reliability of 0.99. Such an array would have higher reliability than conventional low-voltage arrays. A simplified electrical configuration was developed for applications where a 0.96 reliability is sufficient.

SUMMARY

The purpose of the study described in this report was to develop an electrical configuration which provides 15 kW of conditioned power directly from the solar array to loads operating in the range from 2,000 to 16,000 volts, identify development problems, and evaluate the effort required to solve these problems. A highly versatile integrally regulated solar array configuration has been developed. For example, the solar array could power ion thrustors and other loads while the spacecraft climbs from low Earth orbit (185 kilometers) to synchronous orbit (35,800 kilometers) during three months, and then power high-frequency electron tubes for five years of broadcasting.

Problems in reliability, voltage control, and ionizing-radiation damage, identified early in the study, showed that the electrical configuration needed considerable in-flight flexibility with respect to interconnecting solar cell groups. The final conceptual array is an assembly of six block assemblies each consisting of primary building blocks and trimmer blocks. The block assemblies are not necessarily identical in current or voltage output. Each block assembly initially supplies regulated voltage and current to its primary load. Computer directed switching adds trimmer blocks of solar cells to the primary blocks to maintain voltage and current despite temperature effects on the array, load variations, ionizing radiation degradation, and faults caused by micrometeoroids or failure of array elements. Fine voltage regulation is achieved by computer-controlled shunting of various sized solar-cell modules. All block assemblies can be switched together to power a single 16-kV load.

The final conceptual array uses a digital computer to control solid state switching, and opto-electronics to isolate controls from high-voltage circuits. Presently available solid-state devices could be used. However, the array versatility and performance are a strong function of the characteristics of the switching devices used. Gains in performance can be obtained by development of higher voltage switching transistors.

A performance analysis shows that with an estimated reliability of 0.96 the high voltage array, complete with regulation and control, will generate power with a performance loss of only 1.4 watts/lb (4.5%) and 0.27 watts/ft^2 (3.0%) when compared with low-voltage roll-up array which has no provisions for power conditioning or damage control.

Verification is required of the conceptual designs for regulation, switching, protection, and isolation of high and low voltage circuits. This verification consists of selection and test of components such as photo-SCR's and high voltage transistors, integration of these elements into hybrid thick and thin film circuits, and fabrication and test of breadboards.

1.0 INTRODUCTION

This document reports the results of a High Voltage Solar Array Electrical Configuration Study, conducted by The Boeing Company for NASA Lewis Research Center on Contract NAS3-8995. The objectives of this program are to develop the electrical configuration for a 15 kW integrally regulated and controlled solar array operating in the range from 2,000 to 16,000 volts, identify development problems and evaluate the effort required to solve these problems. The electrical configurations examined supply multiple high-voltage loads, or a single high-voltage load, with voltage or current regulated to within 0.1%.

Solar-cell arrays can power ion propelled spacecraft and high frequency electron tubes for broadcasting from synchronous satellites. There are two choices for supplying such loads at 2,000 to 16,000 volts: (1) Conventional transformation of low-voltage power to high voltage, but at the cost of power loss and reliability degradation in the converters; and (2) direct generation of the high voltage with series-connected solar cells. The analyses and designs reported here were based on the direct generation approach.

Our analysis quickly revealed two important problems: (1) The solar cells degrade to about two-thirds of their initial maximum-power output during the 3-month climb from 185 km altitude to synchronous Earth orbit, and (2) the goal of 0.99 probability of full power at full voltage after 5 years is indeed challenging. Our approach to the radiation degradation is to provide solar cells in trimmer blocks that can be added to the primary blocks to replace degraded capacity. Power from these trimmer blocks is available for secondary loads during the early part of the mission. Our approach to achieving reliability is to supply extra solar cell modules to automatically replace failed ones, to by-pass failed cell groups with shunt diodes, to provide quad redundancy in critical transistor circuits, to operate transistors in a switching mode wherever possible, and to use solid-state switching. Solid-state switching devices rated at 16 kV and directly in the high-voltage solar array are not yet available. We developed functional circuits that can use today's devices, and explored the theoretical voltage limits of solid-state switches.

The work described in this report was analytical. The logical next steps are selection and test of components; design, construction, and test of breadboards; integration of elements into thin-film and thick-film hybrid circuits; and development of opto-electronic isolation techniques.

2.0 ARRAY ELECTRICAL CONFIGURATIONS

The conceptual high-voltage solar-array electrical configuration developed in this program consists of six block assemblies, each having a primary building block and trimmer blocks. Each block assembly can independently supply regulated voltage and current to a load. A computer directs addition of trimmer blocks of solar cells to the primary building blocks to maintain voltage and current to the loads despite changes in solar-cell temperature, load variations, ionizing-radiation degradation, and faults caused by micrometeoroids or failed array elements. The block assemblies can be switched together to supply a 15-kW, 16-kV load.

Solar cell performance degradation from radiation by protons and electrons will significantly affect output. The array when launched can generate nearly twice the power it will produce after five years of operation. To take advantage of this extra power we developed for the high-voltage array an advanced electrical configuration (A), which makes available to loads all of the power available from the array from the time of deployment to the end of mission. A less complex basic configuration (B) provides the required power up to the end of five years, but does not deliver the surplus power available prior to radiation degradation.

Each configuration has six blocks which could be switched into several patterns. For example, in the "transfer orbit" pattern, each block can supply one of six loads at different voltages. Then in the "synchronous orbit" pattern all blocks are connected to provide 16 kV to a seventh load. An independent current or voltage regulator is used with each load. Each regulator has a binary shunt stage, control logic, voltage or current reference, and error detector.

2.1 Basic Configuration

The six blocks which form the basic configuration are shown in Figure 1. Note that no two blocks need be identical with respect to output voltage and current. The blocks would be designed so that they could power the six initial or transfer-orbit loads at the required currents and voltages, and later supply a 15-kW, 16-kV load in synchronous orbit. A postulated set of seven loads used for analysis is shown in Table 1.

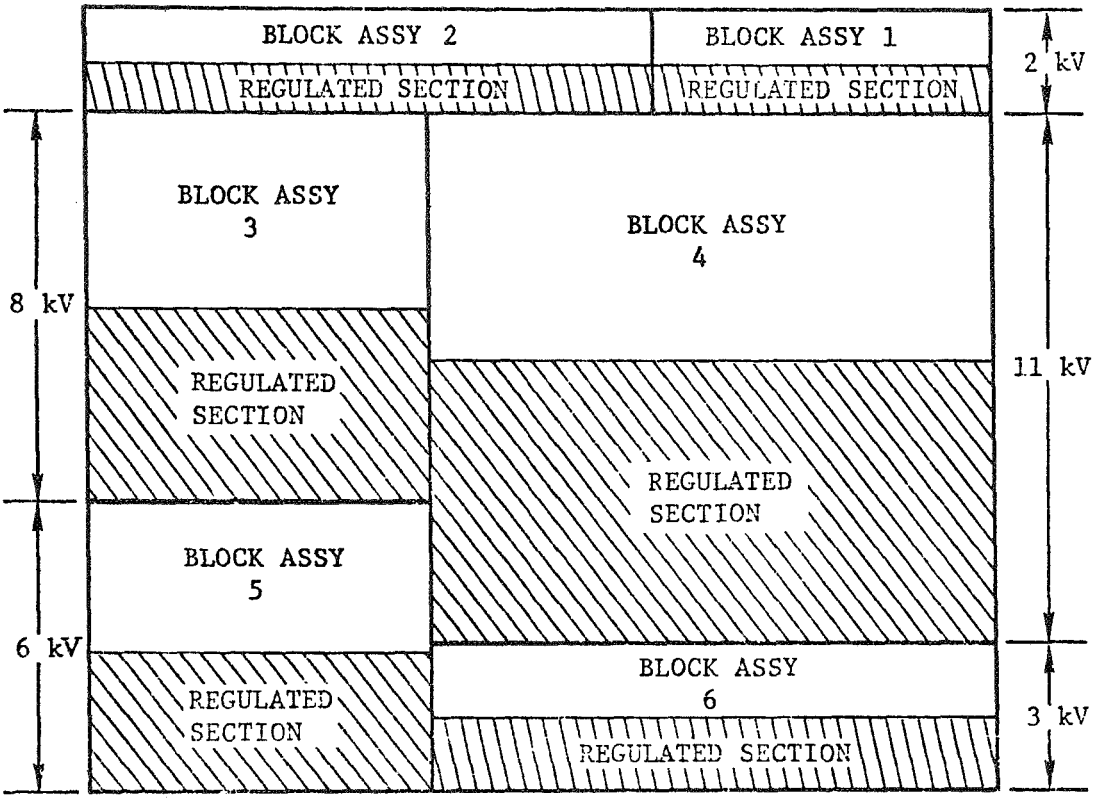


Figure 1: AREA OF BLOCKS IN BASIC CONFIGURATION

Load	Block Assembly	Voltage (kV)	Current (Amperes)	Power (kW)
1	1	2	0.352	0.7
2	2	2	0.586	1.2
3	3	8	0.352	2.8
4	4	11	0.586	6.5
5	5	6	0.352	2.1
6	6	3	0.586	1.7
7	Array	16	0.938	15.0

Table 1: LOAD SPECIFICATION, BASIC CONFIGURATION

Figure 2 illustrates the interconnection of the six blocks at twenty-one cutpoints. A cutpoint is a location in the solar array wiring where a circuit is opened or closed to reconfigure the array. Table 2 defines the state of each cutpoint for the transfer-orbit and synchronous-orbit conditions. The initial power available is 1.8 times the end-of-life required power. Solar cells not required are short circuited until needed and hence generate no power to be dissipated.

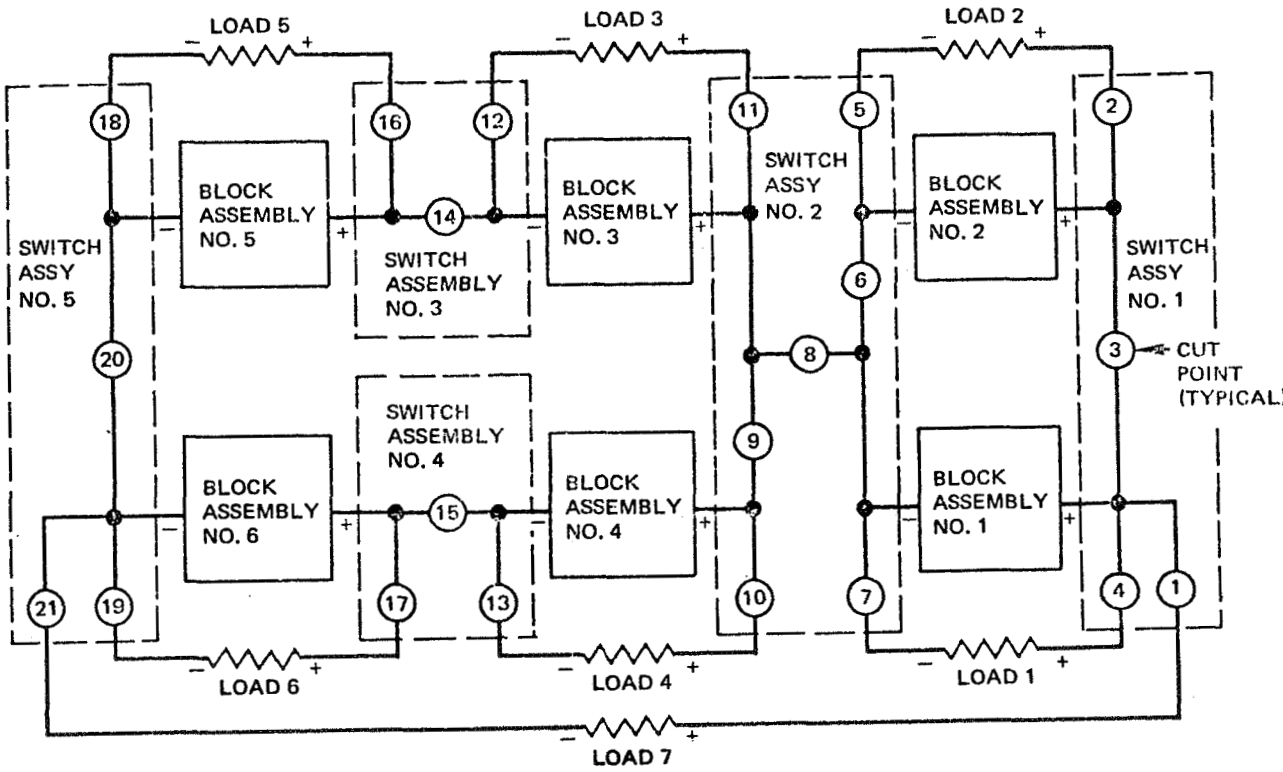


Figure 2: INTERBLOCK SWITCHING

CUTPOINT NUMBER (FIG. 2)	VOLTAGE TO BE SWITCHED (kV)	NUMBER OF TRANSISTORS IN SERIES NOTE 3	POWER, WATTS					
			TRANSFER ORBIT			SYNCHRONOUS ORBIT		
			ON NOTE 1	OFF NOTE 2	TOTAL	ON NOTE 1	OFF NOTE 2	TOTAL
1	3.2	7		0.039		0.793		
2	1.0	2	0.226				0.011	
3	3.2	7		0.039		0.793		
4	1.0	2	0.226				0.011	
5	1.0	2	0.226				0.011	
6	3.2	7		0.039		0.793		
7	1.0	2	0.226				0.011	
8	3.2	7		0.039		0.793		
9	3.2	7		0.039		0.793		
10	5.5	11	1.245				0.062	
11	4.0	8	0.905				0.045	
12	4.0	8	0.905				0.045	
13	5.5	11	1.245				0.062	
14	3.2	7		0.039		0.793		
15	3.2	7		0.039		0.793		
16	3.0	6	0.680				0.035	
17	1.5	3	0.340				0.017	
18	3.0	6	0.680				0.035	
19	1.5	3	0.340				0.017	
20	3.2	7		0.039		0.793		
21	3.2	7		0.039		0.793		
	TOTALS		7.24	0.35	7.59	7.137	0.362	7.86

NOTE 1: Transistors require 0.113 watts each when "ON"
NOTE 2: Transistors require 0.0056 watts each when "OFF"
NOTE 3: Based on a maximum withstand voltage of 700V per transistor. A transistor similar to DTS 702 was assumed (see Table 11).

Table 2: INTERBLOCK SWITCH POWER REQUIREMENTS

Regulation

In section 3 of this document is described in detail the weighted-binary regulation approach, in which groups of series-connected solar-cell submodules in the block are shunted, by transistors to control voltage or current. A submodule is a group of parallel connected solar cells. One transistor in a block will shunt one submodule, a second transistor will shunt two series-connected submodules, a third will shunt four series-connected submodules, and so on. The transistors are controlled by a digital computer, through an up-down counter and opto-electronic isolation, to maintain a current or voltage error signal at essentially zero. The

regulating range need be only as large as the smallest voltage trimmer, for the computer can switch in or out a voltage trimming step whenever regulator range is exhausted.

This regulator requires input power at 5 and 20 volts, which is provided from additional solar cell modules in the unshunted portion of each block.

The tap point, beyond which the block is not shunted by the regulator is based on the highest open-circuit voltage at the lowest operating temperature of the array. The solar array temperature may rise from -180 C to +10 C in three to six minutes as the satellite is illuminated while emerging from the sun-occulted portion of its orbit. The highest expected temperature is 95 C.

If we assume that the load must be regulated with the array temperature at 10^{o}C, then the open-circuit voltage of a 1000 V (nominal) building block will be 1790 volts. Then the tap point would be at 44 percent of the block voltage.

2.2 Advanced Configuration

The advanced configuration compensates for array degradation in incremental steps by adding "trimmer" sections to the primary array. These trimmers are used initially to supply secondary loads until called upon to augment the main array. This requires switching within each block for incremental array adjustments to compensate for performance degradation. The voltage regulator need only cover the range of one incrementally switched voltage trimmer, reducing the power capability that the regulator needs to by-pass.

The following terms will be used in subsequent discussion:

Primary Building Block (or "Block")---A voltage-controlled part of the solar array. The total power output of all primary blocks at launch is sufficient to carry all primary loads.

Trimmer Section---Solar panel section designed to augment the power output of a primary building block in either voltage or current.

Voltage Trimmer---Section which augments block voltage when switched in series with the block.

Current Trimmer---Section which augments block current when switched in parallel with the block.

Trimmer Pair---One voltage and one current trimmer sized for adding simultaneously to the primary block.

Block Assembly---A combination of primary block, trimmers, and interconnecting components.

The postulated primary loads for the advanced configuration are the same as those for the basic configuration (Table 1). Interblock switching is likewise the same (Figures 1 and 2). However, the switching within the block of the advanced configuration has to be more complex to permit connecting unused trimmers to secondary loads.

Operating Concept

The sequence in which trimmers are connected to primary loads is illustrated in Figure 3. The time at which each trimmer is added is a function of load, power capability of the block plus previously added trimmers, and the augmenting capability of the next trimmer to be added. The trimmers are unequal in size so that they can be progressively combined to add the smallest possible increments of output with the smallest possible number of trimmers and switches. No two blocks would necessarily add trimmers simultaneously. The addition of one trimmer pair would not necessarily augment the power capability of any two blocks to the same degree. For instance, the smallest increment of current, produced by a string of single solar cells, when added to a low-current block increases the capability of that block more than if the same increment were added to a high-current block. Thus the mission-time intervals between trimming would be greater for the small block.

The trimmers, prior to being required for maintaining block output to primary loads, are available for carrying secondary loads. The current trimmers can provide power at block voltage; the voltage trimmers generate low-voltage power. Our advanced configuration did not provide for interconnecting combinations of trimmers for larger secondary loads. Such interconnection would be possible, but at the cost of more switches.

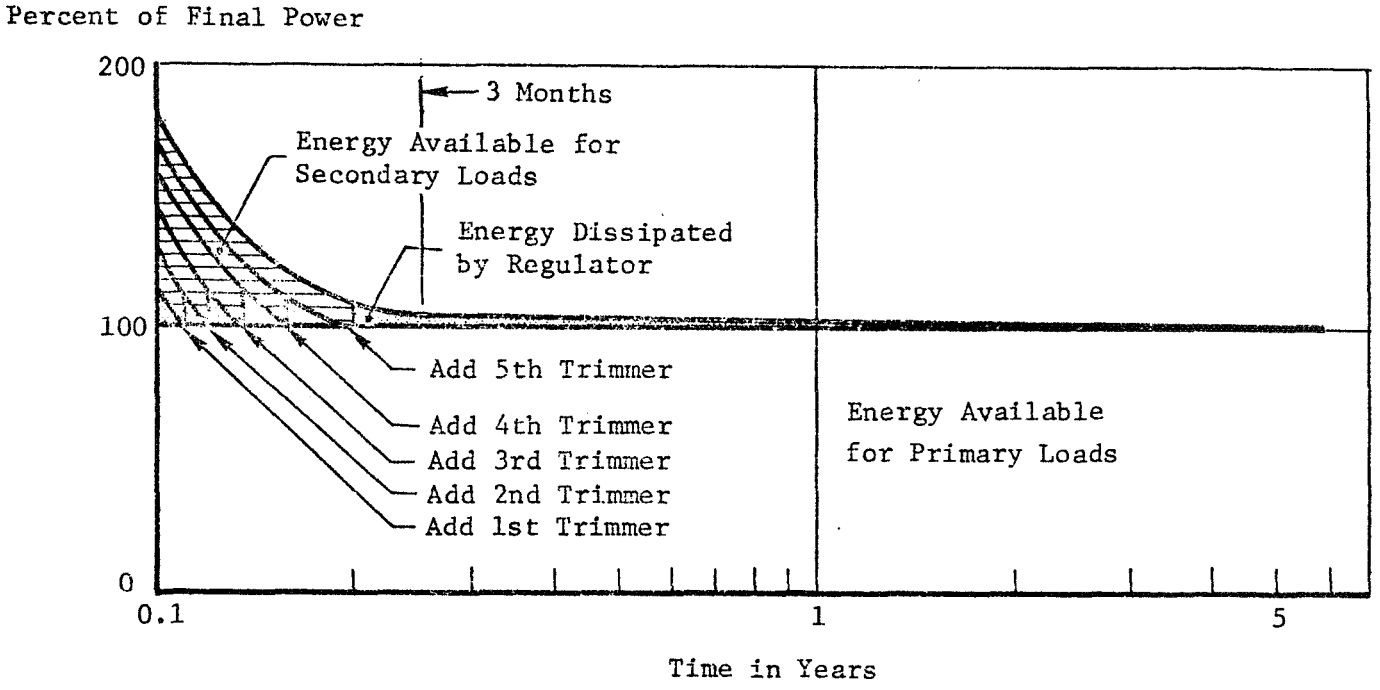


Figure 3: ENERGY RELATIONSHIP

Trimmer Size

The ideal trimmer augments block current and voltage in the exact relationship in which they degrade, restoring the block maximum power point from its degraded value to its original value (Figure 4). This suggests an "L" shaped trimmer having the characteristic AB in Figure 4. However, the power output of trimmer AB for a single load is severely limited by its low current capability. Using two loads, one across the voltage leg and one across the current leg, makes possible total utilization of the power under current-voltage (I-V) curves A and B, provided appropriate loads are available. The advanced configuration separates the two trimmer legs at the expense of more switching for better utilization of trimmer area. Thus two types of secondary loads are postulated for each block--one using the maximum power under curve B and the other, for lower-voltage loads, operating from the voltage trimmers (Curve A).

Block Configuration

The following analysis shows how a block can be designed.

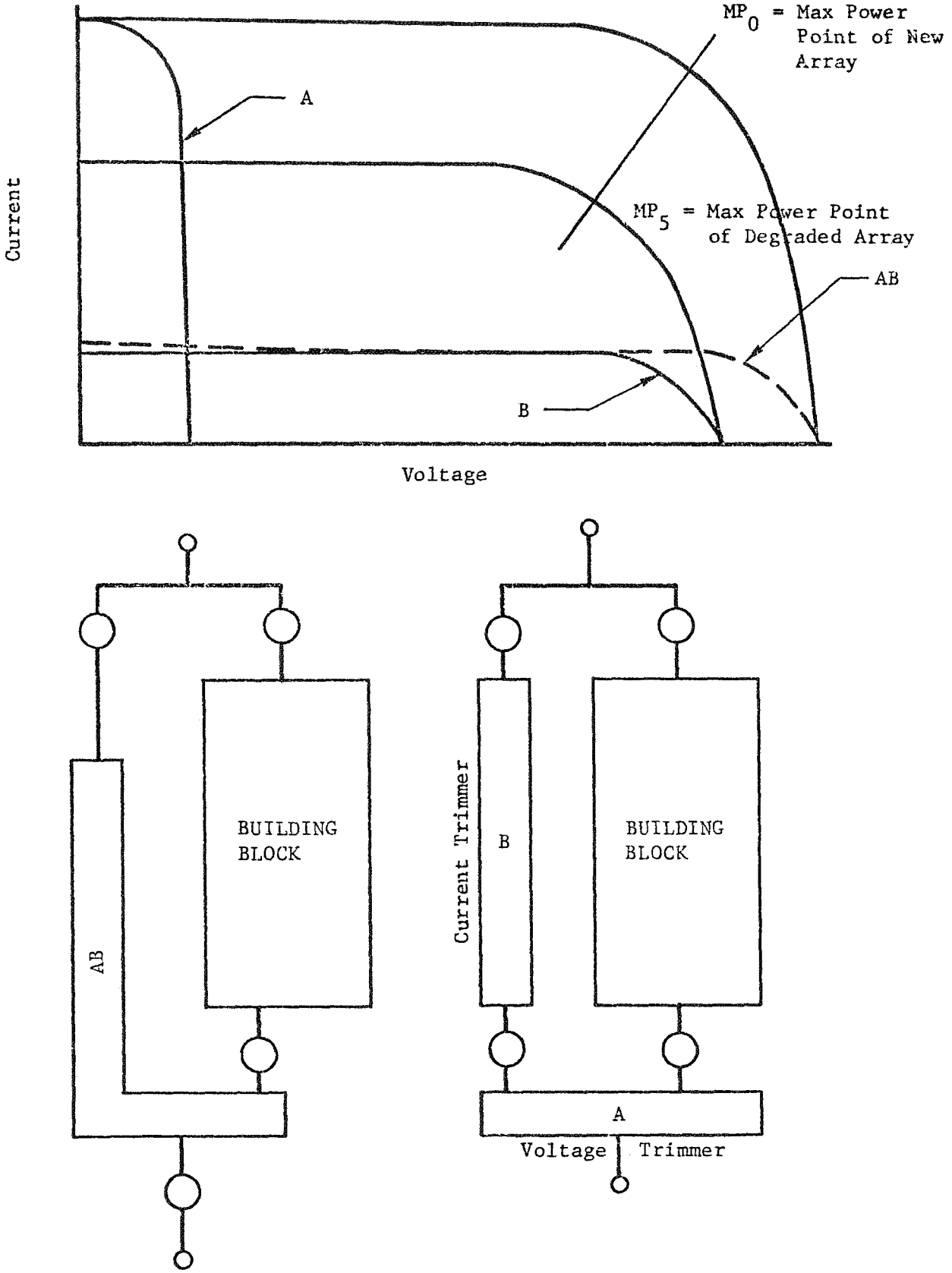


Figure 4: TWO TRIMMING CONCEPTS

Terms used in the analysis are:

I_A = array current at end of mission
I_o = block current at beginning of mission
I_b = block current at end of mission
V_o = block voltage at beginning of mission
V_b = block voltage at beginning of mission
ΔI = block current degradation during mission
ΔV = block voltage degradation during mission
V_{oc} = open circuit cell voltage at end of mission
V_{oco} = open circuit cell voltage at beginning of mission
I_{sc} = short circuit cell current at end of mission
I_{sco} = short circuit cell current at beginning of mission
n_s = number of cells in series
n_p = number of cells in parallel (1 x 2 cm and 2 x 2 cm cells are used)

Primary block	See Figure 5
Regulated Section	See Figure 5
Voltage Trimmer	See Figure 5
Current Trimmer	See Figure 5

Looking for a moment at the whole array, its current capability at end-of-life is

$$I_A = \frac{15{,}000 \text{ kW}}{16{,}000 \text{ kV}} = 0.938 \text{ A}$$

Twelve parallel 2 by 2 cm cells are required to produce the current at 78 ma per cell so width becomes 24 centimeters.

Values of current and voltage degradation are tabulated in Table 3. These solar-cell degradation values are incurred on a spacecraft spiraling in 90 days from 100 nautical miles to synchronous orbit where it remains for 5 years. Consider block 1 of Figure 2, assuming that it must produce 2000 volts at 352 milliamperes.

	PERCENT OF INITIAL VALUE	
ORBIT	SHORT-CIRCUIT CURRENT	OPEN-CIRCUIT VOLTAGE
Transfer	75	82
Synchronous	87.5	94
Combined	65.6	77

Table 3: SOLAR CELL DEGRADATION

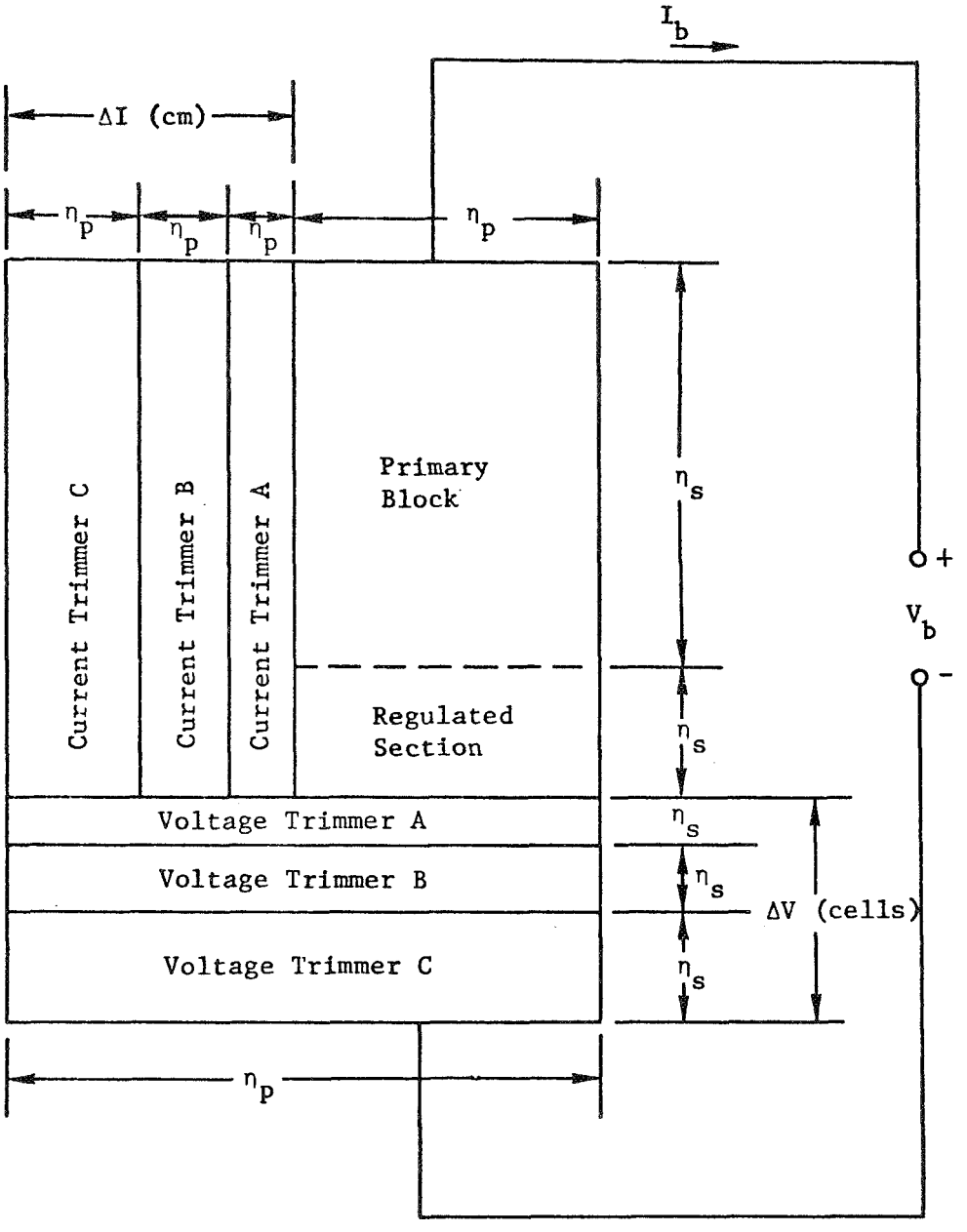


Figure 5: BLOCK ASSEMBLY CONCEPT AND TERMINOLOGY

Applying these degradations to block 1 the launch capability of block 1 is:

$$I_o = \frac{352}{0.656} = 537 \text{ mA}$$

$$V_o = \frac{2000}{0.770} = 2597 \text{ V}$$

The sum of the increments of trimming for the whole mission would be

$$\Delta I = 537 - 352 = 185 \text{ mA}$$

$$\Delta V = 2597 - 2000 = 597 \text{ V}$$

The current augmenting capability of one 1 by 2 cm cell at mission end is calculated from the 24 cm width that could supply the total array current:

$$I_{mp} \text{ (cell)} = \frac{938 \text{ mA}}{24} = 39 \text{ mA}$$

Thus the total number of 1 by 2-cm cells that must be paralleled with primary block 1 at the end of the mission becomes

$$n = \frac{185}{38} = 4.75 \simeq 5$$

No more than five current trimming steps can be used, since 1 by 2-cm is the smallest practical solar cell size. The equivalent of five 1 by 2-cm solar-cell current-trimming steps can also be obtained from combinations of two 2 by 2-cm and one 1 by 2-cm cells. Having only three strings of current trimming solar cells instead of five reduces the number of trimmer switches and the assembly cost of the array. With a digital computer controlling trimming, the difference in programming is trivial, between five single-cell wide trimming steps and the combination of 1 by 2-cm and 2 by 2-cm steps.

If current and voltage trimmers are added to the block in pairs, the voltage increment of one voltage trimmer would be

$$V_t = \frac{597}{5} = 119.4 \text{ volts}$$

The steps of voltage trimming would also be non-equal to permit computer-directed combinations that produce small voltage increments with few switches. For example, the 597 volt V_t would be obtained with two voltage trimmers having 725 cells in series and one trimmer with 361 cells in series.

	Equation	BLOCK NUMBER 1	2	3	4	5	6
Block Current (Amps)		0.352	0.586	0.352	0.584	0.352	0.586
Block Voltage (Volts)		2000	2000	8000	11000	6000	3000
I (Amps)	1	0.185	0.307	0.185	0.307	0.185	0.307
I (cm)	2	4.73 (5)	7.87 (7)*	4.73 (5)	7.87 (7)*	4.73 (5)	7.87 (7)*
V (Volts)	3	597.4	597.4	2389.6	3285.7	1792.2	896.1
V (Cells)	4	1811	1811	7242	9957	5431	2716
Curr. Trim. n_s	5	4249	4249	17000	23377	12751	6375
Curr. Trim. A n_p (1 x 2)		1	1	1	1	1	1
Curr. Trim. B n_p (2 x 2)	1	1	1	1	1	1	1
Curr. Trim C n_p (2 x 2)		1	2	1	2	1	2
Volt. Trim. n_p	7						
(1 x 2)		1	1	1	1	1	1
(2 x 2)		4	7	4	7	4	7
Volt. Trim. n_s	6						
Trimmer A		361	259	1448	1422	1085	388
Trimmer B		725	518	2897	2845	2173	776
Trimmer C		725	1034	2897	5690	2173	1552
Prim. Block							
n_p (2 x 2)	8	2.01 (2)	4.01 (4)	2.01 (2)	4.01 (4)	2.01 (2)	4.01 (4)
n_s (2 x 2)	11	3888	3990	15552	21955	11666	5987
Regulated Sect.							
n_p (2 x 2)	9	2	4	2	4	2	4
n_s (2 x 2)	10	361	259	1448	1422	1085	388

*Primary Block sized for additional current capability: (7.87-7.00 cm)

Table 4: ARRAY CONFIGURATION AND BLOCK ASSEMBLY

The 119.4 volt step is also the voltage range that must be covered by the voltage regulator.

Table 4, "Array Configuration and Block Assembly," describes the configuration resulting from the above calculation. The number of 1 by 2-cm and 2 by 2-cm cells in series (n_s) and in parallel (n_p) are tabulated for the primary block, its regulated section, and all trimmers for each block. The equations used to develop Table 4 are:

$$\Delta I(\text{amperes}) = \frac{I_b}{I_{sc}/I_{sco}} - I_b \qquad (1)$$

$$\Delta I(\text{cm}) = \Delta I(\text{amps})/0.039 \qquad (2)$$

$$\Delta V(\text{volts}) = \frac{V_b}{V_{oc}/V_{oco}} - V_b \qquad (3)$$

$$\Delta V(\text{cells}) = \Delta V(\text{volts})/0.33 \qquad (4)$$

$$\text{Current Trimmer } n_s = V_o/0.33 - \Delta V(\text{cells}) \qquad (5)$$

$$\text{Voltage Trimmer } \eta_s = \Delta V(\text{cells}) \times \frac{\text{current trimmer } n_p(\text{cm})}{\Delta I(\text{cm})} \qquad (6)$$

$$\text{Voltage Trimmer } n_p(\text{cm}) = 2 \times \text{primary block } n_p + \Delta I(\text{cm}) \qquad (7)$$

NOTE: Primary block comprised of 2 x 2 cm cells.

$$\text{Primary block } n_p = \frac{I_b - 0.039\ \Delta I(\text{cm})}{0.078} \qquad (8)$$

$$\text{Regulated section } n_p = \text{primary block } n_p \qquad (9)$$

$$\text{Regulated section } n_s = \text{voltage trimmer "A" } n_s \qquad (10)$$

$$\text{Primary block } n_s = (\text{current trimmer } n_s) - (\text{regulated section, } n_s) \qquad (11)$$

Figure 6 illustrates one block assembly in the array. The components of the block are interconnected at 27 cutpoints. These cutpoints are described in table 5. This table also shows the power consumption of individual transistor switches at the cutpoints for two array conditions--"launch" when the trimmers are all supplying power to secondary loads, and "all trimmers in," a condition at the end of the mission when the trimmers

are connected to replace primary-block capacity lost because of radiation degradation. The switching logic, but not necessarily the power loss data, is applicable to the remaining blocks.

Summary

The advanced configuration provides trimmer sections which make possible a significant increase in the utilization of power, reduce the required range of voltage and current regulation, and increase the opportunity for control of damage from micrometeoroids. The cost of these advantages is added switching complexity.

CUTPOINT			LAUNCH			ALL TRIMMERS IN		
NUMBER	V_{CP} (KV)	N_S	ON P (WATTS)	OFF P (WATTS)	TOTAL P (WATTS)	ON P (WATTS)	OFF P (WATTS)	TOTAL P (WATTS)
	NOTE 3	NOTE 4	NOTE 1	NOTE 2		NOTE 1	NOTE 2	
1	1	2	0.226				0.011	
2	1	2		0.011		0.226		
3	1	2	0.226				0.011	
4	1	2		0.011		0.226		
5	1	2	0.226				0.011	
6	1	2		0.011		0.226		
7	1	2	0.226				0.011	
8	1	2		0.011		0.226		
9	1	2	0.226				0.011	
10	1	2		0.011		0.226		
11	1	2	0.226				0.011	
12	1	2		0.011		0.226		
13	0.6	1	0.113				0.006	
14	0.15	1		0.006		0.113		
15	0.06	1	0.113				0.006	
16	0.06	1	0.113				0.006	
17	0.26	1		0.006			0.006	
18	0.16	1		0.006		0.113		
19	0.12	1	0.113				0.006	
20	0.12	1		0.006			0.006	
21	0.12	1	0.113				0.006	
22	0.24	1		0.006			0.006	
23	0.12	1		0.006		0.113		
24	0.12	1	0.113				0.006	
25	0.12	1		0.006			0.006	
26	0.12	1	0.113					
27	0.12	1		0.006		0.113		
			2.147	0.114	2.26	1.808	0.126	1.93

Note 1: "ON" Power = 0.113 N_S Watts (at 1 amp).

Note 2: "OFF" Power = 0.0056 N_S Watts

Note 3: V_{CP} = Cutpoint Voltage, Based on V_b = 2 kV

Note 4: N_S = Number of Series Transistors based on $V_{CEG(Sust)}$ = 700 V

Table 5: INTRABLOCK (BLOCK 1) SWITCH POWER REQUIREMENTS

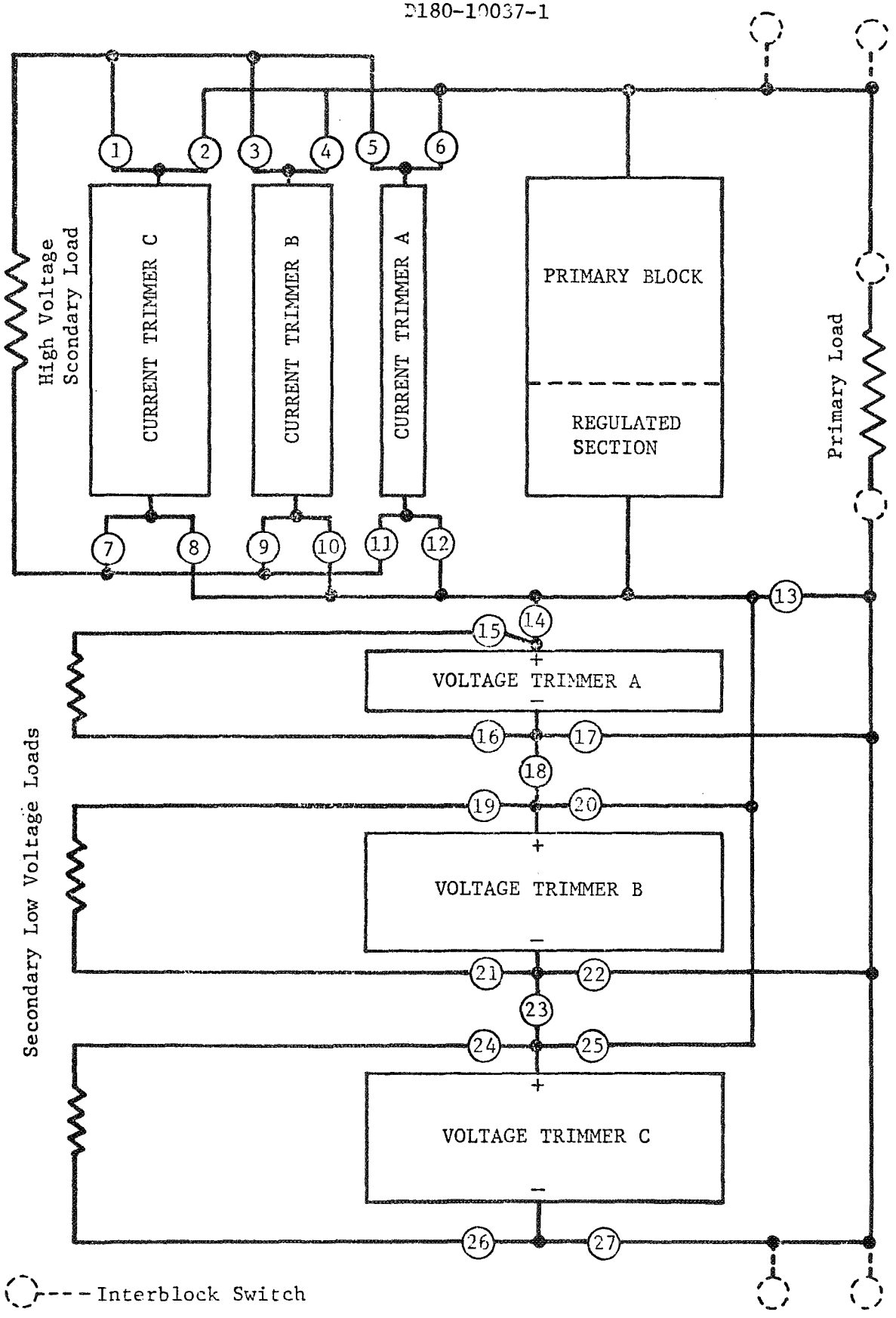


Figure 6 : INTRABLOCK SWITCHING

3.0 VOLTAGE AND CURRENT CONTROL

The current and voltage control has been integrated with surplus power utilization in the advanced configuration array described in Section 2. Power to the load is regulated by adding series and parallel trimmer solar-cell sections in uniform increments, supplemented by digital shunt regulation of the primary block. The same switches used to control the six separate blocks in the transfer orbit configuration are used to control the single 16 kV, 15 kW combination of blocks in synchronous orbit, but the sequence of operation will differ. All logical operations will be done in the central computer.

There will be two voltage and current control modes. In the direct mode the computer will configure the array switches in accordance with preprogrammed instructions or transmitted commands. For example during occultation or when a load is disconnected, the computer will set the switches to establish the configuration that will approximate the requirements when the load is powered again.

In the second or regulation mode the computer will direct an increase or decrease in voltage or current to compensate for sensed deviation from a reference value. This must be a closed loop operation since the increment effected by a switching operation will be a function of temperature and radiation degradation.

3.1 Primary Block Regulation

The primary blocks are regulated by shunting with transistors weighted-binary quantities of solar-cell modules. A primary block has two sections, one unregulated and the other regulated. The regulation section of the block is divided into modules which are in turn composed of series combinations of submodules scaled in the ratio of increasing powers of two (Figure 7). A submodules consists of a group of solar cells connected in parallel. It is possible, by short-circuiting an appropriate combination of modules, to adjust the output voltage of the regulation section to within one weighted

binary unit of any voltage within its range. The weighting factor is a variable function of temperature, illumination, cell degradation and load currents.

The regulation section in the primary block need only provide a regulation range slightly greater than the effect of a trimming increment. There is thus some saving in the number of shunt switches to offset the increased number of series switches required by the trimming concept of surplus power utilization. The size of the regulation sections for the six transfer-orbit primary blocks (Table 6) was derived from the trimmer increments in Section 2.

BLOCK NUMBER	PRIMARY BLOCK SIZE		MINIMUM SIZE OF REGULATION SECTION		BINARY UNIT SIZE	NUMBER OF	WEIGHTED BINARY	OPEN CIRCUIT VOLTS, LARGEST
	VOLTS	AMPERES	SERIES CELLS	PARALLEL CELLS	SERIES CELLS	SHUNTED MODULES	INCREMENT VOLTS	SHUNT MODULE
1	2000	0.352	361	2	4	7	1.52	64
2	3000	0.586	259	4	6	6	2.29	48
3	8000	0.352	1448	2	16	7	6.10	254
4	11000	0.586	1442	4	20	7	7.62	298
5	6000	0.352	1085	2	12	7	4.57	191
6	3000	0.586	388	4	6	6	2.29	95

Table 6: SIZE OF SMALLEST SHUNTED MODULE

3.2 Sizing of Shunt Modules

The number of series cells in the smallest shunted module, or binary size, depends on the minimum voltage increment needed to maintain the specified 0.1% voltage or current regulation. This binary size for the six blocks is shown in Table 6. The unshunted output voltage of each cell is assumed to be its maximum-power point voltage.

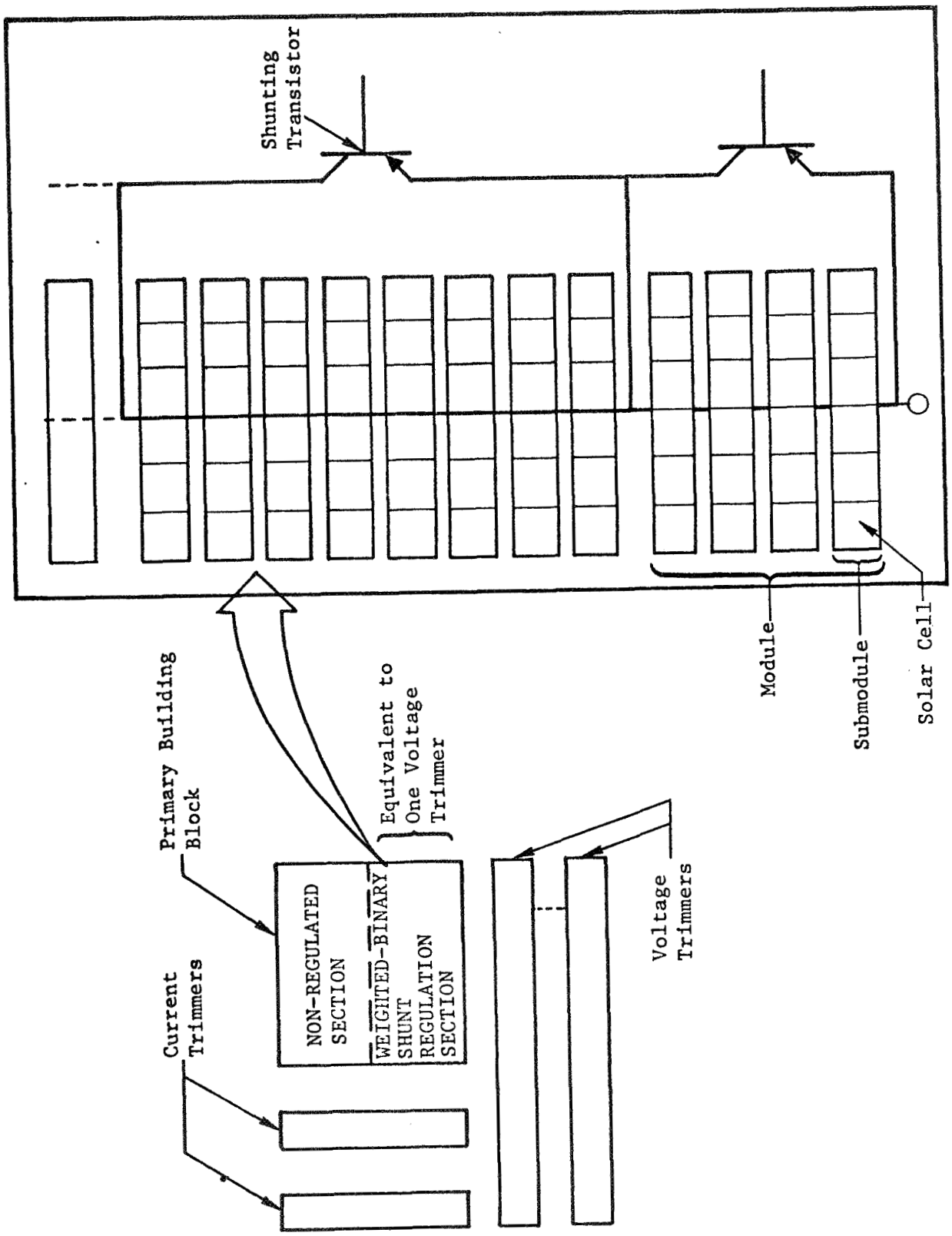


Figure 7: REGULATED AND NON-REGULATED SECTIONS OF A BLOCK

The number of binary modules required to equal or exceed the trimmer is also shown in Table 6. Because of the exponential increase in size of the binary stages the total of shunted cells in most blocks would exceed the number required. Rather than require the shunt switch of the final stage to switch a higher voltage than needed, that stage has been reduced in size to give a total of shunted cells that is just 5% greater than the trimmer increment. There is also the possibility in blocks 4 and 6 of distributing this reduction in shunted cells among the last two highest-voltage modules, further reducing the highest transistor voltage. Sizes of the shunt modules for each block are shown in Table 7. The 5% margin assures continuous regulation. Deviation of the final stage from the binary ratio does not affect the ability of the control to shunt the regulated section to within one binary unit of any voltage output in its range. However, the computer must be programmed to handle the deviation.

In Table 6 the room-temperature open circuit voltage of the largest shunt modules in each section is given. This information is needed for designing the shunt switch.

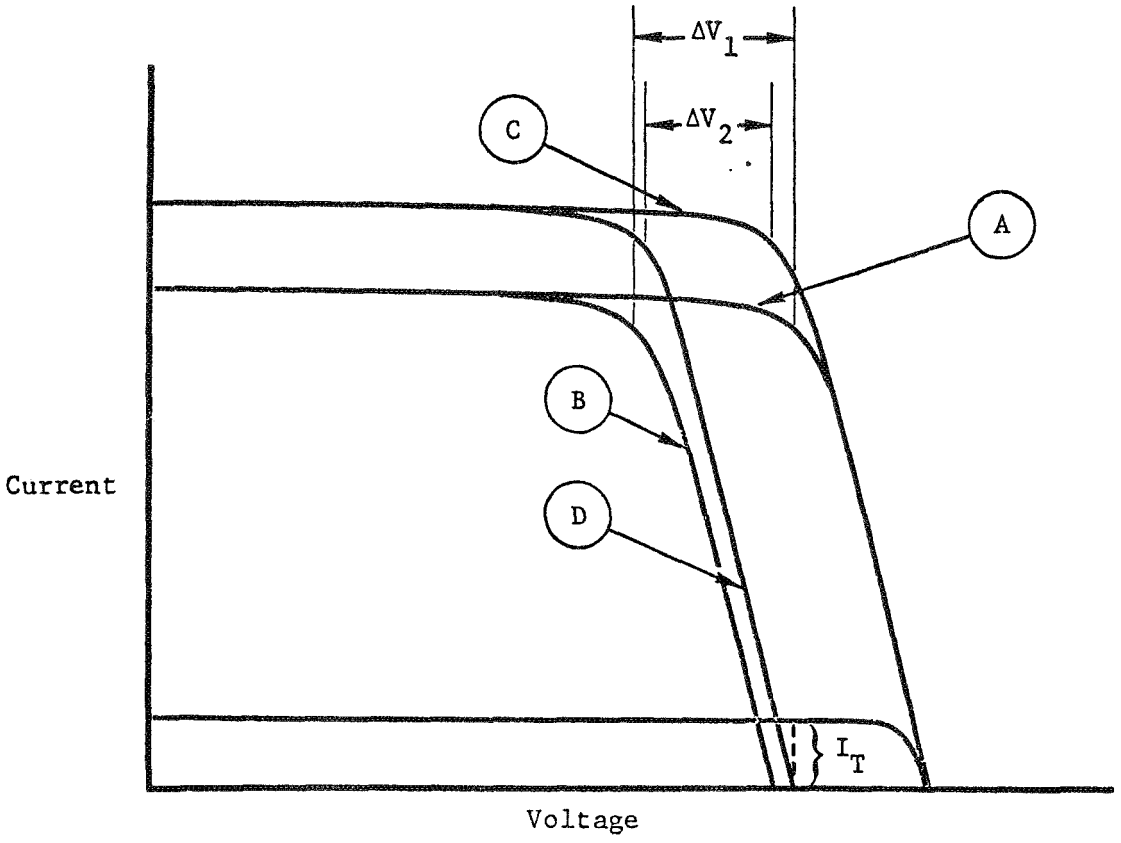
3.3 Effect of Trimmer Sections on Regulation

The addition of the current and voltage trimmer sections to the primary block will change the effect of the shunt regulator on the output. Although the regulation concept calls for current and voltage trimmer sections to be added in pairs of one of each type, the effect on regulation can best be understood by considering their effects separately. The addition of a voltage trimmer will increase the total voltage output of the block, and decrease the proportional range of the regulated section, but not the actual magnitude of the voltage adjustment available.

MODULE NUMBER	BINARY RATIO	MODULE SIZE (SERIES CELLS)					
		BLOCK 1	BLOCK 2	BLOCK 3	BLOCK 4	BLOCK 5	BLOCK 6
1	1	4	6	16	20	12	6
2	2	8	12	32	40	24	12
3	4	16	24	64	80	48	24
4	8	32	48	128	160	96	48
5	16	64	96	256	320	192	96
6	32	128	86	512	640	384	192
7	64	127		512	233	383	29
8	128						
TOTAL SERIES CELLS IN REGULATED SECTION		379	272	1520	1493	1139	407

Table 7: SHUNT MODULES SIZES

The effect of fully shunting the regulated section when the voltage trimmers have been added is illustrated by curves A and B of Figure 8. The range of voltage regulation available is the separation of the maximum power points on the curves and is indicated as ΔV_1. If the current trimmers are now added the output of the unshunted block will be described by curve C. With the regulated section shunted the output is given by curve D. The short circuit current is unchanged but when the block is open circuited there will be a small net flow of current out of the higher voltage current trimmer through the primary block and voltage trimmer. The open circuit voltage is the point at which the positive current of the trimmer section equals the negative current of the primary block plus voltage trimmer, as indicated by I_T on the diagram. The effect is to decrease the size of the voltage adjustment available. This is shown as ΔV_2 in Figure 8.



A. Voltage Trimmers Added, Unshunted Regulation Section
B. Voltage Trimmers Added, Fully Shunted Regulation Section
C. Current and Voltage Trimmers Added, Unshunted Regulation Section
D. Current and Voltage Trimmers Added, Fully Shunted Regulation Section

Figure 8: BLOCK OUTPUT CURRENT-VOLTAGE CURVES

3.4 Regulation Logic

A logic diagram of the closed loop control is shown in Figure 9. The logic assumes that the trimmer increments will be added or subtracted on demand rather than on schedule, although the scheduling alternative is within the general concept.

The inputs to the computer are the error signals from the current and voltage sensors, and the binary switch status loaded in the computer memory. In response to an error signal the computer increases or decreases the number of submodules shunted in the primary-block regulating section until

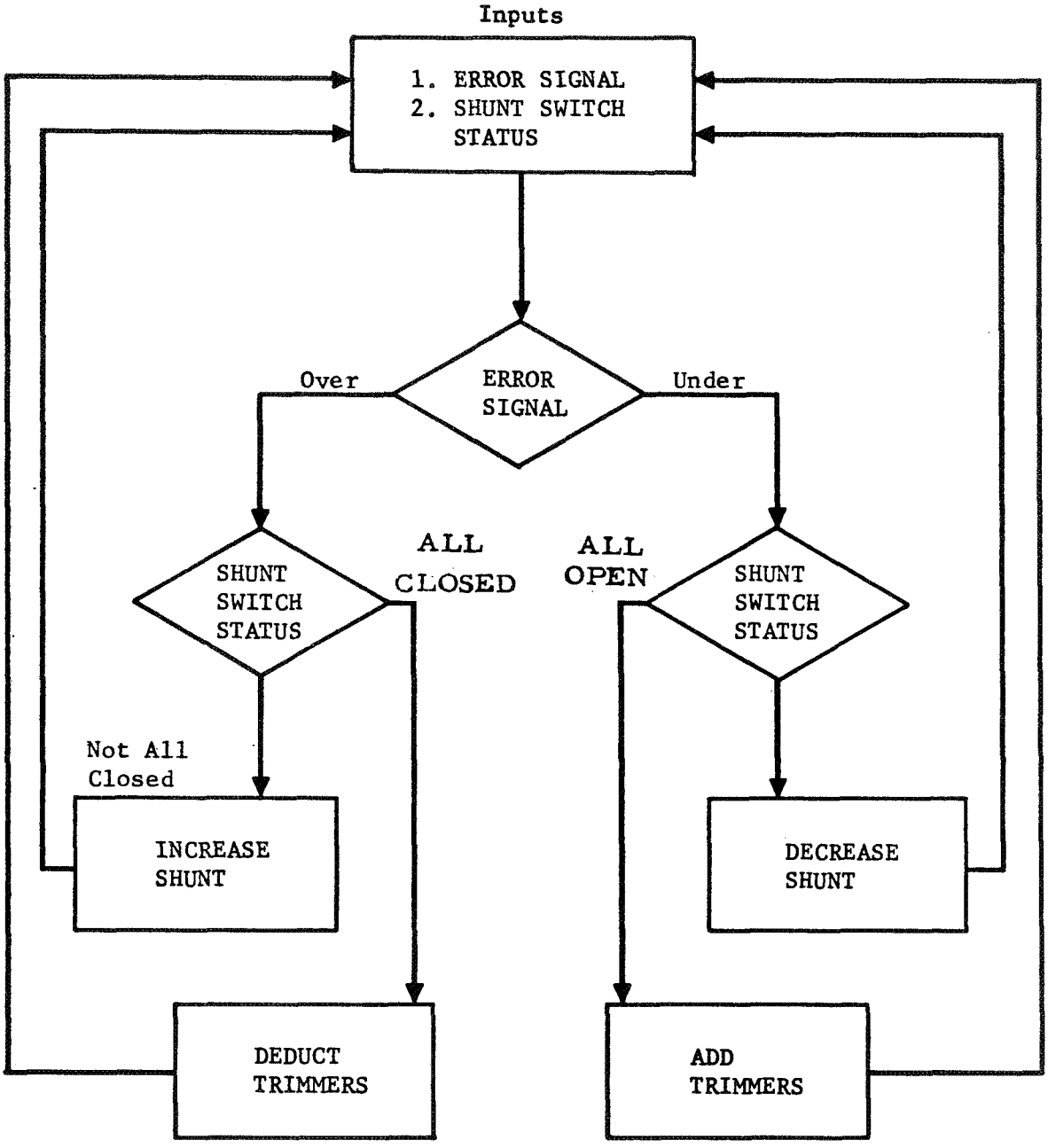


Figure 9: REGULATION LOGIC

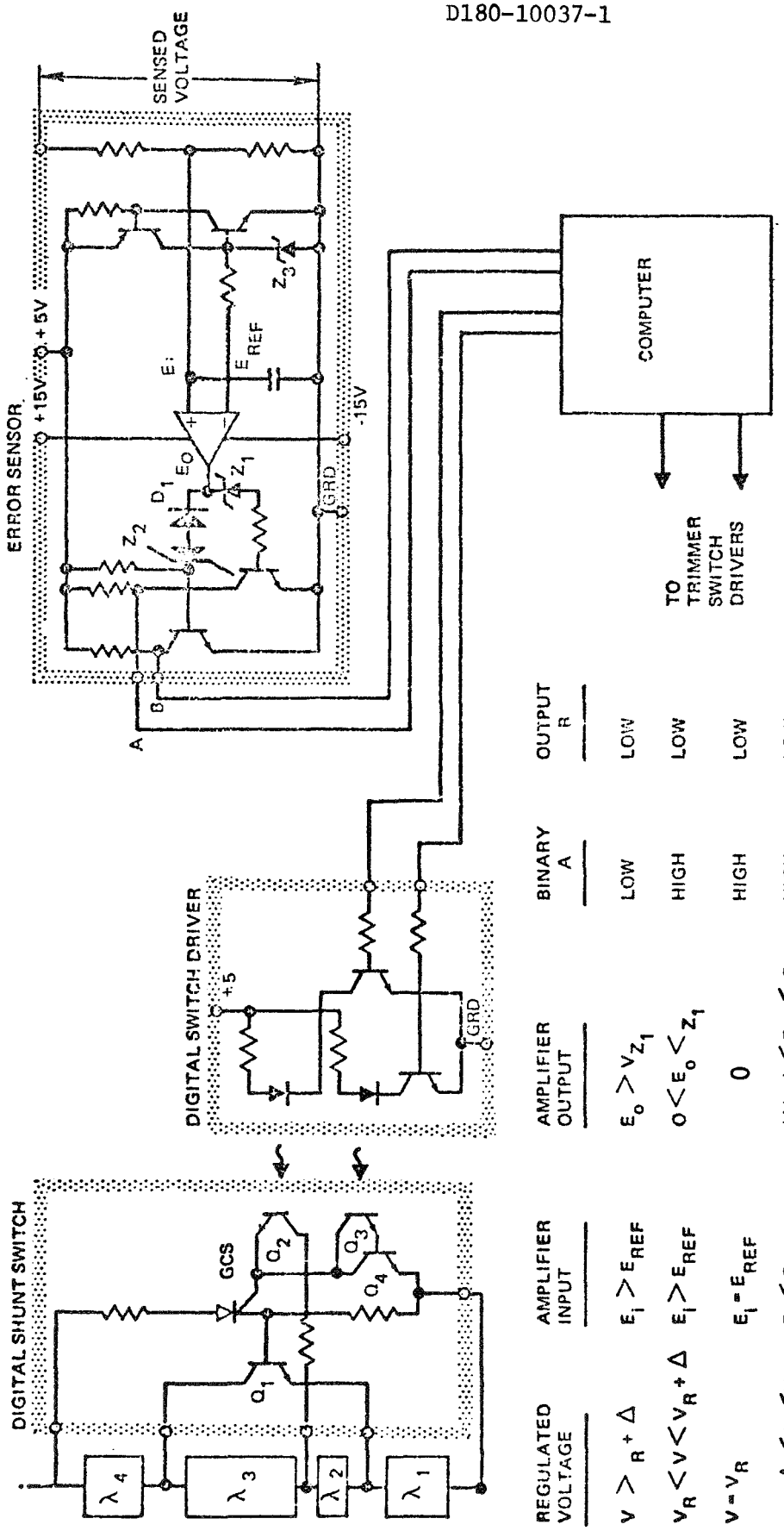
the full range is reached, then it adds or deducts trimmers. For example an undervoltage may be corrected by opening shunts until the full output of the primary block is available. If the sensed voltage remains low a trimmer pair is added. The error may now be overcorrected, and the shunting will be increased by increments until the error signal is cancelled.

The sequence in which individual shunt and trimmer switches will be operated has not yet been defined. Where the trimmer pairs are sized in binary ratio a simple counting routine may be used. The shunt switches may be incremented one binary unit at a time, or successive over and under approximation may be used to speed response.

After reconfiguration of the array to supply a single 16-kV, 15-kW load the computer will use the regulator sections of as many blocks as are required to regulate the total array. Surplus power from unused trimmer sections could be switched to secondary loads.

The circuit for the error sensor (Figure 10) was chosen to be compatible with hybrid microelectronic construction techniques. The voltage error detector circuit is similar to the sensor of the protective system. When the voltage is low outputs, A and B are high. The condition is reversed for over voltage and an "in regulation" state is indicated by A-high, B-low. The error sensor is shown connected directly to the computer. This may not be feasible if the grounds are not common; then photoelectric coupling would be used. An alternative approach to voltage/current sensing is an accurate metering circuit with analog-to-digital conversion. Then a digital reading of the actual voltage would be input to the computer where it is compared with the correct number. Such a circuit would be more elaborate than the circuit in Figure 10. The $\pm$ 15 volt amplifier biases and the 5 volt supply in the illustration are assumed to be provided from the same source as the control computer supply. Only one digital shunt stage is shown. Solar cell modules λ_2 and λ_3 are shunted λ_1 and λ_4 which provide bias for the switch are actually part of the unregulated portion of the block.

The operation of the switch is as follows. The GCS is switched ON by illuminating the photo transistor Q_2, the collector of which is at a higher potential than the GCS gate when the shunt is open. The gate-controlled switch in the transistor bias path provides OFF-ON latching. The switch



REGULATED VOLTAGE	AMPLIFIER INPUT	AMPLIFIER OUTPUT	BINARY A	OUTPUT R
$V > V_R + \Delta$	$E_i > E_{REF}$	$E_o > V_{Z_1}$	LOW	LOW
$V_R < V < V_R + \Delta$	$E_i > E_{REF}$	$0 < E_o < V_{Z_1}$	HIGH	LOW
$V = V_R$	$E_i = E_{REF}$	0	HIGH	LOW
$V_R - \Delta < V < V_R$	$E_i < E_{REF}$	$(-V_{Z_2}) < E_o < 0$	HIGH	LOW
$V < V_R - \Delta$	$E_i < E_{REF}$	$E_o < (-V_{Z_2})$	HIGH	HIGH

V = REGULATED VOLTAGE
V_R = SET VOLTAGE
$V_R \pm \Delta$ = REGULATION BAND

E_{REF} = REFERENCE VOLTAGE
V_{Z_1} = ZENER VOLTAGE OF Z_1
V_{Z_2} = ZENER VOLTAGE OF Z_2 + FORWARD VOLTAGE OF D_1

Figure 10: REGULATION CIRCUIT

is turned OFF by illuminating the photodarlington $Q_{3,4}$. The use of a darlington connection reflects the lower turn-off gain of the GCS as compared to the turn-on gain. Bias current from λ_4 to hold the switch ON will depend on the gain of the transistor and should be about 1 percent of the shunted current. Turn off bias from λ_1 is required only during the turn-off pulse.

The shunt switch shown consumes negligible standby-power and has low ON dissipation. Being pulse driven through a photo-optic coupler, it does not require continuous power to the drive circuit. A planar transistor (Q_1) having low saturation voltage carries the shunted current. The combined gain of the switch and transistor reduce the turn-on drive requirement. This is an important consideration, since the efficiency of the light-emitting diode and photo-transistor coupling is very low, and we wish to avoid including a high gain amplifier that would require an auxiliary power supply.

4.0 SWITCHES AND SWITCHING

Essential to the operation of the high voltage array are reliable, lightweight switches for controlling 2,000 to 16,000-volt direct current. In this study we have evaluated solid state switches, vacuum relays, high voltage relays, mercury-wetted plunger relays and squib operated devices.

"Cutpoints" in our switching study are circuit points at which current flow may be interrupted. Each cutpoint has a current requirement for its closed condition and voltage requirement for its open condition. The cutpoint requirements depend on their location in the circuit and on the order in which they are operated. The order will be either simultaneous, random or sequenced. For example if there are n cutpoints in series between a load and a voltage source V and they are operated simultaneously, the steady state voltage rating of the cutpoint is V/n. If they are operated randomly, so that any one cutpoint may be the first to open or the last to close, then all must be rated at V. On the other hand, if the sequence of operation is known, the steady-state rating of each cutpoint will depend upon its position in the sequence, but only one will be rated at V, with all others rated at a lower voltage. Thus, the worst case cutpoint requirement is 16 kV at 1 ampere. Operating temperature range is from -40°C to 125°C and a design goal of 10 volts forward voltage drop was adopted. Device selection proceeded on this basis.

We surveyed both electro-mechanical and semiconductor devices available currently or within the 1970-1972 period. The results are reported in the following paragraphs.

4.1 Vacuum Relays

Vacuum relays have been used for many years in high voltage applications. The inherently good dielectric characteristics of vacuum provide reliable switching. Recent use of ceramics makes the enclosures more rugged. Weights of 1 to 2 ounces for units rated at 8 to 10 kV are typical. Off-the-shelf relays will interrupt currents of 0.5 to 1.0 A at these voltages, but higher interrupting capacity requires special switches, generally rated at lower voltages, around 2 to 3 kV. A 20 kV relay built to carry 20 A continuously and interrupt 0.5 A could be as small as 3/4 inch diameter by 2-3/4 inches long (1.9 cm diameter by 7.0 cm long).

Discussions with four vendors (Jennings, Kilovac, Eimac, and Torr) indicated that development is required for a latching relay with interrupting capacity higher than 0.5 amp.

4.2 High Voltage Relays

These relays have conventional coil design, but high-voltage dielectric structure and wide gaps. Some have contacts exposed to the environment while others are encapsulated. Voltage ratings of 5 kV are typical. Voltage ratings up to 20 kV are achieved with special oil filled enclosures. Current interrupting capacity is 200 milliamps at up to 8 kV.

4.3 Mercury-Wetted Plunger Relay

This device has a mercury-wetted plunger that is magnetically positioned between axial mercury-wetted contacts (Reference 1). The surface tension of the mercury film makes the device bi-stable in 5-G shock. The switch is very small and light (0.16 cm^3 and 0.1 gram) and a variety of coil configurations are available. Reliability appears good.

This relay is not a high voltage device and its application would be limited to a latching driver for other high voltage switches.

4.4 Explosive Actuated Switches

Squib activated switches were examined for one-shot switching applications. The information collected indicates that reliability is good, current capacity could be attained, and, based on a voltage stand-off capability of 10^4 volts/mm, the voltage requirement is attainable. Development and testing would be required.

The disadvantage of a squib-operated switch is that it can be used only once. The complexity of switching on a high-voltage array quickly becomes unmanageable when multiple reconfigurations must be obtained with explosive actuated switches.

4.5 Semiconductor Switches

Silicon p-n junctions can theoretically be made with very high breakdown voltages but processing technology limits switching devices to a few thousand volts. We show in Appendix 1 that increasing the blocking voltage leads to a corresponding increase in the ON state conduction loss for a given current density and that the most efficient use of silicon is made by blocking the

voltage over several reverse-biased junctions in series. It is also shown that for OFF-ON dc switching capability series transistor configurations are superior to series thyristor configurations. Control electrodes of the series transistors will be at widely separated potentials when the switch is OFF, leading to the recommendation of optoelectronic triggering methods. A conceptual switch design based on the study uses thyristors in the transistor bias supply to minimize the number of power supplies required.

For this study we postulated the following requirements:

A. Blocking voltage when OFF: Up to 16 kV
B. Switching current: 1 ampere maximum
C. Voltage drop across device when ON: Less than 10 volts
D. Operating temperature range: -40°C to +125°C
E. Leakage current while OFF: Less than 5 mA

Switching speed and gain are not critical and may be sacrificed to maximize the specific requirements.

Desirable switch characteristics are potentiality for fabrication in miniaturized form, low power dissipation, and few biasing sources for operating the switch. Switch losses will be conducted to the solar panel and radiated into space. Thus miniaturization of the switch should not lead to concentrated heat generation requiring special heat-conducting structures to distribute the heat over a large panel area.

Comparison of Device Types

Three basic silicon switching devices have high-voltage capability--the transistor, the thyristor, and the junction field effect transistor (FET). The thyristor category refers to all devices having four layers of alternately doped semiconductor material. Of these the silicon controlled rectifier (SCR) and the gate controlled switch (GCS) are of interest in this application. Simplified models of the devices illustrating their basic similarity are shown in Figure 11. The functional operation of these devices is described below. Their basic structure is discussed in Appendix 1.

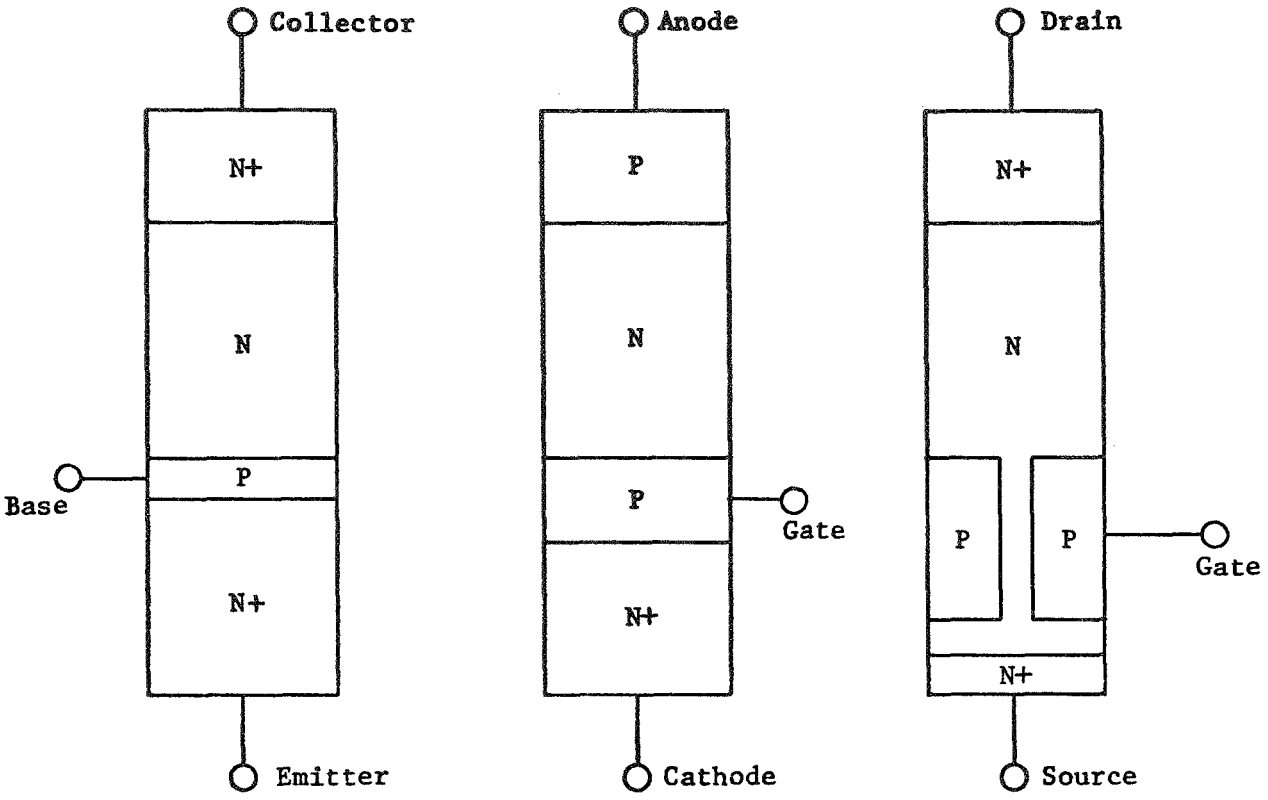


Figure 11: SOLID-STATE HIGH VOLTAGE SWITCHES

The transistor is turned ON and kept conducting by a control current injected at the base. The thyristor devices have the advantage that they will remain conducting after being turned on by a pulse, and require no further control current in the gate-cathode circuit. The SCR can be turned OFF only by interrupting its anode current, an obvious disadvantage in dc circuits; however, the GCS can be turned OFF by a negative polarity pulse to the gate. The FET operates somewhat like a vacuum tube, a negative polarity at the gate electrode will cause the channel between the soure and drain to pinch-off. All three device types are subject to the same practical limitations of material and processing technology with regard to forming high-voltage junctions in silicon. All three have a similar tradeoff between blocking voltage and ohmic conduction loss. We consider the limiting factors in breakdown-voltage and the nature of the voltage-resistance trade-off in Appendix 1. Let us now look at typical specifications of the high voltage devices available today.

Today's High Voltage Transistors and Thyristors

Some parameters of transistors and thyristors representative of the state-of-the-art are shown in Table 8. Two basic transistor structures are offered, planar and mesa. It is seen that the highest breakdown voltages are available in the mesa type. However, we would prefer to use planar transistors for this application because of their inherently better reliability. The different transistor structures are illustrated in Figure 12.

In the planar device the collector-base junction is formed beneath a thermally grown oxide which serves to protect it from contamination. The breakdown voltage will be less than the bulk breakdown voltage associated with the resistivity of the collector silicon because of the high field concentration resulting from the curvature of the base-collector junction.

Device Type	Blocking Voltage	Conduction Voltage Drop	Off Leakage Current	Structure
Transistor	400	1 V at 1.5 A	0.5 ma	Planar
Transistor	1400	2 V at 3 A	1 ma	Mesa
Transistor	700	0.3 V at 1 A	0.5 ma	Mesa
Transistor	1400	0.3 V at 1 A	0.5 ma	Mesa
Transistor	300	0.07 V at 1 A	10 ua	Planar
SCR	1800	0.9 V at 1 A	15 ma	Alloy Diffused
GCS	600	2.5 V at 1 A	10 ma	Planar

Table 8: SOME TYPICAL HIGH-VOLTAGE POWER SWITCHING DEVICES

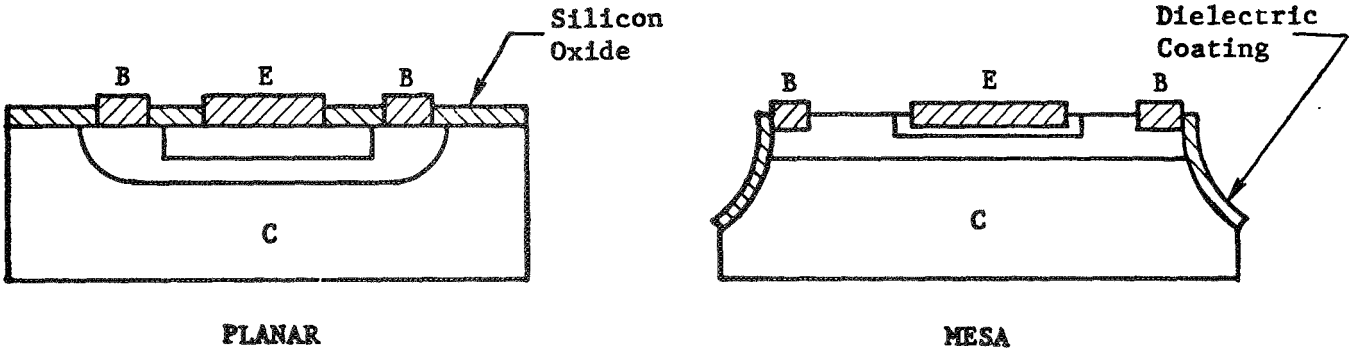


Figure 12: BASIC TRANSISTOR STRUCTURES

This high-field region extends to the surface of the transistor where the critical field for breakdown is less than in the bulk, because of the inherent band bending at the silicon-to-oxide interface. Recent gains in planar voltage capability have come from reducing this surface inversion effect with biased metal electrodes over the oxide, and with doped oxides. One manufacturer has produced 900-V BV_{ceo} planar devices and predicts 1500-V breakdowns within the next few years.

The mesa transistor does not have the high field concentration of the planar structure because the curved region is etched away. The exposed junction and adjacent surface are covered with a dielectric protective film, usually organic. The lower reliability results from exposure to contaminants during the additional processing, and from the inferior protection provided by the organic coating, when compared with the thermally grown oxide.

Both planar and mesa transistors are degraded by defects in imperfect starting material and by present limitations of process control. These degrading factors include crystal defects, pinholes, impurities in the oxide, and impurities on the surface of the silicon sealed in by the oxide. The OFF state leakage currents shown in Table 8 are primarily surface leakage rather than reverse junction leakage. This means that they are a function of the manufacturing process and are resistive in nature. They are not directly proportional to device area nor do they increase exponentially increasing with temperature as would be the case with junction leakage currents.

Looking again at Table 8, the highest voltage devices available today are SCR's. The GCS shown is a planar type that has lately become available on an engineering-sample basis; it has lower voltage ratings than mesa transistors but is superior to planar transistors (Reference 2).

Notwithstanding its superior blocking capability, the difficulty of turning it OFF makes the SCR unsuitable for our application. For each SCR that has to be turned OFF, we would need to add to the array a non-polarized commutating capacitor of even higher voltage rating than the SCR. As compared to the transistor the GCS has the advantage of latching on or off. However, the power saved in eliminating the base current of the transistor will be lost in the higher forward conduction drop of the CGS.

There are no field effect transistors (FET's) currently available with high voltage capability, but a promising recent development suggests that such devices may eventually rival the transistor and thyristor as high voltage switches. The most serious FET problem in high-voltage applications is the channel resistance. Besides adding to the conduction resistance of the drain region, the voltage drop along the length of the channel tends to back-bias the gate near the drain, saturating the channel current. The higher the channel resistivity the lower will be the saturation current for a given channel length. A structure designed to overcome these problems while providing high-voltage and high-current capability was recently announced (Reference 3). Called an analogue FET, the device is said to have 200 volts blocking capability with 200 mA of conduction current.

While the analogue FET is promising, and it should have a breakdown to-resistance trade-off comparable to the transistor, it is still in the experimental stage.

Conceptual Design of a High Voltage Switch

The foregoing discussion indicates that within the next two or three years our choice of a solid state switching device will be restricted to the transistor and GCS. In Appendix 1 we show that in both types of device there is a basic trade-off between breakdown voltage and conduction voltage drop. This tradeoff will favor the transistor over the GCS when both devices have equal blocking voltages. Moreover, our review of current availability indicates that transistors will continue to have higher voltage ratings than the GCS. We therefore will choose the transistor as our basic power switch element notwithstanding the desirable latching characteristics of the GCS.

From equation 32 in Appendix 1 relating V_{SAT} and V_{BD}, the required collector area for a hypothetical 16,000-volt breakdown mesa transistor having 10 volts saturation drop at 1 ampere is 71 sq cm, corresponding to a 3.3 inch square chip. Such a 16 kV transistor is not technically feasible within the foreseeable future, firstly because the largest silicon wafers now available are only 3 inches in diameter, and secondly, because yield falls off very rapidly as voltage specification and chip area increase.

A 16-kV transistor of a smaller size might be developed. Let us assume that such a transistor having a 1 cm^2 collector area can be produced. Seventy-one of these are needed in parallel to obtain the current and saturation

voltage rating needed. This composite switch can be compared to an alternate switch consisting of 23 of today's 700-volt transistors in series. The conduction voltage drop of the 23 transistors in series would be 9.2 volts at 1 ampere, and the total chip area would be only 1/3 as much as required for the parallel transistors. The series transistors would require a more elaborate control circuit and perhaps multiple power supplies.

We think it is clear that our high voltage switch must be put together from a combination of devices in series and/or parallel. We shall now try to answer the question: Should we press to obtain highest possible breakdown voltage devices and increase the cross-sectional area (or parallel devices) to get the conduction voltage drop we need, or should we use a larger number of lower-voltage, lower-resistance devices in series?

The relationship between total chip area and the number of series transistors for a series composite switch with a 16,000 volt breakdown and 10 volt saturation drop at 1 ampere, is plotted in Figure 13.

Two curves are shown, one where each transistor has an independent bias-current supply, and the other where all transistors have a common power supply. With a common power supply each transistor must carry the base current from all transistors higher in the series string as well as the switched current.

The curves were obtained by a computer solution of equation 12 modified for the case of n_s series transistors as follows:

Individual Bias Supplies

$$V_{SAT} = n_s \phi_{CE} + n_s \frac{I}{A} (\text{constant}) \left(\frac{V_{BD}}{n_s} \right) \tag{12}$$

Single Bias Supply

$$n_s \phi_{CE} + \left(\sum_{i=1}^{n_S} \left(\frac{n_s - i}{H_{FE}} \right) + 1 \right) \frac{I}{A} \left(\text{constant} \left(\frac{V_{BD}}{n_s} \right)^{2.6} \right) \tag{13}$$

A current gain, H_{FE}, of 20 and ϕ_{CE} of 0.2 volts were assumed.

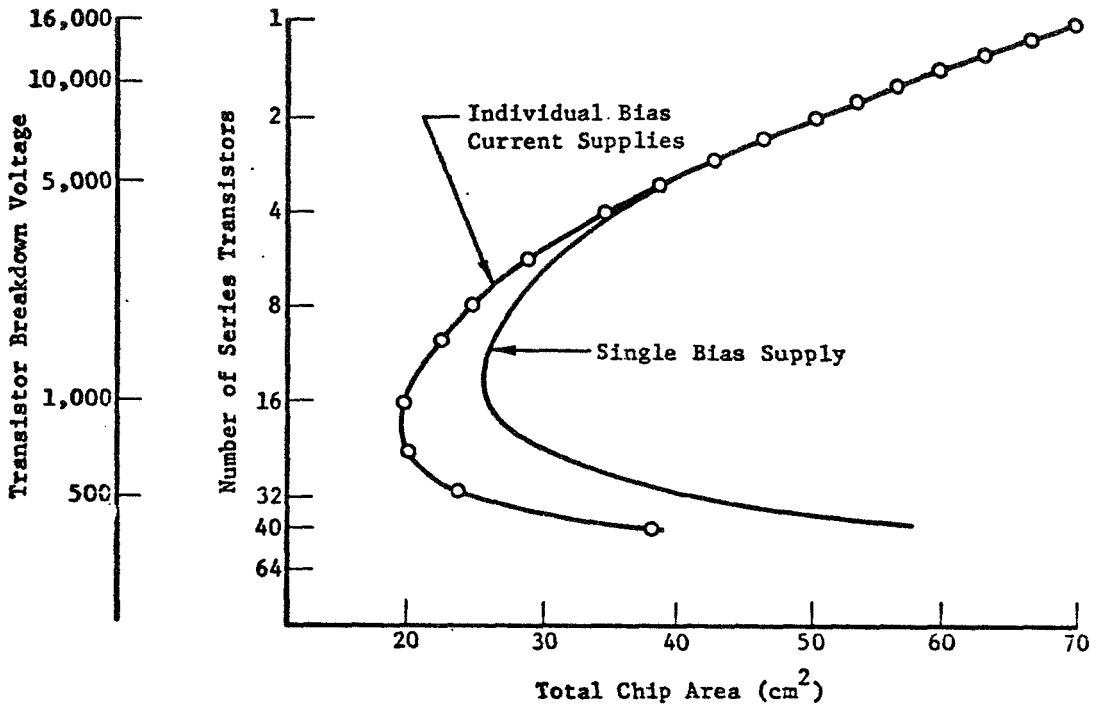


Figure 13: NUMBER OF SERIES TRANSISTORS AND TRANSISTOR V_{BD} VERSUS TOTAL CHIP AREA

The existence of minimum areas reflects the constant term ϕ_{CE} in the equations. For the much lower ϕ_{CE} obtainable for planar transistors the minimum would be very close to the origin.

A basic problem of the series transistor switch is that all transistors must turn ON simultaneously if none is to sustain more than its breakdown voltage. Base current must be supplied to the transistor bases at widely separated potentials when high voltages are switched. A solution that combines the best features of the SCR and transistor is to connect a SCR between the collector and base of each transistor comprising a series switch. The composite will have the turn-on characteristics of the thyristor. The base current to bring the transistor to saturation will be drawn from the source switched and will be blocked when the switch is OFF. As the series transistors approach saturation the voltage difference between the base electrodes is small, so all transistors may be supplied from a single low voltage source, allowing the thyristors to become reverse-biased and so turn OFF.

The wide separation in the potentials of the control electrodes when the transistors are not conducting necessitates a means of voltage isolation. Additionally, the entire switch must be effectively isolated from the controlling computer. Optoelectronic isolation has size and weight advantages over other methods; moreover, there is a wide range of solid-state optical transmitting and sensing devices that are compatible with the hybrid microcircuit type packaging envisioned for the high voltage switch.

A conceptual switch design incorporating these features is shown in Figure 14. The load current is carried by the high voltage transistors $Q_{1,2,3}$.

Additional stages may be added at the collector of Q_3 as determined by the required total blocking voltage and the breakdown voltage of the transistors. $Q_{1,2,3}$ are turned ON by illuminating photo-SCR's $Q_{4,5,6}$. Transistor Q_1 will draw base current from the auxiliary low-voltage source through Q_4; transistors Q_2 and Q_3 will obtain base drive from the switched voltage source through Q_5 and Q_6. As the voltages at the bases of Q_2 and Q_3 fall below the potential of the low voltage source they will also draw current from this source. When Q_2 and Q_3 are fully in saturation, SCR's Q_5 and Q_6 will become reverse-biased and will turn OFF. The switch is returned to the OFF state by briefly illuminating phototransistor Q_7; the Darlington connection of $Q_{7,8,9}$ then shunts the base current from all three switch transistors, also causing SCR Q_4 to turn OFF.

Resistors $R_{2,4,6}$ compensate for variations of the reverse leakage current between transistors assuring that the voltage drop across the transistors will be equal when they are off. It will be more difficult to assure that the voltage across any element does not exceed breakdown voltage during the transition from ON to OFF. In the design of Figure 14 the stored base charge of Q_3 must flow to ground through Q_1 and Q_2 and that of Q_2 through Q_1. Therefore, Q_1 will tend to come out of saturation first, followed by Q_2, then Q_3. The unequal capacitors $C_{1,2,3}$ in parallel with the collector-base capacitances of the transistors are included to illustrate how equalizing time delay might be introduced. Another possible approach is to shunt the bases of the transistors sequentially using a separate photo-transistor shunt for each.

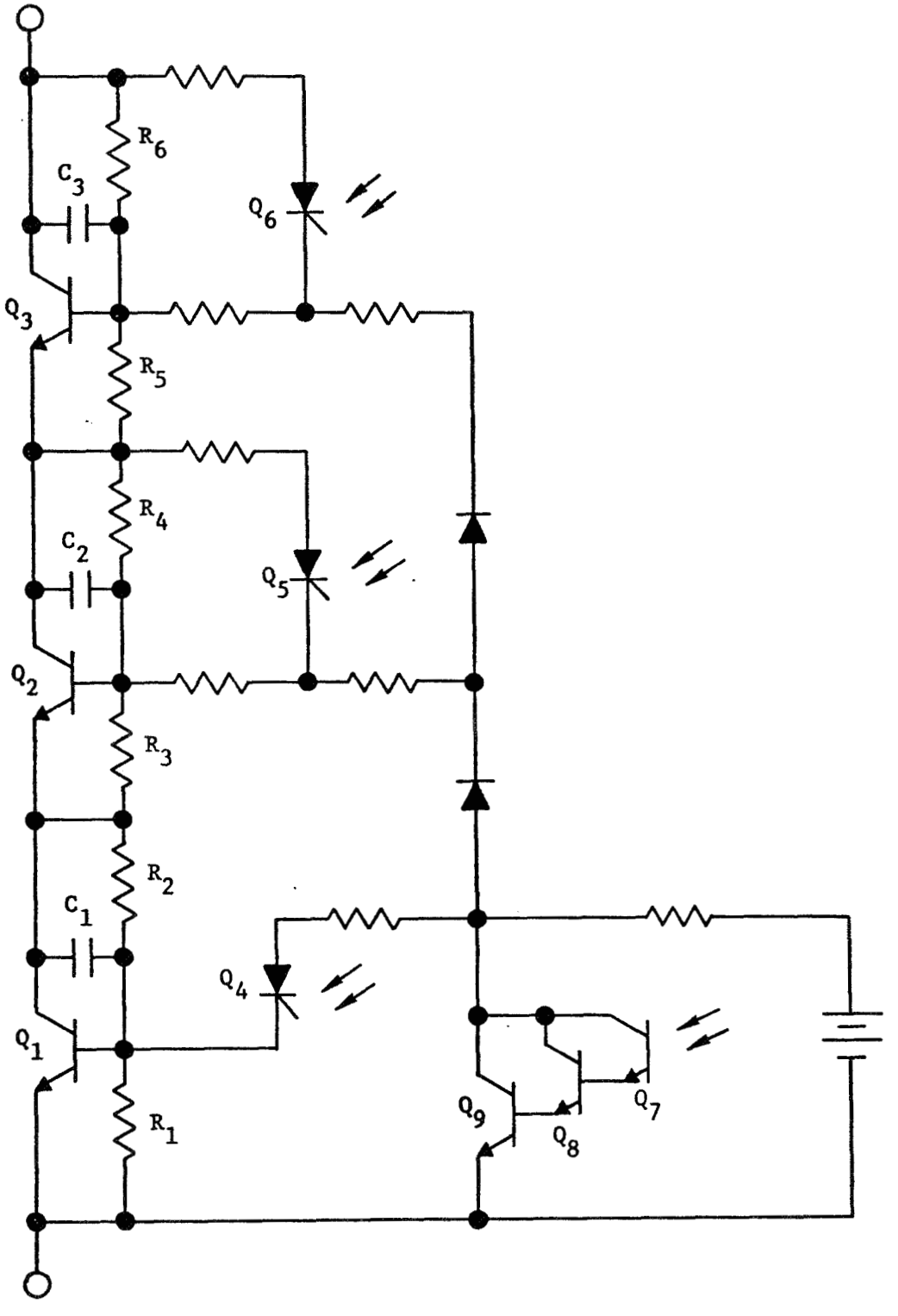


Figure 14: EXAMPLE HIGH VOLTAGE SWITCH

Summary

We have explored some of the theoretical and practical limitations of silicon switching devices as high voltage switches. A conceptual switch design based on the study has been outlined. These design features are:

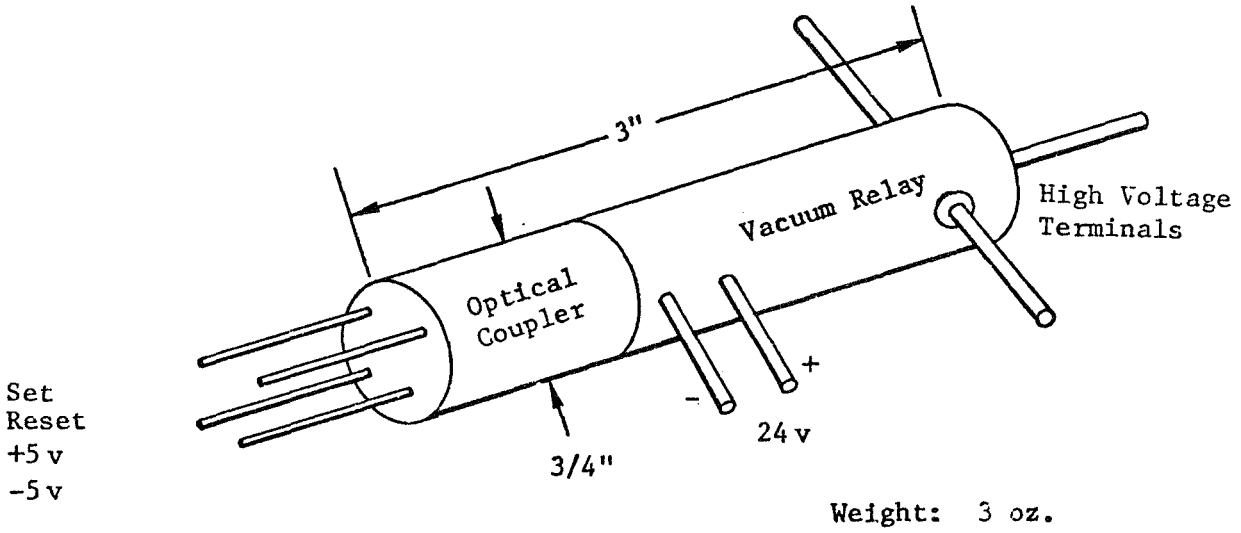
1. A series configuration.
2. Transistors switch the main load.
3. Thyristors are used to turn the transistors on.
4. Control signals are optoelectronically coupled to the switch.

4.6 Opto-Mechanical Relay

The inherent power losses in semiconductor switches suggest the appropriateness of a comparison with switches having metallic contacts. For this comparison, we postulated an opto-mechanical combination of photo-isolation and vacuum switch technology. The conceptual design is shown in Figure 15. Its specifications are:

Working voltage	16 kV
Working current (hot switching)	1 A
Contact resistance	0.015 Ohm
Contact type	SPDT
Latching	Magnetic
Size (Figure 25)	3/4 inch diameter by 3 inches long
Weight	3 Ounces (85 grams)
Isolation to coil driver	Optical
Set-reset pulses	2 ms

Power losses in this switch are compared in the following table with the losses in a 16 kV 1 A series transistor-switch based on the SDT 8805 transistor.



Weight: 3 oz.

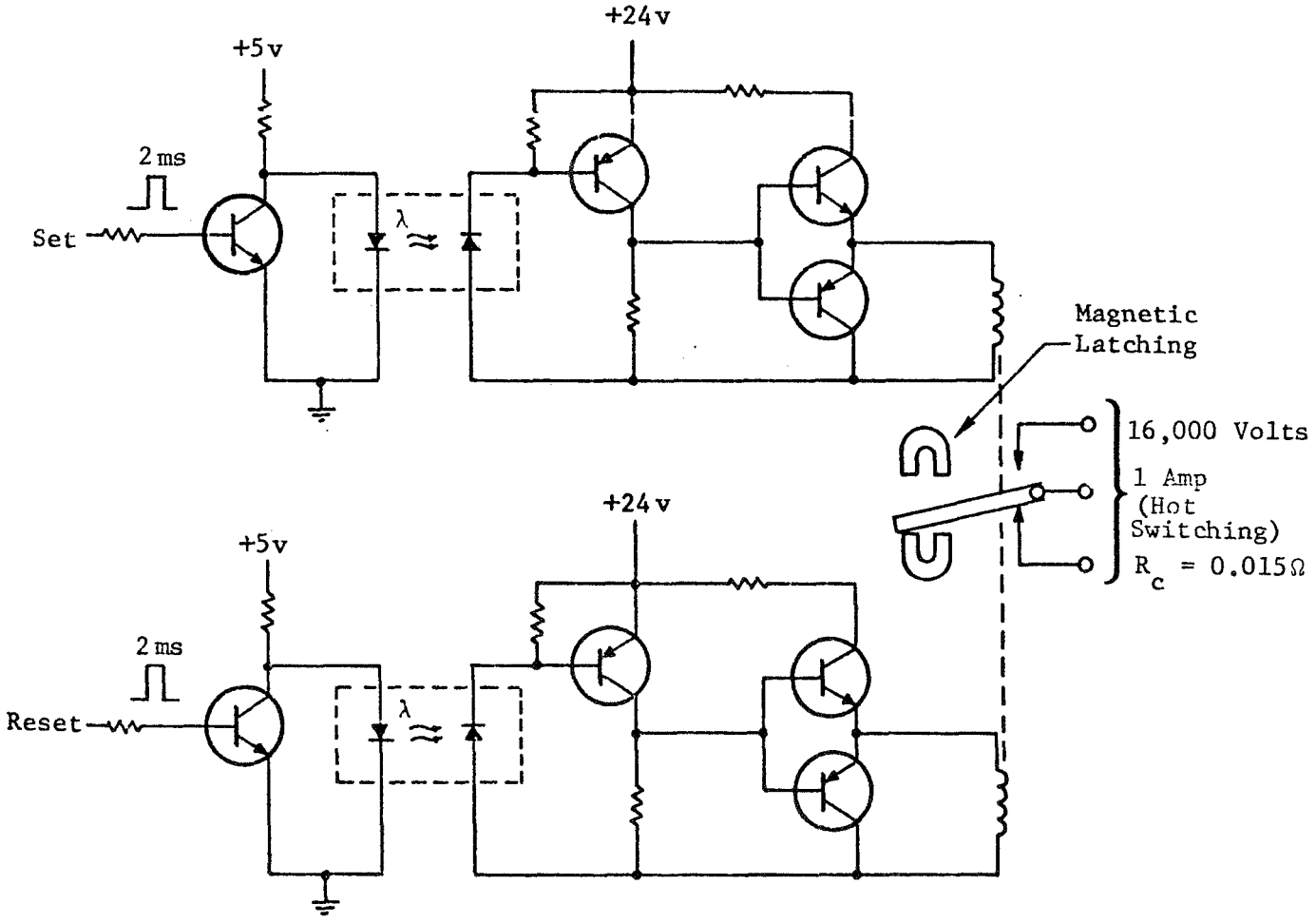


Figure 15 : CONCEPTUAL PHOTOMECHANICAL SWITCH

Switch State	SPST Opto-Mech. Relay		Series Transistor Switch		
	Contacts	Driver	Collector-Emitter		Base Drive
On	0.015 Watt	-	1.71 Watts		0.96 Watt
Transfer	-	Negligible (2 ms pulse)	-		-
Off	0	Negligible (0.0014 W)	Temp.	°C	-
			55	150	
			0.128W	32W	

The advanced configuration would require 57 of the above switches with SPDT contacts and 69 with a SPST contact arrangement.

4.7 Switching Device Summary

Evaluation of the above information clearly shows the possibilities for development of circuitry to utilize the desirable characteristics of semiconductors. Most of the semiconductor technology required is presently available. High voltage transistors and SCR's require additional development. The exceptionally high efficiency predicted for the conceptual opto-mechanical switch indicates this device should also be studied. The technology of such a device has not progressed rapidly in recent past due to lack of emphasis.

4.8 The Switch Assembly

The "cutpoint" concept needs to be related to the electrical capability of single semiconductor devices, their circuitry and their physical arrangement. The concept of the "switch assembly" was developed and is illustrated in Figures 16, 17, and 18 for a unit that receives switching commands optically. Power to operate the assembly comes from one source. The assembly has one or more cutpoints, each made up of a series-parallel matrix of n_s semiconductor devices in series and n_p devices in parallel. Each device includes the supporting circuitry to drive it from the optical signal. An example of a circuit within one cutpoint for which $n_s = 3$ and $n_p = 1$ is provided in Figure 14.

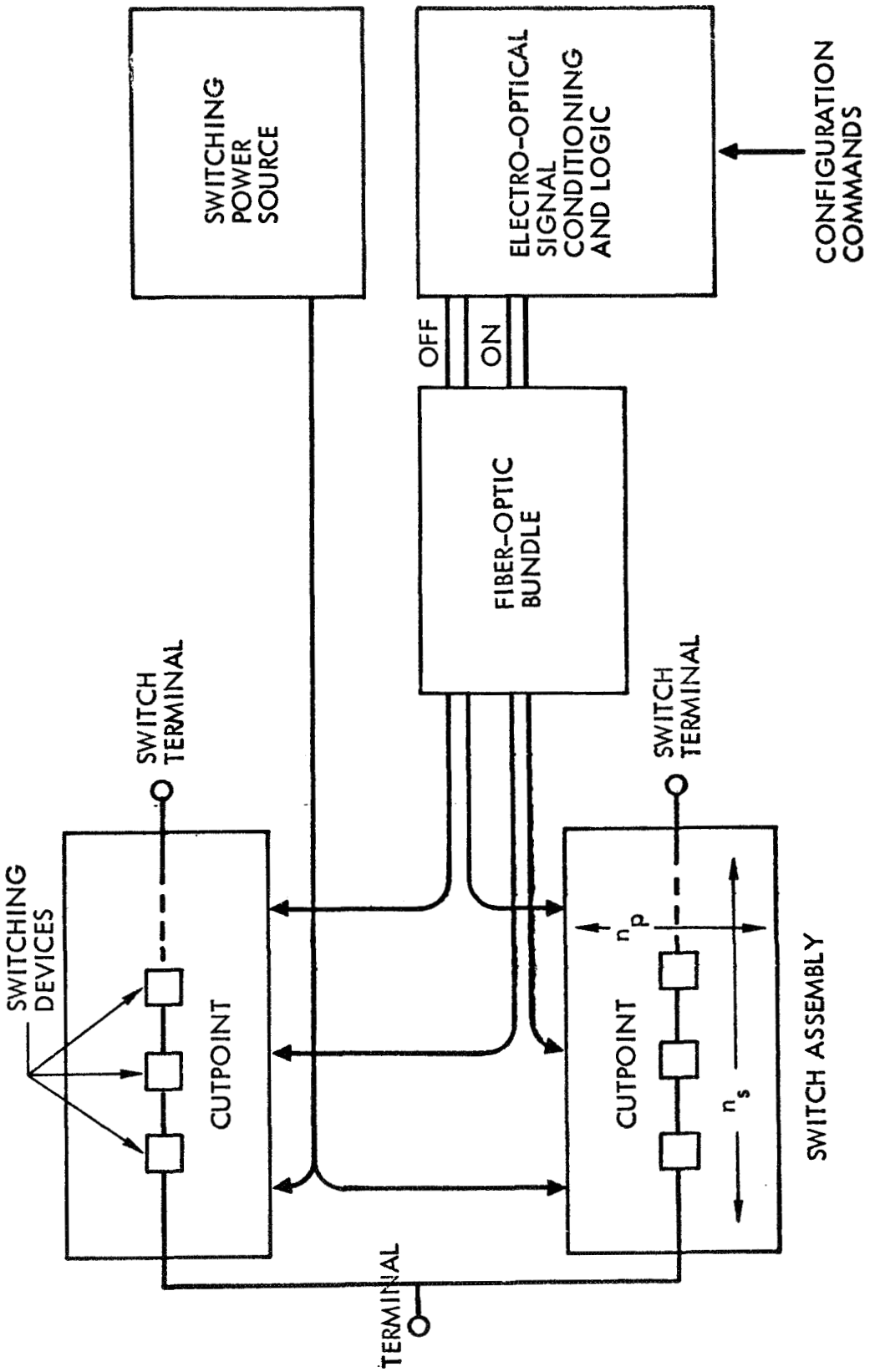


Figure 16: SWITCH ASSEMBLY

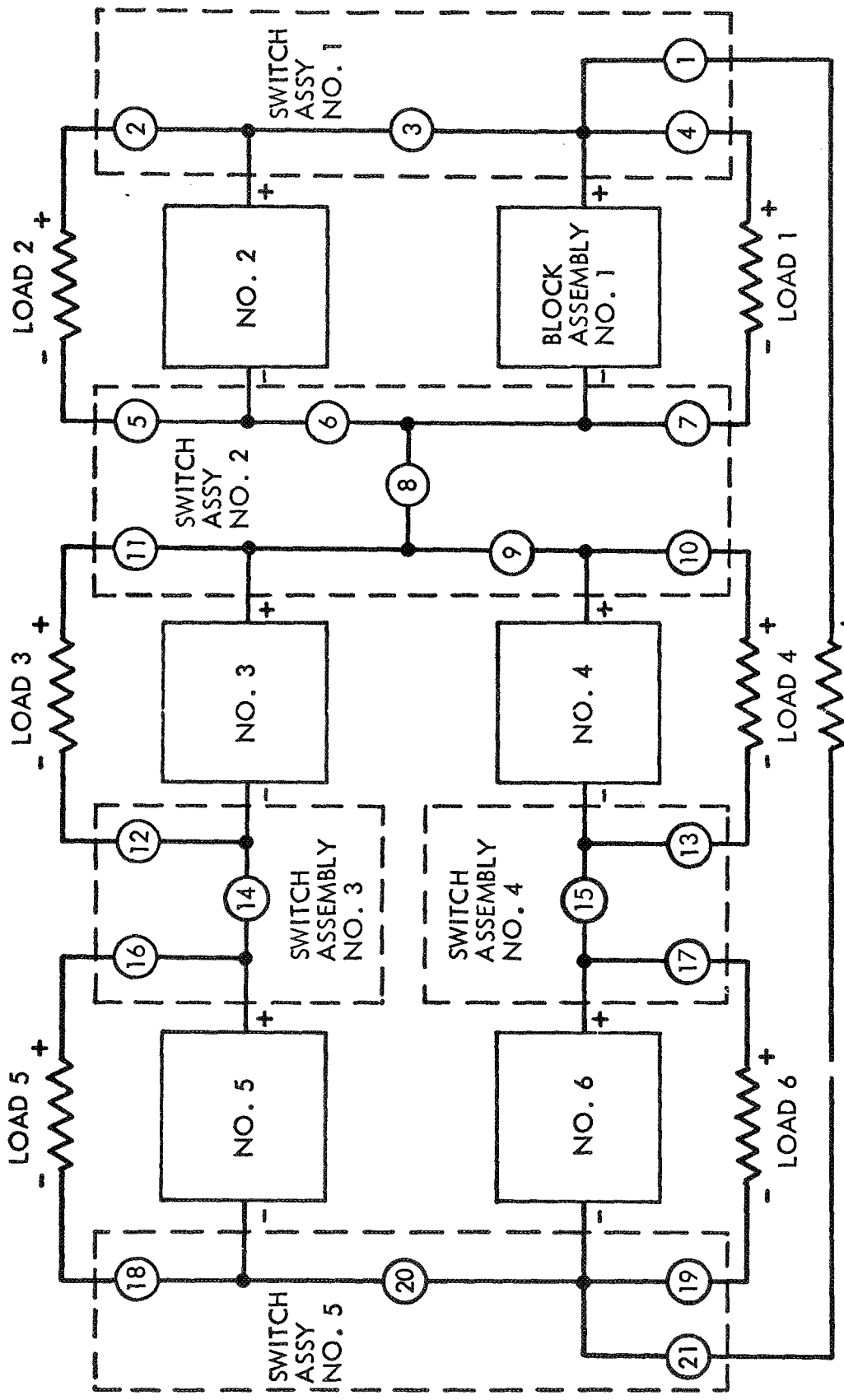


Figure 17: INTERBLOCK SWITCHING

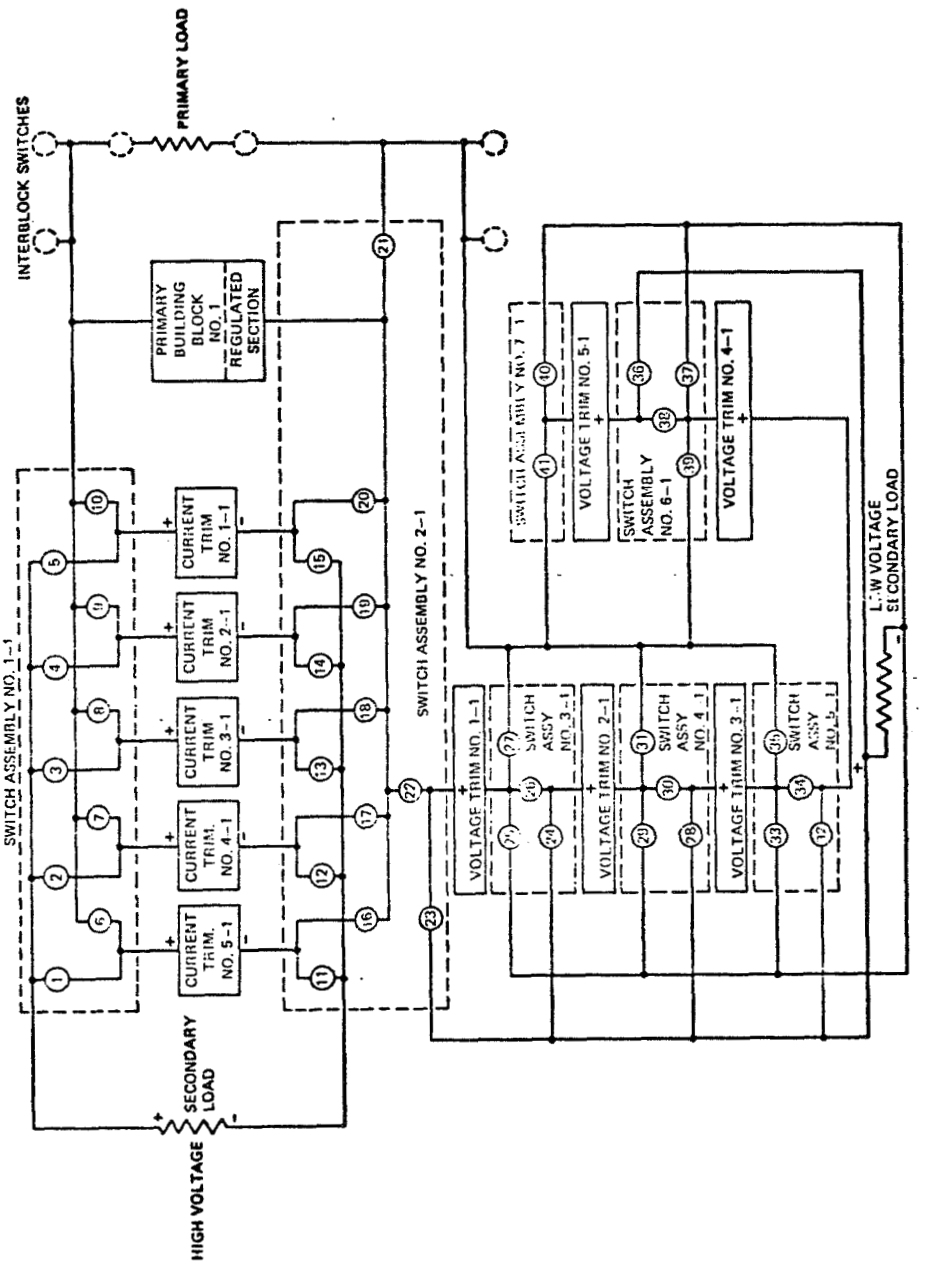


Figure 18: INTRABLOCK SWITCHING

4.9 Switching Complexity, Size, and Weight

A good index of the complexity of a high voltage switching system is the number of switching devices used. With the basic and advanced configurations defined, their complexity can be calculated on this basis as a function of device voltage, array voltage, and block voltage. Figure 19 shows this relationship for the basic configuration while Figure 20 shows it for blocks similar to those used in the advanced configuration but with five trimmers. The following table shows weight and area requirements for switching in the advanced and basic configurations described in section 2.0.

Device operating characteristics assumed in the analysis were:

Working voltage	700 volts
Working current	1 A
Three-Device module weight	10 grams
Module area	2 cm^2

Cutpoints rated for simultaneous switching.

	Configuration	
	Basic	Advanced
Number of Switch Modules	33	273
Total Weight	0.033 kg	2.73 kg
Total Area	0.0132 m^2	0.109 m^2

Note that the greater switching complexity of the advanced configuration is the cost for the better power utilization obtained.

4.10 Switching Losses

Operation of semiconductor switches entails three types of power losses:

- o Forward resistance drop in the ON state
- o Reverse current in the OFF state
- o Bias power required to operate the switch

These losses have been calculated for the switching system which includes the reconfiguration switching and trimmer switching (Figure 17,18). The calculations were made for two conditions:

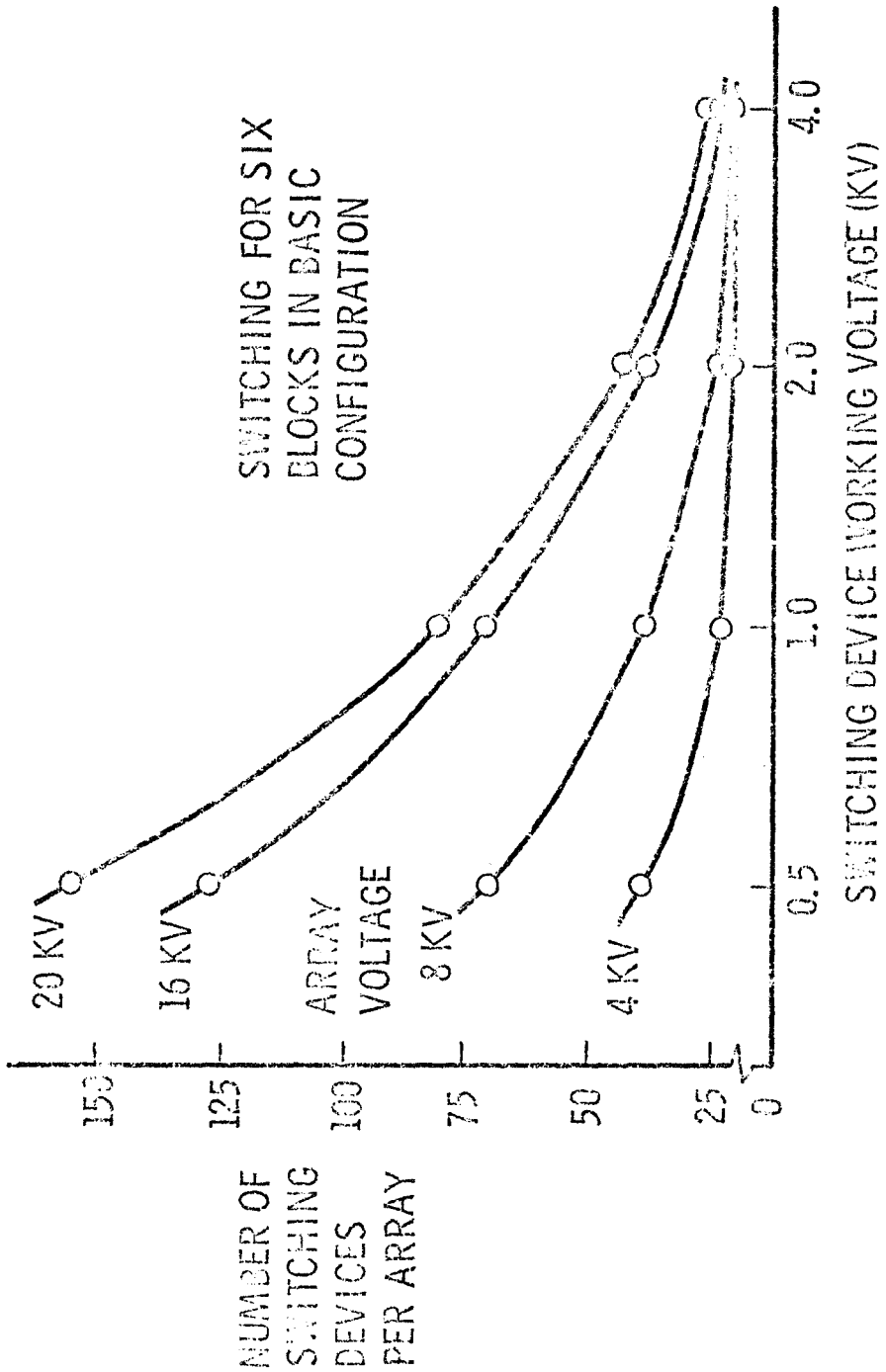


Figure 19: EFFECT OF DEVICE VOLTAGE ON INTERBLOCK SWITCHING COMPLEXITY

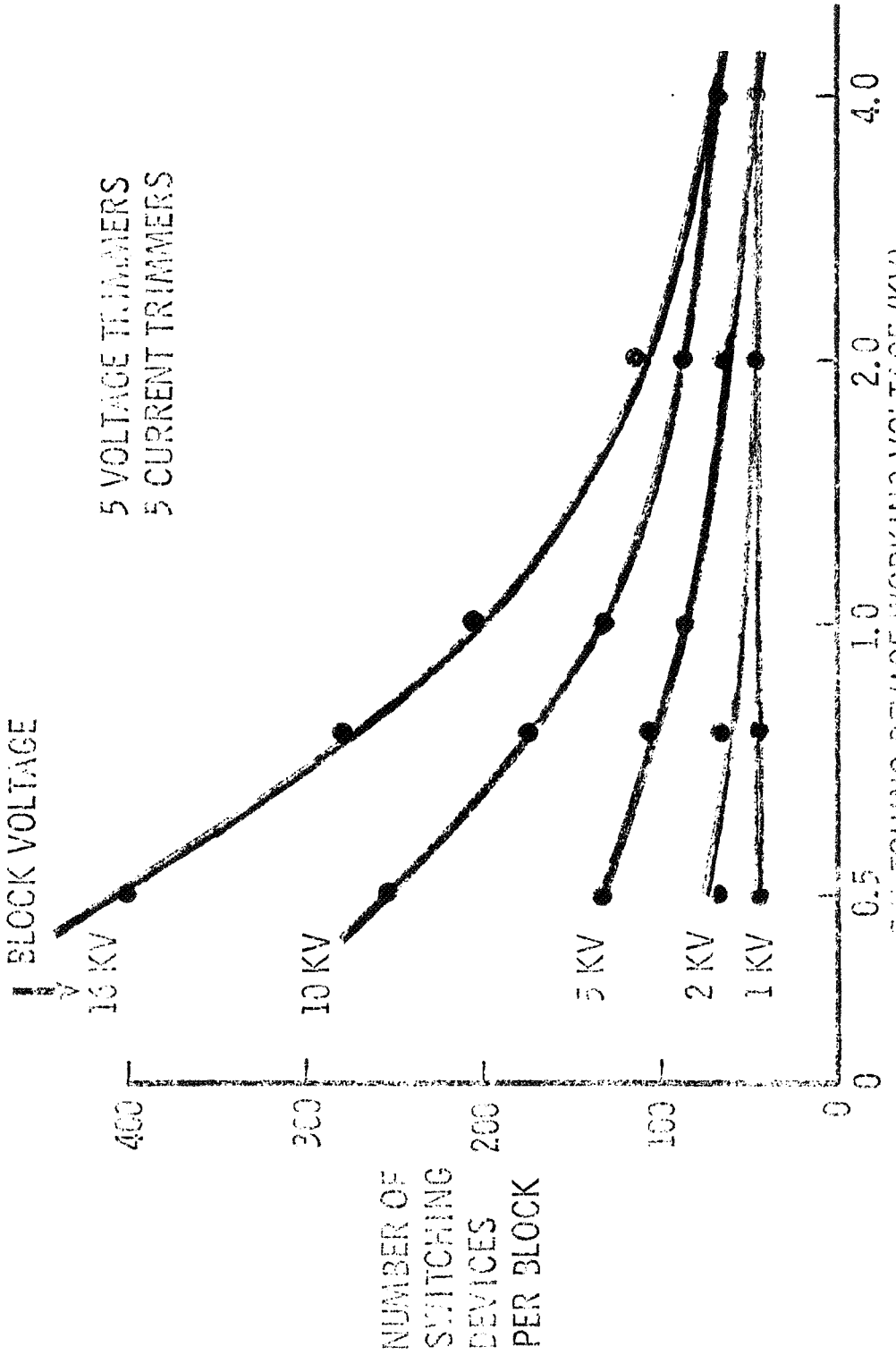


Figure 20: INTRABLOCK SWITCHING COMPLEXITY

a) At launch, with the array configured for transfer-orbit loads, and no trimmers augmenting the basic blocks.

b) At mission end, with the array configured for synchronous-orbit load, and all trimmers connected to the basic blocks.

The switch circuit shown as Figure 14 was used as a model and the following high-voltage transistor characteristics were assumed:

V_{CEO} = 700 volts

H_{FE} = 20 minimum at 1 A, -55°C

V_{SAT} = $V_P + I_c R_c$, where

V_p = 0.045 max at -55°C

R_c = 0.025 max at -55°C

I_{CBO} = 1 mA at 25°C

= 2 mA at 155°C

The transistor base bias is supplied at 5 volts with the base resistors considered part of the switch.

The calculated power for Block 1 intrablock switching and interblock switching are shown in Tables 2 and 5, which appear in Section 2. Intrablock switching power for blocks 2 through 6, shown in Table 9, was calculated from the Block 1 data on the basis of block voltage.

	Switching Power Required (Watts)	
	At Deployment	At Mission End
Reconfiguration Switching (Interblock)	7.59	7.86
Trimmer Switching (Intrablock)		
Block 1 (2 kV)	2.26	1.93
Block 2 (2 kV)	2.26	1.93
Block 3 (8 kV)	9.05	7.75
Block 4 (11 kV)	20.70	10.62
Block 5 (6 kV)	6.80	5.80
Block 6 (3 kV)	3.39	2.90
TOTALS	52.05	38.79

Table 9: SWITCHING POWER SUMMARY

The highest switching power at the time of deployment represents 0.3 percent of the 15-kW total array output.

4.11 Switching Logic

Figure 21 shows logic for inter-block reconfiguration switching by ground command, and also for re-establishing configuration after solar eclipse Checkouts verify switching operations. Anomalous operation requires intervention by ground command. Configurations are commanded from a memory-stored matrix which indexes each cut point for each command. An example of a stored matrix is shown in Table 10. Ground access to on-board computer storage is required for updating configuration requirements and trouble-shooting. Sequential switch operation would occur in the logic blocks (Figure 21) labeled "Turn off Loads", "Reconfigure Signals" and "Apply Loads".

Figure 22 shows the logic for switching trimmers within each block. Block current, I_b, is sensed and compared with its limits I_b(MAX) and I_b(MIN). Trimmers are switched in and out when I_b is out of tolerance and cannot be controlled by regulator action. Sequential switch operation would occur in the logic blocks labeled "Transmit trimming signals to switches". An example of the stored matrix for trimmer switching is shown in Table 11.

		COMMAND			
		SUPPLY LOADS 1 THRU 6		SUPPLY LOAD 7	
CUT POINT	SWITCH ASSEMBLY	OPEN	CLOSED	OPEN	CLOSED
1	1	X			X
2	1		X	X	
3	1	X			X
4	1		X	X	
5	2		X	X	
6	2	X			X
7	2		X	X	
8	2	X			X
9	2	X			X
10	2		X	X	
11	2		X	X	
12	3		X	X	
13	4		X	X	
14	3	X			X
15	4	X			X
16	3		X	X	
17	4		X	X	
18	5		X	X	
19	5		X	X	
20	5	X			X
21	5	X			X

Table 10: INTERBLOCK SWITCHING COMMANDS

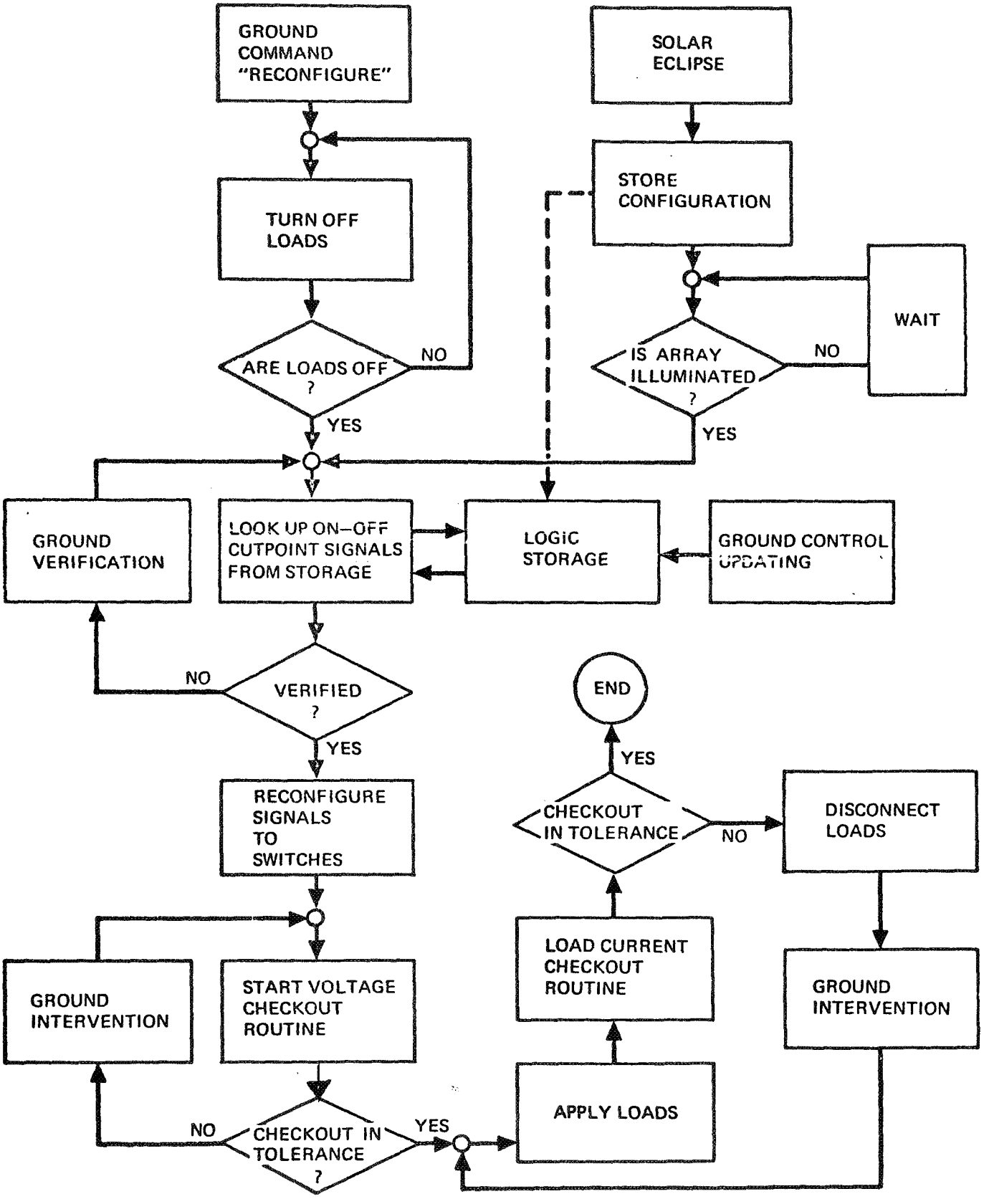


Figure 21: INTERBLOCK RECONFIGURATION SWITCHING LOGIC

FIG. 18 CUTPOINT	SWITCH ASSEMBLY	CUT POINT STATUS											
		STATUS AT DEPLOYMENT		ADD 1ST TRIM. PAIR		ADD 2ND TRIM. PAIR		ADD 3RD TRIM. PAIR		ADD 4TH TRIM. PAIR		ADD 5TH TRIM. PAIR	
		OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED
1	1-1		X		X		X		X		X		X
2	1-1		X		X		X		X	X			X
3	1-1		X		X		X	X		X			X
4	1-1		X		X	X		X		X			X
5	1-1		X	X		X		X		X			X
6	1-1	X		X		X		X			X		X
7	1-1	X		X		X			X		X		X
8	1-1	X		X		X			X		X		X
9	1-1	X		X			X		X		X		X
10	1-1	X			X		X		X		X	X	
11	2-1		X		X		X		X	X		X	
12	2-1		X		X		X	X		X		X	
13	2-1		X		X	X		X		X		X	
14	2-1		X		X	X		X		X		X	
15	2-1		X	X		X		X		X			X
16	2-1	X		X		X		X			X		X
17	2-1	X		X		X			X		X		X
18	2-1	X		X		X			X		X		X
19	2-1	X		X			X		X		X		X
20	2-1	X			X		X		X	X		X	
21	2-1		X	X		X		X			X		X
22	2-1	X			X		X		X	X		X	
23	2-1		X	X		X		X		X		X	
24	3-1		X		X	X		X		X		X	
25	3-1		X	X		X			X		X		X
26	3-1	X		X			X	X		X		X	
27	3-1	X			X	X		X		X		X	
28	4-1		X		X		X	X		X		X	
29	4-1		X		X	X		X			X		X
30	4-1	X		X		X			X	X		X	
31	4-1	X		X			X	X		X		X	
32	5-1		X		X		X		X	X		X	

Table 11: INTRA-BLOCK TRIMMER SWITCHING LOGIC, ADVANCED CONFIGURATION

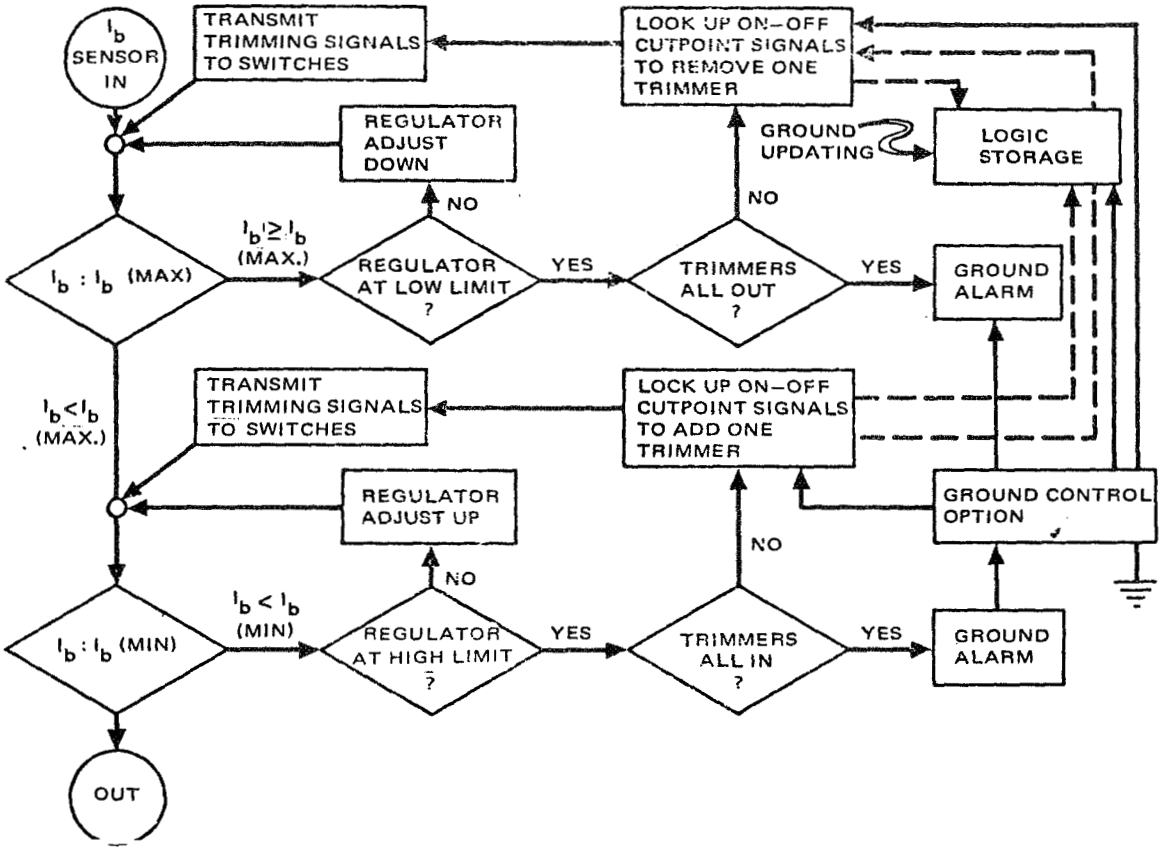


Figure 22: TRIMMER SWITCHING LOGIC

5.0 PROTECTIVE CIRCUIT AND DEVICE REQUIREMENTS AND DESIGN

The protective circuits have these functions:

- o Monitor essential system parameters and detect out-of-tolerance operation
- o Isolate faults internal-to external-to the high-voltage solar array
- o Attempt to compensate faults internal to the array by inserting reserve capacity to bring solar array performance back to within specified tolerance
- o Switch over to stand-by loads if required

Design features such as redundant blocking diodes and parallel shunting-diodes also serve a protective function. Should a blocking diode or shunting diode fail open, the parallel diode will carry the full current. These features provide automatic fault compensation, and require no sensing.

5.1 Causes of Failures

The first step in the development of an economical protection circuit, one that has few parts and consumes little power, is an analysis of the consequences of part failures. Possible part failures are:

Solar Cells - Tests have shown that an average of 40 percent of the area of a solar-cell is lost per solar cell fracture (Reference 4). These fractures may be caused by meteoroids, thermal cycling, or mechanical stressing during propulsion maneuvers. Systematic failures are assumed to have been eliminated by proper design and qualification testing.

Diodes - The observed failure modes in order of probability are leakage current degradation, breakdown voltage reduction, open-circuit, and short-circuit.

Table 12 shows the effects of these changes in diode characteristics on the solar array.

LEAKAGE CURRENT DEGRADATION	FORWARD CONDUCTANCE DEGRADATION	BREAKDOWN VOLTAGE REDUCTION	OPEN CIRCUIT	SHORT CIRCUIT
1. SHUNT DIODES				
POSSIBLE LOSS IN USEFUL POWER	LOSS IN USEFUL POWER IF REQUIRED TO CONDUCT	LOSS IN POWER IF EXCESSIVE	LOSS OF BYPASS CAPABILITY IN EVENT OF CELL OPEN CIRCUIT	SUBMODULE OUTPUT IS LOST
2. BLOCKING DIODES				
LOSS OF POWER IF BLOCKING ACTION IS REQUIRED (DEFECTIVE ARRAY BLOCK MAY BE ISOLATED BY SWITCHING)	LOSS IN USEFUL POWER; DIODE MAY OVERHEAT AND FAIL SHORTED	DIODE MAY FAIL OPEN OR SHORTED	LOSS OF ARRAY OR BLOCK ASSEMBLY IF DIODES IN DIFFERENT LEGS FAIL	LOSS OF ISOLATION

Table 12: EFFECTS OF DIODE FAILURES

Figure 23 shows the compensation that shunting diodes provide for solar-cell open-circuit failures. The intersection of the load line with the submodule I-V characteristic for 13 cells in parallel is at point A. One failure, leaving 12 cells operational moves this intersection to point B. Two failures, leaving 11 cells operational, drops the submodule voltage to -10 volts (point C) if there are no shunt diodes. Shunt diodes will limit the operating point to the forward bias voltage of the diode or about -0.7 volts (point D).

Transistor Switch - The solar array regulation may be affected by degradation in the operating characteristics of the power transistors which shunt the primary block regulating modules. Whether performance is affected depends on factors such as array capability, load magnitude, and availability of trimmers. The worst transistor failure modes from a performance standpoint are open and short-circuit. The most prevalent failure in a transistor is, however, excessive leakage current when the transistor is in the OFF mode.

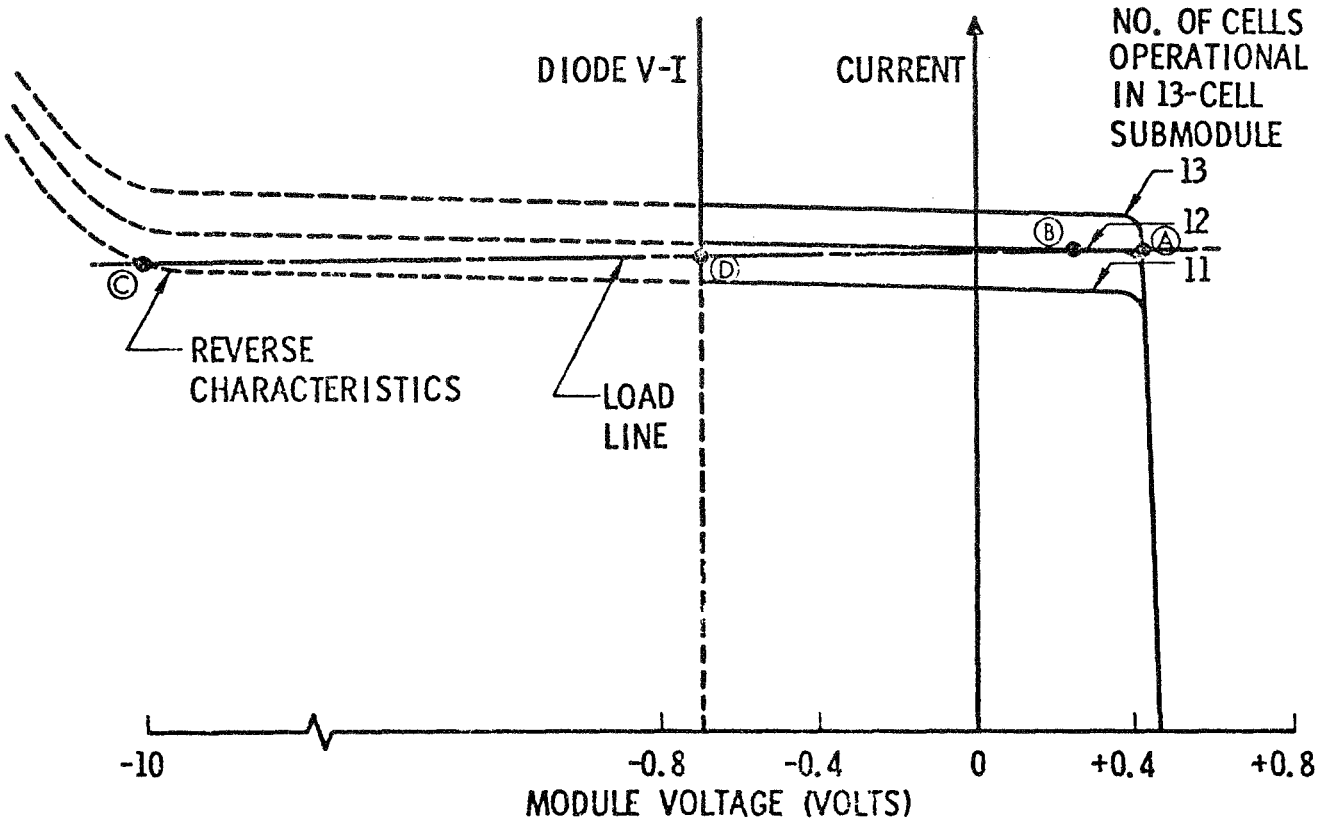


Figure 23: EFFECT OF SOLAR CELL OPEN CIRCUITS

It is evident that some modes of degradation, such as a moderate increase in saturation resistance are benign, and will not cause out-of-tolerance performance. To avoid thermal run-away, the transistor heat sink should be designed to dissipate significantly more power than required when the transistor is ON.

Switches - Failures in both load and reconfiguration switches are compensated for by redundancy design.

Regulator - Failures within the regulator are also compensated for by providing the level of part redundancy established by the reliability analysis.

5.2 Protection Concept

Having identified the modes of possible failures within the array, an overall fault-protection design approach was developed. This approach (Figure 24) starts with sensing the loaded array current and voltage and the open circuit voltage. These three parameters are transmitted to a central computer programmed to answer the following questions:

- Does an out-of-tolerance condition exist?
- Is this condition caused by a malfunction in the source or the load?
- What command will remove the out-of-tolerance condition?

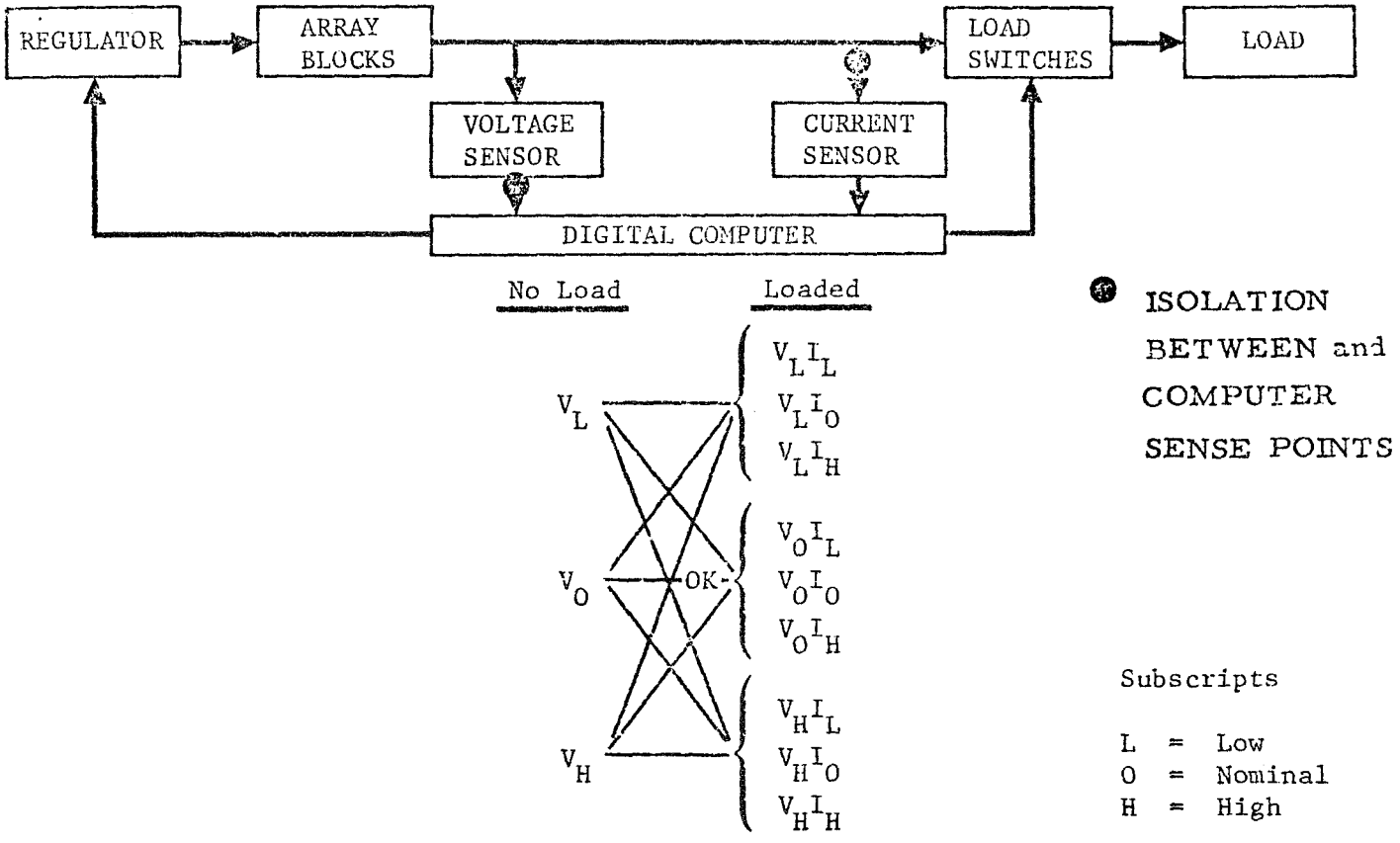


Figure 24: PROTECTION CONCEPT

The logic required to achieve the proper fault compensation is illustrated in Table 13. By knowing the bus voltage and current, the source open circuit voltage and the type of load supplied, the failure can be determined and corrective action initiated. Loads can be typed as constant resistance (R), constant current (I) or constant power (P).

CASE	NO LOAD VOLTAGE	LOAD V & I	LOAD	FAILURE	CORRECTIVE ACTION
1	V_L	$V_L I_L$	Const.R Const.R) Const.P)	Regulator Under Voltage Insufficient Current Trimmers	A,C,S A,C,S
2	V_L	$V_L I_o$	Const.I	Regulator Undervoltage	A,C,S
3	V_L	$V_L I_H$	Const.P	Regulator Undervoltage	A,C,S
4	V_L	$V_o I_L$	-	-	-
5	V_L	$V_o I_o$	Any	No failure will be sensed	None
6	V_L	$V_o I_H$	-	-	-
7	V_L	$V_H I_L$	Const.P	Too Many Current Trimmers & Reg. Under-V	A,C,S
8	V_L	$V_H I_o$	Const.I	Too Many Current Trimmers & Reg. Under-V	A,C,S
9	V_L	$V_H I_H$	Const.R	Too Many Current Trimmers & Reg. Under-V	A,C,S
10	V_o	$V_L I_L$	Const.R, I or P	Insufficient Current Trimmers	A,C,S
11	V_o	$V_L I_o$	Const.I	Insufficient Current Trimmers	A,C,S
12	V_o	$V_L I_H$	Const.P Any	Insufficient Current Trimmers Load Short Circuit	R,C,A,D,S
13	V_o	$V_o I_L$	Any	Open Circuit Load Switch - or High Resistance in Circuit	R,D
14	V_o	$V_o I_o$	Any	OK	None
15	V_o	$V_o I_H$	-	Load Resistance Lower than Normal	R,C,D
16	V_o	$V_H I_L$	Const.P Any	Too Many Current Trimmers Load Open Circuit - or High Resistance in Circuit	C,A,D,S

(Continued on next page)

Table 13: PROTECTION LOGIC

CASE	NO LOAD VOLTAGE	LOAD V & I	LOAD	FAILURE	CORRECTIVE ACTION
17	V_o	$V_H I_o$	Const.I	Too Many Current Trimmers	A,C,S
18	V_o	$V_H I_H$	Const.R	Too Many Current Trimmers	A,C,S
19	V_H	$V_L I_L$	Const.R, I or P	Insufficient Current Trimmers & Reg. Over-V	A,C,S
20	V_H	$V_L I_o$	Const.I	Insufficient Current Trimmer & Reg. Over-V	A,C,S
21	V_H	$V_L I_H$	Const.P	Regulator Overvoltage or Too Many Current Trimmers	A,C,S
22	V_H	$V_o I_L$	-	-	-
23	V_H	$V_o I_o$	Any	No Failure Will be Sensed	None
24	V_H	$V_o I_H$	-	-	-
25	V_H	$V_H I_L$	Const.P	Regulator Overvoltage or Too Many Current Trimmers & Reg. Over-V	A,C,S
26	V_H	$V_H I_o$	Const.I	Regulator Overvoltage or Too Many Current Trimmers & Reg. Over-V	A,C,S
27	V_H	$V_H I_H$	Const.R	Regulator Overvoltage or Too Many Current Trimmers & Reg. Over-V	A,C,S

CORRECTIVE ACTIONS: R - Open Load Switch, Wait, Reclose Switch;
A - Alternate Switching by Regulator;
C - Change Loads;
D - Drop Load, Connect Alternate Load;
S - Source Bad, Drop Source & Load or Change Source.

SUBSCRIPTS: L = Low, o = Nominal, H = High

Table 13: PROTECTION LOGIC (Continued)

There are two ways of processing voltages and current information:

a) The voltage and current are sensed and compared against a reference, then their status is transmitted as discrete OVER or UNDER signals to the computer (Figure 25).

b) Voltage and current are sensed, transmitted as analog signals to the computer, and compared in the computer (Figure 26).

Method (a) has the advantage that the signals to the computer can be transmitted economically. On the other hand, this concept requires array-mounted references and logic elements for making comparisons.

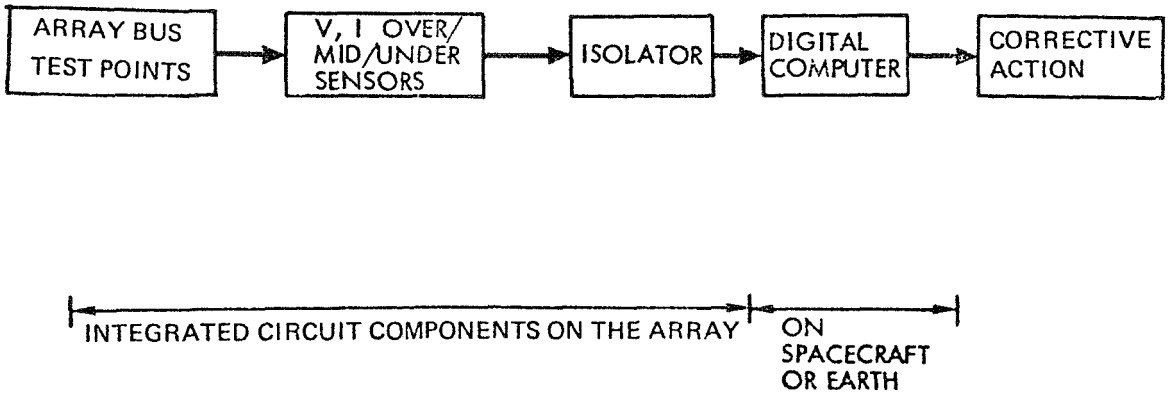


Figure 25: OVER-MID-UNDER SENSING

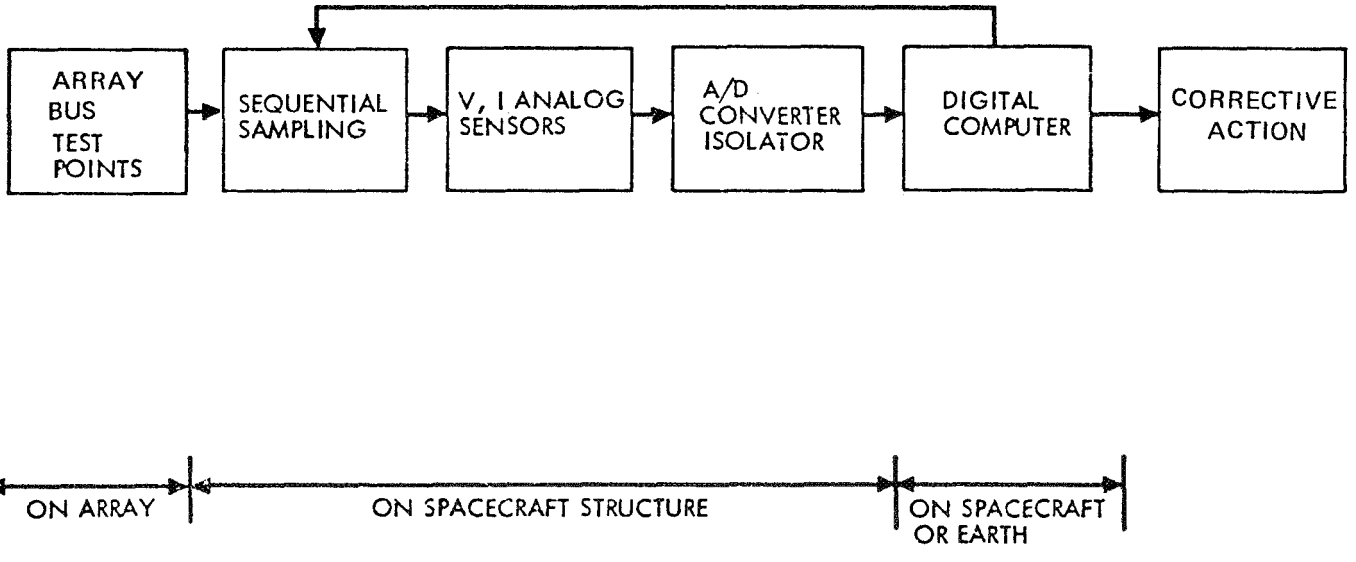


Figure 26: MAGNITUDE MONITORING

Changing the tolerance band during flight would require additional circuitry, and reduce the transmission economy with respect to method (b).

Method (b) has the flexibility of reprogramming tolerances within the computer, by command link. Also, studies on the Boeing AWACS program have shown that in general, it is more economical to design a computer buffer capable of receiving a variety of analog or raw signals, and process these signals to a standard format within the computer. On the other hand, analog signals are harder to transmit without loss of accuracy across the high-voltage to low-voltage isolation barrier.

After identifying an out-of-tolerance condition, the computer will try to compensate for this condition by issuing one of the following commands:

a. Open and reclose load switch
b. Open load switch to isolate a load fault
c. Switch source to an alternate load
d. Add current trimmers
e. Add voltage trimmers
f. Switch load to an alternate source

These functions must be accomplished by a computer that is isolated electrically from the loads to eliminate undesirable coupling. Thus the computer should be powered from an isolated section of the solar array. Similarly, voltage and current sensors must be electrically isolated from the bus which they are sensing.

5.3 Sensor Requirements

The requirements for the voltage and current sensors are derived from the range of voltages and load power in the statement of work.

The requirements of the voltage sensor are:

1. Voltage signal range: 2kV to 16 kV. Sensors will be designed for each specific load voltage. For example, a 16 kV sensor will be designed for the maximum load voltage.
2. Minimum detectable variation: $\pm$ 1 percent. With regulation of the array blocks to 0.1%, the allowable tolerance on a voltage signal is 10 times regulation accuracy. This band allows for voltage drops in switches and small variations in sensing components.

3. Isolation between sensor and signal circuits: 5kV to 40 kV. The isolator must insulate up to 40 kV, depending on its location on the array. It would be possible to have as much as 54 kV under open-circuit conditions at -170°C when the array is in a 100 nautical-mile orbit. However, this voltage can be limited by shorting the array, prior to its emergence from the Earth's shadow, by means of battery-supplied power. This can reduce the upper voltage limit to about 16 kV.
4. Signal level: The signal voltage corresponding to maximum bus voltage should be as high as the computer can accommodate to keep signal-to-noise ratio high. High versus low impedance signal transmission remains to be compared.

The requirements of the current sensor are:

1. Current signal range: 0 to 8A The sensor ranges can be more closely specified after the loads are identified.
2. Minimum detectable current variation: $\pm$ 1 percent
3. Isolation: The proposed configurations permit locating the current sensors on the low-voltage sides of power circuits. It follows that no unusual isolation is required except with loads whose both terminals are significantly different from the spacecraft reference potential.
5. Signal level: As with voltage, the optimum signal level and circuit impedance remain to be established after the loads are defined.

Voltage Sensors

An optically isolated voltage sensing circuit is shown in Figure 27. The operational amplifier can be National Semiconductor Corporation's model LM101. The size of the chip is 0.045 by 0.045 by 0.008 inches (0.11 by 0.11 by 0.02 cm). Gain control as well as feedback may be required for stability. The remainder of the thick-film circuitry will be on a chip about 0.1 by 0.1 by 0.015 inches in size (0.25 by 0.25 by 0.038 cm). The entire sensor will be about 0.25 by 0.25 by 0.015 inches (0.62 by 0.62 by 0.038 cm) in size and about 5 to 8 grams in weight. There will be 7 voltage sensors on the entire array, assuming 6 power sources during the first part of the mission and one source for the remainder of the mission.

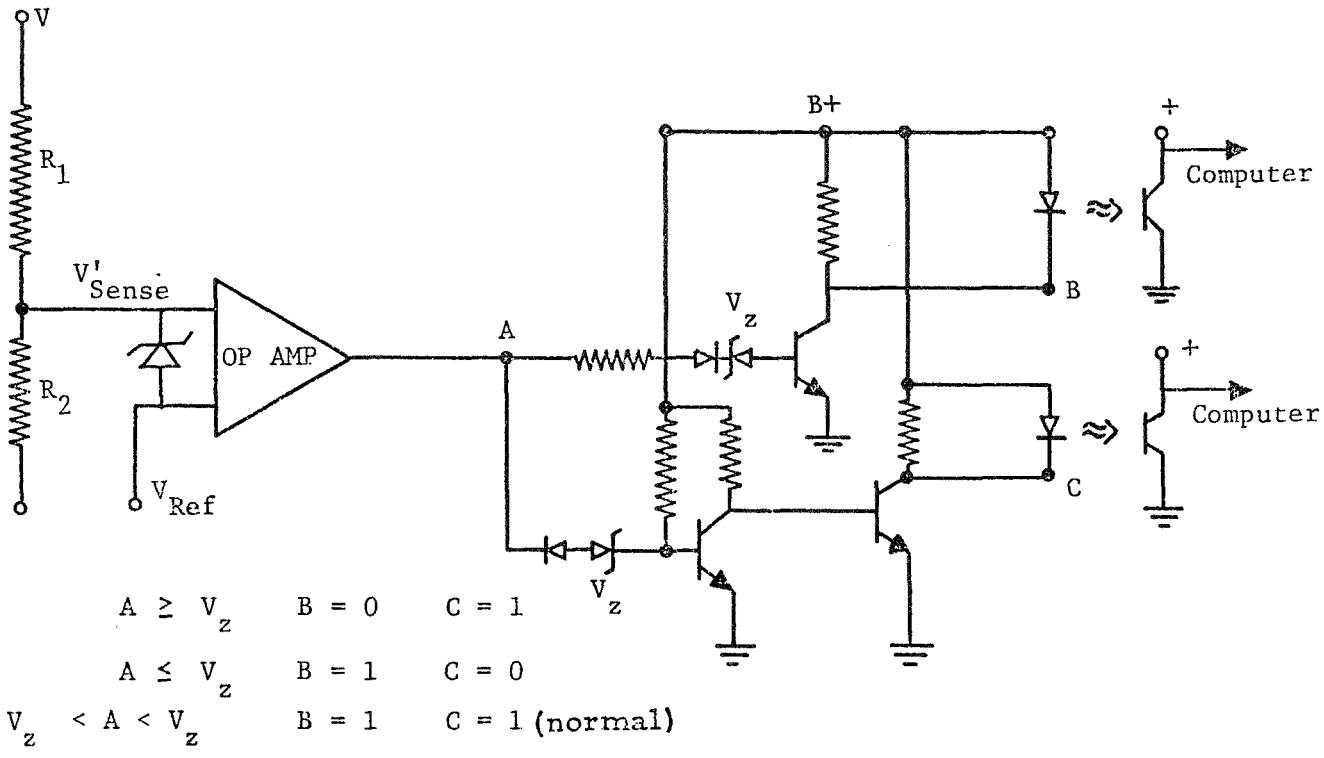


Figure 27: OVER/MID/UNDER SENSING---OPTICAL ISOLATION

Current Sensors

Current can be sensed with a transductor circuit (Figure 28) which provides an output voltage proportional to direct current. The circuit consists of an ac source, magnetic transductors, a full-wave bridge rectifier, a filter capacitor, and a resistive burden. Each transductor is alternately driven into saturation each half cycle of the oscillator voltage. One core will saturate after absorbing some volt-seconds of the applied ac voltage; its winding then appears as a short on the winding of the remaining core. This reduces circuit impedance to zero, even though the second transductor has not saturated, and the remainder of the applied ac voltage appears across the resistive burden. When the applied ac voltage changes polarity, the action is repeated with the second transductor being driven into saturation first. The voltage that appears across the resistive burden is converted to a direct voltage by the full-wave bridge, thus providing a dc voltage output.

When direct current flows through the control windings, the cores become saturated so that they will absorb less volt-seconds of the applied ac voltage. This results in a larger portion of the ac cycle appearing across the resistive burden, increasing the average output voltage of the transductor circuit in direct proportion to the current in the control windings.

The transductor elements are available in the smaller current ratings and could probably be developed for applications up to 8 amperes. The estimated weight is 8.5 grams and package size is 2 by 0.6 by 0.3 inches (5.1 by 1.5 by 0.75 cm). The square wave generator is a thick-film oscillator, 0.25 by 0.25 by 0.15 inches (0.64 by 0.64 by 0.38 cm) and weighs about 5 grams. The bridge would weigh 2 grams and be 0.25 by 0.12 by 0.015 inches (0.64 by 0.30 by 0.038 cm) in size. The generator and bridge could be custom designed for lighter weight. The output would use a detector similar to the voltage sensor previously described (Figure 27). The total package would weigh about 20 grams and require 0.7 square inches (4.5 cm^2).

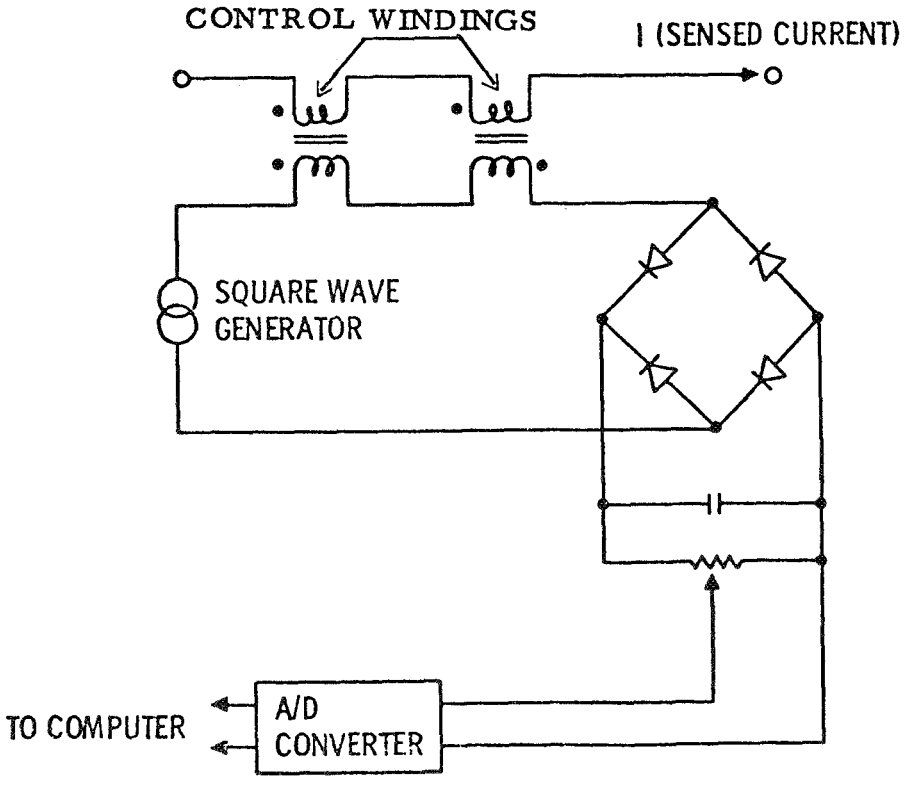


Figure 28: CURRENT SENSING - TRANSDUCTOR

A voltage sensing circuit that is magnetically isolated is shown in Figure 29. The operational amplifier can again be an LM101. The voltage-to-frequency converter is a thick-film circuit. The operational amplifier and converter would be about 0.10 by 0.10 by 0.015 inches (0.25 by 0.25 by 0.038 cm) in size and about 6 grams in weight. The magnetics would weigh about 10 grams and have a size of about 0.5 inch (1.2 cm) in diameter by 0.2 inch (0.50 cm) thick. The counter consists of two SN7493 integrated circuits (IC's) for input and two SN7494's for output to the computer. Each IC is about 0.785 by 0.310 by 0.06 inches (2.0 by 0.78 by 0.15 cm) and weighs 5 grams. It is assumed that the computer will have an internal clock capable of providing a 1 second gate. The total package will weigh about 30 grams and require an area of 1.25 square inches (8.1 cm^2). Optical coupling between the decoder and the computer may be required to provide sufficient isolation. This design with its magnetics and counters has an obvious disadvantage in weight and area compared to the first design.

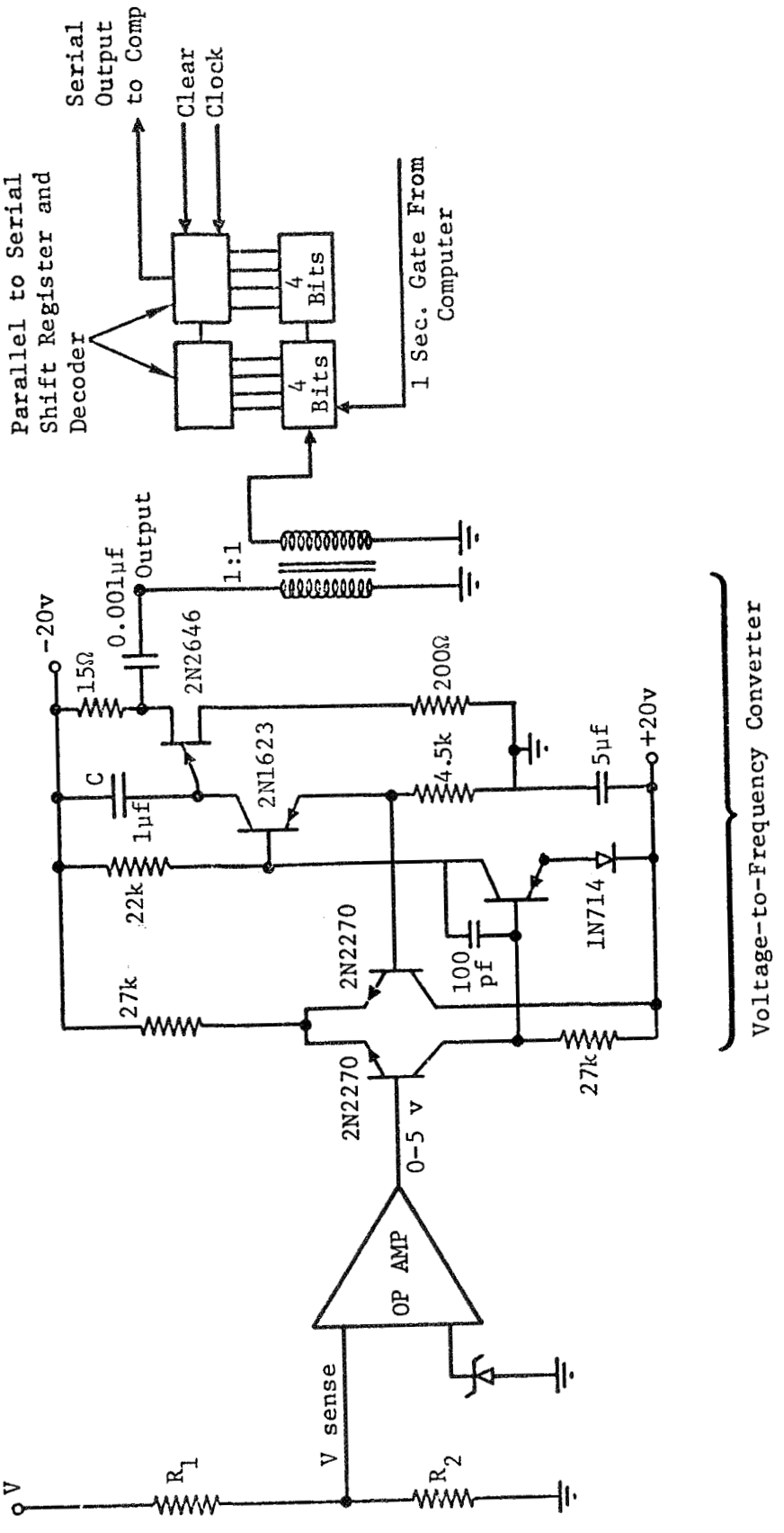


Figure 29: MAGNITUDE MONITORING---MAGNETIC ISOLATION

6.0 SOLAR CELL REQUIREMENTS

A solar cell configuration consists of a coverslide, a solar cell, a substrate, an interconnector, and adhesives to bond the coverslide and substrate to the solar cell. In this section we discuss how trapped radiation high voltages, and the ionospheric plasma affect the selection of a solar cell configuration. Emphasis is placed on comparing the benefits of different solar cell base resistivities and thicknesses as well as various coverslide thicknesses. A particular configuration is selected to allow comparison of high voltage array performance and weight with those of a low voltage array.

6.1 Radiation Effects

In the mission defined for this study, solar cells are exposed to a severe radiation environment, especially when in the trapped protons encountered during the 90-day orbit transfer. This section describes a method used to determine the equivalent 1-MeV electron fluence accumulated during the entire five year mission. Published solar cell performance data, corresponding to the calculated radiation level, were used in comparing cells of different thickness and base resistivity.

The minority carrier diffusion length of 10 ohm-cm N/P silicon solar cells was calculated for the end of the mission. This was done with a digital computer program which calculates how much the diffusion length changes each day of the mission, based on stored proton flux data and the proton damage coefficient for 10 ohm-cm cells on page IV-15 of Reference 5. The equivalent 1-MeV electron fluence and diffusion-length loss are affected by coverslide thickness, as shown in Table 14. The calculations assumed an isotropic proton flux, and 3 mils of polyimide and 1 mil of adhesive protecting the backside of the cell (References 6, 7). Radiation damage due to solar flares was not included in the calculation.

Degraded solar cell performance data was obtained from Reference 8 which presents the maximum-power output of bare silicon solar cells with different base resistivities and thickness as a function of 1-MeV electron fluence. By selecting data which corresponds to the fluences in Table 14, and correcting the data to 55°C, we obtained the end-of-mission output

Coverslide Thickness (mils)	Final Diffusion Length (microns)	Equivalent 1-MeV Electron Fluence (electrons/cm^2)
3	11.9	1.0×10^{16}
6	15.0	6.0×10^{15}
10	16.5	5.0×10^{15}
20	20.0	3.3×10^{15}

Table 14: EQUIVALENT 1-MeV ELECTRON FLUENCE

power of 10 ohm-cm and 2 ohm-cm cells for different solar cell and coverslide thicknesses (Table 15). The corresponding power-to-weight ratios for an array are shown in Table 16, which indicates that the use of 4-mil cells results in more than a 20 percent higher power-to-weight ratio than attained with 8-mil cells when 3-mil coverslides are used.

Base Resistivity (ohm-cm)	Cover Thickness: 3 mil			6 mil			10 mil			20 mil		
	Solar Cell Thickness (mils): 4	8	12	4	8	12	4	8	12	4	8	12
2	26.2	25.5	26.3	28.3	27.6	28.4	29.0	28.3	29.2	30.9	30.1	31.0
10	26.4	26.6	26.8	27.7	28.0	28.1	28.0	28.3	28.6	29.6	29.9	30.1

Maximum power values are given in milliwatts and correspond to 140 mw/cm^2, AMO light intensity at 55°C. Transmission loss in cover is included.

Table 15: END-OF-MISSION MAXIMUM-POWER OUTPUT OF 2 X 2 cm SILICON SOLAR CELLS

Base Resistivity (ohm-cm)	Cover Thickness: 3 mil			6 mil			10 mil			20 mil		
	Solar Cell Thickness (mils): 4	8	12	4	8	12	4	8	12	4	8	12
2	122	100	89	108	98	89	104	89	82	84	73	69
10	123	104	91	105	100	88	100	89	80	80	73	67

Solar-array power-to-weight ratios are given in percent of the value for 8 mil, 2 ohm-cm cells with 3-mil covers at 55°C.

Table 16: RELATIVE POWER-TO-WEIGHT RATIOS AT END-OF-MISSION

6.2 High Voltage Effects

During the orbit transfer the array will operate in the peak ion-density portion of the ionosphere at 300 kilometers altitude, unless it is chemically boosted to a higher altitude. Unless the array is electrically insulated from the surrounding plasma a substantial power loss could result from the collection of electrons or ions by high voltage portions of the array (Reference 7). Fused silica coverslides will insulate the front side of the solar array except for the area between cells. Poly-p-xylylene (Reference 9) and a polyimide (Reference 6) are promising insulating materials for filling the gaps between cells (Reference 7) and thus completely insulating the front side of the array. The polyimide sheet, is stable in space environments, and can form an insulating substrate which has excellent dielectric properties as well as being light and flexible.

The thicknesses of fused silica, poly-p-xylylene and polyimide required to withstand voltages as high as 16,000 volts are not yet known for an environment where a plasma is one of the electrodes and a solar cell the other (Reference 7). Whether or not a destructive voltage breakdown can occur depends upon the intrinsic dielectric strength of the insulation, the number, size and gaseous content of bubbles in the insulation, and the capability of the plasma on the space side of the insulation to sustain an electric breakdown. For example, were it not for imperfections,

a 3-mil coverslide of fused silica would provide adequate insulation, the intrinsic dielectric strength of fused silica exceeding 12,000 volts/mil. However, bubbles in the coverslide decrease the actual dielectric strength markedly although the magnitude of this decrease is not known for the situation where a plasma is one of the electrodes. Some evidence suggests that the plasma "electrode" will limit current and permit only non-destructive breakdown. Future experimental work, such as that proposed in Reference 7, is required to establish the destructive breakdown strength of insulators with known bubble content under plasma conditions.

Extrapolation of published data (Reference 9) indicates that 4-mils of polyimide film can withstand 16 kV for 44,000 hours in vacuum. Since, in the mission defined for this study, the insulation on the array is required to sustain high voltages only during some 2000 hours of passage through the ionosphere, we believe that 3-mil polyimide film is sufficient substrate insulation, although experimental confirmation is desired. Both poly-p-xylylene and fused silica have higher dielectric strengths than polyimide film, so 3-mil thicknesses of these other insulators should also be sufficient. Thus, the specific configuration described in Section 6.4 is based on a 3-mil thickness of poly-p-xylylene, fused silica or polyimide where insulation is required.

6.3 Selection of Solar Cell and Coverslide

On the basis of highest end-of-mission power-to-weight ratio, the best selection is a 4-mil, 10 ohm-cm cell with a 3-mil cover (Table 17). A strong second choice is the 4-mil, 2 ohm-cm cell with a 3-mil cover, which has only a one percent less power-to-weight ratio at the end of the mission, but has a much higher value at the start of the mission. The 2 ohm-cm cell may be the best choice if the extra power can be used at the beginning of the mission, or if the initial chemical boost is to an altitude above much of the trapped proton radiation. Conversely, the more radiation-resistant 10 ohm-cm cell may be the best choice if a more time-invariant output is desired, or if the mission occurs during a period of high solar activity when solar protons can degrade array performance.

Combination Number	Power-to-Weight Ratio of Array		Base Resistivity	Solar Cell Thickness	Cover Thickness
	End of Mission at 55°C	Start of Mission at 95°C			
	% of Combination No. 7	% of Combination No. 7	(ohm-cm)	(mils)	(mils)
1	123	86	10	4	3
2	122	103	2	4	3
3	108	91	2	4	6
4	105	76	10	4	6
5	104	88	10	8	3
6	104	79	2	4	10
7 (Combination Selected in Ryan Study (Reference 10))	100	100	2	8	2
8	100	79	10	8	6
9	100	66	10	4	10
10	98	90	2	8	6

Table 17: COMPARISON OF SOLAR CELL AND COVER COMBINATIONS

Power-to-weight ratios are not the only factors to consider in the selection of cell and coverslide thicknesses. The 4-mil cell thickness and 3-mil cover thickness may be too costly; in 1970, 4-mil cells and 3-mil covers cost twice as much as the thicker ones. Furthermore, the breakage rate of the thinner cells and covers is higher than for thicker ones. However, costs of thin cells and covers may come down if large quantities are being ordered. Nevertheless, we feel that 4-mil cells and 3-mil coverslides should be seriously considered because of their high end-of-mission power-to-weight ratio (about 20 percent higher than that of 8-mil cells with 3-mil coverslides).

6.4 Proposed Configuration

It is useful to compare the power and weight characteristics of low voltage and high voltage solar arrays. This is done in Section 9.0. The comparison low-voltage array was one developed by Ryan (Reference 10). The proposed

high-voltage solar cell configuration differs from that selected by Ryan in the choice of solar cell base resistivity, solar cell thickness, substrate thickness, interconnector material, and interconnector insulation (Table 21). The adhesives are the same. Except for interconnector insulation, the above features are not used in the performance analysis (Section 9.0) because they would affect a high voltage as well as a low voltage array.

The 4-mil cells were found to be better for the high-voltage array than the 8-mil cells in the Ryan design. The reason is that at the end of the mission the 4-mil cells produce as much power as 8-mil cells do, but weigh

ELEMENT	CHOICE BOEING HIGH VOLTAGE SOLAR ARRAY	RYAN LOW VOLTAGE SOLAR ARRAY
Solar Cell		
Type	N/P Silicon	N/P Silicon
Size	2 x 2 cm*	2 x 2 cm
Base Resistivity	2 or 10 ohm-cm	2 ohm-cm
Thickness	4 mil	8 mil
Cover	3 mil	3 mil
Substrate	Kapton, 3 mil (Dupont)	Kapton, 1 mil (Dupont)
Interconnector Material	Silver Mesh	Silver-Clad Copper
Interconnector Insulation	Parylene (Union Carbide) and PYRE M-L (Dupont)	None
Coverslide Adhesive	RTV 602 (General Electric)	RTV 602 (General Electric)
Solar Cell Adhesive	RTV 3145 (Dow Corning)	RTV 3145 (Dow Corning)

*1 by 2 cm cells are used in some current trimmers in the advanced configuration.

Table 18: PROPOSED SOLAR CELL CONFIGURATION

only half as much. The 10 ohm-cm cells were chosen over 2 ohm-cm cells for reasons previously discussed. The silver mesh interconnector material, rather than the silver clad copper in the Ryan design, was chosen because of its lower density and greater flexibility.

Selection of a 3-mil polyimide sheet, rather than Ryan's 1-mil, was based on a 16,000 volt electric breakdown requirement. Vacuum-deposition of poly-p-xylylene (Reference 7) or a polyimide casting resin (Reference 6) were selected for insulation between cells.

6.5 Alternate Configurations

Some cell configurations other than the one just described will need to be evaluated as the high-voltage solar array requirements become more firm. For example, the use of 1 by 2-cm cells may allow greater flexibility in switching-type voltage regulation, whereas 2 by 6-cm cells may increase the packaging factor, reduce cost, and improve the power-to-weight ratio. By boosting the spacecraft to higher altitudes, radiation damage to the cells from trapped protons may be reduced, permitting use of the more efficient 2 ohm-cm solar cells. Future research in high-voltage current collection from a plasma may suggest elimination of the requirement for insulating the interconnectors. Also, technology advances in cadmium sulfide solar cells and thermal annealing of radiation-damaged silicon solar cells may make better configurations possible.

Although a detailed analysis of cadmium sulfide solar cells for a high-voltage array is beyond the scope of this study, a few comments on the subject seem appropriate. It is likely that 5-percent-efficient cadmium sulfide solar cells which are resistant to proton, electron, and ultra-violet radiation will be a reality soon. Since silicon solar cells are only about 5-1/2 percent efficient at the end of the mission, the light weight, flexibility, and electrical insulation inherent in cadmium sulfide solar cells may make the latter more desirable. Cost reliability and thermal cycling stability of cadmium sulfide solar cells are parameters which must be improved, however, before these cells can compete with time-proven silicon solar cells.

7.0 ELECTRICAL MODEL

A mathematical model of the selected conceptual building block configuration has been developed. The building block (Figure 30) consists of the following:

1. A set of 2 by 2-cm, 8-mil, 10 ohm-cm, solar cells.

2. A set of submodules, each made up of N_p solar cells connected in parallel. Each submodule is shunted by a set of Q shunting diodes ($Q \geq 1$). The shunting diodes are so connected that they are reverse-biased when all the cells in the associated submodule are operating normally.

3. A set of modules, each made up of N_m submodules in series. Some but not necessarily all modules are shunted by a power transistor that is operating either in the saturated or OFF mode. For computational simplicity, the equations are developed as if all modules were shunted by transistors operating in one of three modes, i.e., their emitter-collector conductance (G_{xs}) being:

   a) that corresponding to operation in the saturated region
   b) that corresponding to operation in the "starved", or OFF, region
   c) zero conductance.

   Zero conductance describes those modules that have no shunting transistor.

4. A string made up of a set of N_{st} modules connected in series. The string is connected to the load bus through a set of M parallel blocking diodes. N_{st}, $M \geq 1$.

The following symbols are used in the equations that define the electrical model.

A = Solar cell empirical fitting constant
C_{dd} = Diode diffusion capacitance
C_{jd} = Diode junction or transition capacitance
C_o = Constant of diode junction capacitance equation
$G_{(load)}$ = load conductance
G_{sd} = Diode internal shunt conductance

G_{sh} = solar cell internal shunt conductance

G_{xs} = transistor collector-emitter conductance

I = solar cell current

I_c = transistor collector current

I_d = ideal diode current

I_{dd} = actual diode current

I_g = solar cell light generated current

I_{ld} = load current

I_{mp} = solar cell maximum power current

I_{ms} = s^{th} module current

I_o = solar cell reverse saturation current

I_{sc} = solar cell short-circuit current

I_{sm} = submodule current

I'_{sm} = submodule current without shunt diodes

I_{st} = string current

K_d = diode diffusion capacitance constant (pfd/ma)

M = number of parallel blocking diodes

N_m = number of submodules in a module

N_p = number of parallel-connected cells in submodule

N_{st} = number of modules in a string

Q = number of shunt diodes across submodule

q = electron charge

R_d = diode internal series resistance

R_{ld} = load resistance

R_s = solar cell internal series resistance

R_{sd} = diode shunt resistance

R_{sh} = solar cell internal shunt resistance

T = temperature of a single solar cell

V = solar cell voltage

$V_{(bus)}$ = bus voltage or load voltage

V_c = transistor collector-emitter voltage

V_d = diode voltage

V_j = diode junction voltage

V_{mp} = solar cell maximum power voltage

V_{ms} = s^{th} module voltage

V_o = built-in potential in diode junction

V_{oc} = solar cell open circuit voltage

V_{sm} = submodule voltage

V'_{sm} = submodule voltage without shunt diodes

V_{st} = string voltage

θ = slope of ln I_d versus V_j for diode (volts^{-1})

Electrical Model Development

The electrical model will be a combination of the models for a solar cell, a diode and a transistor. First we examine the solar cells.

As shown in Appendix 2, the following equation can describe the current-voltage (I-V) characteristic of a single silicon solar cell:

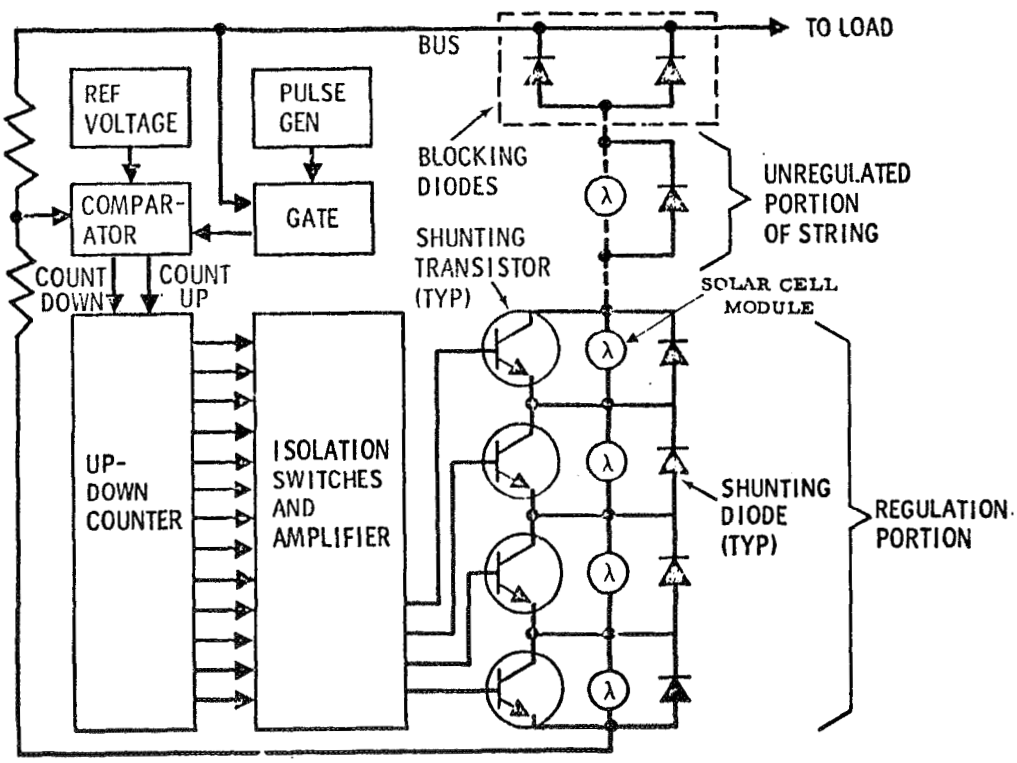


Figure 30: TYPICAL BUILDING BLOCK

$$I = I_g - I_o\left\{\exp\left[\frac{(V + IR_s)}{AkT}\right] - 1\right\} - \frac{(V + IR_s)}{R_{sh}} \qquad (114)$$

The coefficients that provide a ± 1 percent fit to published experimental results for a 2 by 2 cm cell, except near open-circuit voltage, are given in Appendix 2 for T = 28°C = 301°K.

The effect of changes in the value of the solar cell coefficients of Equation 14 on the I-V locus of an illuminated cell is discussed in Ref. 11. Inspection of the expected I-V curves after a predicted level of radiation degradation of the cells indicates that an acceptable fit can be achieved by merely changing the coefficients R_s, I_g, and 1_o. Example values of these coefficients are given in Table 19.

The equation relating the current and voltage of a submodule is obtained from Equation 14.

$$I_{sm} = N_p\ (I) \tag{15}$$

One or more shunting diodes may be connected across each submodule. The model for such a diode is detailed in Appendix 3. From the diode models in Ref. 12 we can determine the effect of a diode on submodule current and voltage. Diode IN4001, having a forward current rating of 1.0A and a PRV of 50 V is representative of the diode type suitable for shunting a 1 A solar array. Its model elements are:

$R_{sd} = 6.4 \times 10^{5}$ kilohms

$I_o = 8 \times 10^{-6}$ mA

$K_d = 2.5 \times 10^{4}$

$V_o = 1.0$

R_d = 0.0 kilohms (i.e., negligible)

$\theta = 21.0$

$C_o = 13.0$

$n = 0.41$

The static diode equation is:

$$I_d = 8 \times 10^{-6}\ (\exp\ (21\ V_j)-1)\ \text{mA}$$

$$\text{for } V_j \geq$$

For the case where $V_j<0$, the diode reverse leakage current is:

$$I_d = V_d G_{sd}$$

e.g., when $V_d = -0.4V$

$$I_d = (-0.4/6.4 \times 10^{-5}) = -6 \times 10^{-7}\ \text{mA}$$

Since I_d << (I) of even a single solar cell, it can be neglected in any practical computation restricted to where $V_{sm} \geq 0$. This approximation must be checked against the characteristics of the shunting diode that is finally chosen. For example, an ion-implanted diode has favorable forward characteristics at the expense of a higher reverse-bias conductance.

The submodule current (I_{sm}), including diode leakage current is:

$$I_{sm} = N_p\left[I_g - I_o(\exp K_o(V_{sm} + I_{sm}R_s/N_p) - 1) - \frac{(V_{sm} + I_{sm}R_s/N_p)}{R_{sh}}\right] - QV_dG_{sd} \quad (16)$$

where $K_o = \frac{q}{AkT}$

A module consists of a set of submodules connected in series, and in turn shunted by one or more transistors. The I-V characteristics of a module, including diode leakage current, will be

$$I_m = N_p\left[I_g - I_o(\exp(K_oB_m) - 1) - B_mG_{sh}\right] - Q(V_m/N_m)\,G_{sd}. \quad (17)$$

where: V_m, I_m = module voltage and current and $B_m = \left[V_m/N_m + I_m(R_s/N_p)\right]$

Orbit Time	R_s ohms	R_{sh} ohms	I_g Amps	I_o Amps	A (no dimensions)
0	0.4	250	0.1425	5.49×10^{-10}	0.969
3 months	0.6	250	0.107	1.3×10^{-8}	0.969
5 years	0.55	250	0.093	4.2×10^{-8}	0.969

These coefficients are based on the following cell characteristics

Time	I_{sc} Amps	V_{oc} Volts	I_{mp} Amps	V_{mp} Volts
0	0.1423	0.497	0.130	0.381
3 months	0.1067	0.411	0.093	0.300
5 years	0.0928	0.377	0.080	0.280

Table 19: SOLAR-CELL COEFFICIENTS (55°C)

Shunting Transistors

A shunting transistor is connected in parallel with each module. For simplicity let all the modules 1 to (ss) have shunting transistors, and let some of these transistors have zero collector-to-emitter conductance. The current (I_{sm}) produced by a given module is shared by the load, through the other series modules in the block, and by shunting transistors:

For the $s^{\underline{th}}$ module:

$$I_{ms} = I_{ld} + I_c \quad s = 1,2, \ldots,ss. \tag{18}$$

Let the transistor collector-emitter characteristics in the saturated and OFF state be approximated by a linear conductance, i.e., G(sat) and G(OFF). Then:

$$\left.\begin{aligned} &I_c = V_c\, G(sat) = V_m G(sat) \\ &\text{or} \\ &I_c = V_c\, G(OFF) = V_m\, G(OFF) \\ &\text{or} \\ &I_c = 0 \text{ for the case of unshunted modules} \end{aligned}\right\} \tag{19}$$

The load current (I_{ld}) can be expressed as a function of the bus voltage $V_{(bus)}$, rather than a function of the string voltage V_{st}. The $V_{(bus)}$ voltage is downstream of the blocking diodes.

$$I_{ld} = V_{(bus)}\, G(load)$$

From Equation 18, the current I_{ms} for the $s^{\underline{th}}$ module is:

$$I_{ms} = V_{(bus)}\, G(load) + V_{ms} G_x \tag{20}$$

where

G_x = one of the three states given in Equation 32 above.

The solar cell string is the sum of all modules which are either shunted or unshunted by transistors.

$$I_{st} = I_{ld} = V_{(bus)}\, G(load) \tag{21a}$$

$$V_{st} = \sum_{1}^{ss} V_{ms} \tag{21b}$$

The blocking diode voltage can be related to its current.

From Appendix 3, Equation 44 we have

$$I_{dd} = (1 + R_d/R_{sd})^{-1} \left[I_o(\exp(\theta (V_d - I_{dd}R_d)) - 1 + V_d G_{sd}\right]$$

when

$R_d = 0$, this simplifies to:

$$I_{dd} = I_o (\exp(\theta V_d) - 1) + V_d G_{sd} \quad (22)$$

The diode voltage drop can be expressed as a function of the bus voltage and the solar-cell string voltage:

$$V_d = V_{st} - V_{(bus)}$$

The equation relating a solar-cell string connected to the bus via M parallel blocking diodes is from Equation 22.

$$I_{st} = M \left[I_o (\exp(\theta (V_{st} - V_{(bus)})) - 1) + (V_{st} - V_{(bus)}) G_{sd}\right] \quad (23a)$$

Substituting $V_{(bus)} = 1_{st}R_{1d}$:

$$1_{st} = (1 + MR_{1d} G_{sd})^{-1} M \left[I_o (\exp(\theta (V_{st} - I_{st} R_{1d})) - 1) + V_{st} G_{sd}\right] \quad (23b)$$

This equation can be solved by estimating the value of I_{st}, inserting this trial value in the right-hand side and solving for I_{st}. Usually no more than two iterations will produce convergence to within three significant figures.

For a 1N4006 blocking diode having a forward current rating of 1A and PRV = 800 V, and for M = 2, R_{1d} = 1.0 kilohm:

$R_{sd} = 8.2 \times 10^6$ kilohms, $R_d = 0.0$

$I_o = 8 \times 10^{-6}$ mA, $\theta = 21.0$

$\hat{E}(1_{st}) = 1$ A. where $\hat{E}$ = estimated value of,

$$I_{st} = (1 + 1.22 \times 10^{-7})^{-1} \quad (2) \left[8 \times 10^{-6} \exp 21 (V_{st} - 1000) - 1\right)$$

$$+ 1.22 \times 10^{-7} V_{st}\Big]$$

When the M blocking diodes are conducting:

$$\hat{E} (V_{st} - V_{(bus)}) = 0.7V$$

The leakage resistance (R_{sd}) is sufficiently high in this case, that the last term on the right-hand side of Equation 23a can be neglected. In most computations Equations 23b can be simplified to:

$$I_{st} = M \left[I_o \left(\exp \theta (V_{st} - I_{st} R_{ld}) - 1 \right) \right] \qquad (24)$$

Having developed the blocking diode equation in terms of I_{st}, V_{st}, $V_{(bus)}$ and R_{ld}. Equation 23 or its approximate equivalent, Equation 24, can now be combined with Equation 21 to solve for the string current, given the bus voltage or the load impedance, and given the state of each transistor associated with modules 1 through (ss).

Summary

The set of equations developed above describe completely the state of a digital regulator for a prescribed set of regulator commands. The set of equations can be used to determine the performance of a digital-shunt regulated solar-cell array at any temperature, and with one or more devices having malfunctioned. For example, the effect on performance of a set of open-circuited solar cells or diodes can be calculated. Similarly the effect of a spread in the transistor saturation characteristics can likewise be quantified. Such analysis is essential in the design of a digital regulator where the designer needs to develop a configuration that covers the full range of regulation states, yet requires the minimum number of regulator parts.

8.0 RELIABILITY

Reliability models were developed to support design trade studies. The reliability analyses identified areas requiring enhancement to meet design reliability goals of either 0.96 or 0.99 after 5 years. Methods of enhancing reliability were postulated and evaluated. The reliability analysis results were used to identify areas of uncertainty which require further study. Details of the reliability models and calculation are given in Appendix 4.

8.1 Reliability Criteria and Requirements

The high reliability goal for the high voltage solar array necessitated these design requirements:

- No single failure shall cause an open circuit failure of an entire voltage block.
- Protective circuits shall be provided to guard against cascading or sequential failures.
- All parts shall be screened to eliminate defects.

8.2 Reliability Summary

The analyzed solar array configurations consisted of building blocks connected to electrical busses and interconnected by switches to provide the required voltage and power levels. Each building block had a primary voltage section, digital-shunt regulated sections, shunting switches, a voltage regulator, and blocking diode. The advanced configuration also included voltage and current trimmer sections and trimmer switches.

The results of the reliability analyses, summarized in Table 20, indicated that initially switches accounted for most of the solar array failure risk.

The effect of switch failure is loss of voltage and power from the section controlled by that switch. The postulated reliability goal can be achieved if part redundancy is provided within each switch element, and one additional shunt section of the largest size is provided for each building block. Failure of more than one switch is then required before block failure occurs. Failure probability distribution then becomes that shown in the "Improved" column in Table 20.

	CONFIGURATION			
	BASIC		ADVANCED	
	INITIAL	IMPROVED	INITIAL	IMPROVED
Inter-block switches	27.2	69.2	9.9	66.4
Block-to-bus connectors	0.1	0.2	Neg.	0.2
Bus	0.1	0.2	Neg.	0.2
Voltage Regulator	10.0	25.4	3.6	24.3
Shunting switches	57.6	Neg.	5.0	Neg.
Interconnectors	4.7	4.1	6.5	6.3
Blocking Diode	0.3	0.8	0.1	0.8
Solar cell submodules	Neg.	Neg.	Neg.	Neg.
Trimmer switches	N/A	N/A	74.8	1.8
TOTALS	100.0	100.0	100.0	100.0

(NOTE: "Improved" design meets 0.99 reliability goal.)

Table 20: SOLAR ARRAY FAILURE PROBABILITY DISTRIBUTION BY DESIGN ELEMENT

In the advanced configuration addition of a redundant voltage trimmer section and current trimmer section with the required switches is necessary to achieve a higher reliability goal. With this improvement the solar array reliability is determined primarily by the reliability of the inter-block switches and the voltage regulator in each building block.

Part redundancy was also considered for each element in the voltage regulator and inter-block switches. Although the resulting reliability estimate exceeds the desired goal, further study should be undertaken to determine the optimum redundancy mechanizations for these elements.

Figures 31 and 32 show the percentage of solar array failure risk attributable to the major design elements for the advanced and basic configurations. Failure probability calculations for the switches and voltage regulator assumed part-level redundancy for all elements. We assumed sufficient solar cell design margin in the form of extra submodules to limit the failure probability from submodule failures to 10^{-8} per basic building block or trimmer section.

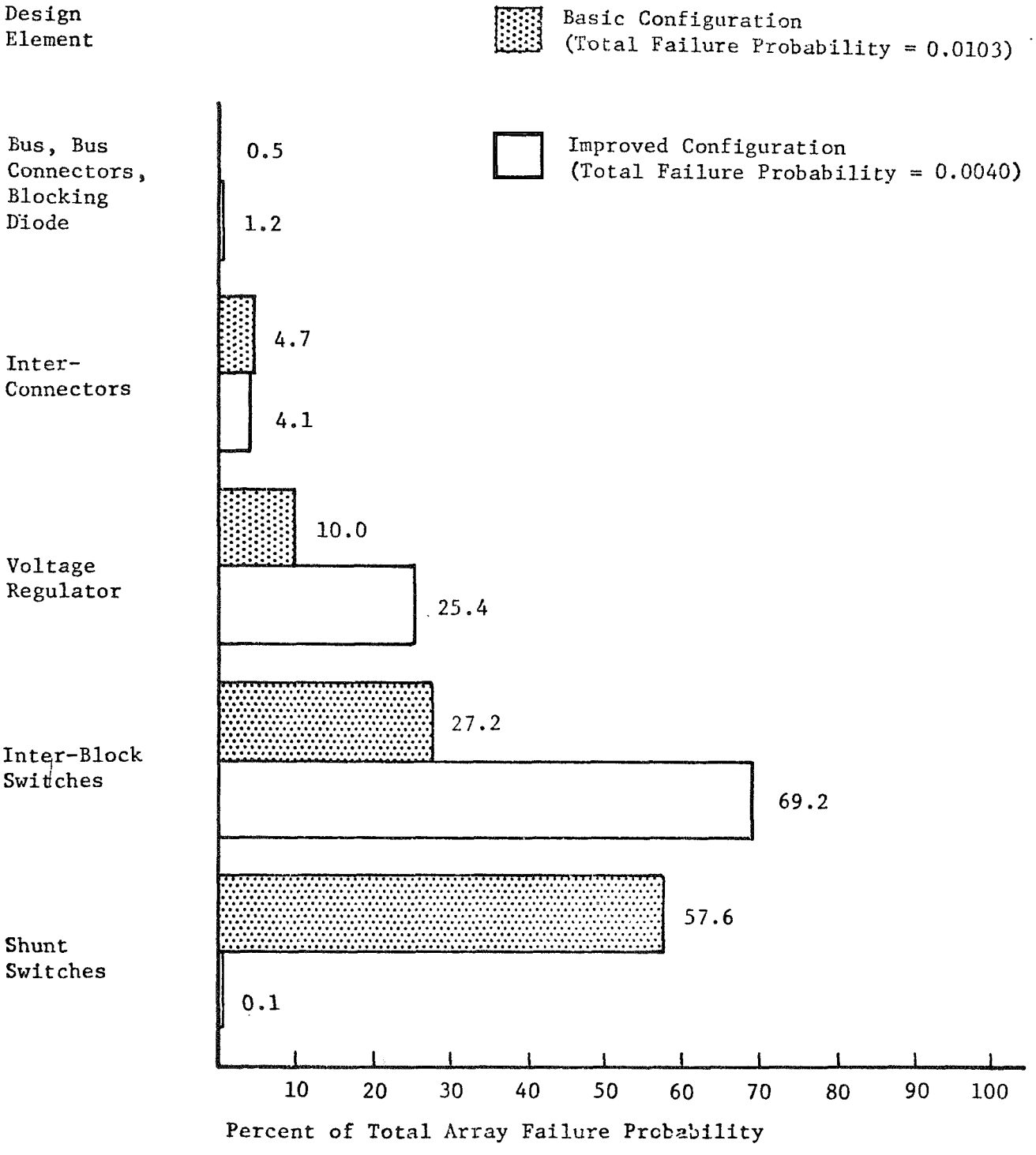


Figure 31: FAILURE PROBABILITY DISTRIBUTION BASIC CONFIGURATION

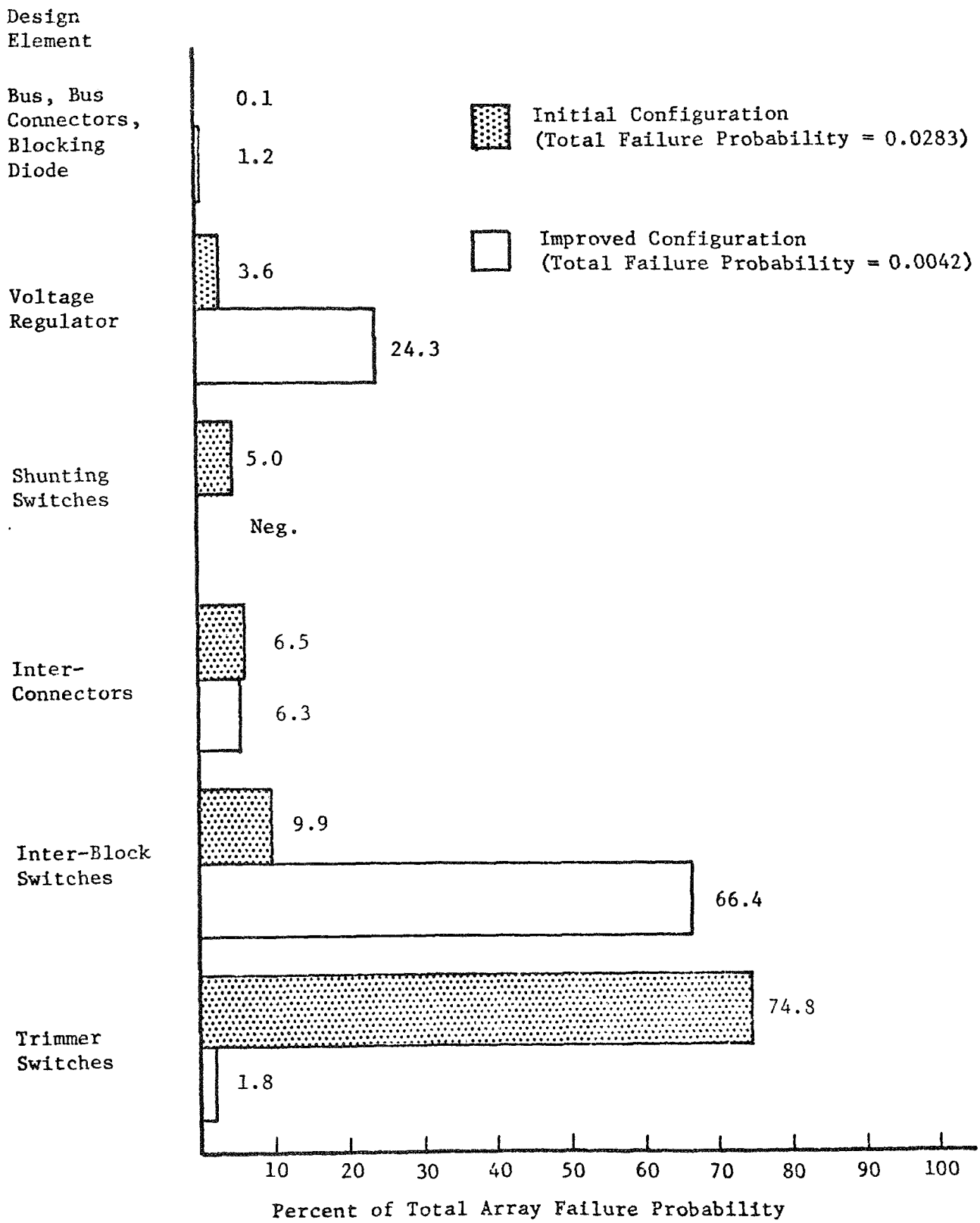


Figure 32: FAILURE PROBABILITY DISTRIBUTION
ADVANCED CONFIGURATION

8.3 Reliability of Simplified Array

The assumption that each submodule must have a shunting diode penalizes array weight and cost. We therefore calculated the reliability that could be achieved with fewer shunting diodes. We postulated connecting a shunting diode across every 10 submodules in regulator sections, and across each 50 submodules in other sections. We also reduced the trimmer sections from five to three, but provided the same current and voltage steps by having the trimmers sized in a ratio of 2:2:1. As a consequence, 40 percent fewer trimmer switches are needed. An open string then follows an open interconnection failure or a combination of all cells in a submodule failing open and the shunting diode failing open in the same section. The possible overheating and breakdown of cells because of multiple open-cell failures in a submodule was not considered.

The total number of diodes required for this alternate configuration is 6,427. The reliability prediction for this alternate configuration is 0.96 which does not meet the goal of 0.99. The array weight and cost, however, are affected favorably.

8.4 Reliability Conclusions

We recommend further study of redundancy mechanizations for the switching circuits and voltage regulator elements.

A 0.99 probability of design power after 5 years is achievable if we do this:

ELEMENTS	ACTION
Switches	Add extra switch and section to building block Add extra trimmers and switches
Submodule	Add design margin
Components	Use part redundancy, careful design
Parts	Select, burn-in, screen, and derate

Further improvement is constrained by the regulator, which needs study.

9.0 PERFORMANCE ESTIMATE

A performance estimate has been made to determine the incremental changes in weight and area resulting from the high-voltage and integral-power-conditioning features of the high-voltage solar array. The low-voltage solar array weights and areas used as reference are those estimated in the "Feasibility Study 30 Watts per Pound Roll-Up Solar Array - Final Report." This work was done by Ryan on JPL contract 951971. The advanced high voltage array configuration was selected for this comparison. Significant design factors are shown on Figure 33.

The performance estimate is based on the following assumptions:

1. Performance is calculated at the beginning of the mission.
2. The solar cell and cover assembly, cell interconnectors, packing factor (cells per unit area), and substrate in the Ryan array are also used in the high-voltage array.
3. Performance of the high and low voltage arrays is compared in terms of the power to weight ratio, P_W, and power to area ratio, P_A.
4. Array estimated reliability is 0.96.

To obtain 15,000 watts power output at the end of the mission the high-voltage array has been increased in area using radiation degradation factors discussed in Section 4.0 and summarized in Table 21.

SOLAR-CELL MAXIMUM POWER OUTPUT (mW)		CONDITIONS
Initial	After 5 Years	3 mil (76 μm) cover, 8 mil (0.02 cm) thick, 2 ohm-cm, 2 by 2 cm solar cells operating at 55°C temperature, and 140 mW/cm^2 AMO sunlight
45.3	25.5	

Table 21

The output of the high-voltage solar array prior to radiation degradation then becomes: Initial Power = $15,000 \times \frac{45.3}{25.5} = 26,700$ watts.

The performance of the Ryan reference array is

$P_A = 10$ W/ft^2 (107.6 W/m^2) $\qquad P_W = 31.16$ W/lb (68.7 W/kg)

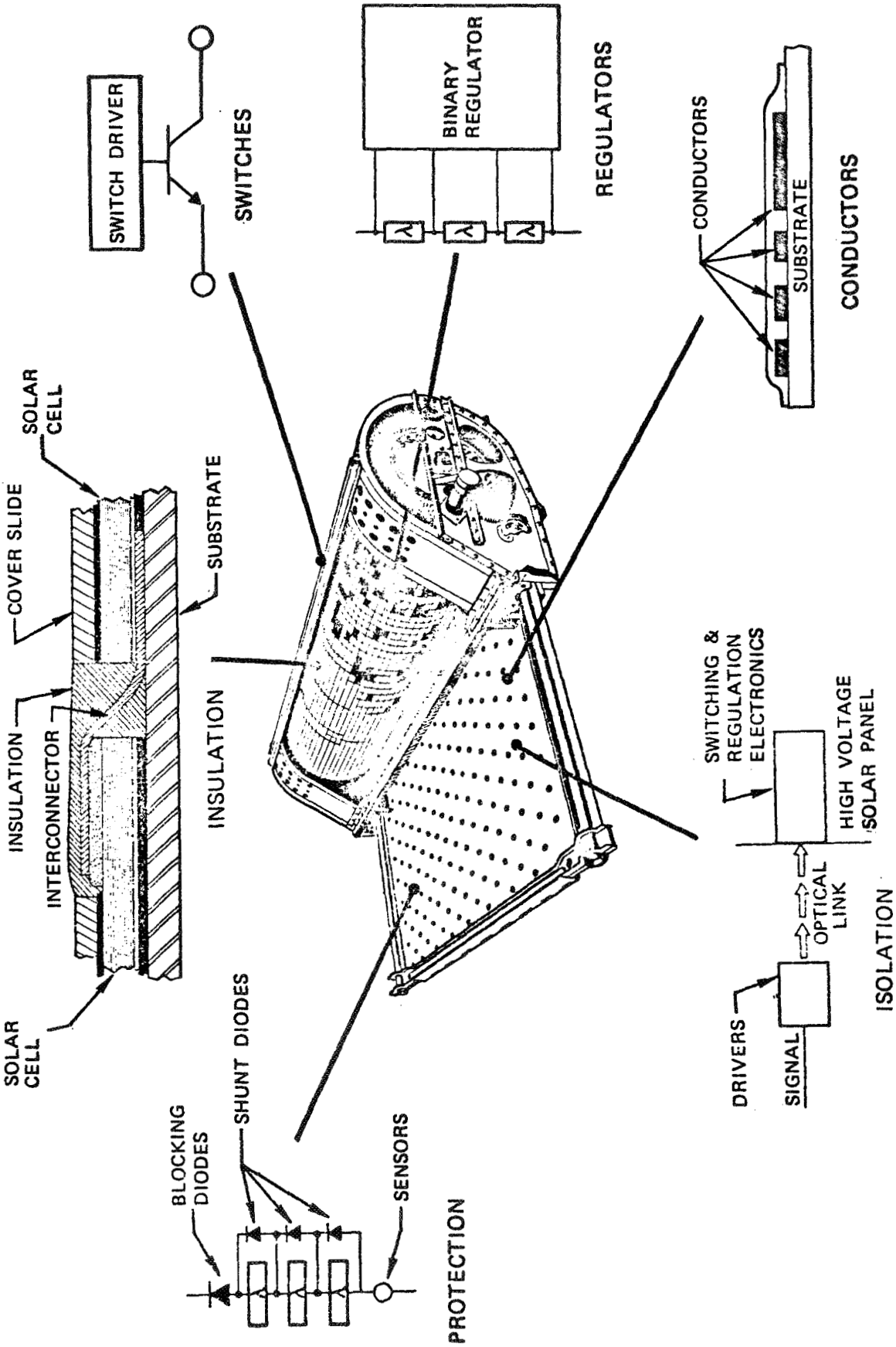


Figure 33: SIGNIFICANT DESIGN FACTORS

The area and weight of a Ryan-type array producing 26,700 watts would be

$$\text{Total Area} = \frac{26,700}{107.6} = 248.1 \text{ m}^2$$

$$\text{Total Weight} = \frac{26,700}{68.7} = 388.6 \text{ Kg.}$$

9.1 Array Insulation-Illuminated Side

Insulating the interconnectors and space between solar cells with poly-p-xylylene or a polyimide resin will increase the weight. The Ryan-design packing factor (f_p) was used to calculate the insulated area. Ryan assumed placement of 224 cells/ft^2 on the array. The insulation is assumed to be the same thickness as the combined solar cell, cover and adhesive sandwich, 13 mils (0.033 cm).

$$f_p = \frac{224 \text{ cells/ft}^2 \times 4 \text{ cm}^2}{144 \text{ in}^2/\text{ft}^2 \times (2.54)^2 \text{ cm}^2/\text{in}^2} = 0.968$$

Thus 3.2 percent of the illuminated surface of the array would be insulated. For poly-p-xylylene which has a density of 1.3 g/cm^3, the weight increase (ΔW) would be:

$\Delta W = (1 - 0.968)\ 248.1 \text{ m}^2 \times 0.013 \text{ inch} \times 2.54 \text{ cm/inch} \times 10 \times 1.3 = 3.41 \text{ kg}$

$$\text{then } \Delta P_W = \frac{26,700}{388.6+3.4} = 68.7 = -0.6 \text{ W/kg}$$

where ΔP_W is the change in power output per unit weight attributable to the high-voltage feature.

9.2 Power Busses

High voltage operation will decrease the power bus weight; however, multiple loads offset this. For this reason no area and weight increments are applicable.

9.3 Solid-State Switching

Each switch module is assumed to weigh 10 grams, require 4 cm^2 of array area and withstand 2100 volts. Table 22 shows the number of switch modules required by the advanced configuration.

	Number of Switch Modules	Number of Regulator Modules
Intrablock		
Block 1	27	15
Block 2	27	13
Block 3	39	15
Block 4	66	15
Block 5	54	15
Block 6	27	13
Interblock	33	--
TOTAL	273	86

Table 22: NUMBER OF SWITCHING AND REGULATOR MODULES IN ADVANCED CONFIGURATION

Section 4.9 gives the power, weight, and area required by the switching system at mission end. The area increment, ΔA, is the sum of the area required by the switches (A_{SW}) plus the array area needed to supply the losses (A_{loss}).

$$A_{SW} = \frac{273 \times 4}{10,000} = 0.109 \text{ m}^2$$

$$A_{loss} = \frac{38.8}{107.6} = 0.36 \text{ m}^2$$

The area increment,

$$\Delta A = 0.109 + 0.36 = 0.469 \text{ m}^2$$

The power/area increment is:

$$\Delta P_A = \frac{26,700}{248.1 + 0.469} = 107.6 = -0.19 \text{ W/m}^2$$

The weight increment (ΔW) is the sum of the switch weight (W_{SW}) plus the array weight needed to supply the losses (W_{loss}).

$$W_{SW} = \frac{273 \times 10}{1000} = 2.73 \text{ kg}$$

$$W_{loss} = \frac{38.8}{68.7} = 0.56 \text{ kg}$$

$$\Delta W = 2.73 + 0.56 = 3.29 \text{ kg}$$

The power/weight increment is

$$\Delta P_W = \frac{26,700}{388.6 + 3.29} - 68.7 = -0.569 \text{ W/kg}$$

9.4 Protection Equipment

The weight and area of the sensors required for the protection are:

14 voltage sensors

weight: 8 grams each

area: 0.40 cm^2 each

14 current sensors

weight: 20 grams each

area: 4.5 cm^2

The weight increment is:

$$\Delta W = \frac{(14 \times 8) + (14 \times 20)}{1000} = 0.392 \text{ kg}$$

$$\Delta P_W = \frac{26700}{388.6 + 0.392} - 68.7 = -0.06 \text{ W/kg}$$

The area increment is:

$$\Delta A = \frac{(14 \times 0.40) + (14 \times 4.5)}{10,000} = 0.0069 \text{ m}^2.$$ This is negligible.

9.5 Regulation

The number of regulator modules, shown in Table 22, is based on two IC units per binary shunt and one error sensor per block. Each module weighs 8 grams, is 4 cm^2 in area and will dissipate 8 watts. The area increment, ΔA is the sum of the area required by the regulator chips (A_{reg}) plus the array area represented by their losses (A_{loss}).

$$A_{reg} = \frac{86 \times 4}{10,000} = 0.0344 \text{ m}^2$$

$$A_{loss} = \frac{86 \times 8}{107.6} = 6.394 \text{ m}^2$$

$$\Delta A = 0.0344 + 6.394 = 6.43 \text{ m}^2$$

The power/area increment is

$$\Delta P_A = \frac{26,700}{248.1 + 6.43} - 107.6 = 02.70 \text{ Watts/m}^2$$

The weight increment is calculated from the sum of the regulator chip weight (W_{reg}) and the array weights needed to supply the regulator power (W_{loss}).

$$W_{reg} = \frac{86 \times 8}{1000} = 0.688 \text{ kg}$$

$$W_{loss} = \frac{86 \times 8}{68.7} = 10.01 \text{ kg}$$

$$\Delta W = 0.688 + 10.01 = 10.69 \text{ kg}$$

The power/weight increment is

$$\Delta P_W = \frac{26,700}{388.6 + 10.69} - 68.7 = -1.83 \text{ watts/kg}$$

9.6 Shunt Diodes

Reliability is increased when shunt diodes are connected across groups of solar-cell submodules, thus providing a by-pass circuit if there is an open circuit in one of the shunted submodules. Current trimmers, voltage trimmers and the primary blocks have one diode across each 50 submodules. The regulation section has one diode across each 10 submodules. This concept applied to the advanced configuration requires 6,427 diodes as shown in Table 23. The array reliability, using this number of shunt diodes, is estimated to be 0.96 for the 5-year mission.

Each diode is assumed to weigh 50 milligrams and require an area of 0.04 cm^2. Calculating the area increments,

$$A = \frac{6427 \times 0.04}{10,000} = 0.0256 \text{ m}^2$$

$$P_A = \frac{26700}{248.1 + 0.0257} - 107.6 \quad 0$$

The weight increment is:

$$W = \frac{6427 \times 0.05}{1000} = 0.32 \text{ kg}$$

$$P_W = \frac{26,700}{388.6 + 0.32} - 68.7 = -0.05 \text{ W/kg}$$

	Block 1	Block 2	Block 3	Block 4	Block 5	Block 6
Current Trimmers						
$\frac{3\ N_S}{50}$	255	255	1020	1402	765	383
Voltage Trimmers						
A $N_S/50$	8	6	29	29	22	8
B $N_S/50$	15	11	58	57	43	16
C $N_S/50$	15	21	58	114	43	32
Primary Block						
$N_S/50$	78	80	312	440	234	120
Regulating Section						
$N_S/10$	37	26	145	142	109	39
BLOCK TOTALS	408	399	1622	2184	1216	598
ARRAY TOTAL: 6427						

Table 23: SHUNT DIODES REQUIRED

9.7 Blocking Diodes

Blocking diodes improve reliability by preventing a shorted block assembly from loading the rest of the array. The present concept uses four diodes in quad-redundancy per block assembly, and the 24 blocking diodes would have negligible impact on P_A and P_W.

9.8 Summary

Table 24 shows the result of applying the combined increments to the low voltage power/area and power/weight ratios.

	P_A	P_W
Low Voltage Design	107.6 W/m^2 (10 W/ft^2)	68.7 W/kg (31.2 W/lb)
High Voltage Design	104.7 W/m^2 (9.7 W/ft^2)	65.59 W/kg (29.7 W/lb)

Table 24: PERFORMANCE ESTIMATE SUMMARY

Details of the performance analysis are shown in Table 25.

LOW VOLTAGE DESIGN STARTING REFERENCE (POWER = 26.7 KW)		DESIGN IMPACT				REFERENCE
		AREA (m^2)	WEIGHT (kg)	P_a Watts/m^2	P_w Watts/kg	
		248.	388.6	107.6 (10 W/ft^2)	68.7 (31.16 W/lb)	PARA.9
DESIGN ELEMENT	CHANGE DESCRIPTION	INCREMENTAL VARIATIONS				
Solar Cells, Covers, Packing Factor, Interconnectors, and substrate	No Change	- -	- -	- -	- -	Para. 9.0
Array Insulation	13 mils of insulation at 1.3 gr/cm^3 with packing factor = 0.968	- -	+3.4	- -	-0.6	Para. 9.1
Solid State Switching	273 switch modules at 10 grams, and 4 cm^2, dissipating 38.8 watts total	+0.469	+3.29	-0.190	-0.569	Para. 9.3
Protection	14 voltage sensors 8 gr, 0.40 cm^2; 14 current sensors 20 gr, 4.5 cm^2	Neg.	+0.39	- -	-0.06	Para. 9.4
Regulation	110 Reg. Modules, 8 Gr. & 4 cm^2, dissipating 8 W each	+6.43	+10.69	-2.70	-1.83	Para. 9.5
Shunt Diodes	6427 diodes per Table 26. Each diode 0.05 Gr, 0.04 cm^2	+0.026	+0.32	- -	-0.05	Para. 9.6
Increment Totals				-2.89	-3.11	
High Voltage Design P_a and P_W Ratios				104.71	65.59	Para. 9.8

Table 25: PERFORMANCE COMPARISON AT BEGINNING OF MISSION

9.9 Radiation Resistant Cells

To reduce radiation degradation, 10 ohm-centimeter resistivity solar cells would be used in the array instead of the 2 ohm-centimeter cells shown in the performance estimate. While 10 ohm-centimeter cells produce a small improvement in the end-of-mission power, their effect on the performance at the beginning of the mission is to decrease P_A and P_W because of their initially lower output. The applicable power/area increment is

$$\Delta P_A = \frac{0.9 \times 26{,}700}{248.1} - 107.6 = 10.76 \text{ W/m}^2$$

9.10 Optomechanical Switches

An optomechanical switch was shown in Section 4.6. The following evaluation in terms of power/weight and power/area ratios enables comparison of these switches with the solid-state switching used in the performance analysis.

$$\Delta W = W_{SW} + W_{loss}$$

As losses in mechanical switches are negligible,

$$\Delta W = \frac{126 \times 3 \text{ oz.}}{16 \text{ oz/lb} \times 2.205 \text{ lb/kg}} = 10.7 \text{ kg}$$

$$\Delta P_W = \frac{26{,}700}{388.6 + 10.7} - 68.7 = -1.83 \text{ W/kg}$$

$$\Delta A = A_{SW} + A_{loss}$$

However, A_{loss} is again negligible, so

$$\Delta A = \frac{126 \times 0.75 \text{ in.} \times 3 \text{ in.} \times (2.54)^2 \text{ cm}^2/\text{in}^2}{10{,}000 \text{ cm}^2/\text{m}^2} = 0.183 \text{ m}^2$$

$$\Delta P_A = \frac{26{,}700}{248.1 + 0.183} - 107.6 = -0.06 \text{ W/m}^2$$

The following table compares optomechanical switches with solid-state switches.

SWITCH TYPE	AREA A_2 (m^2)	WEIGHT W (kg)	POWER/AREA P_A (watts/m^2)	POWER/WEIGHT P_W (watts/kg)
Solid State	0.469	0.833	-0.190	-0.139
Optomechanical	0.183	10.7	-0.06	-1.83

Table 26

10.0 VERIFICATION OF CONCEPTS

The high-voltage solar array electrical configuration study has clearly established the feasibility of developing designs that will meet the voltage, power, flexibility, reliability, and other requirements, even with today's components. Component developments in the next two years can bring about even lower weight and area for the solar array. Alternate solutions are available for the critical switching problem.

The appropriate next objective in high-voltage solar array electrical configuration development is achievement of technology readiness. This is a status where there are no unsolved technology problems, where all components are developed, and where all needed design data are documented. Application of the array to a particular space mission then requires only detailed design, manufacturing, and qualification testing.

Completion of the following tasks will achieve technology readiness:

- Evaluate analytically and by test, parts which are not properly characterized for the high-voltage application. These include opto-electronic high-voltage isolation, high-voltage switching transistors and SCR's, and opto-mechanical high-voltage latching switches.
- Conduct dynamic analyses of the weighted-binary switching shunt voltage regulator, and develop computer programming for performing regulation.
- Select components, design, breadboard, and test hybrid thick-film and thin-film components such as a switch assembly, shunting switch, voltage sensor, current sensor, opto-electronic isolation link, and up-down counter.
- Construct and test a block assembly using breadboard components and electronic simulation of solar array temperature and other extremes. Adequate proving of the voltage regulator will require some solar-cell modules.
- System analysis, reliability monitoring, interface definition, and interface control activities are required during this development period to assure that all analytical and development activity is pertinent to the objectives and that all components will be compatible with overall system requirements.

A test plan relating component tests to hybrid circuits and breadboard tests is provided in Figure 34. Test plans have been developed for the binary-regulator breadboard, block-assembly breadboard, high-voltage switch assembly breadboard, and system-breadboard tests. These plans appear in Figures 35 to 38.

Optoelectronic devices need be studied to determine their voltage limitations. No presently marketed devices meet the total needs of the high voltage array. However, optoelectronic development can be a straightforward extension of existing technology. In each illustration test items are shown within the dashed lines. Test equipment, loads, computer and environmental chambers are also shown.

Whether to provide actual or simulated power sources and loads is an important decision affecting the technical and economic aspects of the testing. Providing solar array panels for all tests would be excessively costly and would severely limit the operating conditions which could be evaluated. For example, since solar array characteristics vary widely with temperature, meaningful evaluation of stability of regulation control would need to be made at a variety of array temperatures with constant illumination provided by a solar simulator. Large solar simulators and temperature controlled chambers are available and would eventually be needed for qualification testing. On the other hand, simulation of loads and power sources permits circuit development and several tests to proceed simultaneously.

Since a central computer will be used for voltage and current-control of switching, simulation of this function is necessary. A laboratory computer such as the PDP8 is suggested.

A modest effort will be required to verify that array-mounted solid state circuit elements are protected from electron and proton radiation during flight through the Van Allen belts.

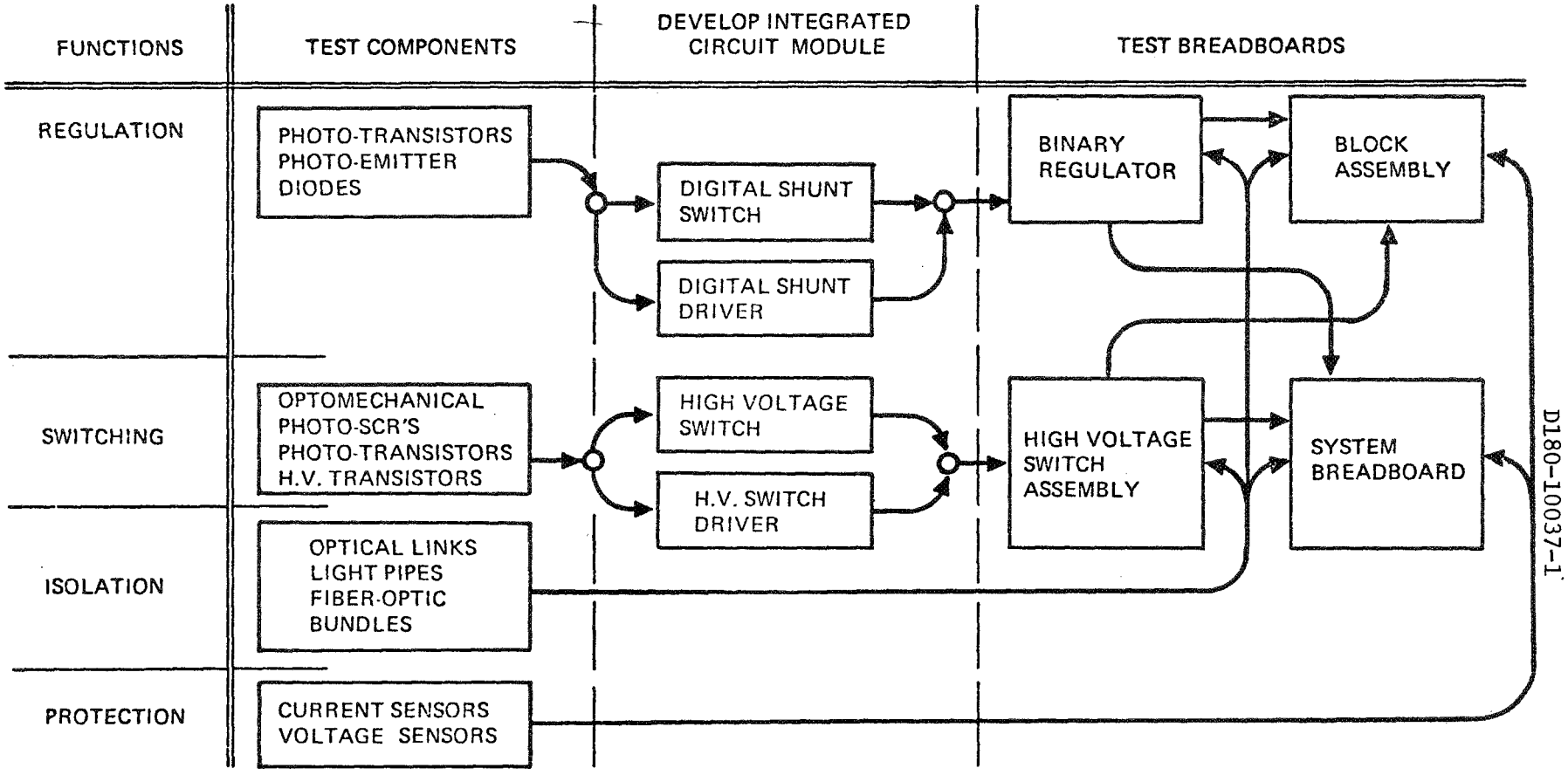


Figure 34: CONFIGURATION VERIFICATION TEST PLAN

PURPOSE: FUNCTIONAL VERIFICATION THAT INTEGRATED-CIRCUIT COMPONENTS MEET ELECTRICAL SPECIFICATIONS AT TEMPERATURE LIMITS

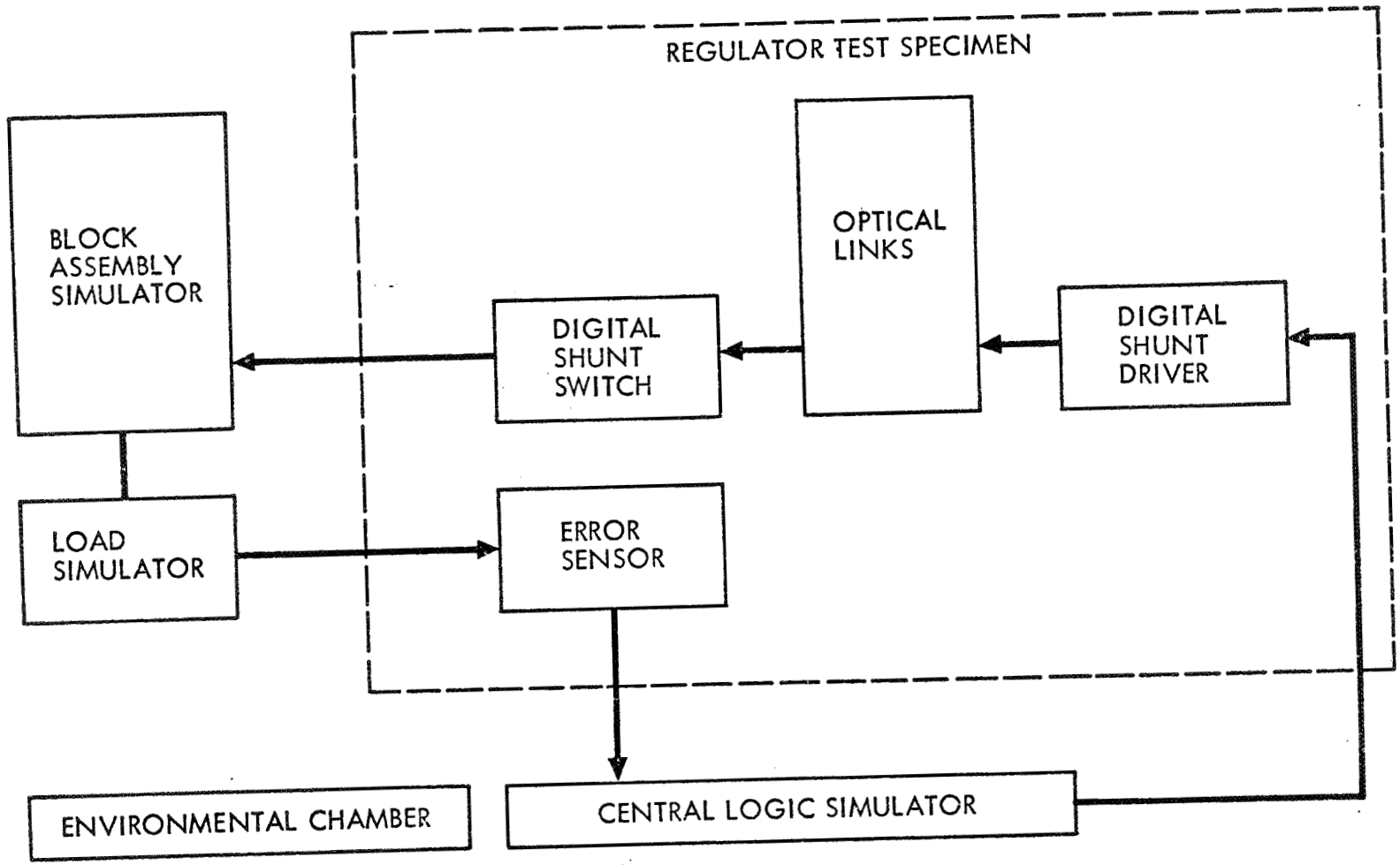


Figure 35: BINARY REGULATOR BREADBOARD TEST

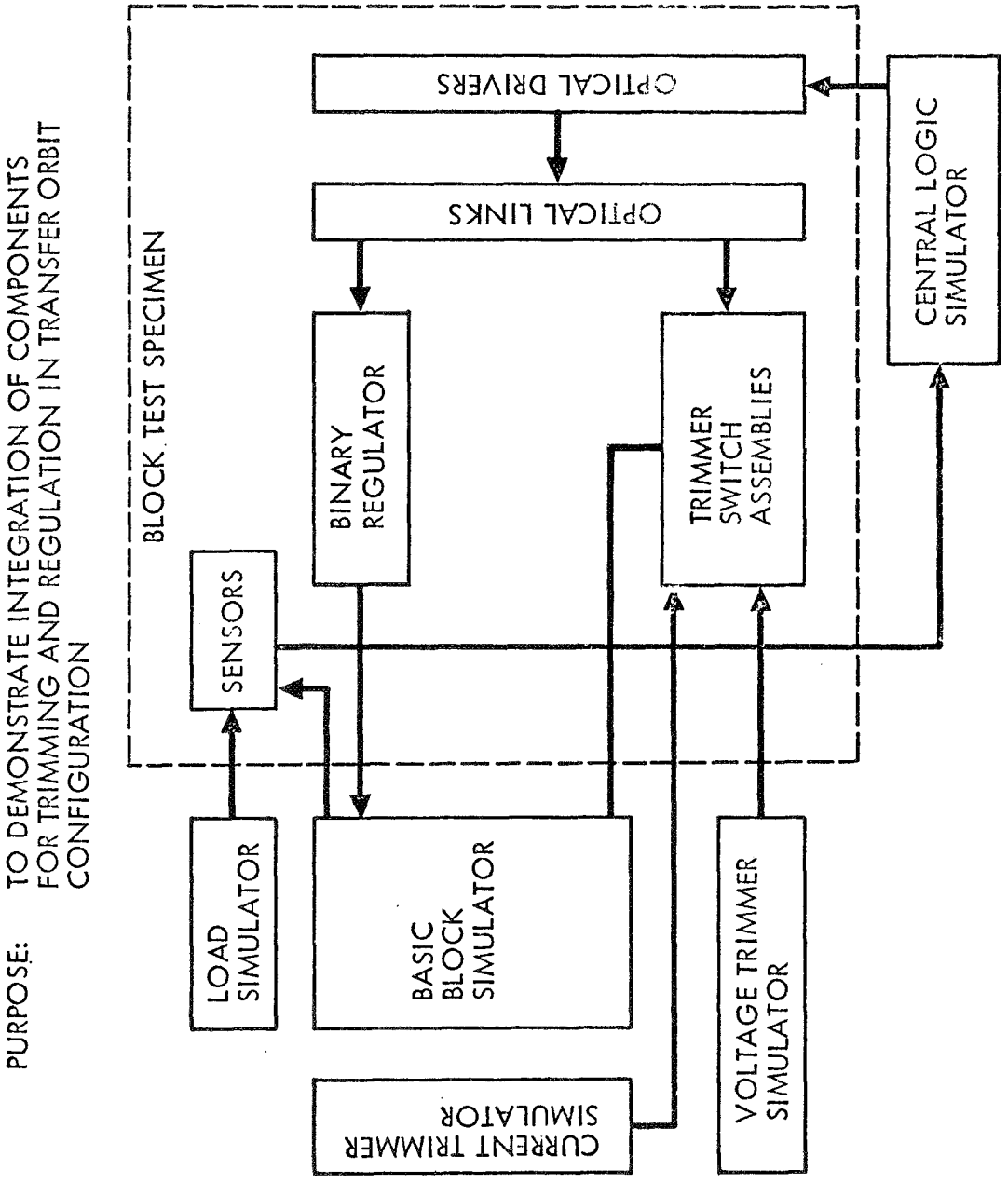


Figure 36: BLOCK ASSEMBLY BREADBOARD TEST

PURPOSE TO VERIFY:

- INTEGRATION OF TYPICAL SWITCH-MODULE COMBINATIONS
- INTEGRATION OF SWITCH MODULES, OPTICAL LINKS AND DRIVER MODULES
- FUNCTIONAL RELIABILITY AT HIGH VOLTAGE AND AT TEMPERATURE LIMITS

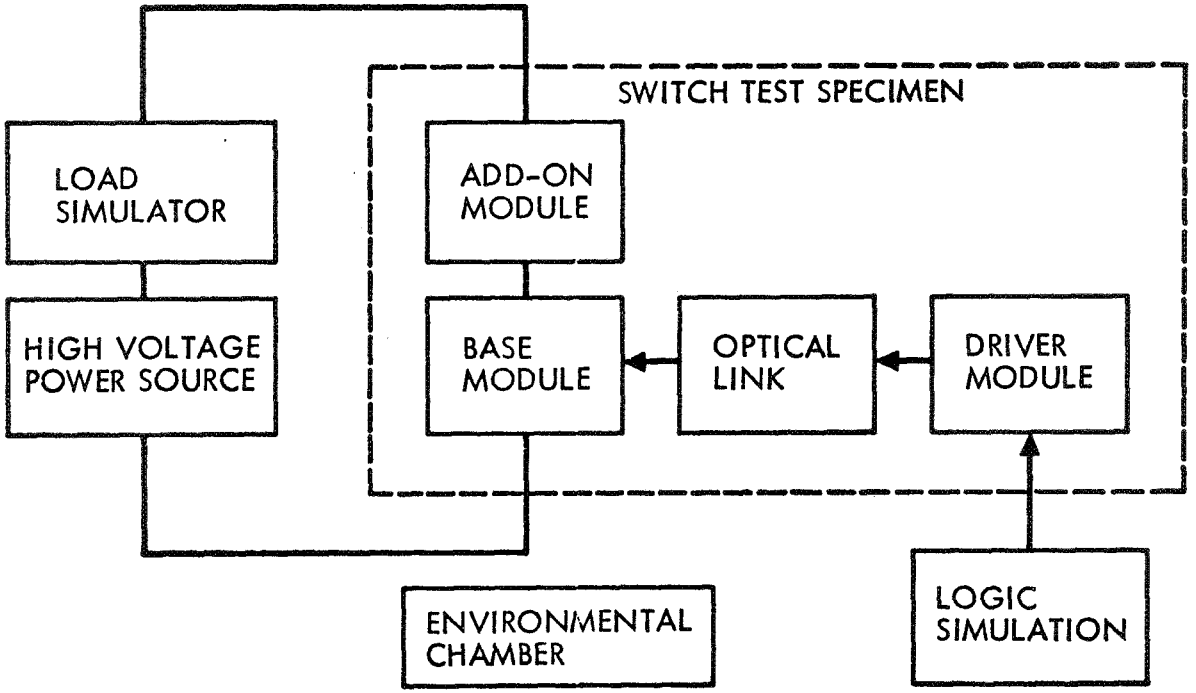


Figure 37: HIGH VOLTAGE SWITCH ASSEMBLY BREADBOARD TEST

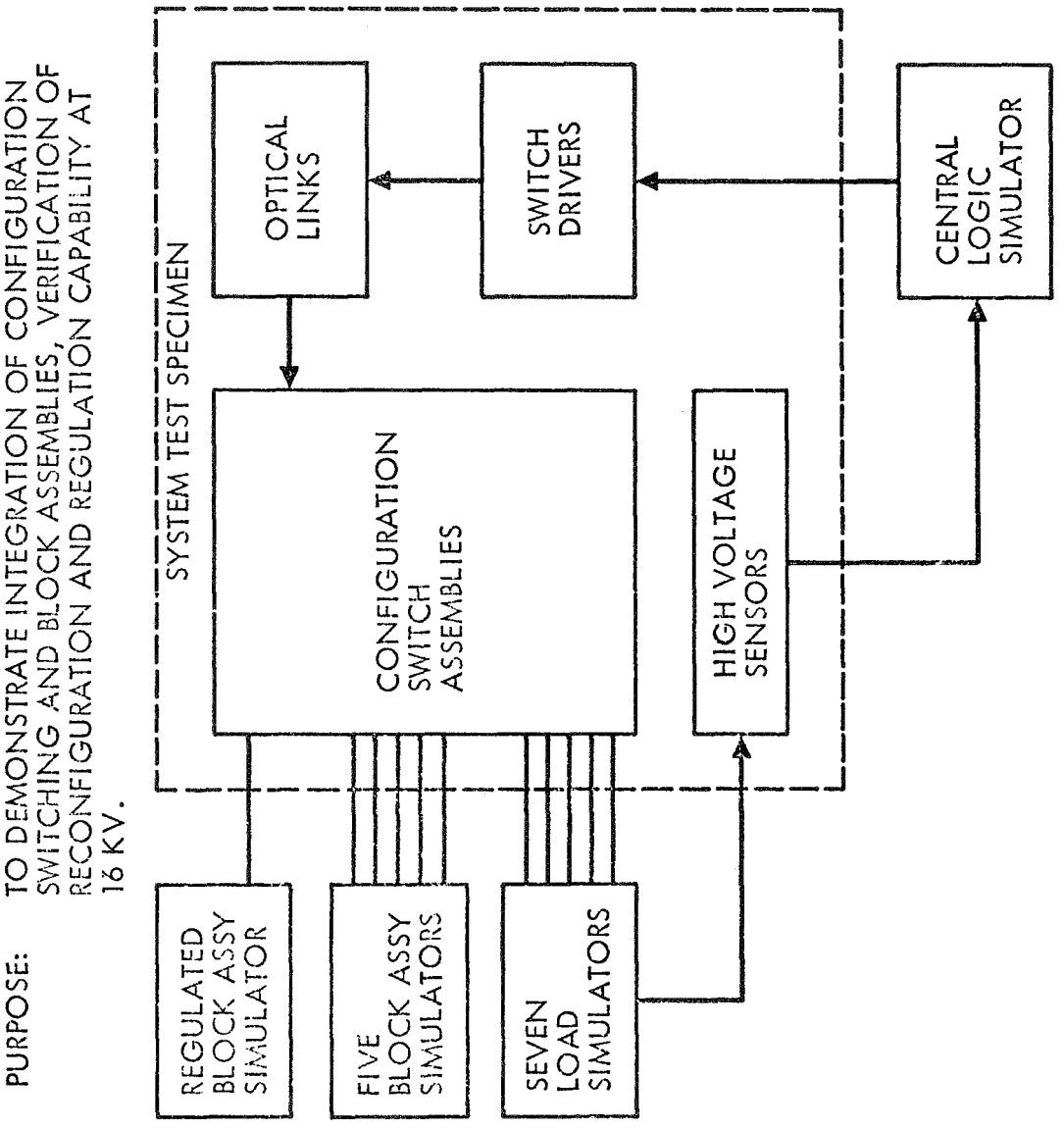


Figure 38: SYSTEM BREADBOARD TEST

11.0 CONCLUSIONS

The analysis documented in this report has established that with respect to the electrical configuration it is feasible to develop a solar array that (1) supplies a variety of loads following deployment in Earth-orbit space, and, (2) is later reconfigured to supply a single 16,000-volt, 15-kW load. Further flexibility in the high-voltage solar array can be achieved by providing extra solar-cell sections organized into current and voltage trimmers that are connected into power-producing solar-cell blocks to restore block output following radiation degradation of the solar cells when traversing through Van-Allen radiation belts. These trimmers can be used to power their own loads prior to being needed for the trimming function. The trimmers, supplemented by a weighted binary regulator that shunts out solar-cell modules in the blocks, can be used to maintain 0.1 percent current or voltage regulation in block or array output.

Estimated reliability of the high voltage array is 0.99. A design with an estimated reliability of 0.96 can be achieved with significantly less weight and array area.

Improvements in switching devices that can be made within two years will increase the efficiency of the integrally regulated solar array. However, even with today's solid-state switching devices a high voltage array is feasible. The latching characteristics and predicted efficiency of an optomechanical switch make this device worthy of further study.

Protective circuit and device requirements can be satisfied with present technology. Fault analyses need to be extended to specific loads.

Solar cell configuration designs can be based on present and modestly-improved cell and packaging technology. A four to eight-mil thick, two to ten ohm-cm resistivity, N/P silicon solar cell with a three mil cover is recommended, pending specific mission requirements.

Regulation and reconfiguration can be done with computer-controlled binary logic, and optical isolation between high voltage and low voltage switch drivers.

Capability for ground-control updating of computer switching-logic is a necessary and intrinsic part of the conceptual high voltage electrical configuration. Ground control of array configuration follows as part of this capability.

The high-voltage solar array will produce a 104.7 watts/m^2 (9.7 W/ft^2) and 65.6 watts/kg (29.8 W/lb). This compares with an unregulated Ryan low-voltage array that produces 107.6 watts/m^2 (10 W/ft^2) and 68.7 watts/kg (31.2 W/lb).

The next steps in the development of a high-voltage solar array electrical configuration are selection of devices, integration into hybrid thick film and thin film circuits, packaging, and verification of operating characteristics. This work, when followed by assembly of active and simulated components into block and array tests, will achieve technology readiness for the high-voltage solar array electrical configuration.

12.0 REFERENCES

(1) Logell, Fifth Dimension, Inc., Princeton, N.J.

(2) R. H. Cushman, "Gate-Controlled Switches May Make it Yet", EDN, pp 63-70; March 15, 1970.

(3) Electronics, pp 64-65, February 2, 1970.

(4) J. D. Gum, "Solar Arrays Utilizing Large Area Silicon Solar Cells", p 7, Heliotek Company

(5) Cooley, W. C., and M. J. Barrett, "Handbook of Space Environmental Effects on Solar Cell Power Systems", Contract NASW-1345, Exotech Incorporated (1968).

(6) Kaptoy, Pyre-ML, E. I. Dupont de Nemours & Co., Wilmington, Del.

(7) Springgate, W. F., Final Report "High Voltage Solar Array Study" The Boeing Company, NASA-Lewis Research Center NASA CR 72674.

(8) Ralph, E. L., J. H. Martin and R. L. Statler, "Radiation Damage to Thin Silicon Solar Cells", Proceedings of the 1967 Intersociety Energy Conversion Engineering Conference (1967).

(9) McMahon, E. J., "The Chemistry of Corona Degradation of Organic Insulating Materials in High-Voltage Fields and Under Mechanical Strain", IEEE Transactions on Electrical Insulation, EI-3, pp. 3-10 (1968).

(10) Ryan Aeronautical Company, "Feasibility Study - 30-Watt-per-Pound Rollup Solar Array", Final Report No. 40067-4, prepared under Contract JPL 951107 (June 21, 1968).

(11) Kennerud, K. L., "A Technique for Identifying the Cause of Performance Degradation in CdS Solar Cells", Intersociety Energy Conversion Engineering Conference Proceedings, 1969.

(12) W. A. Cordwell, "Transistor and Diode Model Handbook, AFWL-TR-69-44, October 1969.

(13) L. A. Hahn, "The Saturation Characteristics of High Voltage Transistors", Proc. IEEE, Vol. 55, pp 1384-1388, August 1967.

(14) A. B. Phillips, Transistor Engineering, New York: McGraw-Hill, 1962.

(15) Parylene, Union Carbide Co., Cleveland, Ohio.

13.0 APPENDICES

13.1 Appendix 1, Analysis of Transistor and Thyristor Voltage Limitations

Basic Limitations of Silicon Devices

The following analysis considers the limiting factors for breakdown voltage and the tradeoff between breakdown voltage and conduction resistance in high-voltage switching-transistor design. These considerations also apply to thyristor and junction field-effect transistor, because of the basic similarity of the devices as illustrated in the simplified structural models of Figure 11.

In each device the high voltage is blocked at the junction between the p-type control layer and the broad, high-resistivity n-type layer above it; this region will be the collector of the transistor, the drain of the FET, and the intermediate n layer of the thyristor.

When an external bias is applied to make the n region positive with respect to the p region the conducting electrons or holes are drawn from the junction leaving a depletion region of fixed charge. The depletion region will extend mainly into the higher resistivity n-layer. Avalanche breakdown occurs at the reverse-biased junction when the electric field in the n-region becomes high enough to ionize a critical number of minority carriers. There is an inherent trade-off between the breakdown voltage and the ohmic conduction loss since the n-layer must be made wide enough to contain the depletion region at the breakdown voltage and, when the device is on, the conducted current flows across this high resistivity region with consequent ohmic loss.

Transistor Voltage Limitation

In the transistor breakdown occurs at the reverse-biased collector-base junction due to avalanche multiplication of minority carriers. The additional effect of current multiplication which would make the collector-emitter breakdown voltage lower than that of the collector-base junction may be effectively eliminated by the application of a small reverse bias across the base-emitter junction of a transistor. The collector-emitter breakdown voltage then becomes essentially equal to the collector-base junction reverse breakdown voltage.

To analyze the collector-emitter breakdown and forward saturation characteristic, the transistor model in Figure 39 was used. Doping levels are

assumed to change abruptly at the boundaries of the regions as shown. Actually the fabrication processes generate graded impurity profiles in all available silicon high-voltage transistors, but when the high resistivity (ν) region of the collector is wide the abrupt junction model gives a good approximation as well as an upper limit to the breakdown voltage for a transistor having a given collector resistivity (Reference 13).

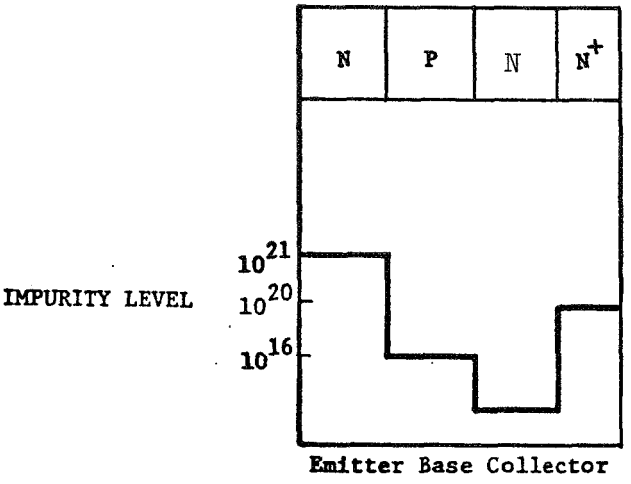


Figure 39: HIGH VOLTAGE TRANSISTOR MODEL

For an abrupt junction with the resistivity on one side much higher than on the other, the breakdown voltage (V_{BD}) is given by

$$V_{BD} = \frac{k\varepsilon_o E_m}{2qN} \tag{25}$$

where k is the dielectric constant of a silicon, N is the impurity concentration on the high resistivity side, E_m the critical field, q the electron charge, and ε_o the permittivity of free space (Reference 14). If a value of E_m could be specified, equation 25 would enable us to calculate the breakdown voltage obtainable with any resistivity of collector material. Unfortunately E_m varies with resistivity in a complex way and is also a function of the fabrication technology. The best information on voltage breakdown is obtained experimentally. A relation widely used in the design of silicon planar and mesa transistors is given by Phillips (Reference 14).

$$V_{BD} = 1.58 \times 10^{13} N^{-0.715} \tag{26}$$

Impurity concentration and resistivity are related by

$$N = \frac{1}{\rho q \mu} \tag{27}$$

where μ is the mobility of the majority carrier in cm^2/volt-second, N is in atoms/cm^3 and ρ in ohm-cm. Above resistivities of a few ohm-cm, the room-temperature mobilities are essentially independent of resistivity and are μ_n = 480 cm^2/volt-second and μ_p = 1350 cm^2/volt-second. Break-down voltages have been plotted against collector resistivities to 1000 ohm-cm in Figure 40.

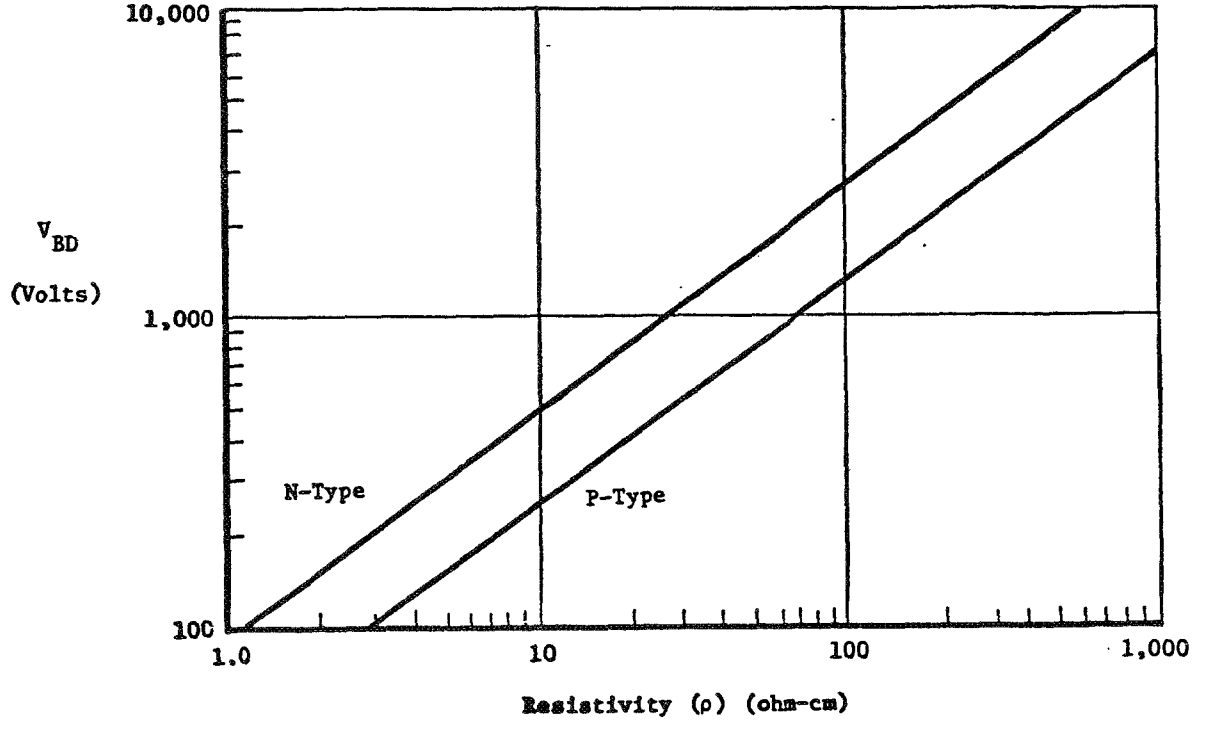


Figure 40: ABRUPT JUNCTION BREAKDOWN VOLTAGE VERSUS RESISTIVITY

Single crystal silicon is available in resistivities to 30,000 ohm-cm, but practical processing techniques now limit transistor collectors to a few hundred ohm-cm. Figure 41, a plot of the compensated impurity concentration against resistivity, indicates that very slight contamination will greatly alter or even invert the resistivity of closely compensated material. Within this limitation, V_{BD}'s of several thousand volts should be possible. As shown in the next section such devices would have to operate at low current densities to have useful saturation voltage (V_{SAT})

in power switching applications. Here the practical limitation is in the falling yield since as chip size is increased there is a greater probability of a voltage limiting defect being included in the active region of the transistor.

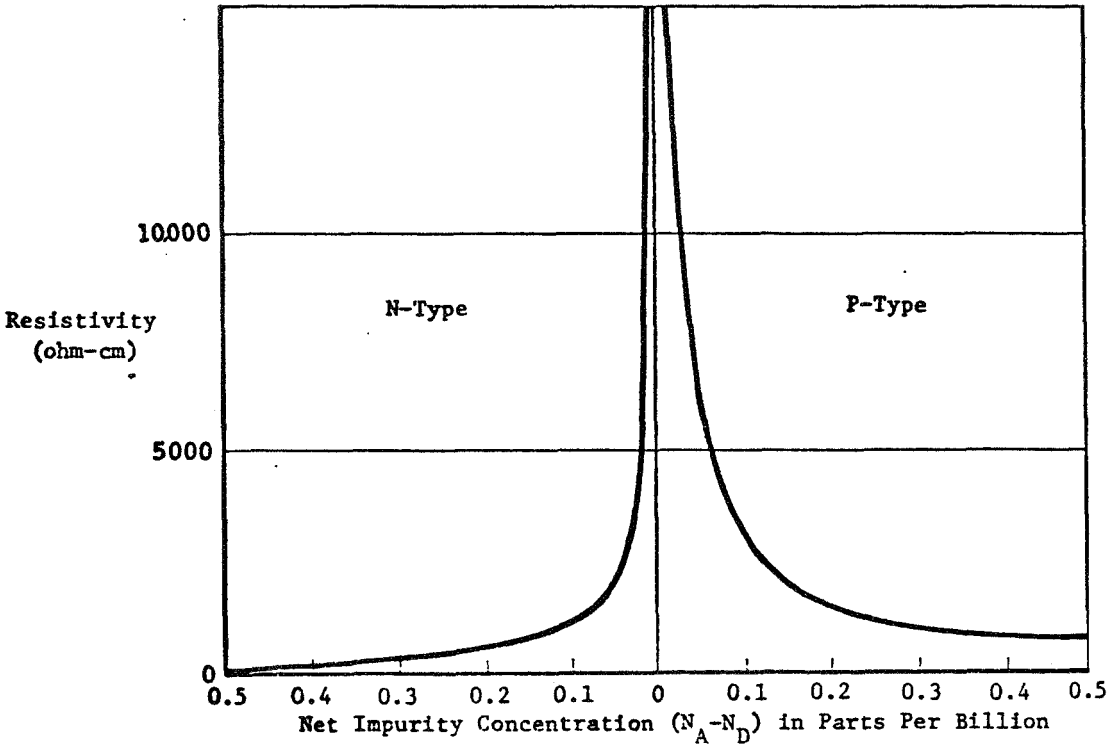


Figure 41: RESISTIVITY VERSUS IMPURITY CONCENTRATION

Transistor Voltage-Resistance Tradeoff

In the model of Figure 39 the conduction current from collector to emitter must flow through the high resistivity N region. To sustain the depletion region created by the application of V_{BD} across the junction, the high resistivity region must have a minimum thickness equal to the depletion region width (X_m) which for our model is given by the equation,

$$X_m = \left(\frac{2K\epsilon_o V_{BD}}{qN}\right)^{1/2} = 3.8 \times 10^3 \left(\frac{V_{BD}}{N}\right)^{1/2} \qquad (28)$$

(Reference 14)

For a collector region of resistivity ρ_c and depletion region thickness X_m a thermal-equilibrium collector resistance can be defined.

$$R_{CEQ} = \frac{\rho_c X_m}{A} \qquad (29)$$

where A is the area of the junction. For transistors in saturation, the forward bias on the collector-base junction will lead to minority-carrier injection with consequent conductivity modulation of the collector region (Reference 13). However, the main collector current sets up a field opposing the injection of carriers and the conductivity modulation effect decreases rapidly with increasing current densities. This is particularly true in practical power transistor structures because lateral voltage drops in the base region and the emitter fingers lead to local current concentration. Therefore, a resistive collector voltage drop

$$V_{CR} = I_C R_{CEQ} \tag{30}$$

is an optimistic estimate. The total saturation voltage drop is

$$V_{SAT} = \phi_{CE} + I_C R_{CEQ} \tag{31}$$

where ϕ_{CE} is the offset voltage associated with the collector-base junction. The offset voltage ϕ_{CE} depends principally on the inverse current gain, α_I, of the transistor, that is, the gain when the collector and emitter are interchanged, and will increase with decreasing base width. The value of ϕ_{CE} can be estimated from the manufacturer's data for saturation voltage. The mesa transistors of Table 8 have an ϕ_{CE} of about 0.2 volts while the 300-volt planar has an ϕ_{CE} of less than 0.01 volts.

The foregoing equations may be combined to give the relation between V_{SAT} and V_{BD} at room temperature:

$$V_{SAT} + \phi_{CE} + \frac{I}{A} (9.4 \times 10^{-9}) (V_{BD})^{2.6} \tag{32}$$

A plot of this equation with current density as a parameter appears in Figure 42. The validity of the design equation was tested by applying it to the 700-volt mesa and the 300-volt planar transistors of Table 8. The calculated collector areas for the specified V_{SAT} are 1.02 cm^2 and 0.365 cm^2. These figures are within 20% of the observed collectors areas.

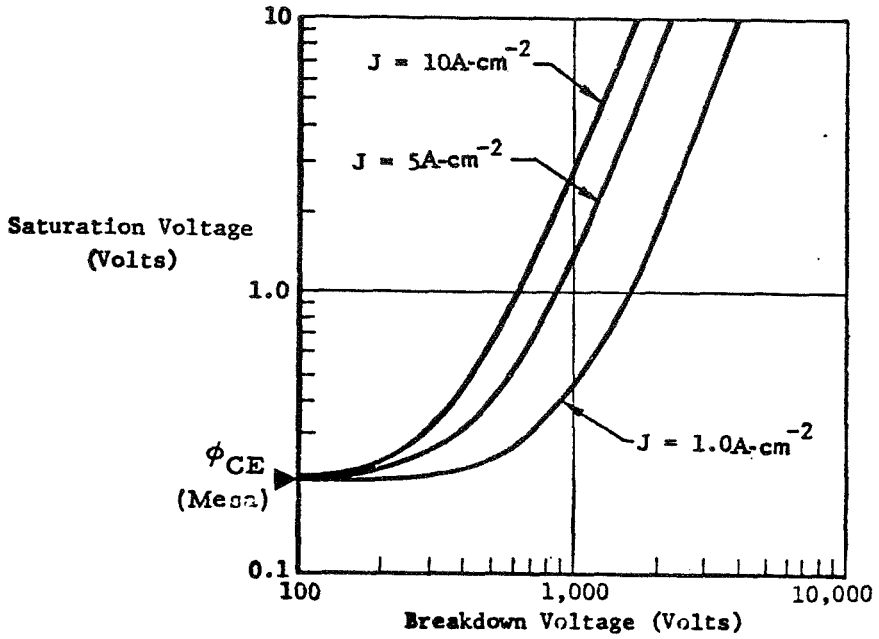


Figure 42: EFFECT OF SATURATION VOLTAGE ON BREACKDOWN VOLTAGE IN SILICON NPN TRANSISTORS

Extension of Transistor Analysis to Thyristors and Field Effect Devices

Figure 43 shows the thyristor structure with its transistor analogy. As compared with a transistor the intermediate p region of the thyristor will be wider and of higher resistivity than the base region of the transistor which must be kept narrow for acceptable gain. This feature gives the thyristor its superior blocking-voltage capability since the space-charge at the blocking junction may expand into both n and p layers, with a significant part of the voltage being across the p-layer depletion region.

The wider p-region is possible in the thyristor because the gain requirement of the npn segment of the thyristor is much less than for a useful transistor. The current gain (α_1) for a thyristor npn segment is

$$\alpha_1 = \frac{I_{c_1}}{I_{e_1}} \tag{33}$$

where I_c is the collector current and I_e is the emitter current. This gain is from 0.8 to 0.95 in typical devices. The total gain of the

thyristor for turn-on, the sum of the α's of the pmp and npn segments, will generally be much higher than that of the transistor.

The higher blocking voltage of the thyristor is obtained at the expense of a conduction drop greater than in the transistor. The reasons are: the higher resistance of the intermediate p region, the forward voltage drop of the added emitter junction, and the fact that the transistor segments cannot saturate as they have their bases clamped to their collectors. Typically, SCR's conducting 1 to 5 amperes will have conduction drops of 1.5 to 2 volts. GCS's, because of modificatons to attain turn-off gain, will have even higher conduction drops--about 2 to 2.5 volts at the same currents.

In the OFF condition with the gate open, the anode current (I_A) of a thyristor is given by

$$I_A = \frac{I_{ceo}}{I - \alpha_1 - \alpha_2} \tag{34}$$

where I_{ceo} is the leakage current across the blocking junction and α_2 the current gain of the pnp transistor segment. When the device is blocking, I_{ceo} is small and $\alpha_1 + \alpha_2$ is less than unity. Turn-on is obtained by injecting base current for the npn transistor at the gate connection. As the npn emitter current increases, α_1 increases, and when $\alpha_1 + \alpha_2 = 1$, the device switches to the stable ON state in which the anode current is limited by the external load and internal conduction voltage drop.

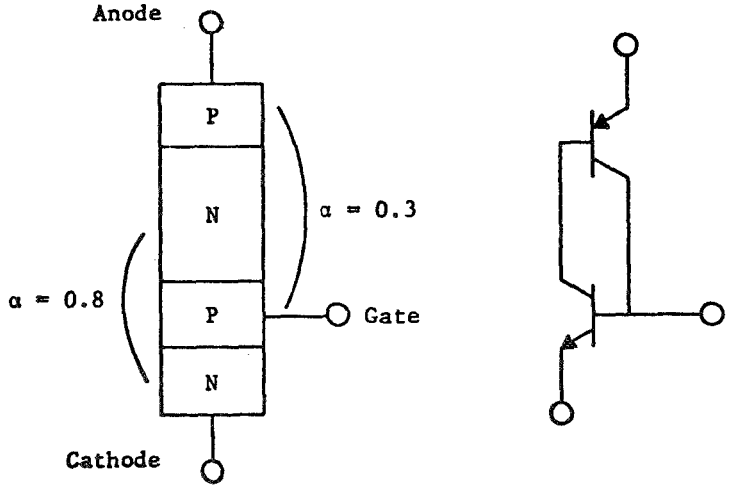


Figure 43: TWO TRANSISTOR MODEL OF THYRISTOR

The reverse process, turn-off, can be accomplished in a GCS by extracting sufficient current from the gate to reduce the α of the npn transistor. In an SCR the internal resistance between gate contact and the saturated middle junction prevents removal of sufficient current. The GCS is designed with a lower npn-segment gain and is also made to have a lower gate resistance by use of the same design techniques that reduce base spreading resistance in transistors.

In junction field-effect transistor switches, conduction is by majority-carrier flow from the "source" and to the "drain" end. Turn-off of the switch is obtained by reverse biasing the gate junction between the source and the drain so that the space charge region fills the cross-section of the channel and the current is blocked or "pinched off." The bias voltage between the drain and the gate in the pinch-off condition is always greater than the blocked voltage between the source and drain, that is, the gate will be negative with respect to the drain.

The analogue FET structure (Figure 44) is similar to the simplified FET in Figure 11. The channel is formed by diffusing the gate region as a shallow lattice into the high resistivity material that forms the drain. This is covered by an epitaxial layer into which the source region is diffused. When the device is ON, the field across the short channel is very high and the charge carriers move between source and drain much as electrons in a vacuum tube. Thus the channel has virtually no ohmic resistance and the device does not saturate as readily as do conventional FET's with relatively long channels. Current capability is obtained from having many small channels close together.

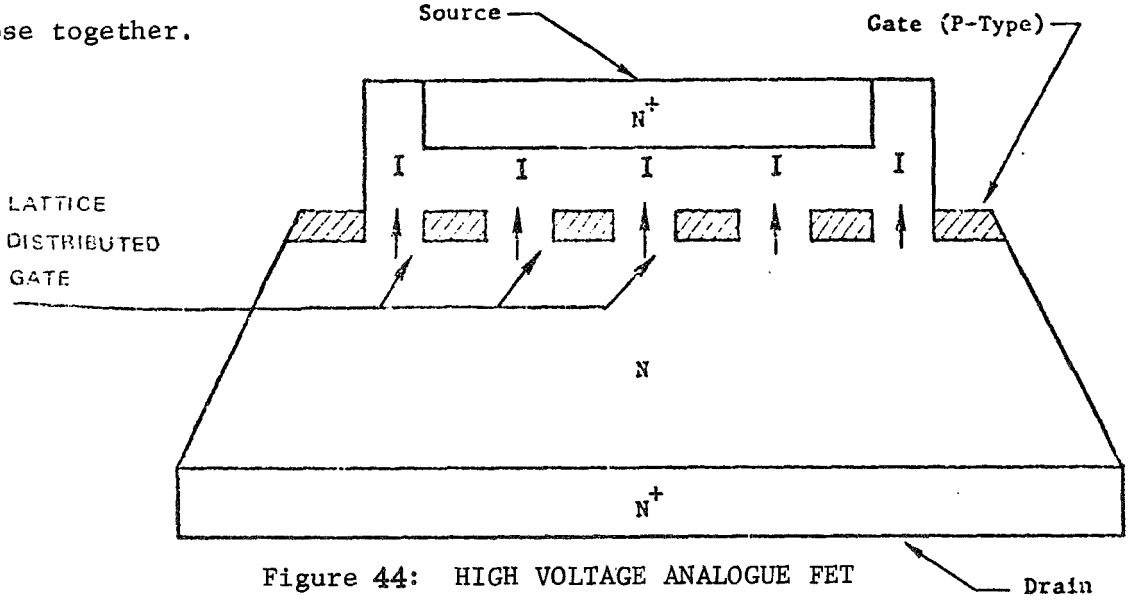


Figure 44: HIGH VOLTAGE ANALOGUE FET

APPENDIX 2

13.2 Solar Cell Model

The solar cell model is based on the classical equation for a solar cell that includes the effect of an equivalent shunt resistance (Reference 11).

$$I = I_g - I_o \left\{ \exp\left(\frac{q(V + IR_s)}{AkT} \right) - 1 \right\} - \left(\frac{(V + IR_s)}{R_{sh}} \right) \qquad (35)$$

where:
- I = current output of the cell
- I_g = light-generated current
- I_o = reverse saturation current
- q = electronic charge
- A = empirical fitting constant which is 1 for an ideal junction
- k = Boltzmann constant
- T = absolute temperature, °K
- V = the voltage appearing at the cell terminals
- R_s = series resistance
- R_{sh} = shunt resistance

The equivalent circuit of this model is shown in Figure 45.

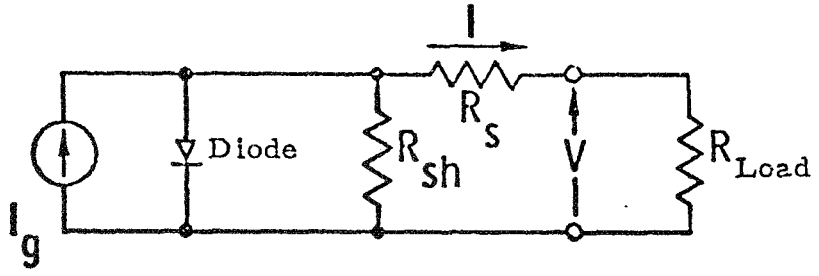


Figure 45: SOLAR CELL EQUIVALENT CIRCUIT

With the values of the five parameters given (I_g, I_o, A, R_s, and R_{sh}), the I-V curve is calculated by solving Equation 35 for I at various values of V. The coefficients of Equation 35 are arrived at by solving 5 independent non-linear equations using the Newton-Raphson iteration method as detailed in Reference 10.

These five parameters can also be extracted readily with the aid of a desk calculator (e.g., Wang 360) to a satisfactory level of accuracy from the following points on a solar cell I-V curve:

1. Open circuit
2. Short circuit
3. I & V at maximum power
4. I-V slope at V = 0
5. I-V slope at I = 0

The following approximate equations can be used to determine the five needed parameters from these five points on the solar cell I-V curve.

Let $K_o = q/kAT_o$ and let A = 1.0 then:

$$I_o = I_{sc}/\exp\ (K_o V_{oc}) \tag{36}$$

$$R_s = \left[-\left(K_o I_o\right) \exp K_o V_{oc} \right]^{-1} - \left[\left(\frac{dI}{dV}\right)_{I=0} \right]^{-1} \tag{37}$$

$$R_{sh} = - \frac{\left[1 + R_s \left(\frac{dI}{dV}\right)_{V=0}\right]}{\left(\frac{dI}{dV}\right)_{V=0}} \tag{38}$$

$$I_g = I_{sc}\ (1 + (R_s/R_{sh})) \tag{39}$$

$$\ln K_o + K_o(V_{mp} + I_{mp} R_s) \quad \ln \left[I_o^{-1}\ (I_{mp}/(V_{mp} - R_s I_{mp})) - G_{sh} \right] \tag{40}$$

where: I_{mp} = current at maximum power point

V_{mp} = voltage at maximum power point

G_{sh} = shunt conductance = $1/R_{sh}$

$\left.\frac{dI}{dV}\right|_{I=0}$ = slope of I-V curve at open circuit point

$\left.\frac{dI}{dV}\right|_{V=0}$ = slope of I-V curve at short circuit point

In fitting the model to experimental data of a 2 by 2 cm, 10 ohm-cm, 8 mil silicon cell, it was found that the RMS error can be minimized if the slope (dI/dV) @ I=0 used in equation 37 to determine R_s, is actually taken at $I = 0.3\ I_{sc}$. In one example, equation 37 is applied literally, then $R_s = 0.28$. Using the value of the slope @ $I = 0.3\ I_{sc}$, we get $R_s = 0.42$. Using the latter value, the curve-fit near the maximum power point was improved from an error of 6% to an error of less than 1%. Equation 40 provides a better estimate for K_o, hence A, than A = 1.0. The new estimate should be used in a second estimate of I_o, R_s, R_{sh} and I_g. Usually two iterations are sufficient to obtain convergence to three significant figures.

The resulting coefficients for the above example cell are:

$R_s = 0.42$ ohms $\qquad I_o = 4.1869 \times 10^{-11}$ A

$R_{sh} = 250$ ohms $\qquad A = 0.969$

$I_g = 0.14115$ A $\qquad T = 301°K$

The equation for a solar array made up of N_p parallel cells and N_s series cells at nominal temperature is:

$$I_{st} = N_p \left\{ I_g - I_o \exp \left[K_o \left(V_{st}/N_s + I_{st} R_s/N_p \right) \right] - \left(V_{st}/N_s + I_{st} R_s/N_p \right) G_{sh} \right\} \quad (41)$$

where: 1_{st}, V_{st} = string current and voltage

$K_o = q/kAT_o$

13.3 Appendix 3, Blocking and Shunt-Diode Models

Mathematical models, geared to computer simulation, have been developed for a representative group of diodes and transistors. One such collection is in Reference 12. The dynamic diode model is shown schematically below:

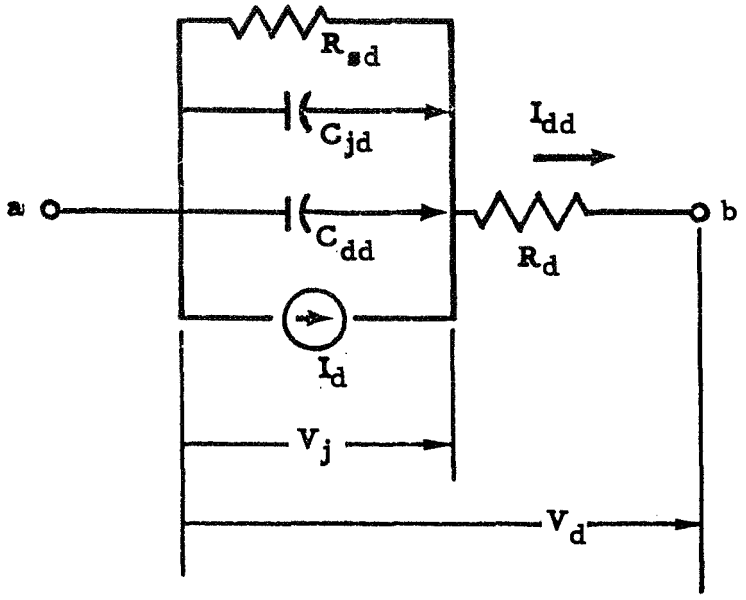


Figure 46: DIODE DYNAMIC MODEL

where $I_d = I_o (\exp(\theta V_j) - 1)$ mA (42)

$C_{dd} = K_d (I_d + I_o)$ pfd (43)

If $I_d >> I_o$, Equation 45 simplifies to:

$C_{dd} \cong K_d I_d$ pfd

$C_{jd} = C_o/(V_o - V_j)^n$ pfd

$I_{dd} = I_d + V_j G_{sd}$ mA

where K_d, C_o, θ, V_o, and n are experimentally determined coefficients.

where $G = R^{-1}$

$V_d = V_j + I_{dd} R_d$

$$V_d = V_j + R_d \left\{ I_o \left[\exp(\theta V_j) - 1 \right] + V_j G_{sd} \right\}$$

$$I_{dd} = (1 + R_d/R_{sd})^{-1} \left[I_o (\exp(\theta (V_d - I_{dd} R_d)) - 1) + V_d G_{sd} \right] \quad (44)$$

APPENDIX 4

13.4 Reliability Models and Calculations

The array configurations defined during this study consist of building blocks which are interconnected by switches to provide the desired currents and voltages. Each building block has a primary voltage section, digital-shunted sections, shunting switches, a voltage regulator and a blocking diode. The primary and shunted sections consist of solar cell submodules, connected in series to produce the required voltage and power levels. A submodule consists of a group of parallel-connected solar cells. Submodules are connected in series to form a module. Modules in the shunted section of the array are parallelled with shunting switches. The voltage regulator consists of the logic elements that control the block voltage to meet the load requirements. A blocking diode isolates a failed building block to prevent cascading or sequential failures. Shunt diodes are connected to bypass open-circuited submodules, thus eliminating open-circuited cells as a cause of catastrophic failure.

Three levels of reliability models were developed to relate the above design elements to reliability. These models, which were used to calculate submodule, building block, and total array reliability, are defined in general terms as follows:

1. Submodule Reliability (R_{SM})

$$R_{sm} = 1 - (Q_{sc} + Q_{oc}) \tag{44}$$

Where Q_{sc} = Submodule short circuit unreliability

Q_{oc} = Submodule open circuit unreliability

The submodule short circuit unreliability can be expressed as a function of solar cell short circuit unreliability and shunting diode short circuit unreliability. Submodule open circuit unreliability is expressed as a function of solar cell open circuit unreliability.

The submodule unreliability times the number of submodules per building block gives the average number of expected submodule failures per building block. We then assumed an additional shunt section consisting of (n) submodules such that the probability of more than (n) failures is $\leq 10^{-8}$.

The voltage and current trimmer sections of the advanced configuration must also be provided with extra submodules to compensate for random submodule failures. The number of submodules (n) to be added per section is also assumed such that the probability of more than (n) failures is $\leq 10^{-8}$ per section.

2. Building Block Reliability (R_{BB})

$$R_{BB} = 1 - Q_{BB}$$

Where Q_{BB} is building block unreliability.

$$Q_{BB} = (Q_p + Q_{ss} + Q_{vr} + Q_d + Q_t) \quad (45)$$

Where Q_p = Primary section unreliability

Q_{ss} = Shunt section unreliability

Q_{vr} = Voltage regulator unreliability

Q_d = Blocking diode unreliability

Q_t = Trimmer section unreliability

Q_t = 0 for basic configuration

The primary section unreliability can be expressed as a function of primary section open-circuit unreliability and design-margin unreliability. The primary section open-circuit unreliability is a function of the interconnection open-circuit unreliability, and the joint probability of solar cell open-circuit unreliability and shunting diode open-circuit unreliability. Design margin unreliability is the probability that the number of submodule failures experienced will exceed the additional submodules provided.

The shunt section unreliability is a function of shunting switch unreliability and shunt section open-circuit unreliability. The trimmer section unreliability is a function of trimmer switch unreliability and trimmer section open-circuit unreliability.

3. Solar Array Reliability (R_{SA})

$$R_{SA} = 1 - Q_{SA}$$

Where Q_{SA} is the solar array unreliability.

$$Q_{SA} = (\Sigma Q_{BB} + \Sigma Q_{sw} = \Sigma Q_c + Q_b)$$

Q_{sw} = Interblock switch unreliability

Q_{BB} = Building block unreliability

Q_c = Bus connector unreliability

Q_b = Bus unreliability

Table 27 shows the failure probabilities or unreliabilities which were developed for making reliability estimates of the solar array configurations.

Fault Tree Analysis

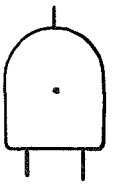
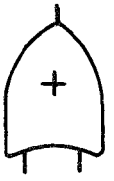
Reliability models relate the system elements in a manner that simplifies identification of critical reliability areas. A useful model in this respect is a fault tree diagram, constructed by postulating an undesired event, and identifying by a logical analysis the combination of occurrences which can lead to this undesired event. The undesired event for this program is failure of the array to produce 15 kW at 16 kV. This event should have a 0.99 probability of not occurring in 5 years, or a 0.01 probability of occurring.

Two basic logic operations, AND and OR, are used in a fault tree diagram to relate the events or combinations of events which result in the next higher level event. Their symbols are:

FAILURE	BASIC CONFIGURATION		ADVANCED CONFIGURATION	
	INITIAL	IMPROVED +	INITIAL	IMPROVED +Δ
BLOCK 1	0.00067	0.00021	0.00255	0.00020
2	0.00067	0.00021	0.00255	0.00020
3	0.00170	0.00030	0.00560	0.00027
4	0.00223	0.00034	0.00713	0.00031
5	0.00137	0.00027	0.00458	0.00024
6	0.00086	0.00022	0.00306	0.00021
POWER NOT DISTRIBUTED ALONG BUS	0.00002	0.00002	0.00002	0.00002
INTERBLOCK SWITCH	0.00281	0.00281	0.00281	0.00281
Σ	0.01033	0.00438	0.0283	0.00426
RELIABILITY ≃ (1-Σ)	0.9897	0.9956	0.9717	0.9957

+ EXTRA 128-VOLT REGULATED SECTION/BLOCK
Δ EXTRA VOLTAGE AND CURRENT TRIMMER/BLOCK

Table 27: FAILURE PROBABILITIES

Logic Operation	Symbol	Definition
AND GATE	output  inputs	A logical operation where the coexistence of all input events is required to produce the output event.
OR GATE	output  inputs	A situation where the output event will exist if one or more of the input events exist.

Fault tree events that result from the combination of fault events through the input logic gate are represented by rectangles. A circle describes a basic fault event that requires no further development. The diamond is used to simplify a fault tree for numerical evluation. The causes of the events are not shown on the fault tree. The house indicates an event that is normally expected to occur. The triangle is used to represent an event that is transferred to another diagram,  , or has been transferred from another diagram  .

Fault tree diagrams were constructed at the three levels for which reliability models were developed. Fault tree construction proceeds downward through a configuration until we can identify all basic fault inputs for which probability-of-occurrence estimates can be made.

Figure 47 is a fault tree diagram for the High Voltage Solar Array. The top level undesired event, "failure to produce 15 kW at 16 kV after 5 years of operation," has a numerical probability of 0.01. This probability is the sum of the probability of occurrence of the 8 immediate lower level events identified. The transfer-in symbols for block-failure events indicate that these probabilities are developed on other fault tree diagrams.

ARRAY FAULT TREE

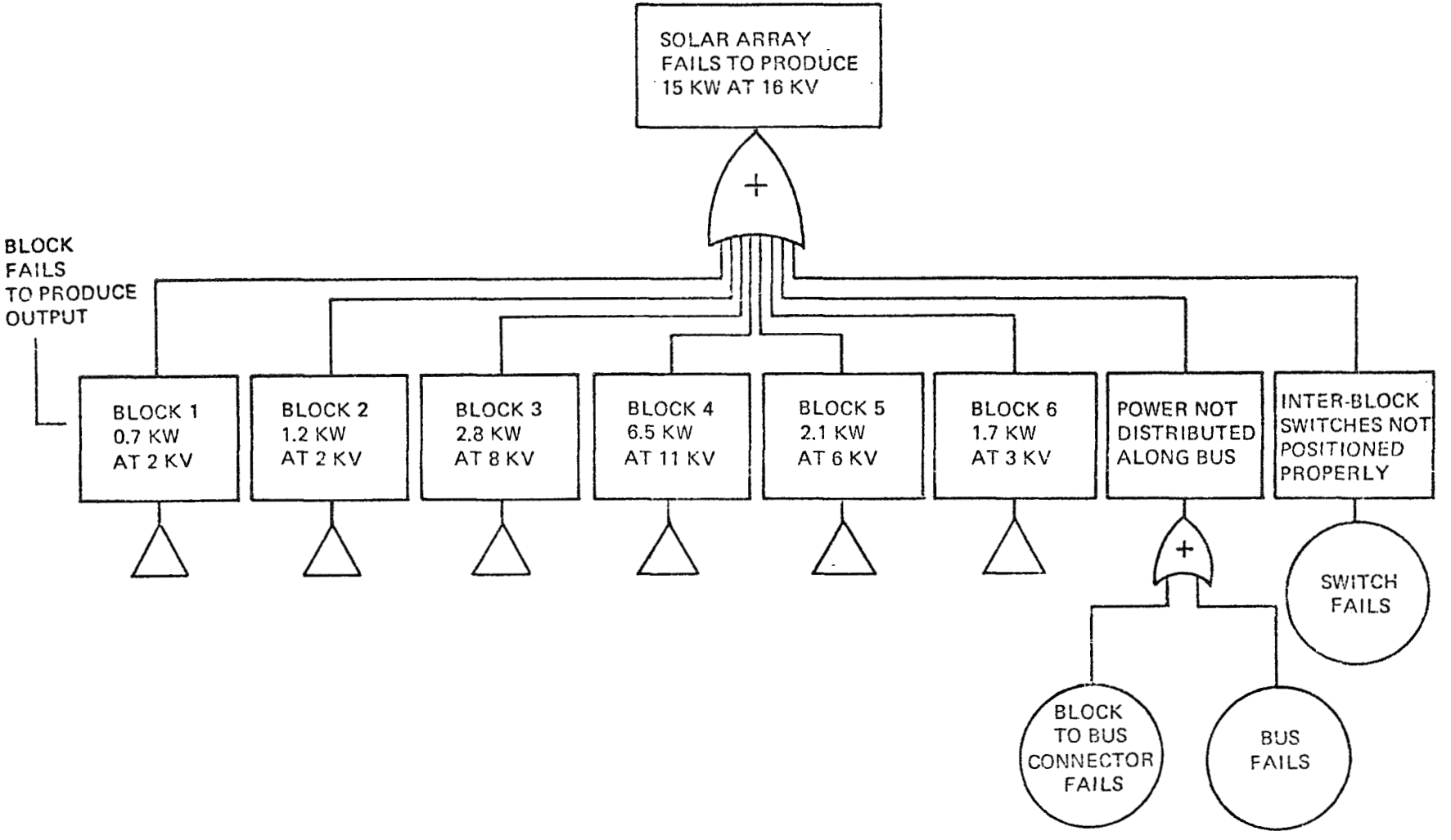


Figure 47: SOLAR ARRAY FAULT TREE

The fault tree in Figure 47 is the same for the basic and advanced configurations. The differences appear in lower level tree diagrams. Table 27 shows the probability of occurrence of each event on Figure 47. The analysis of the initial configuration produced reliabilities lower than 0.99. Figures 31 and 32 show that 57.5 percent of the basic-configuration failure probability was attributed to the shunting switches, and about 80 percent of the advanced-configuration failure probability was attributed to the trimmer switches and shunting switches.

The improved basic configuration has an extra 128-volt shunt section in each building block. With this redundancy, failure of a single shunting switch will not result in failure of the block to produce the required power and voltage. The improved advanced configuration also includes in each block the extra section, plus one extra voltage trimmer section and current trimmer section with required switches. Failure of the block as a consequence of switch failure now requires that one of the following events occur: (1) Two voltage trimmer switches fail, (2) two current trimmer switches fail, or (3) two 128-volt shunt-section switches fail.

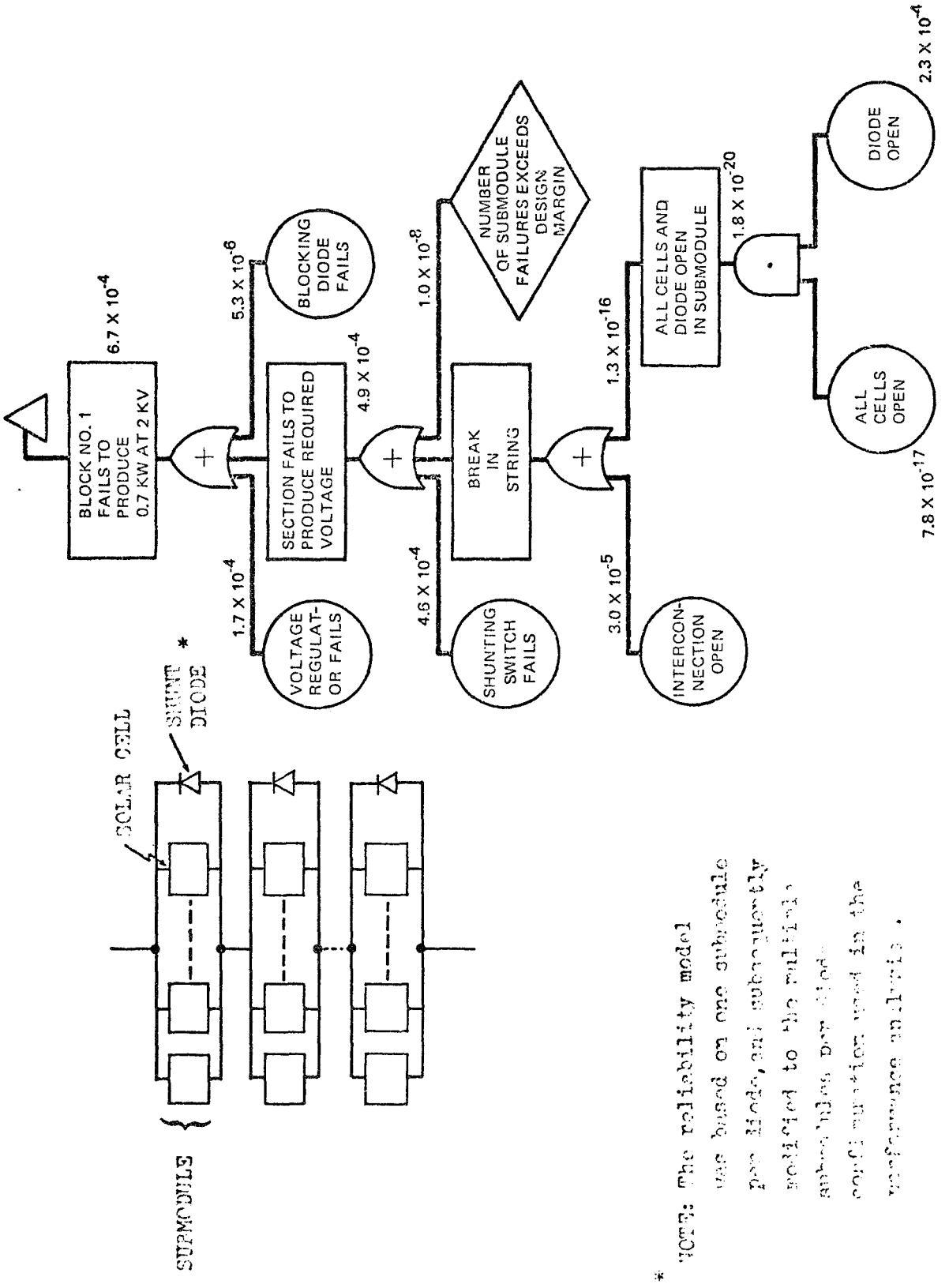
The analyses show that configurations with the above improvements can meet the 0.99 reliability goal.

Reliability Calculations

Building Block Calculations

Figure 48 shows a fault tree diagram of building block 1 of the basic configuration. Block failure occurs if the voltage regulator fails, the blocking diode fails, or the primary section or one or more shunt section fails to produce the required voltage. A shunt section fails if one or more shunting switches fail or the section string is broken.

A submodule fails if one or more cells in the submodule fail shorted, or a shunting diode fails shorted, or one or more cells fail open. A submodule failure becomes important only if the number of submodule failures exceeds the design margin. The joint event of all cells in a module failing open and the shunting diode failing open, a 1.8×10^{-20} possibility, results in an open string in that section. Open circuit failure of one or more interconnectors in a section also results in an open string in that section.



* NOTE: The reliability model
was based on one submodule
per block, and subsequently
modified to the multiple
submodules per block
configuration used in the
performance analysis.

Figure 48: BUILDING BLOCK FAULT TREE---BASIC CONFIGURATION

The total failure probability for this block is shown as 6.7×10^{-4}. It is evident from the probability values on the tree that the shunting switch failure is the greatest hazard, constituting 69 percent of the failure probability.

Adding a 128-volt shunt section and switch changes the failure criteria from one or more shunting-switch failures to two or more shunting-switch failures. This reduces the failure probability for that event from 4.6×10^{-4} to 1.2×10^{-7} and reduces the total block failure probability from 6.7×10^{-4} to 1.9×10^{-4}, which is 3.5 times better.

A fault tree diagram for an advanced-configuration building block (Figure 49) shows basically the same fault events as shown in Figure 48. Voltage and current trimmer sections make the diagram more complex.

To achieve 0.99 probability of full output after five years, two shunting diodes would have to be connected across the single-cell submodules in the current trimmer sections. With only one shunting diode across each submodule, the probability of a break in the string caused by failure of both cell and diode was calculated to be 2.9×10^{-3}, compared to the value 9.1×10^{-5} with two diodes. Doubling the diodes reduces the block failure probability from 5.4×10^{-3} to 2.6×10^{-3}. It should be noted that the performance estimate in Section 9.0 is based on one diode across every 50 cells in series except in regulated sections where there is one diode across every 10 cells in series. The resulting array reliability is 0.96 for five years.

It is also evident from the probability values shown in Figure 49 that switch failures account for most of the block failure probability (2.25/2.55 = 88%). By including an extra 128-volt digital shunt section and switch, an additional voltage trimmer section and switches, and an additional current trimmer section and switches, the total block failure probability can be reduced to 2.0×10^{-4}, a 13-fold improvement.

Differences in failure probabilities among building blocks arise from differences in number of cells per submodule, string length, sizes of the primary and shunt sections, and number of shunt sections.

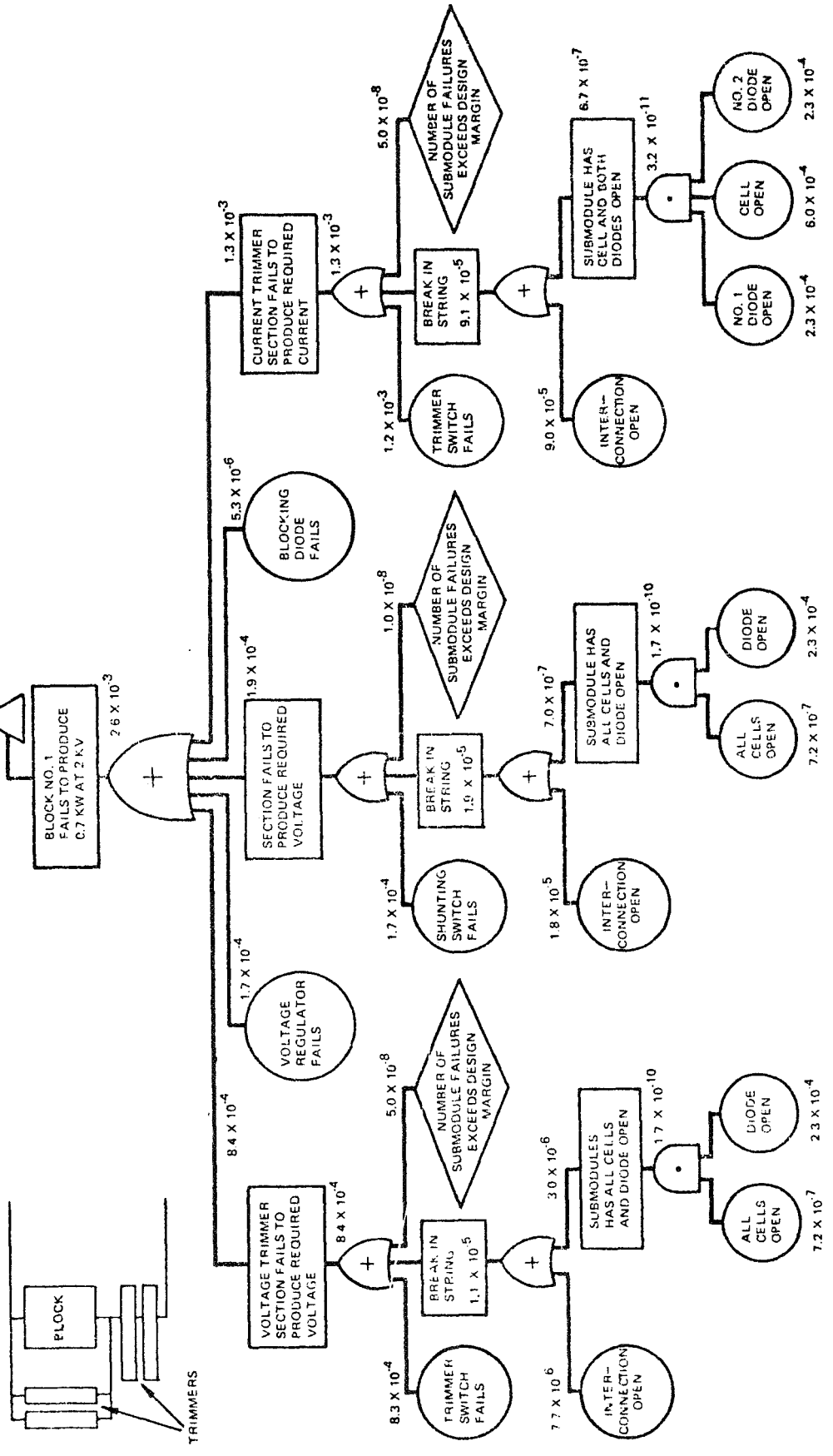


Figure 49: BUILDING BLOCK FAULT TREE---ADVANCED CONFIGURATION

Submodule Calculations

A submodule fails if one or more cells fail shorted, or one or more cells fail open, or a shunting diode fails shorted (Figure 50). Open-circuit failure of all cells and shunting diode is shown on the building-block fault tree, since the effect of this failure is loss of an entire section rather than failure of a single submodule.

Voltage reversal occurs across a submodule with one open cell if the number of parallel cells is five or less. A submodule with eight parallel cells will be down to 0.12 volts after one cell fails open. Both conditions are considered to be submodule failures.

Submodule failure probabilities were multiplied by the submodule count to give the average expected number of submodule failures (E) per block. The Poisson and normal distribution functions were then used to determine the number of extra submodules (N) required to make the probability of r>N failures less than or equal to 10^{-8}, where r is the actual number of failures. In the worst case for the basic configuration, 1.3 percent additional submodules are required. Increasing the probability of r > N to 10^{-4} results in a design margin requirement of a 1.1 percent. For the total array, a design margin of 0.87 percent achieves a 10^{-8} failure probability per building block. If the goal were 10^{-4}, the design margin is 0.75 percent. These values do not include the margin provided by adding a 128-volt shunt section to each building block. The array design margin including this improvement is about 3 percent.

Figure 51 shows a detailed fault tree for a submodule with only one cell and two shunt diodes. Short circuit failure occurs if either diode fails shorted or the cell fails shorted. Open circuit failure occurs if the cell fails open. Again, open-circuit failure of both diodes and the cell is considered a section failure rather than a submodule failure. The events whereby neither diode fails open are represented by houses on the fault tree.

As an example of submodule failure probability, consider block 1 of the advanced configuration. The current trimmer sections of this block have 4240 single-cell submodules in series. The average expected number of failures is $(4.24 \times 10^{3})\ (1.29 \times 10^{-3}) = 5.47$. Assuming the Poisson distribution function, 23 additional submodules will result in a probability of 10^{-8} that the number of failures will not exceed the design margin.

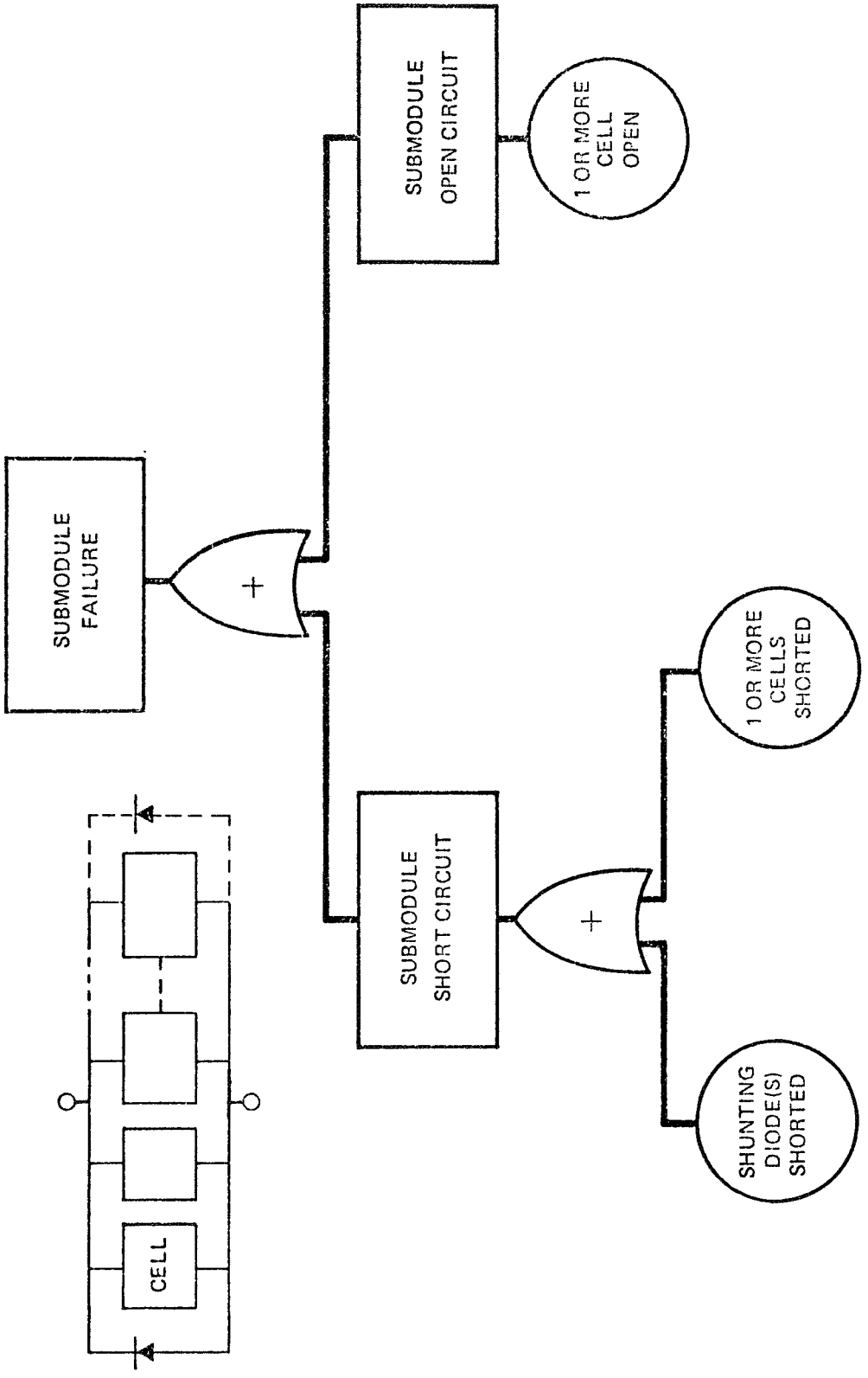


Figure 50: SUBMODULE TREE

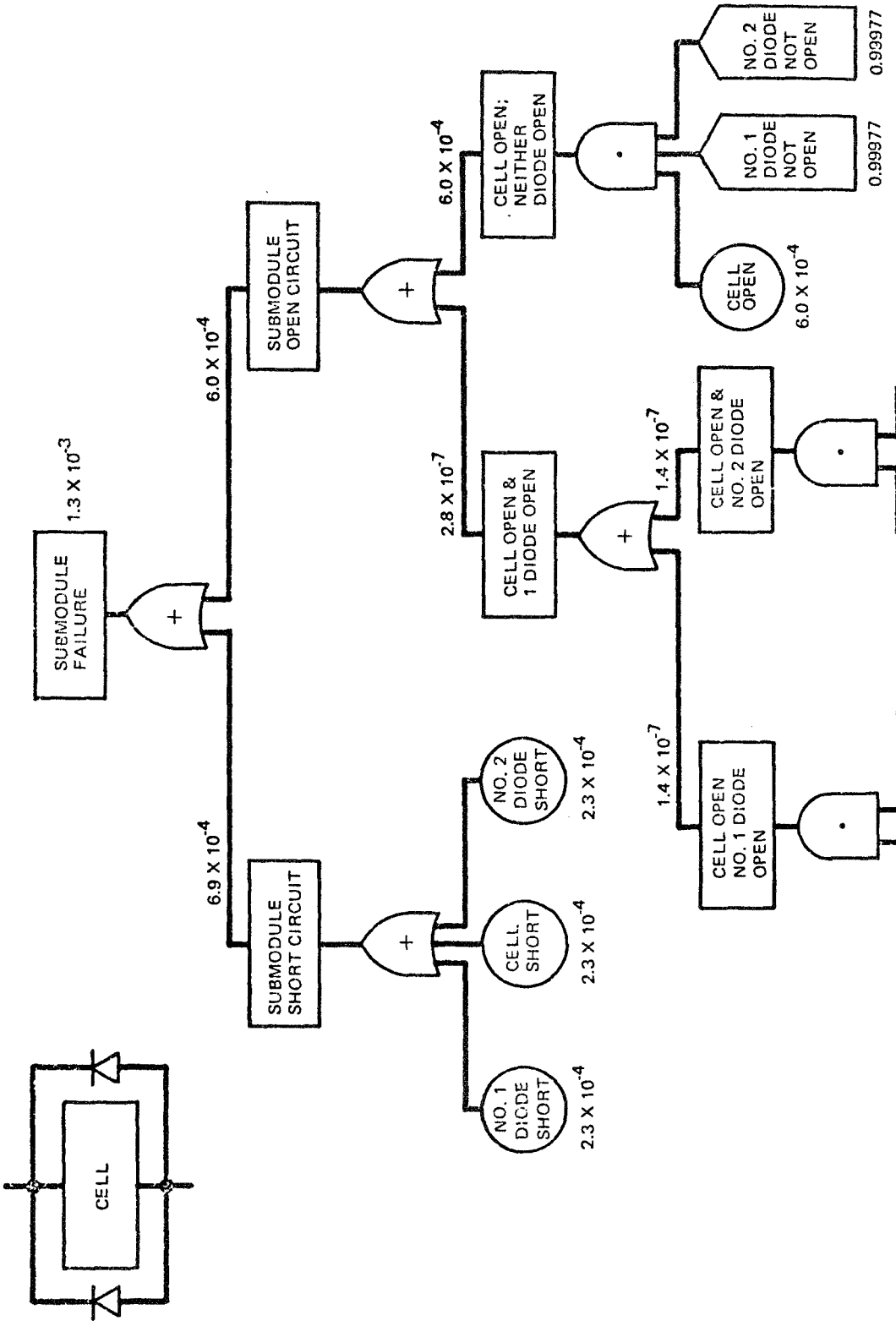


Figure 51: SUBMODULE FAULT TREE--1 CELL WIDE

Figure 52 shows a detailed fault tree diagram for submodules of 2, 5, and 8 parallel cells. Submodule short circuit failure occurs if the shunting diode fails shorted or if one or more cells fail shorted. Submodule open circuit failure occurs when one or more cells fail open. The probability values shown represent the two-parallel-cell submodules. Total submodule failure probabilities are also shown for the five and eight parallel-cell submodules.

As an example, consider again block 1 of the basic configuration, having five parallel cells per submodules. There are 7055 submodules in the building block, each with a failure probability of 4.38×10^{-3}. The average expected number of failures is $(7.055 \times 10^{3})\ (4.38 \times 10^{-3}) \cong 31$. Using the Poisson distribution function for E = 31, sixty-six additional submodules will result in a probability of 10^{-8} that the number of failures will not exceed the design margin.

The appropriate form for this design margin is an additional shunt section containing 66 submodules.

Mathematical Models

The exponential failure frequency distribution was assumed for calculating individual part reliability. The reliability is calculated as $R = e^{-t}$ where R is the average failure rate of the part and t is the operating time. This distribution is a reasonable approximation, over normal use periods, for devices which have been stabilized through burn-in procedures. The frequency distribution is described by the equation:

$$f(t) = \lambda e^{-\lambda t}$$

where λ represents a constant average failure rate over the time period (t).

For elements whose reliability is a function of the product of the reliability of several parts the following approximation was used for ease of calculation:

$$R = e^{-\lambda t} \simeq 1 - \lambda t \qquad (46)$$

This is a close approximation for values of $\lambda t \leq 0.01$. For example, if $\lambda t = 0.01$:

$$R = e^{-\lambda t} = 0.99005$$

$$R = 1 - \lambda t = 0.99000$$

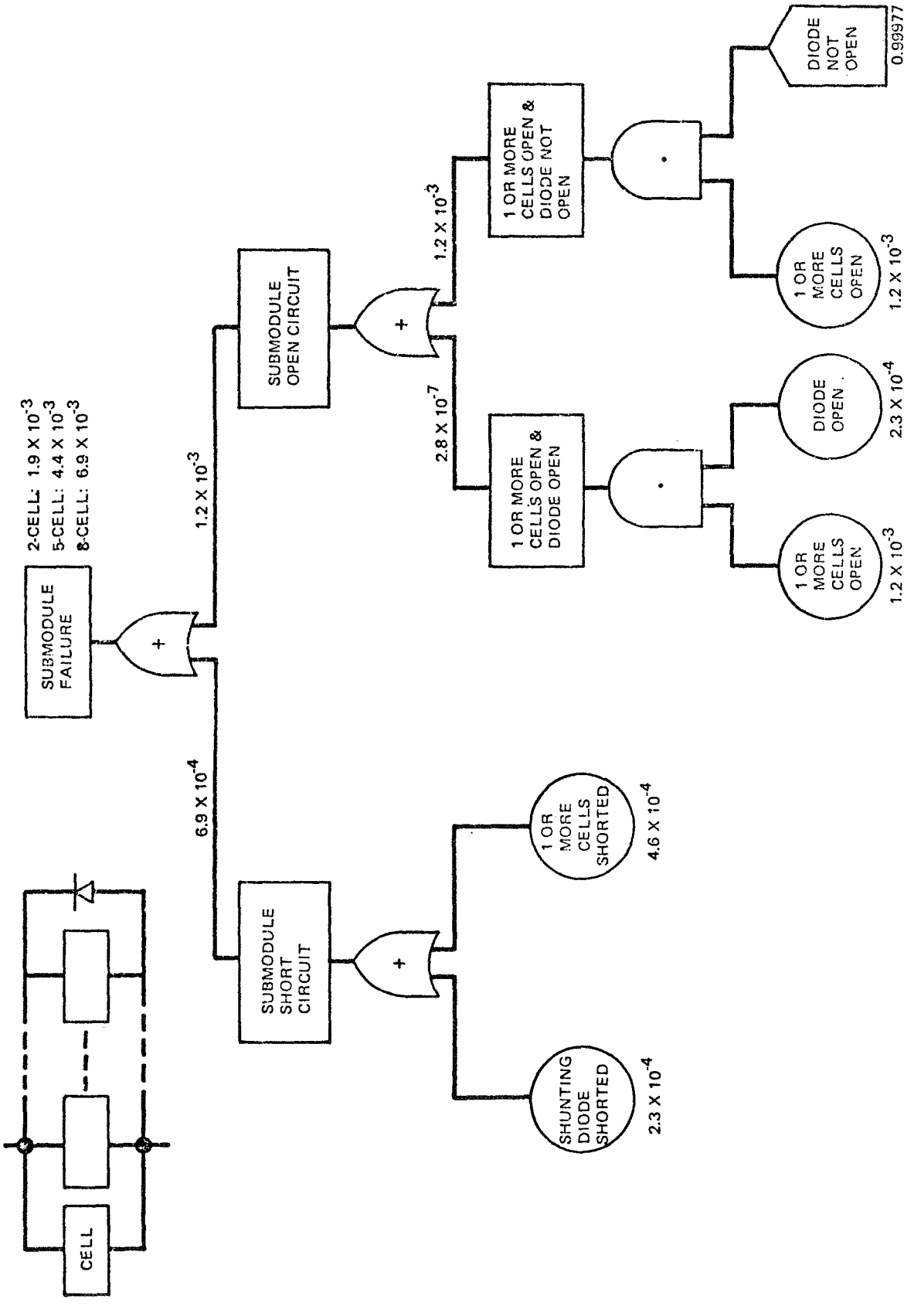


Figure 52: SUBMODULE FAULT TREE---2, 5, 8 CELLS WIDE

For $\lambda t = 0.001$:

$$R = e^{-t} = 0.9990005$$

$$R = 1 - \lambda t = 0.999000$$

The reliability of an element consisting of several series parts, can then be approximated by:

$$R = 1 - \left[(\lambda t)_1 + (\lambda t)_2 + (\lambda t)_3 + \ldots (\lambda t)_n\right]$$

$$= 1 - \sum_{i=1}^{n} (\lambda t)_i \qquad (47)$$

The unreliability (probability of failure) is therefore approximated by:

$$1 - R = \sum_{i=1}^{n} (\lambda t)_i \qquad (48)$$

Reliability Data

The part failure rates that were used in the reliability analyses were based on the following selection, control and application procedures:

- o Rigid design and procurement specifications
- o Careful parts selection
- o Parts screening
- o Parts derating
- o Burn-in
- o Qualification tests

The selection of a best failure rate estimate from the range of electronic part failure-rate values (Table 28) was based on similarity of application, dates of estimates, anticipated reliability growth, and state-of-the-art development. Failure-rate estimates for parts which have limited or no application data were based on the assumption that failure rates comparable to current achievements could be realized by the expected flight date.

Table 29 shows the part failure rates that we selected for the reliability analyses. Also listed are the sources of failure rate data which were used in developing these estimates.

PART	FAILURE RATE (FAILURES PER 10^6 HOURS)
Diode, silicon less than 1 watt	0.002 - 0.016
Diode, silicon more than 1 watt	0.014 - 0.24
Diode, zener	0.01 - 0.11
Resistor, Fixed composition	0.001 - 0.005
Transistor, silicon low power	0.01 - 0.08
Transistor, silicon power	0.06 - 0.38

Table 28: ELECTRONIC PART FAILURE RATES - RANGE OF ESTIMATES

PART	FAILURE RATE (FAILURES PER 10^6 HOURS)
Transistor, Field Effect	0.06
Up-down Counter	0.10
Gating Logic	0.02
Zener Diode	0.05
Transistor, unijunction	0.06
Capacitor	0.004
Resistor	0.002
Transistor, NPN General Purpose	0.02
Transistor, Power	0.06
Operational Amplifier	0.10
Transistor, PNP General Purpose	0.04
Diode, Light Emitting	0.05
Photo - SCR	0.05

Table 29: ELECTRONIC PART FAILURE RATES USED IN RELIABILITY ANALYSES

FAILURE RATE DATA SOURCES

1. MIL-HDBK-217A, "Reliability Stress and Failure Rate Data for Electronic Equipment," 1 December 1965.

2. Minuteman: D2-20473-1, "Minuteman Failure Rate, Mode, Cause, and Maintenance Data," C. R. Henry and R. E. Tidball, The Boeing Company, 29 December 1964.

3. NASA: "Parts Reliability Problems in Aerospace Systems," W. M. Redler, Reliability and Quality Assurance, NASA, Washington, D. C.

4. Satellite (Hughes). "Design for Reliability," Frank A. Barta, Space Systems Division, Hughes Aircraft Company.
"Hughes Satellite Operational Data Analysis," E. Long, Oct. 1968.

5. Bell Telephone Laboratories: "Operational Reliability of Components in Selected Systems," T. L. Tanner of B.T.L.

6. Martin-Marietta: "The Long Life Spacecraft Problem," R. W. Burrows, Martin-Marietta Corporation, Paper No. 67-880, AIAA 4th Annual Meeting and Technical Display, October 1967 (N-74).

7. TRW Systems: E-7441.2-005, "Power System Configuration Study and Reliability Analysis," TRW Systems, January-April 1967 (ASTIC 051561).

8. Nortronics: NORT 67-85, "Proposal for AWACS Navigation Subsystem," Volume I, pp 16-21, 22 May 1967 (F/D G357-67-116).