High-Voltage Vertical GaN p-n Diodes by Epitaxial Liftoff From Bulk GaN Substrates

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***Abstract*— High-performance vertical GaN-based p-n junction diodes fabricated using bandgap selective photoelectrochemical etching-based epitaxial liftoff (ELO) from bulk GaN substrates are demonstrated. The epitaxial GaN layers and pseudomorphic InGaN release layer were grown by MOCVD on bulk GaN substrates. A comparison study was performed between devices after liftoff processing (after transfer to a Cu substrate) and nominally identical control devices on GaN substrates without the buried release layer or ELO-related processing. ELO and bonded devices exhibit nearly identical electrical performance and improved thermal performance, compared with the control devices on full-thickness GaN substrates. The breakdown voltage, ideality factor, and forward turn-ON performance were found to be nearly identical, indicating that the transfer process does not degrade the quality of the p-n junctions. The devices exhibit turn-ON voltages of 3.1 V at a current density of 100 A/cm^2, with a specific ON-resistance (R_{ON}) of 0.2–0.5 m$\Omega \cdot$ cm^2 at 5 V and a breakdown voltage (V_{br}) of 1.3 kV. Both optical and electrical characterization techniques show that the thermal resistance of ELO devices bonded to a Cu carrier is approximately 30% lower than that for control devices on GaN substrates.**

***Index Terms*— GaN p-n junctions, epitaxial lift-off, thermal resistance.**

I. Introduction

VERTICAL GaN (and related III-N materials)-based devices are promising for power electronics due to both the exceptional properties of the III-N material system and the advantages of vertical device architectures [1]–[7]. However, vertical GaN-based device performance is often limited due to the use of lattice-mismatched foreign substrates, resulting in high dislocation densities as well as limited thermal conductivity for heat removal [8], [9]. Bulk GaN substrates are becoming available commercially, but their high cost and limited availability pose challenges for widespread adoption. The use of epitaxial lift-off (ELO) offers an approach to address these issues [10]–[13]. Removing the substrate and bonding the lifted-off device film to a high-thermal-conductivity substrate eliminates the thermal resistance associated with conventional substrates through direct thermal and electrical bonding to the heat sink. Furthermore, ELO can result in improved economics by enabling re-use of the original GaN substrates [14]. ELO processing has previously been demonstrated to improve the performance of GaN Schottky diodes grown on sapphire substrates [15], [16], and low-voltage mesa-isolated vertical ELO GaN p-n diodes have also been demonstrated [17], [18]. To improve device performance and scalability, a vertical p-n diode fabrication process with ion-implantation edge termination (ET) and sputtered SiN_x passivation was demonstrated for GaN-on-GaN diodes, with performance approaching the fundamental material limits of GaN [4], [19]. This process was previously used in conjunction with ELO to bond thin-film GaN p-n diodes to a metallized alumina carrier; this first demonstration resulted in $V_{br} = 800$ V and $R_{on} = 0.5$ m$\Omega \cdot$cm^2 [21]. In this work, we report significantly improved breakdown performance for ELO diodes bonded to high-conductivity Cu carriers, as well as a study of the thermal resistance associated with the ELO process for GaN-on-GaN vertical diodes. Breakdown voltages of 1.3 kV and differential on-resistances between 0.2-0.5 mΩ-cm^2 have been achieved. Both electrical [22], [23] and optical methods [24] were utilized to estimate the thermal resistance of layer-transferred GaN p-n diodes. It is found that the thermal resistance of ELO devices on Cu carriers is reduced by >30% compared with the control devices on bulk GaN substrates.

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II. Device Fabrication

The device design for the implant-isolated vertical p-n junctions consists of (in growth order) an n^+ GaN buffer, pseudomorphic InGaN release layer, and 2 μm n^+ cathode layer, followed by a 12 μm n^- drift layer (Si: 1×10^{16} cm^{-3}) and 450 nm p^+/20 nm p^{++} anode layer. The epitaxial material was grown using MOCVD on a 2" n^+ bulk GaN substrate (Fig. 1. (a)). For comparison, a nominally-identical control structure but without the buried InGaN release layer was also grown. Vertical GaN p-n diodes were fabricated in parallel on

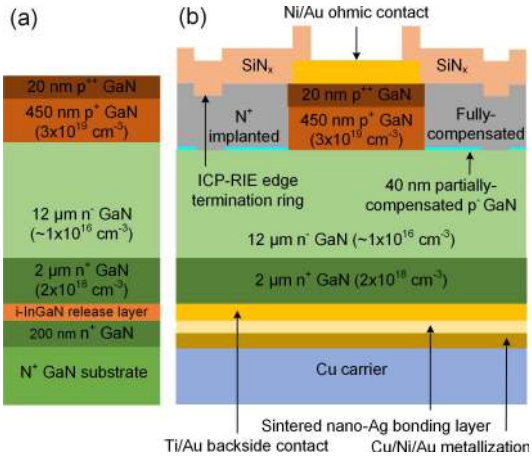

Fig. 1. (a) Heterostructure used for the ELO devices. The control sample has the same epitaxial structure, except for omission of the InGaN release layer. (b) Schematic cross-section of p-n diode after lift-off and bonding to the carrier.

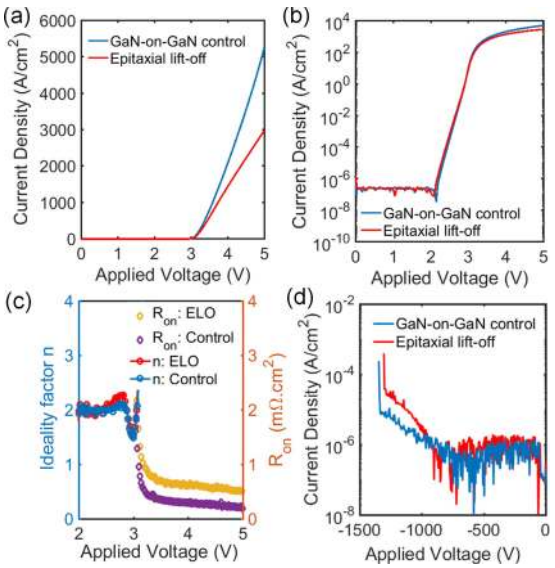

Fig. 2. (a) & (b) Measured forward I-V characteristics on linear and semi-log scales; (c) ideality factor and differential on-resistance; (d) reverse-bias characteristics.

both the ELO and control structures. P-GaN ohmic contacts with low resistance were obtained using a two-step surface treatment [17] and thermal annealing of evaporated Ni/Au (20/500 nm) contacts. A 0.5 μm thick Au top layer was used on the anode contacts to reduce probe resistance on large devices [25]. A triple nitrogen implant and a shallow trench etch (Fig. 1. (b)) were used to create fully-compensated (gray) and partially-compensated (light blue) edge termination regions for device isolation. The top surface of the devices was passivated with sputter-deposited SiN_x. After completion of the top-side device fabrication, a 25 μm thick metal support layer was electroplated on the top surface. The device layers were then lifted off using photoelectrochemical (PEC) selective wet etching to dissolve the buried InGaN release layer. The PEC ELO process is performed in a KOH solution, with the sample acting as the anode, and a Pt wire as the cathode of the resulting electrochemical cell. A high-power LED-based UV light source shining through the substrate from the back acts to drive the electrochemical dissolution reaction. The peak irradiance of the UV light is at a photon energy below the bandgap of GaN to ensure that optical absorption occurs primarily in the InGaN release layer. Full details of the ELO process have been published previously [16], [18]. Following lift-off, the back side of the ELO devices was metallized using evaporated Ti/Au (40/100 nm), and the lifted-off device film was bonded to a Cu carrier using nanosilver paste [20] and sintered for 1 hour at 260 °C (Fig. 1. (b)). After bonding to the copper carrier, the top support metallization was removed by selective wet chemical etching. For the control sample, a conventional Ti/Al/Ni/Au (30/100/50/50 nm) metallization on the back of the wafer was used for the cathode contact.

III. Results and Discussion

Figure 2 shows measured characteristics of representative control and ELO devices. As can be seen, the devices after ELO have nearly identical electrical performance to those on full-thickness GaN substrates. In the reverse-bias region, when the reverse voltage is smaller than 700 V, the leakage current shown in Fig. 2. (d) is too small to be measured (the data shown reflects the measurement noise floor of $\sim$ 1 nA). For larger reverse voltages, the reverse current rises gradually, before an abrupt breakdown at approximately 1.30 kV. The ELO p-n diode exhibits a V_{br} of 1.30 kV, within 30 V of the control sample's V_{br} of 1.33 kV. In both cases, the breakdown was limited by the edge termination. Higher breakdown voltages have been achieved with optimized edge termination processes [4]. In forward bias, both the ELO and control diodes show forward currents below the measurement noise floor for biases below 2 V. For applied voltages from 2 V to approximately 2.5 V, the extracted ideality factor n is approximately 2.0 for both the control and ELO devices, indicating Shockley-Read-Hall (SRH) recombination dominated operation. Above 2.5 V, the extracted ideality factor shows a transition from 2 down to approximately 1.54 and 1.48 at 3 V for the ELO and control samples, respectively, indicating the onset of diffusion current (with theoretical ideality factor of 1). A turn-on voltage of 3.1 V (at 100 A/cm^2) is measured for both cases, as expected for a GaN homojunction. Also, above the turn-on voltage, the apparent n rises due to the diode's series resistance. A differential R_{on} of 0.50 mΩcm^2 and 0.20 mΩcm^2 (at 5 V) was measured for the ELO and control samples, respectively. As can be seen in Fig. 2, the only significant difference between the ELO and control devices is the increased R_{on} of the ELO devices. This is attributable to the unoptimized Ti/Au contact to the N-face cathode. From transfer-length method (TLM) measurements, we find the specific contact resistance for the N-face contact to the control samples (using Ti/Al/Ni/Au) is approximately 3.3×10^{-6} Ω cm^2, while the unalloyed Ti/Au contact on the ELO samples is $1.4\times10^{-5}\Omega$ cm^2. Use of more heavily doped n^+ GaN cathode contact layers in the future is expected to improve the contact resistance [26]. The nearly identical ideality factor under forward bias, and leakage current and breakdown voltage under reverse bias, suggests that ELO of bipolar GaN devices can be achieved without introducing

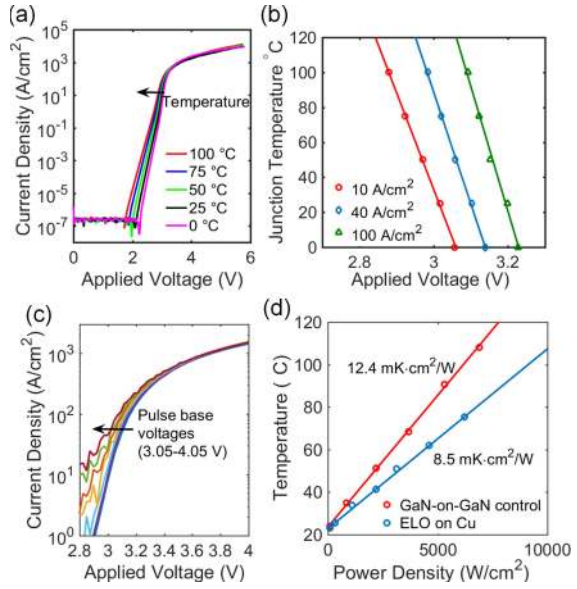

Fig. 3. (a) DC I-V vs. temperature for ELO devices. (b) Temperature-voltage characteristics for selected current densities, as extracted from the temperature-dependent I-V. (c) Pulsed I-V characteristics for a typical ELO device for several pulse base voltages above the turn on voltage. (d) Temperature vs. power density for ELO and control devices. The thermal resistance is extracted from the slope of the least-squares fit to these data.

recombination centers or other defects that would compromise performance.

A potentially valuable feature of band-gap selective PEC etching ELO processing is that it offers the ability to maintain fully coherent single-crystal material from the bulk substrate through the device epitaxial layers [14], while at the same time providing a route to reduce the thermal resistance by removal of the substrate and mounting the device active layers directly on a heat sink. The thermal performance of the fabricated diodes was assessed using both electrical and optical methods. For the electrical approach, a pulsed I-V technique was used [22]. To allow the diode characteristics to be measured without self-heating from the measurement impacting the temperature, a pulsed I-V sweep with 500 μs pulses and period of 500 ms was used. DC sweeps were performed at baseplate temperatures from 0 °C-100 °C (Fig. 3. (a)) to obtain relationships between junction temperature and applied voltage at selected current densities (Fig. 3. (b)). Pulsed I-V sweeps were then taken for a range of quiescent (forward) biases. The quiescent bias induces self-heating in the devices, while the 0.1% duty cycle of the sweep allows the I-V characteristics to be obtained (Fig. 3. (c)) without significantly impacting the temperature. From these sweeps, the applied voltage that corresponds to the specified current density can be read out, and by using Fig. 3. (b) as a mapping between voltage and temperature, the effective junction temperature can be obtained as shown in Fig. 3. (d). The power density shown on the x-axis of Fig. 3. (d) is the quiescent power dissipation contributing to the self-heating. Using this technique, the ELO devices exhibit a thermal resistance of 8.5 mK·cm^2/W, which is approximately 30% lower than that of the GaN-on-GaN control devices (12.4 mK·cm^2/W).

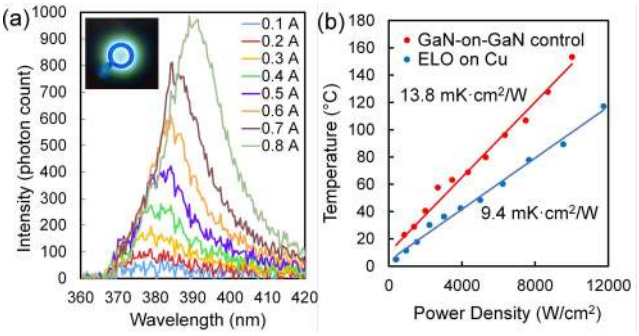

Fig. 4. (a) Electroluminescence intensity vs. wavelength for a 160 μm ring contact p-n diode at different bias currents; the inset shows a device with light emission. (b) Device temperature inferred from the peak of the electroluminescence vs. applied power for control and ELO devices.

Electroluminescence measurements were also performed to provide another estimate of the thermal resistance. As shown in Fig. 4. (a), electroluminescence spectra were measured over a range of applied forward bias currents using an Ocean Optics USB2000+ spectrometer. The junction temperature was then extracted by using the variation of band gap with temperature, as estimated from the peak of the emission [27]. An extracted thermal resistance of 9.4 mK·cm^2/W was obtained for the ELO devices, vs. 13.8 mK·cm^2/W for the control devices (Fig. 4. (b)). These results are in good agreement with the electrical characterization approach. In addition, these thermal resistances are broadly consistent with the thermal resistance estimated from analytical calculations using the thermal conductivity of GaN reported in [28].

IV. Conclusion

High performance vertical GaN p-n diodes fabricated using ELO by band gap selective PEC wet etching from bulk GaN substrates and bonding to Cu carrier wafers have been demonstrated. The p-n diodes obtained V_{br} of 1.3 kV with an R_{on} of 0.2-0.5 m$\Omega \cdot$ cm^2 (giving a Baliga figure of merit of 3.4-8.5 GW/cm^2). Compared with GaN-on-GaN control diodes without ELO processing, the electrical performance for the ELO devices was nearly unchanged, while the thermal resistance is reduced by more than 30%. No degradation in the SRH-regime performance was observed in the ELO devices, suggesting that ELO processing does not introduce additional defects in the material. Epitaxial lift-off of vertical GaN-on-GaN diodes may contribute to the development of GaN-based thin-film optoelectronics, power electronics, and flexible electronics/optoelectronics for wearables and medical applications.

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