Higher-order Incremental Delta-Sigma Analog-to-Digital Converters

Summary of the Original Contributions of the PhD Thesis

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1 Introduction

Analog-to-digital conversion, which takes continuous-time, continuous amplitude signals (voltage, temperature, sound, etc.) and converts them into a series of numbers to be used for digital signal processing, is becoming the key element of the scholarly and industrial applications of measurement and data acquisition, and A/D converters are surrounding (though invisible in most cases) also our everyday life.

The requirements of different A/D converters used in various applications are usually contradicted by each other: high resolution and high bandwidth indicates more complex hardware, which should have low power- and area-consumption (especially for portable, battery-operated equipment), and should have great tolerance on environmental effects (noise, temperature, etc.) at the same time. In addition, today's trend in system design is that the analog and mixed-signal interfaces are integrated into the same integrated circuit (IC) as the digital signal processing units (System-on-a-Chip, SoC design). This gives two serious limitations on high-resolution classical A/D converter design: first, in today's widely used low-voltage CMOS digital circuit implementation technology it is not possible to manufacture high-precision analog elements (resistors, capacitors, etc.) on which Nyquist-rate converters rely so much. Second, in such an integrated environment, designers have to deal with the switching-noise interference originating from the high-speed clock signal of the digital circuits. In general, as matching of analog elements cannot be made better than 0.1% (which indicates a signal to mismatch error ratio of 1000, equivalent to about 10-bit resolution), classical Nyquist-rate converters with resolution greater than about 12 bits can be manufactured either with individual (and thus expensive) laser wafer trimming or has to be designed with sophisticated on-line or off-line self-calibration methods.

One possible solution to these problems is using an A/D converter based on Delta-Sigma ($\Delta\Sigma$) or Sigma-Delta modulation, especially if its analog circuitry is implemented by using switched capacitor (SC) technique.

Using switched capacitor circuit has two advantage. First, in an SC circuit the information is not stored in continuous signals such as current or voltage, but in charge delivered in a given time interval, which is much less sensitive to the pulse-like noise originates from the high-speed switching of the associated digital circuitry. Second, in a SC circuit the cut-off frequencies, gains, etc., are realized by capacitor ratios with mismatch error as good as 0.1% in a CMOS IC, while using classical RC technology the error of the cutoff frequency due to the mismatch of the elements may reach even 20% [JM97, Ch. 10].

The advantage of using $\Delta\Sigma$ modulation in the converter compared to those operated at the Nyquist-rate is that the required resolution is not achieved by relying on precise analog circuit elements, but using *oversampling* and *noise-*

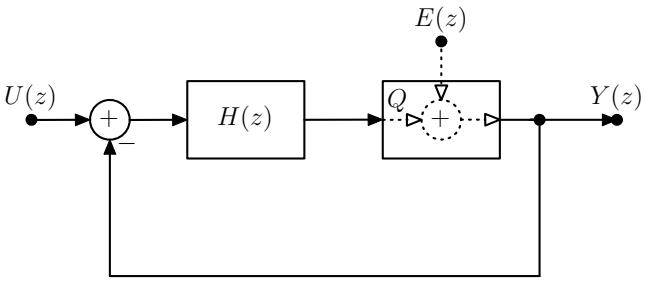

Figure 1: Simplified z-domain model of a $\Delta\Sigma$ converter. Dashed lines show the additive noise model of the quantizer (Q). $Y(z)$, $U(z)$, $E(z)$ and $H(z)$ is the z-transform of the output signal, the input signal, the additive noise signal and the transfer function of the converter's loop filter, respectively.

shaping. Oversampling means that the sampling rate of the converter is much higher than twice the bandwidth of the input signal, while noise-shaping is a technique, which (high-pass) filters the (usually low-resolution) quantization error of the quantizer in the $\Delta\Sigma$ loop [NST97, Sec. 1.2]. This oversampled signal is converted back to Nyquist-rate samples by digital low-pass filtering and downsampling (*decimation*) [NST97, Sec. 1.3].

Fig. 1 shows the z-domain model of a general $\Delta\Sigma$ A/D converter [NST97, Sec. 1.2]. Utilizing the additive noise-model of the quantization error (see, e.g., [NST97, Sec. 2.3]), one can get the approximate linear model of the original nonlinear circuit, from which the following input-output relationship can be derived:

$$Y(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z), \tag{1}$$

where $Y(z)$, $U(z)$, $E(z)$ and $H(z)$ is the z-transform of the output signal, the input signal, the additive noise signal and the transfer function of the converter's loop filter, respectively.

Based on this equation, it can be easily shown that if the input signal bandwidth (B) is much smaller than the system sampling rate (f_s), and the loop filter gain is high in the band of interest (B), while otherwise small (i.e., the filter is integrating or low-pass type), then in the band of interest $H(z)/(1+H(z)) \approx 1$ and $1/(1+H(z)) \approx 0$, while at high frequencies $1/(1+H(z)) \approx 1$. This means that the output contains the input signal without any significant changes, while the quantization noise at low frequencies is negligible, and it shows up at higher frequencies (noise-shaping). Using adequate (low-pass) digital filter and downsampling, the input signal with high signal to quantization noise ratio can be reconstructed from the output signal. Since these conclusions are derived from the linear model of a non-linear system, in the real architecture other problems

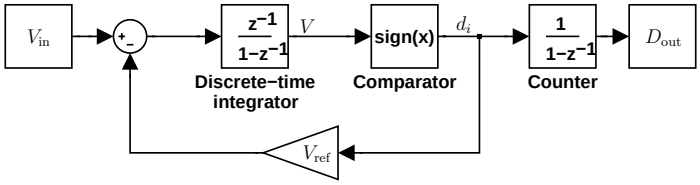

Figure 2: First-order incremental $\Delta\Sigma$ converter. V_{in}, V_{ref} and V is the input signal, the reference signal and the output of the analog integrator, respectively. d_i is the output of the modulator in cycle i, while D_{out} is the converted digital signal at the end of the conversion.

may arise (stability, non-uniform quantization error, limit cycles, etc.), which are not addressed here.

In the PhD thesis I examine such analog-to-digital converter structures which give optimal trade-off between circuit complexity and conversion efficiency in a given application area (conversion of signals with high dynamics and low frequency, e.g., pressure sensors, weight scales, temperature measurement), and their tolerance on circuit element mismatches is also great. According to this, the thesis discusses the theoretical problems and design issues of high-precision, transient operation DC-measuring $\Delta\Sigma$ A/D converters.

1.1 High Precision Incremental $\Delta\Sigma$ Structures

In instrumentation and measurement, there is a growing demand for A/D converters with low or medium bandwidth, but with high absolute accuracy (e.g., sensors, DC-measurement applications). High linearity and small offset are also among the requirements, as well as small power-consumption and low sensitivity to environmental noise (such as the periodic noise coupled from the mains or digital switching noise). Manufacturing classical Nyquist-rate converters with resolution higher than 16 bits is very expensive and requires individual trimming. Nevertheless, $\Delta\Sigma$ A/D converters used in commercial and professional audio or in telecommunication applications cannot deal with the low DC-offset requirement and they usually cannot be applied for the conversion of signals around DC.

One solution to the problem is the incremental (or charge-balancing) $\Delta\Sigma$ converter [RTV$^+$87], which is basically a first-order $\Delta\Sigma$ A/D converter, operated in transient mode (Fig. 2). The converter represents a hybrid between the classical dual-slope converter [vdP94] and the $\Delta\Sigma$ one. Its operation is similar to that of the dual-slope converter, the only difference is that in a dual-slope converter the integration of the unknown and the reference voltage are followed by each

other, while here the two integration are interwoven in time. Nevertheless, the converter structure is similar to that of a first-order $\Delta\Sigma$ converter, but there are significant differences in its operation: (i) the converter operates in transient mode, up to N cycles; (ii) at the beginning of a new conversion, both the analog and the digital memory elements (integrators) must be reset; (iii) the digital (decimation) filter can be realized with a much easier structure than in the case of a $\Delta\Sigma$ modulator.

Among the advantages of the converter is that its analog and digital hardware is easy to realize, there is no need of precise analog components, its operation can be easily extended to bipolar operation even with single reference and its area- and power-consumption is also very moderate [RTV$^+$87].

The main disadvantage of the converter is that to achieve a given resolution (n_{bit}), the converter must be operated through $N = 2^{n_{\text{bit}}} + 1$ cycles, thus, its conversion rate is very slow compared to its clock frequency.

During my research, I was looking for such $\Delta\Sigma$ structures which keep most of the advantages of the introduced converter, while operate more efficiently. The main motivation of the research was given during my 14 months stay at Oregon State University, OR, USA, under the supervision of Gabor C. Temes. In 2001, an IC manufacturer asked our mixed-signal research group to develop a DC measurement A/D converter capable of at least 20 bit resolution. This project gave the initial impulse of the long research and development process, whose theoretical results are summarized in this thesis.

2 Research Methods

In my PhD thesis, theoretical operation and practical applications of analog-to-digital converters are examined. In general, in the analysis of such a functional circuit, first usually the ideal model of the circuit is set up, which can be used to verify the expected operation. Then, different non-ideal effects (noise, non-linearity, mismatch errors, offset, etc.) may be analyzed and included into the model one-by-one.

A/D converters are special circuits from many aspects, since due to their function, half of the circuit may be described as continuous-time system, while the other half of the circuit can be modeled as discrete-time system. The two parts are connected by the one or more bit quantizer, which is a strong non-linearity in the system. In the case of $\Delta\Sigma$ converters, the analysis is even harder, since the continuous and discrete parts, along with the low-resolution quantizer are placed into a loop with negative feedback. Due to the complexity of such converters, a general exact method which proves the stability of such a system for arbitrary input signal is still not available.

Due to the lack of exact mathematical analysis, usually the additive noise

model of the quantization error is used. Since this way the nonlinear element of the circuit is replaced by a linear noise source, linear system analysis tools may be used. The analysis is even more easier if the analog part of the circuit is realized with switched capacitor circuit, since in this case the whole system may be described using discrete-time system analysis methods. The problem using this technique is the limitation of the model, since the additive noise model is only conditionally valid for the low-resolution quantizer in the modulator. Despite of its limitations, the model is still useful for the evaluation of the circuit's expected operation and first-order effects of non-idealities.

Another limitation of the discrete-time model is that in a switched capacitor circuit, the system may contain delays which equal to half (or quarter) of the basic sampling rate, which cannot be taken into account in a simple discrete-time model. One possible solution is to model the circuit with multiple sampling rate (double-sampling), using exact time-domain analysis or using modeling tools developed for switched-capacitor circuit analysis (e.g., SwitCap).

According to the limitations of the methods described above (absence of exact analysis, limited modeling possibilities), the theoretical results must be accompanied with and verified by simulations. For (numerical) behavioral modeling, several programming languages and simulation environments are available. One of the most prevalent environment in scholarly applications is the MATLAB and the Simulink environment built onto it. Several $\Delta\Sigma$ modulator design and simulation toolboxes have been developed for these program families. At circuit level, one can use the SwitCap tool developed for ideal switched capacitor circuits, and to model implementation-related problems, transistor and layout-level simulation is also possible.

After the circuit is verified by simulation, the next step is to build the actual converter and support the theoretical results with measurements made on the real circuit.

According to the discussion above, during my research, I analyzed the discrete-time linear system originated from the original structure, in the time-, discrete radian- and z-domain by using the additive noise model of the quantizer error. In same cases, I also used exact time-domain analysis of the original nonlinear circuit. The theoretical results were verified by simulations. Based on these results, an integrated circuit has also been manufactured. Measurements made on this circuit support the theoretical results.

3 Summary of the Original Contributions

The new scientific statements concern the design theory of incremental $\Delta\Sigma$ A/D converters. The achieved results are collected into three statements.

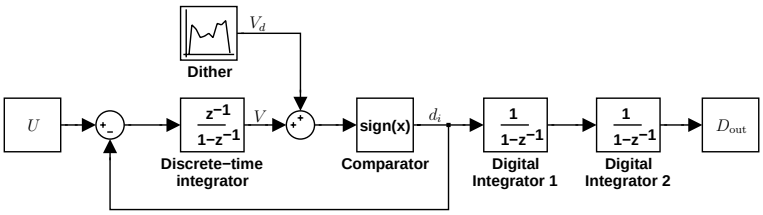

Figure 3: First-order incremental converter with second-order digital filter and dither signal injected into the loop.

Statement 1: I have modified the first-order incremental A/D converter by adding one more digital integrator at the output and injecting dither signal in front of the quantizer. I have analyzed the structure in detail and I have proven that it is more efficient than the original one.

The modified structure is shown in Fig. 3.

Statement 1.1: *I have shown that in the new structure much less cycles are required to achieve a given resolution at the expense of the added complexity. The required number of cycles (N) can be calculated as follows:*

$$N \geq 3.9 \cdot 2^{\frac{2n_{\text{bit}}}{3}}, \tag{2}$$

where n_{bit} is the required resolution in bits.

Statement 1.2: *I have derived the quantization error ($q[N]$) of the output signal for zero input signal analytically:*

$$q[N] = \pm\frac{1}{N+1}, \tag{3}$$

without dither signal, while

$$q[N] = \frac{2}{N+1}\frac{1}{N}\sum_{i=0}^{N/2}\text{sign}(V_d[2i]), \tag{4}$$

with dither signal, where $V_d[2i]$ is the $(2i)$th sample of the injected dither signal. Based on this result, I have shown that the quantization error around zero fulfills the specified accuracy if dither signal is used in the loop.

Since the quantizer in the loop may saturate for large input signals due to the presence of the dither signal, either the input signal or the dither signal must be limited. The next statement is about efficient methods to limit these signals.

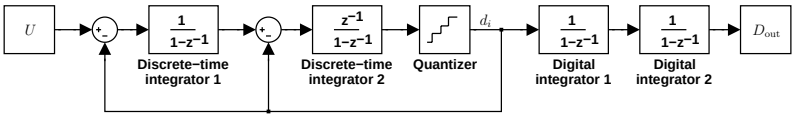

Figure 4: A possible realization of an incremental converter consists of a second-order modulator with pure differential noise transfer function ($NTF = (1-z^{-1})^2$) and same-order digital Cascade-of-Integrators filter.

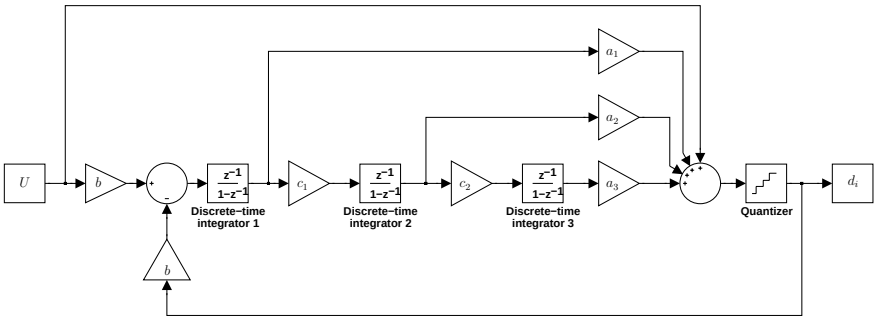

Figure 5: Third-order Cascaded-Integrators, Feed-Forward (CIFF) $\Delta\Sigma$ modulator architecture, with additional feed-forward path from the input signal to the input of the internal quantizer.

Statement 1.3: *To avoid saturation problems, I have suggested using either efficient scaling of the input signal, or three-level quantizer in the loop to decrease the amplitude of the required dither signal.*

More details and proofs of Statement 1 can be found in Sections 3.1 and 5.2 of the thesis, as well as in publications [3, 12].

Statement 2: I have extended the original first-order incremental converter to higher-order $\Delta\Sigma$ modulators and showed that the new architecture requires significantly less cycles to achieve a given resolution.

I proposed two different extensions. The first extension can be used for modulators with pure differential noise transfer function ($NTF = (1 - z^{-1})^{L_a}$, where L_a is the order of the modulator) shown in Fig. 4, while the other extension applies to modulators which have stabilized noise transfer function ($NTF = (1 - z^{-1})^{L_a}/D(z)$), and are realized by the Cascaded-Integrators, Feed-Forward (CIFF) architecture, with a feed-forward path from the input signal to the input of the internal quantizer (Fig. 5).

Statement 2.1: *I have derived that in the case of pure differential NTF, the quantization error of the converter is linearly related to that of the internal quantizer in the Nth cycle, if the digital filter following the modulator is an L_ath-order Cascade-of-Integrators filter, where L_a is the order of the analog modulator (cf. Fig. 4). The required number of cycles (N) to achieve a given resolution (n_{bit}) can be calculated from the following equation:*

$$\prod_{i=0}^{L_a-1}(N+i)=\frac{2^{n_{\mathrm{bit}}}L_a!}{(l-1)U_{\max}}, \tag{5}$$

where L_a is the order of the modulator, $U_{\max}$ is the normalized maximum input signal and l is the number of levels in the internal quantizer.

Additional advantage of the proposed structure is that its final quantization error can be modeled as a stochastic signal with uniform distribution, while the distribution of the quantization error of further proposed structures is approximately Gaussian.

I have also examined the case when the output digital filter consists of L_a+1 digital integrators. In this case, however, similarly to the first-order one (cf. Statement 1), dither signal is also required, and the structure is efficient for high resolutions only.

Statement 2.2: *I have derived that using CIFF architecture, the digital output may be calculated without knowing the value of the coefficients in the analog loop, i.e.,*

$$D_{\mathrm{out}}=\frac{1}{\binom{N}{L_a}}\underbrace{\sum_{k_{L_a}=0}^{N-1}\sum_{k_{L_a-1}=0}^{k_{L_a}-1}\cdots\sum_{k_1=0}^{k_2-1}}_{L_a}d_{k_1}, \tag{6}$$

where D_{out} is the digital output, N is the number of cycles the converter operates, L_a is the order of the analog modulator and d_{k_1} is the output of the modulator in the k_1th cycle.

Based on this result, I have proven that the quantization error of the converter is linearly related to the output of the last analog integrator in cycle N, if the digital filter following the modulator is an L_ath-order Cascade-of-Integrators filter. The required number of cycles (N) for a given resolution (n_{bit}) can be calculated from the following equation:

$$\prod_{i=0}^{L_a-1}(N-i)=\frac{2^{n_{\mathrm{bit}}}L_a!}{U_{\max}\left(\prod_{i=1}^{L_a-1}c_i\right)b} \tag{7}$$

where L_a is the analog modulator order, $U_{\max}$ is the normalized maximum input signal, and c_i and b are scaling coefficients in the loop (cf. Fig. 5).

Statement 2.3: *I have proven that by realizing a modulator with pure differential NTF using CIFF architecture, the following relationship is true for the quantization error of the converter (q), the output of the last integrator (V_{L_a}) and the error of the internal quantizer (ε):*

$$-V_{L_a}[N + L_a] = \varepsilon[N] = 2V_{\text{ref}}q[N], \tag{8}$$

i.e., in this case the two extensions are equivalent.

Statement 2.4: *I have proven that the introduced converter structure is capable of reducing input noise significantly. If the input noise variance is σ_g^2, then its contribution to the output noise variance (σ_y^2) in second-order case*

$$\sigma_y^2 < \frac{4}{3}\frac{\sigma_g^2}{N}, \tag{9}$$

while in third-order case

$$\sigma_y^2 < \frac{9}{5}\frac{\sigma_g^2}{N}, \tag{10}$$

where N is the number of cycles the converter operates.

Detailed discussion of the results of Statement 2 can be found in Sections 3.2, 4.1.1 and 5.3 of the thesis, and also in the publications [3, 7, 9, 14].

Statement 3: I have designed optimal higher-order digital sinc**-filters for higher-order incremental $\Delta\Sigma$ converters for suppression of periodic noise disturbances.**

Statement 3.1: *I have shown that either same-order ($L_d = L_a$, where L_d is the order of the digital* sinc*-filter, while L_a is the order of the analog modulator) or higher-by-one order ($L_d = L_a + 1$) digital* sinc*-filter gives an optimum between periodic noise suppression and the required number of cycles.*

Statement 3.2: *I have derived the required number of cycles (N) for converters with pure differential NTF. In the case of third-order modulator and third-order* sinc*-filter,*

$$N = 3N_3, \tag{11}$$

where

$$N_3 = \sqrt[3]{\frac{2^{n_{\text{bit}}+3}}{U_{\max}(l-1)}}, \tag{12}$$

where n_{bit} is the resolution, $U_{\max}$ is the normalized maximum input signal, while l is the number of levels in the internal quantizer.

In the case of third-order modulator and fourth-order digital filter

$$N = 4N_4, \tag{13}$$

where

$$\sqrt[3.5]{\frac{3\sqrt{6}\cdot 2^{n_{\mathrm{bit}}}}{U_{\max}(l-1)}} < N_4 < N_3. \tag{14}$$

Statement 3.3: *I have derived the required number of cycles for a given resolution for 1-bit, stabilized CIFF modulators. The required number of cycles (N) in the case of third-order modulator and third-order* sinc*-filter (assuming that $N_{3,p} \gg m$, which is fulfilled if the resolution is higher than 12 bit):*

$$N = 3N_{3,p} + m, \tag{15}$$

where m is the length of the transient of the stabilizer poles in the system, while

$$N_{3,p} = \sqrt[3]{\frac{2^{n_{\mathrm{bit}}+3}}{bc_1c_2U_{\max}}}, \tag{16}$$

where n_{bit} is the resolution, $U_{\max}$ is the maximum input signal, while b and c_i are scaling coefficients in the loop.

In the case of third-order modulator and fourth-order sinc*-filter, applying the same conditions,*

$$N = 4N_{4,p} + m, \tag{17}$$

where m is the length of the transient of the stabilizer poles in the system, while

$$N_{4,p} > \sqrt[3.5]{\frac{2^{n_{\mathrm{bit}}}\sqrt{20}}{bc_1c_2U_{\max}}\sqrt{\frac{\left(\sum_{i=1}^{m} w_d[i]\right)^2}{\sum_{i=1}^{m} w_d[i]^2}}}, \tag{18}$$

where $w_d[i]$ is the ith sample of the impulse response of the stabilizer poles of the system, while the other parameters are the same as in the previous case.

Detailed discussion of the results of Statement 3 can be found in Sections 4.2 and 5.3 of the thesis, as well as in the publications [3, 7, 14].

4 Applications of the Results

The results of the research are used in two different fields of electrical engineering. During the first period of my research, a toolbox for A/D converter testing has been developed [16]. The program is used by the international community, through the EUPAS (European Project for ADC Standardization) project. Additionally, further co-operation has been formed with the Lawrence Livermoore National Laboratory (LLNL, USA). Note that the international interest of the toolbox is supported by the fact that during the last 4 years I have found in various conference proceedings and periodicals seven independent citations of my publications regarding to the software tool ([1, 2, 5, 6]).

The results achieved in the topic of incremental converters has been utilized in a design co-operation between Oregon State University and Microchip Technology Inc. Based on the theoretical results, a 22-bit DC-measuring A/D converter has been designed and fabricated. Another fruit of the co-operation was a circuit-level implementation patent [9].

5 Publications Related to the PhD Thesis

5.1 Papers in Periodicals in English

[1] J. Márkus and I. Kollár, "Standard environment for the sine wave test of ADC's," *Special Issue on ADC Modeling and Testing of the Measurement Journal*, vol. 31, no. 4, pp. 261–69, June 2002.

[2] T. Z. Bilau, T. Megyeri, A. Sárhegyi, J. Márkus, and I. Kollár, "Four-parameter fitting of sine wave testing results: Iteration and convergence," *Computer Standards and Interfaces*, vol. 26, no. 1, pp. 51–56, Jan. 2004.

published also: in *Proceedings of the 4th International Conference on Advanced A/D and D/A Conversion Techniques and their Applications; 7th European Workshop on ADC Modelling and Testing (ADDA-EWADC 2002)*, Prague, Czech Republic, 26–28 June 2002, pp. 185–190.

[3] J. Márkus, J. Silva, and G. C. Temes, "Theory and applications of incremental delta-sigma converters," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 51, no. 4, pp. 678–690, Apr. 2004.

[4] J. Márkus and I. Kollár, "On the monotonicity and linearity of ideal radix-based A/D converters," *IEEE Transactions on Instrumentation and Measurement*, 2005, accepted for publication.

5.2 Papers in International Conference Proceedings

[5] I. Kollár and J. Márkus, "Sine wave test of ADC's: Means for international comparison," in *Proceedings of the IMEKO TC4 5th European Workshop on ADC Modelling and Testing (EWADC)*, P. Daponte, L. Michaeli, M. N. Durakbasa, and A. Afjehi-Sadat, Eds., Vienna, Austria, 24–26 June 2000, pp. 211–16.

[6] J. Márkus and I. Kollár, "Standard framework for IEEE-STD-1241 in MATLAB," in *Proceedings of the IEEE Instrumentation and Measurement Technology Conference (IMTC'2001)*, vol. 3, Budapest Convention Centre, Budapest, Hungary, 21–23 May 2001, pp. 1847–52.

[7] J. Márkus, J. Silva, and G. C. Temes, "Design theory of high-order incremental converters," in *Proceedings of the IEEE International Symposium on Intelligent Signal Processing (WISP'2003)*, Budapest, Hungary, 4–6 Sept. 2003, pp. 3–8.

[8] J. Márkus and I. Kollár, "On the monotonicity and linearity of ideal radix-based A/D converters," in *Proceedings of the IEEE Instrumentation and Measurement Technology Conference (IMTC'2004)*, vol. 1, Como, Italy, 18–20 May 2004, pp. 696–701.

5.3 Foreign Patent

[9] G. C. Temes, J. Silva, and J. Márkus, *Switched Capacitor Signal Scaling Circuit*, Assignee: Microchip Technology Inc., Mar. 2004, US patent application, filed on March 23, 2004.

5.4 Presentations at Hungarian Conferences

[10] J. Márkus, "Sine wave test of analog to digital converters," in *Proceedings of the 7th PhD Mini-Symposium.* Budapest, Hungary: Budapest University of Technology and Economics, Department of Measurement and Information Systems, 27–28 Jan. 2000, pp. 24–25.

[11] J. Márkus, "A MATLAB tool to use and test the ADC-standard," in *Proceedings of the 8th PhD Mini-Symposium.* Budapest, Hungary: Budapest University of Technology and Economics, Department of Measurement and Information Systems, 31 Jan. – 1 Feb. 2001, pp. 26–27.

[12] J. Márkus, "Enhancing the resolution of incremental converters with dither," in *Proceedings of the 10th PhD Mini-Symposium*. Budapest, Hungary: Budapest University of Technology and Economics, Department of Measurement and Information Systems, 4–5 Feb. 2003, pp. 38–39.

[13] J. Márkus, "Monotonicity of digitally calibrated cyclic A/D converters," in *Proceedings of the 11th PhD Mini-Symposium*. Budapest, Hungary: Budapest University of Technology and Economics, Department of Measurement and Information Systems, 3–4 Feb. 2004, pp. 8–9, (Best presenter's award in the category of third-year PhD students).

5.5 Other Works

5.5.1 Technical Reports

[14] J. Márkus, J. Silva, and G. C. Temes, "20-bit delta-sigma ADC system design progress report," Oregon State University, Tech. Rep., Aug. 2001, 15 p.

[15] J. Márkus, "A comparison of DAC-error calibration algorithms," Oregon State University, Tech. Rep., Sept. 2002, 34 p.

5.5.2 Software with User's Manual

[16] J. Márkus, *ADC Test Data Evaluation Program for Matlab*, Budapest University of Technology and Economics, Department of Measurement and Information Systems, URL: http://www.mit.bme.hu/projects/adctest/, 2002.

5.6 Publications Not Directly Related to the PhD Thesis

5.6.1 Papers in Periodicals

[17] János Márkus and Gabor C. Temes, "An efficient delta-sigma ADC architecture for low oversampling ratios," *IEEE Transactions on Circuits and Systems I. – Special Issue on Advances on Analog-to-Digital and Digital-to-Analog Converters*, vol. 51, no. 1, pp. 63–71, Jan. 2004.

[18] Balázs Bank, János Márkus, Attila Nagy, and László Sujbert, "Signal- and physics-based sound synthesis of musical instruments," *Periodica Polytechnica, Ser. Electrical Engineering*, vol. 47, no. 3–4, pp. 269–295, 2004.

5.6.2 Papers in Conference Proceedings

[19] János Márkus and László Sujbert, "Signal model based synthesis of the sound of organ pipes," in *Proceedings of the International Békésy Centenary Conference on Hearing and Related Sciences*, Budapest, Hungary, 24–26 June 1999, pp. 194–199.

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