Highly Adaptive Transducer Interface Circuit for Multiparameter Microsystems

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***Abstract*—A reconfigurable transducer interface circuit that combines the communication and signal conditioning necessary to link a variety of sensors and actuators to a microsystem controller is reported. The adaptive readout circuitry supports high-resolution signal acquisition from capacitive, resistive, voltage and current mode sensors with programmable control of gain and offset to match sensor range and sensitivity. The chip accommodates sensor self test and self calibration and supports several power management schemes. It provides digital and analog outputs to control actuators and a standard interface to peripheral components. The 2.2×2.2 mm CMOS chip was fabricated in 0.5-μm, 3-metal, 2-poly process, dissipates ~ 50 μW at 3.3 V in a typical multisensor application utilizing periodic sleep mode, and can read out a wide range of sensors with high sensitivity. A prototype microsystem with a microcontroller and MEMS pressure, humidity, and temperature sensors has been implemented to characterize interface chip performance.**

***Index Terms*—Adaptive circuits, microsystem, sensor interface.**

I. Introduction

MULTI-PARAMETER microsystems take advantage of the diversity of miniature sensors available through microelectromechanical systems (MEMS) and nanoscale technologies to realize highly integrated systems, combining various transducers with interface, signal processing, and communication electronics [1]–[3]. The transducer interface circuitry plays a very important role in such systems, extracting useful data from a variety of device types (resistive, capacitive, etc.) that can vary widely in range and sensitivity. In the trend to develop so-called *smart sensors*, interface circuits have taken many different configurations. Most have been tailored to specific sensors, achieving high performance by precisely addressing a limited set of requirements. The popularity of low-power capacitive sensors led to a variety of more versatile interface circuits capable of reading out a range of capacitive devices [4]–[8]. The drive to include more and more sensors within a microsystem has led to interface circuits that readout multiple types of sensor signals, particularly resistive and capacitive [9]–[11] or an even wider range [12]–[14]. System architecture also plays a big role in interface circuit configuration. Dedicated interfaces with point-to-point communication with an external system are very common. Some interfaces are formed monolithically with transducers [12], [15], while others have been developed using field programmable analog arrays [16]. As sensor networks have evolved, many interface circuit with extensive communication capabilities have been introduced [4], [5], [12] including some without sensor readout circuit [17], [18]. System architecture also dictates the signal processing capability required within interface circuits, and some sensor interfaces with full microprocessors have been developed [17], [19].

Of this wide range of sensor interface configurations, those with highly specialized capabilities and performance are well suited for large volume products, typically single parameter/sensor components for industrial and commercial applications. However, many emerging microsystems will require an assortment of sensors and actuators to construct highly functional systems for distributed measurement and control applications. In the near future, these microsystems are likely to be developed for low volume niche markets, where the cost to develop specialized sensor interfaces will be prohibitive [20]. An attractive example is low-power sensor networks, for which a wide range of microsystems will be needed to perform application specific tasks. Interface circuits with fixed architectures and capabilities are not well suited for these microsystems. Similarly, sensors that require significant in-node signal processing do not efficiently utilize the shared resources available in highly integrated microsystems. For these next generation microsystems, there is a significant need for a versatile sensor interface, suitable for use across many system platforms and tailored for operation within a low-power, multisensor environment.

In this paper, we address the challenges of identifying a single sensor interface chip that effectively resolves the tradeoffs between versatility and performance. Adopting a highly adaptive microsystem architecture, we have analyzed the interface chip functionality needed for a wide range of multisensor microsystems and determined the most valuable and feasible capabilities within the size and power limitations common to microsystems. The resulting universal microsensor interface (UMSI) is a highly configurable mixed-signal integrated circuit that implements a unique set of transducer interface features desirable for next generation multifunctional microsystems. The utility of this compact yet versatile interface facilitates the rapid development of many different microsystems without the time and cost of designing specialized sensor interface circuitry, providing new monitoring and control capabilities to a wide range of applications, including environmental oversight, industrial process monitoring, health care, and security.

This paper first describes the microsystem and interface chip architectures and the features they provide. The operation and capabilities of the chip's communication and control unit are then described. The design of the adaptive sensor readout block

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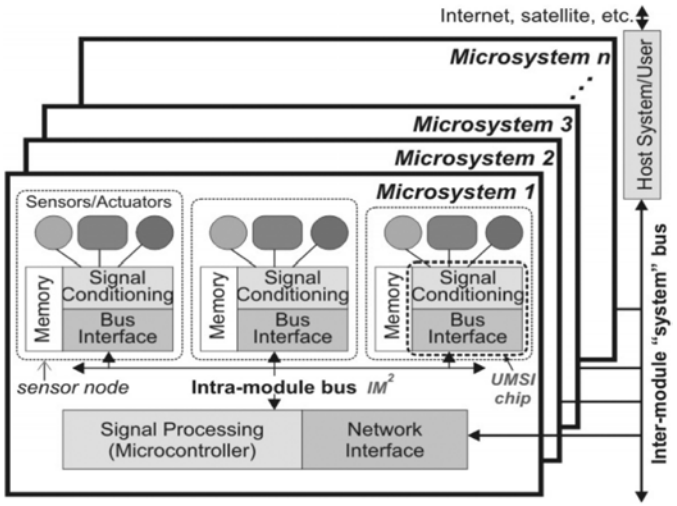


Fig. 1. Microsystem network architecture illustrating ideal locations for signal conditioning, signal processing and communication hardware.

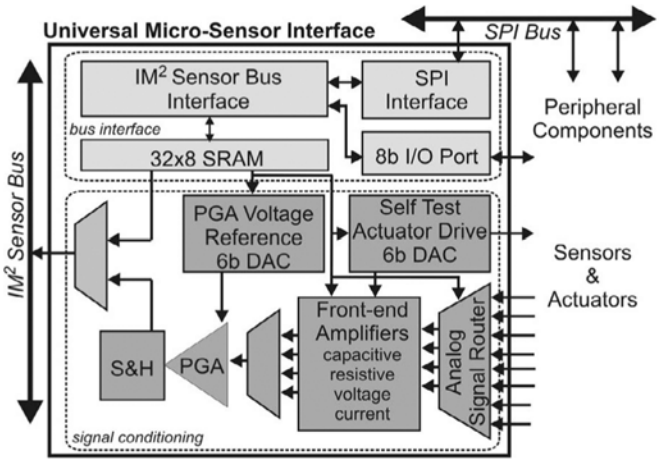


Fig. 2. Block diagram of the UMSI with optional external components within a sensor node module.

is then discussed. Finally, chip performance is reported, and an example microsystem implementation is described.

II. Microsystem and Chip Architecture

A. Microsystem Architecture

The architecture of the overall microsystem plays a significant role in determining the required functions and performance of the interface circuit. To support the collection of a wide array of transducers in a modular and flexible system, we adopted our multilayered network structure [21] shown in Fig. 1. This scheme is tailored to low-power microsystems where transducer data is transported through a series of increasingly sophisticated electronics and power hungry resources are shared among sensor nodes. Within each modular microsystem, an intramodule sensor bus links multiple sensor nodes to a centralized controller that, in turn, communicates with other microsystems or a host system using an application specific, hardwired or wireless, networking scheme. Front-end signal conditioning is preformed within each sensor node while higher level signal processing such as sensor fusion and digital calibration/compensation are managed by the microsystem controller. Data analysis, long-term storage, user access, and communication with other networks are provided by the host system.

The desired capabilities of microsystems within the network described by Fig. 1 impose many design requirements that must be supported by the sensor node interface circuitry. Although the interface needs of transducers vary widely, system requirements common to all sensor nodes advocate the use of a single, generic interface circuit that accommodates many different transducers to achieve significant advantages in terms of cost, system development time, and application adaptability. In addition to providing readout and control of a variety of transducers, the generic interface circuit must be low power and reliable to support long system life span. As a multiuse component, it must be able to adapt to a reconfigurable set of transducers and facilitate the expansion of its capabilities through a standard communication link, and it must enable sensor self test and self calibration. In short, it must combine many features of a traditional microcontroller with a versatile set of high-performance sensor readout circuits under the severely limited size and power constraints associated with microsystems.

B. Chip Functional Blocks

The UMSI chip was developed to provide a judiciously chosen set of signal conditioning and communication electronics that address the tradeoffs between features and performance common to multipurpose devices. Under constraints imposed both by transducers and microsystem architecture, our goal was to develop a universal interface chip that could be configured to support many different transducers with different signal conditioning needs, could be adapted to different applications without replacing interface hardware, and could accommodate the addition of peripheral devices to meet the needs of future microsystems. Through careful consideration of design tradeoffs between performance and versatility iterated over several generations of transducer interface circuits [4], [5], [13], the organization of functional blocks shown in Fig. 2 was determined to best meet these goals. A sensor bus interface block provides bidirectional communication with the microsystem controller over an intramodule microsystem (IM^2) sensor bus [21]. A built-in serial peripheral interface (SPI) can route bidirectional data between a selected peripheral device and the microsystem controller. An 8-bit input–output (I/O) port can be read or written through the sensor bus to control actuators or monitor digital outputs from sensors or other peripheral devices. The analog data path starts with a signal router that allows multiple sensor elements to be simultaneously connected to the UMSI chip. Sensor data is routed to the appropriate front-end amplifier block for gain and offset signal conditioning and conversion to a voltage signal. Two on-chip digital–analog converters (DACs) support sensor and circuit self test, provide a means for online calibration of the amplifier offset, and generate an analog output for actuator control.

TABLE I
COMPARISON OF FEATURES ON THE UMSI CHIP WITH REPORTED GENERIC/UNIVERSAL SENSOR INTERFACES

	Wouters '94 [9]	VDGoes '97 [11]	Yazdi '00 [4]	Chavan '99 [5]	Kraver '01 [19]	Chao '04 [14]	Mackensen '05 [16]	UMSI
multi-node bus interface			X	X	X			X
multi-sensor readout	X	X	X	X	X	X	X	X
readout signal mode	C, R	C, R	C	C, R	C, R, V, I	C, R, V	C, R, V, I	C, R, V, I
gain/offset configurable	?	?	X	X	X	~		X
self test	?	?	X	X				X
online calibration		X		X				X
actuator control				X				X
peripheral interface					X			X
plug-n-play (hot swap)					?			X
power management	X	X			X	?	~	X

Legend: X = included, ~ = partial, ? = undetermined

C. Features and Capabilities

The features and capabilities of the UMSI chip are described below and summarized in Table I, which compares UMSI to all known chips reported as universal or generic sensor interfaces. The UMSI chip offers the most extensive set of capabilities while being optimized for compact, low-power microsystems.

High-performance transducer interface is achieved primarily through the low noise, highly sensitive front-end readout circuits on the UMSI chip. Performance capabilities are further improved by the built-in mechanisms for self test of the sensor-circuit data path and self calibration of the readout circuit. Managed by calibration routines on the microsystem controller, UMSI hardware enables online test and adjustment of the readout chain, improving performance and reliability of the sensor node.

A key component of the UMSI chip is the sensor bus interface, which allows any UMSI-equipped sensor node to be employed within an intramodule multidrop network. The sensor bus allows sensor data to be uploaded to the controller as serial digital data, or buffered analog voltages can be transmitted to utilize the analog–digital (A/D) on the controller. Data downloaded from the controller identifies which sensor node is active, specifies which transducer within the sensor node is being addressed, and configures the analog portion of the chip by storing control parameters within the embedded SRAM. Up to eight sensor elements can be read out sequentially by circuits tailored to capacitive, resistive, current, and voltage mode signals. Reconfigurable gain and offset parameters allows each measurement to be matched to needs of individual sensor elements. Actuators within the sensor node can be activated and controlled by the 8-bit I/O port and 6-bit DAC on the UMSI chip. Thus, a total of 17 transducer elements can be managed by a single UMSI chip, linking these devices to the microsystem controller through a standard sensor bus that allows up to 255 sensor nodes per microsystem. The SPI expansion bus, digital I/O port, and reconfigurable sensor readout block were chosen to provide a highly adaptive sensor node interface that can easily support a variety of transducers and be expanded to meet the specific needs of many microsystem configurations and applications. This flexible, multiuse component can significantly reduce microsystem development time and facilitates quick and easy addition or exchange of transducers through a streamlined plug-n-play scheme supported by the IM^2 sensor bus and the UMSI chip.

Although there are many advantages to general purpose implementation, the size and power constraints inherent to microsystems require a strategic balance between flexibility and hardware minimization. By methodically analyzing this tradeoff, it was determined that the UMSI chip should contain only a carefully chosen adaptable hardware core for transducer interface, sensor node communication, and peripheral expansion, while maximizing utilization of microsystem controller resources common to all sensor nodes. For example, the IM^2 bus minimizes the communication hardware necessary within each sensor node and allows the A/D converter on the microsystem controller to be shared by all sensor nodes, thus minimizing overall microsystem power consumption and size. The UMSI chip also supports system-level power management schemes such as periodic low-power sleep modes and wake up based on sensor driven interrupts. Finally, power routing on the UMSI chip allows individual functional blocks to be activated by hardwired connections, minimizing UMSI power consumption based on application needs.

III. COMMUNICATION AND CONTROL

A. Communication Bus

The UMSI chip utilizes the IM^2 sensor bus [21] which has evolved from prior work with microsystems [1]. IM^2 is a hardware compatible extension of the IEEE P1451.2 Transducer Independent Interface (TII) [22] but relies on a modified protocol to support distributed multidrop sensor nodes. The bus consists of eight signal and three power lines whose functions are described in Table II. Applications that do not require some of the advanced feature support, such as sensor interrupts and new device detection/reconfiguration, can implement only a subset of the bus signals to reduce wiring complexity. The optional POWER2 signal accommodates power management schemes that require continuous power to monitor sensors for events during periodic power down of the sensor front-end.

Bidirectional serial communication between the microsystem controller and sensor nodes is achieved by the DIN, DOUT, DCLK, and NACK signals with NIOE delimiting the start and end of the communication, as defined in IEEE P1451.2. To support a multidrop network configuration, an additional chip ID

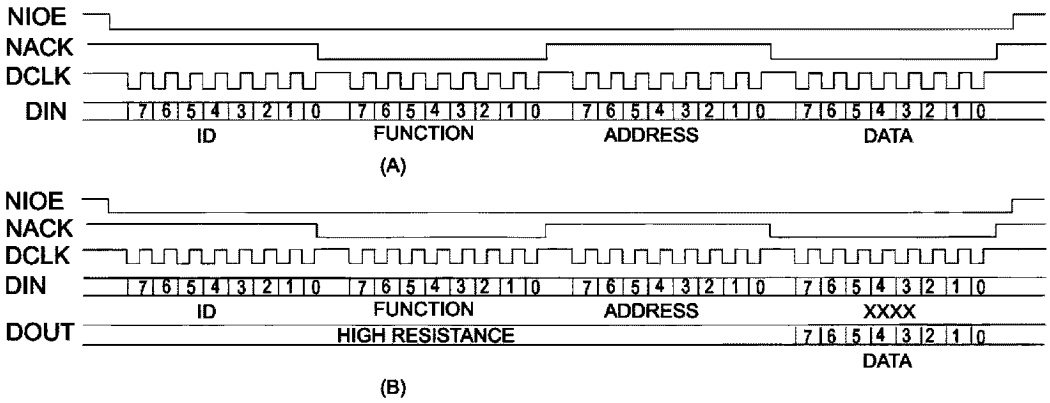


Fig. 3. Timing diagram in IM^2 bus protocol using the full 8-bit address mode. (a) Write data to sensor node. (b) Read data from sensor node.

TABLE II
IM^2 SENSOR BUS SIGNALS AND FUNCTIONS

Line	Description
DIN	Serial data line from microcontroller to the interface
DOUT	Data line from the interface to the microcontroller
DCLK	Positive edge clock latches data on DIN and DOUT
NIOE	Signals that the data transport is active and delimits the data frame
NTRIG	Performs triggering function
NACK	Trigger acknowledge and data transport acknowledge
NINT	Request service from the microcontroller
NSDET	Detect the presence of a new sensor node
COMMON	Reference voltage
POWER	"Always on" power supply. Used for the front-end components that cannot be switched off
POWER2	Controllable power supply and analog reference. Can be switched off to conserve power

byte is added to the IEEE P1451.2 data transport frame to identify an individual sensor node. The addressed sensor node receives the remainder of the message and acquires sole access to the DOUT line while all other nodes become inactive awaiting the beginning of the next communication cycle. The UMSI chip implements two addressing modes to minimize power consumption and communication time within a given microsystem configuration. The full address mode allows up to 255 sensor nodes within a microsystem. Fig. 3 shows a timing diagram for typical read and write operations using the IM^2 sensor bus. Bus protocol allows node IDs to be hardwired (defined by packaging) or determined by the microsystem controller and stored in a preset address of a peripheral memory component connected via the SPI bus on the UMSI chip. By including a memory component within the sensor node, sensor-specific parameters can be stored within the node and uploaded to the microsystem controller, similar to the transducer electronic data sheet (TEDS) described by the IEEE P1451 standard. The IM^2 bus accommodates sensor data in both analog and digital formats through the shared DOUT bus line, and a mixed-signal multiplexer on the UMSI chips ensures only the addressed node will drive the DOUT line.

In conjunction with a new device detection routine running on the microsystem controller, the UMSI uses the NSDET signal to implement a plug-n-play scheme wherein sensor nodes added

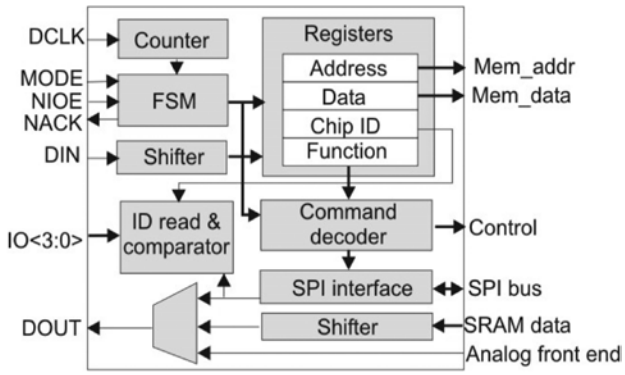


Fig. 4. Block diagram of the UMSI digital control circuit.

to or replaced within the system can be recognized and automatically configured during periodic resets or wake-ups of the sensor nodes. Sensor events can generate interrupts using the NINT signal, and the UMSI chip can manage up to four interrupt sources within each sensor node. This feature allows for sensor monitoring even during sleep mode, where the sensor node would wake up the system to handle the interrupt accordingly. NTRIG is included in the IM^2 bus to provide additional functionality and maintain hardware compatibility with the TII bus, but this signal is not utilized by the UMSI chip.

B. Digital Control

Compared to other multidrop sensor busses that require fewer signal lines, the IM^2 bus requires a relatively simple interface circuit, resulting in area and energy savings when multiple sensor nodes are employed within a microsystem. Fig. 4 describes the UMSI digital control circuit that interfaces to the IM^2 sensor bus, directs data to/from the on-chip memory and the digital I/O and SPI ports, and generates control signals to manage chip operation. The mode pin on the UMSI chip defines the addressing scheme, setting the node ID to either 4-bits or 8-bits. During communication, an 8-bit counter blocks off incoming bytes and drives a finite state machine (FSM) that dispatches message bytes to the appropriate register and assists in decoding the command byte. The chip ID of the incoming message is compared to the pre-assigned node ID to determine which sensor node is being addressed. If the IDs match, data and

control information are distributed to the appropriate UMSI circuit, and/or data is retrieved from the chip and uploaded to the microsystem controller, depending on the command. During a read command, the decoder controls a mixed-signal multiplexer to select output from memory, the analog front-end, the SPI bus, or the interrupt arbitration unit.

An embedded SRAM was implemented to store configuration parameters for the analog transducer interface circuits, providing dynamic reconfiguration of the amplifier gain and offset, DAC values, input sensor selection, etc. An 8-bit I/O port provides general purpose I/O, useful for controlling actuators or peripheral components. Four bits of this port also double as node ID inputs if hardwired addressing is utilized. The other four bits of the port double as chip select pins for the on-chip SPI port. The SPI port can accommodate additional components within the sensor node, thus allowing for expansion to support specific transducers while minimizing the core UMSI hardware requirements. When SPI mode is enabled by an IM^2 bus command, the microsystem controller is put in direct communication with a specific peripheral component within a specific sensor node. This feature can be used, for example, to upload sensor parameters for digital calibration from an external memory.

IV. Adaptive Analog Front-End

A. Architecture

In the UMSI chip, the analog front-end is responsible for linking a broad diversity of transducers to the microsystem controller through the sensor bus. A vast majority of state-of-the-art microsensors generate changes in capacitance or resistance that must be measured, amplified, and converted to signals useful to the overall microsystem. Many other sensors directly generate voltage or current outputs. The adaptive analog front-end was designed to accommodate all of these types of output signals, provide variable offset adjustment and gain settings to match the range and sensitivities of different sensor elements, implement self test and auto calibration capabilities, and control external actuators. These reconfigurable resources enable the UMSI chip to interface with multiple sensor types within a single sensor node, offering cost-effective support to a range of applications.

Fig. 5 shows the main functional blocks of the analog front-end. Based on data within a sensor bus read instruction, the analog signal router directs one of eight sensor inputs to the appropriate readout block. A low-noise charge integrator performs capacitive readout, a differential preamplifier interfaces with resistive sensor, and an attenuator adjusts the level of sensors with voltage output. The three readout blocks are connected to a programmable gain amplifier (PGA) and a sample-and-hold (S/H) circuit. An on-chip voltage reference generates a $V_{dd}/2$ analog ground for the amplifiers, and a multiphase clock generator produces nonoverlapping clocks for the switched capacitor circuits. A 6-bit DAC provides a programmable reference voltage for the PGA, and a second 6-bit DAC generates a signal that can drive an external actuator or supply a self test signal at the input of the amplifier chain. The UMSI chip also contains a current-mode interface that will not be covered in this paper. Many of the circuit operation parameters are controlled by data

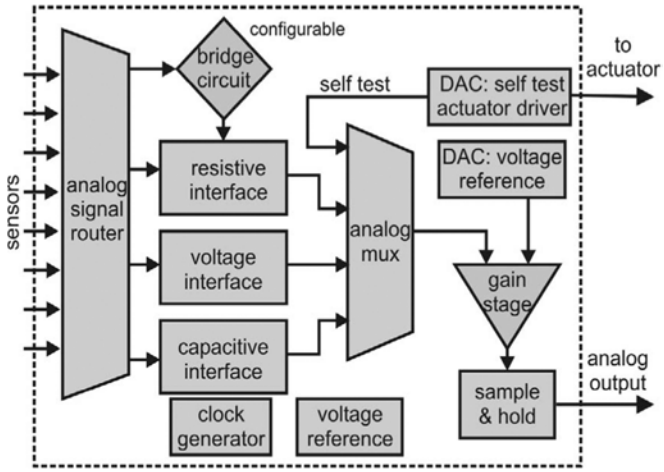


Fig. 5. Diagram of the mixed-mode multisensor readout circuit block.

TABLE III
Programmable Features of the UMSI Chip

Features	Signals/Bits
Analog Inputs	8, multiplexed to amps
Analog Output	6b DAC
Gain Amp: gain control	8b
Gain Amp: ref. Voltage control	6b DAC
Gain Amp: self-test input	6b DAC
Capacitive Amp: offset control	8b, 50 fF – 6.4 pF
Resistive Amp: reference	6b, 3.75 kΩ – 30 kΩ
Resistive Amp: gain control	6b
Voltage Buffer: attenuator	6b

stored in the embedded SRAM, which can be written by the microsystem controller via the sensor bus. The programmable features of the UMSI chip are summarized in Table III. The analog block also utilizes multiple power supplies to minimize power consumption by activating only the circuitry needed for a specific application.

B. Reconfigurable Sensor Readout

Configuration of sensor readout circuits is realized through binary-weighted programmable capacitors, binary-weighted programmable resistors, and various multiplexer selections. Configuration parameters can be stored on the microsystem controller and uploaded to the embedded SRAM before activating a specific readout channel for a specific sensor element. A 6-bit sensor mode register controls the 8-to-4 analog signal router to direct sensor outputs to the correct readout channel, selecting from up to eight capacitive inputs, up to four full-bridge (differential), half-bridge, or single-element resistive inputs, and up to eight voltage inputs. After pre-amplification and removal of offset (equivalent to adjusting for sensitivity and range) within a specific readout channel, final scaling is done in the PGA stage. The final output voltage is stored on a capacitor in the S/H stage and fed to an analog multiplexer controlling access to the sensor bus data output line. The design and operation of the readout blocks are detailed below.

1) Programmable Capacitive Readout: Readout of capacitive sensors typically utilizes a capacitance-to-frequency converter, a capacitive ac-bridge, or a switched-capacitor circuit.

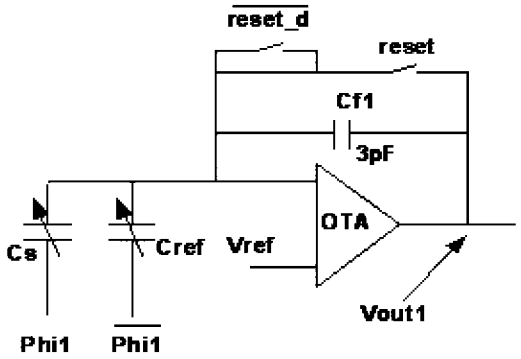


Fig. 6. Switched-capacitor integrator stage of the capacitive readout circuit.

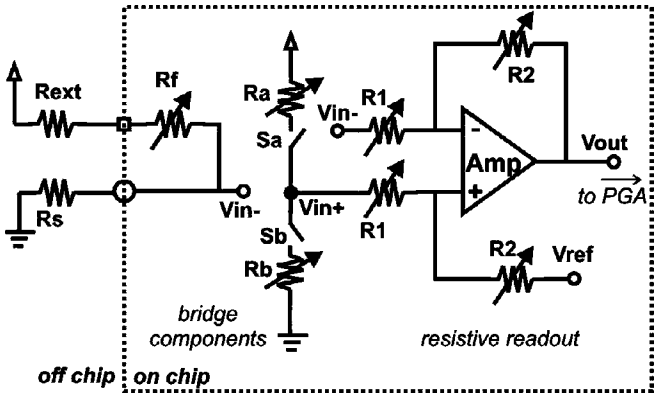


Fig. 7. Configurable resistive readout supporting full bridge, half-bridge, and single-element resistive sensors.

Capacitance-to-frequency conversion [23]–[25] requires only a simple oscillator circuit but is highly affected by parasitics, drift and temperature sensitivity. Proper design of switched-capacitor circuits, on the other hand, can eliminate these effects. This property, along with their high sensitivity, has made them very attractive for capacitive sensor readout [26]–[28]. A switched-capacitor front-end consisting of a low-noise charge integrator and a digitally programmable gain stage was developed for capacitance readout. The integrator stage shown in Fig. 6 includes a dummy switch to minimize clock switching noise and a large integrating capacitor (C_{f1}) to reduce thermal noise. An operational transconductance amplifier (OTA) with a high open loop gain is used so the output voltage will be insensitive to input parasitics and temperature drift, which can be significant sources of error in capacitive microsensors.

In Fig. 6, C_s is the selected sensor capacitor and $C_{\rm ref}$ is an on-chip, 8-bit programmable, binary-weighted, reference capacitor that can realize values from 50 fF to 12.75 pF. The programmable reference capacitor provides input offset control and allows the UMSI chip to match the nominal values of many capacitive sensors. An external capacitor can be used to match sensors with greater than 12.75-pF nominal value, with fine turning provided by the on-chip reference. The capacitors are connected to $\rm phi1$ and $\overline{\rm phi1}$ so that the net change in charge at the input is $(C_s - C_{\rm ref})(V_{dd} - V_{ss})$. This differential charge is transferred to the feedback capacitor C_{f1}, and the magnitude of the output voltage is proportional to the difference between the sensor and reference capacitors

$$V_{\rm out1} = V_{\rm ref} + (V_{dd} - V_{ss}) \cdot \frac{(C_s - C_{\rm ref})}{C_{f1}}. \qquad (1)$$

2) Programmable Resistive Readout: Resistive sensors are implemented in many different configurations; some have built-in full bridges, some have built-in reference elements forming a half-bridge, and others are single-element resistors. Several resistive readout circuits have been designed for sensor applications [29]–[31]. To achieve the flexibility of reading out all resistive sensor configurations, the configurable Wheatstone bridge interface shown in Fig. 7 has been developed. This circuit can accommodate full-bridge, half-bridge, and single resistor element sensors by reconfiguring on-chip programmable resistors to form a full-bridge for any input. An on-chip half-bridge contains two 3-bit (5–35 kΩ) binary-weighted programmable resistors. A second half-bridge is formed by the sensor resistance along with one on-chip 8-bit (50 Ω − 8.75 kΩ) tuning resistor and, if greater than 8.75 kΩ is required, an external resistor. If the sensor includes a full bridge, its two outputs are connected to $V_{\rm in}+$ and $V_{\rm in}-$ while switches Sa and Sb are turned off and the tuning resistor port is unconnected. If the sensor includes a half-bridge, Sa and Sb are turned on, Ra and Rb are set to values close to the sensor baseline resistance, and the sensor output is connected to $V_{\rm in}-$. This same configuration is used if the sensor is a single-element resistor, but an external matching resistor is added and the tuning resistor is used to accurately match the sensor resistance.

The bridge output voltage is applied to the input of a closed loop differential amplifier. The gain of this amplifier is given by the ratio of $R2$ to $R1$, where $R1$ and $R2$ are 2 and 4 bits, respectively, on-chip binary-weighted programmable resistors. The opamp used in this readout provides a high gain for precision, a large output voltage swing, and an output buffer to drive current into the resistive load. The output voltage for single resistive sensor readout can be expressed as

$$V_{\rm out} = V_{\rm ref} + \frac{\frac{R_a}{R_{\rm ref}} - \frac{R_b}{R_a}}{\left(1 + \frac{R_a}{R_{\rm ref}}\right)\left(1 + \frac{R_b}{R_a}\right)} \cdot V_{dd} \cdot \frac{R_2}{R_1}. \qquad (2)$$

In full-bridge and half-bridge configurations, the output voltage of resistive readout is given by

$$V_{\rm out} = V_{\rm ref} + (V_{\rm in-} - V_{\rm in+}) \cdot V_{dd} \cdot \frac{R_2}{R_1}. \qquad (3)$$

3) Voltage Interface: The voltage interface allows the UMSI chip to connect sensors with voltage-mode outputs, like many preconditioned commercial components, to the sensor bus. This front-end block serves as a unity gain buffer or it can attenuate sensor inputs to bring them within the voltage scale of the UMSI circuits, with gain provided by the PGA if necessary. The voltage readout circuit is shown in Fig. 8, where a 6-bit programmable resistive attenuator feeds the noninverting input of a

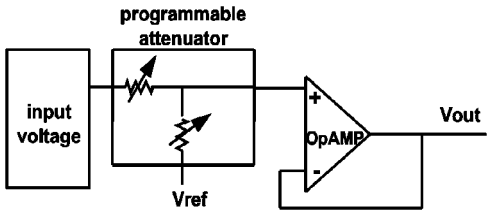


Fig. 8. Interface to voltage mode signals with optional attenuation by a programmable resistive network.

high-gain CMOS opamp. The opamp has the same characteristics as the resistive readout amplifier and is configured as a unity gain buffer such that

$$V_{\text{out}} = V_{\text{ref}} + k_v \cdot (V_{\text{in}} - V_{\text{ref}}) \tag{4}$$

where k_v is the gain of the programmable attenuator, which ranges from 0.125 to 1 V/V. This circuit accepts inputs within the 600-mV to 10-V range and provides a 60-μV resolution. This front-end block also permits self-test/self-calibration beyond the built-in capabilities by applying an external high-resolution DAC as a sensor input.

4) PGA and S/H: Each of the front-end transducer readout blocks generate a pre-amplified and offset adjusted voltage that is fed, through a 4:1 multiplexer, to the PGA stage. Because the PGA does not have to drive resistive loads, to save power it is formed using a switched capacitor topology. The PGA has a gain ranging from 0.035 to 31.75 V/V using on-chip binary-weighted 10-bit programmable capacitors. Online gain calibration of the PGA can be achieved by applying a known voltage to the input via the self test DAC. A second DAC at the PGA reference input allows offset voltage to be tested and tuned to improve the reliable lifetime of the interface circuit. The PGA output is stored on a capacitor in the S/H stage that drives sensor data onto the sensor bus for A/D conversion and, if necessary, digital calibration on the microsystem controller.

Fig. 9 shows the PGA and S/H stages. Combinations of C_{in} (7-bit programmable) and C_{f2} (3-bit programmable) provide configuration of the PGA gain. When phi2 goes high, the PGA is reset. C_{in} then absorbs a charge $Q1 = C_{\text{in}}(V_{\text{out1}} - V_{\text{ref}})$. Clock phases phi3 and phi4 are slightly delayed phi1 and phi2 clocks, respectively, so the PGA can be synchronized with the capacitive readout circuit. When phi3 goes high, C_{in} is discharged and, since phi2 goes low, the feedback capacitor C_{f2} absorbs a charge $Q2 = C_{f2}(V_{\text{ref}} - V_{\text{out2}})$. Charge conservation at the inverting amplifier input requires that the PGA output voltage is

$$V_{\text{out2}} = V_{\text{ref}} + (V_{\text{out1}} - V_{\text{ref}}) \cdot \frac{C_{\text{in}}}{C_{f2}}. \tag{5}$$

As expected, calculation of the z-domain transfer function reveals that the PGA ac gain (not considering dc bias) is a frequency-independent constant C_{in}/C_{f2}.

While $\text{phi}s$ (same phase as phi3) is high, the PGA output is sampled and held on capacitor C_h. The S/H stage uses a dummy switch to reduce clock-switching noise at the high impedance

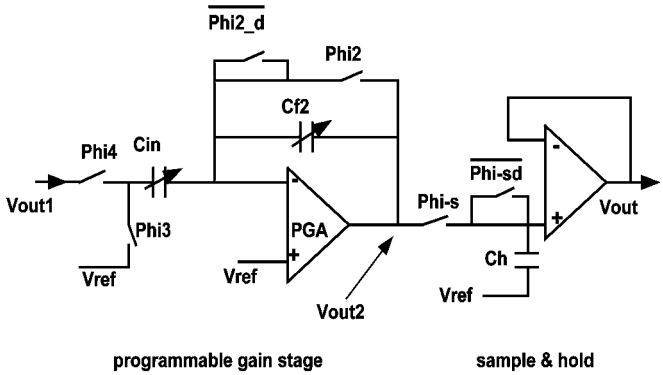


Fig. 9. Simplified schematic of the PGA and S/H stages.

nodes, and the S/H output holds the value of the PGA from the previous phase. All switched capacitor circuits, including the capacitive readout block, are designated to operate with a nominal 50-kHz clock. The on-chip clock phase generator produces nonoverlap times and clock phase delays of 250 ns.

5) Amplifiers: Amplifier topology greatly influences the overall performance of the readout circuit, and different readout blocks perform better with different types of amplifiers. Although the details of amplifier design are beyond the scope of this paper, it is valuable to note that the UMSI chip utilized two different amplifier topologies. The voltage and resistive front-ends and the DACs are required to drive resistive loads. Therefore, these blocks utilize a high gain $(> 80$ dB$)$ buffered amplifier with low output impedance. The capacitive front-end and the PGA and S/H stages utilize switched capacitor configurations for low-power operation and improved noise performance. They use folded cascode operational transconductance amplifiers (OTA), which provide sufficient dc gain and improved power supply noise rejection. This amplifier has a dc gain of 79dB and phase margin of 72° optimized for switched capacitor implementation. The output swing is 2.5 V, and the bandwidth is 24 MHz. The preamplifier uses pMOS inputs to minimize thermal and 1/f noise, whereas the other stages use nMOS inputs to maintain a higher bandwidth for resistive and voltage signals.

V. Results and Applications

A. Implementation

The functionality of the digital control circuit, memory, and I/O ports was described in Verilog and the modules were synthesized using the Cadence Buildgates synthesis tool. This block was integrated with the custom-designed analog circuits to implement the overall mixed-signal UMSI chip. Physical design of the analog front-end was carefully considered to maximize performance. Capacitive coupling from parallel and overlapping interconnects of sensitive nodes were avoided by cautious routing and ground shielding with ample substrate contacts. Common centroid layout techniques were used to reduce input offsets and match passive component values. Charge injection was also reduced by using delayed clocks on switches in the circuit design [32]. All switches in the critical signal path were realized as complementary MOSFET switches to reduce resistance and

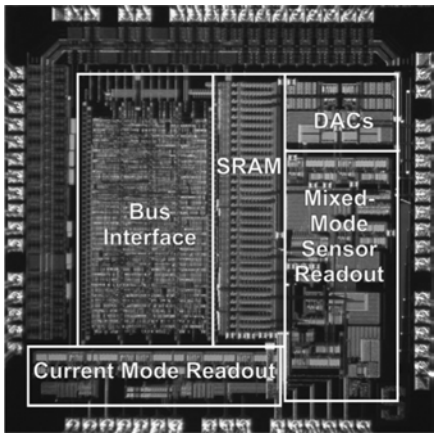
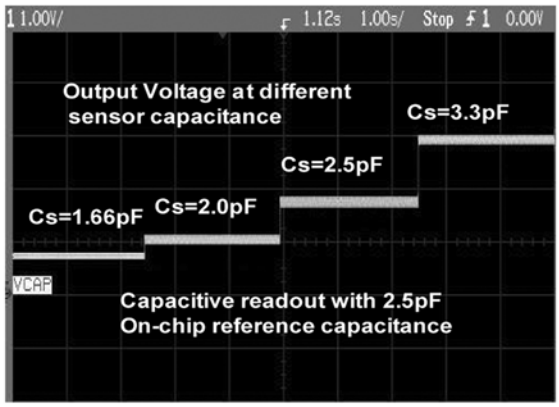


Fig. 10. Die photograph of the UMSI chip that integrates a sensor bus interface, embedded SRAM, and an adaptive mixed-mode sensor readout circuit.

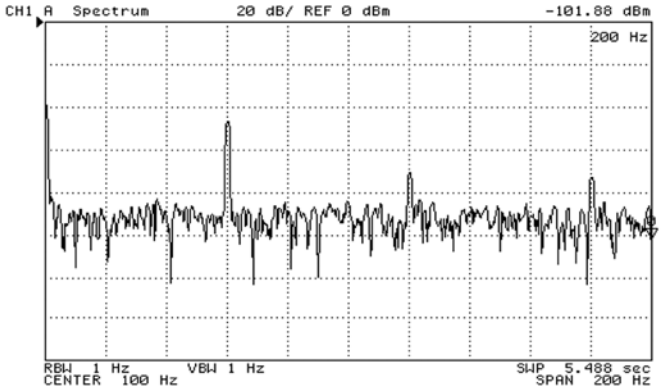
allow full voltage swings. Binary-weighted programmable capacitors and resistors were constructed from exact copies of unit cells. Separate power and ground rails were created for the digital and analog blocks to reduce noise coupling from the supply rails. The 2.2 mm $\times$ 2.2 mm UMSI chip shown in Fig. 10 was fabricated in a 0.5-μm CMOS process that offers good analog performance, low leakage currents to reduce power consumption, and digital performance and density well suited to microsystem applications. Analog performance was verified from 2.7 to 3.3 V to support battery powered applications. At a nominal 3.3-V supply with all circuit blocks turned on, the chip draws 3.3 mA. However, the chip implements a low-power sleep mode that requires only 40 μW while monitoring for sensor-driven interrupts. Power consumption can be further tuned by wiring supply voltage only to the analog blocks needed for a specific application. For example, in a typical application with four sensors scanned periodically, the UMSI chip dissipates 53μW for a 1 sec scan period or 171 μW for a 0.1 sec scan period. These results use a 2 mA chip configuration and a liberal 500 μsec to program the chip and readout each sensor.

B. Measurement Results

Simulation results indicate proper operation of all switched-capacitor circuits from 10 to 100 kHz. Capacitive readout measurements of the fabricated chip were performed at 50 kHz while the remaining blocks were verified at 10 kHz. Fig. 11(a) shows the capacitive readout output for various sensor values, agreeing well with simulation results. Fig. 11(b) plots the measured noise level of capacitive readout showing about -90 dBm noise power. The spikes in Fig. 11(b) are due to 60-Hz power supply noise and associated harmonics. Detailed measurements show a maximum sensitivity of 30 mV/fF and a resolution above the noise floor of 1fF in the 10-Hz bandwidth. The measured response of the capacitive interface at several PGA gain settings is plotted in Fig. 12, where the off chip sensor capacitance is held constant and the on-chip programmable reference capacitor is varied in 50-fF steps. The response is very linear with sensitivity of 1, 2, and 4 mV/fF



(a)



(b)

Fig. 11. (a) S/H output for capacitive readout with 2.5-pF reference and sensor capacitances shown in the plot. (b) Noise spectrum of capacitive readout with about -90 dBm noise power.

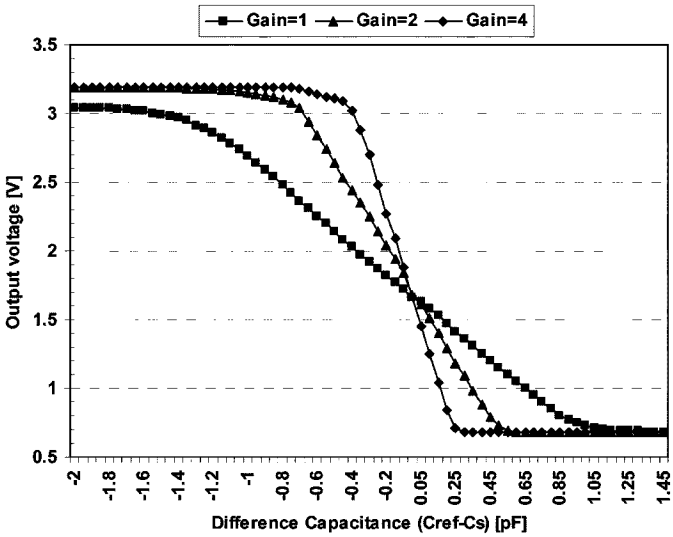


Fig. 12. Measured performance of capacitive readout at different PGA gain settings.

at PGA gain settings of 1, 2, and 4 V/V, respectively. Fig. 12 verifies that gain and offset can be programmably adjusted.

Voltage readout and half-bridge resistive readout were evaluated by applying a 100-Hz test signal to the inputs of the

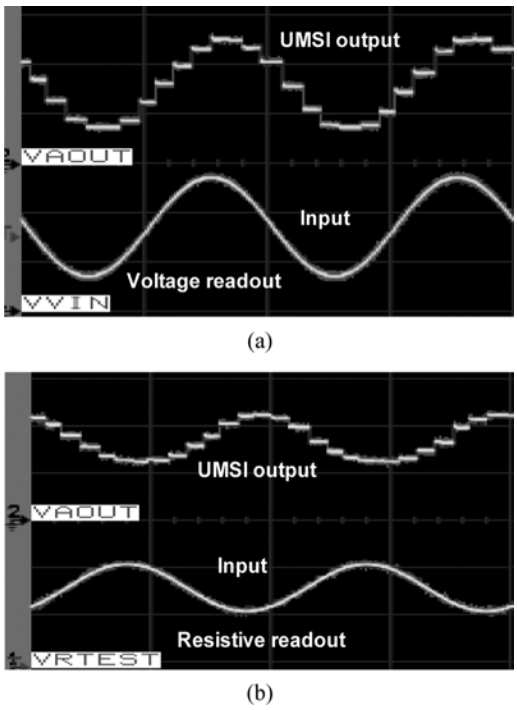


Fig. 13. S/H outputs with PGA at unity gain for (a) voltage and (b) resistive half-bridge readout configurations.

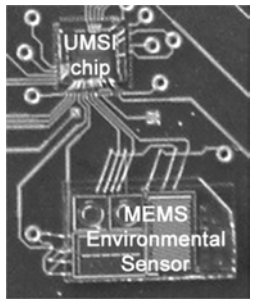


Fig. 14. Prototype sensor node with UMSI chip and multiparameter MEMS sensor chip.

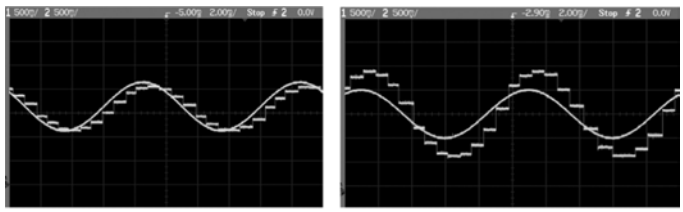


Fig. 15. Voltage readout on the prototype microsystem with PGA gain settings of (a) 1 and (b) 2 V/V, verifying the operation and programmability of the UMSI chip.

analog signal router and directing the signals to the appropriate readout block. S/H outputs of the voltage and resistive readouts are plotted in Fig. 13(a) and (b), respectively. In half-bridge configuration, the resistive amplifier is inverting, providing phase shift observed in Fig. 13(b). Detailed tests of the resistive interface for a nominal sensor/reference value of 22 kΩ show sensitivities of 2 mV/50Ω with a unity gain PGA and 18 mV/Ω at maximum gain.

C. Calibration and Self Test Features

In our analysis of multisensor microsystems, self test capabilities have proven to be instrumental in the reliability and long-term performance of these complex systems. Self test is also an important complement to a gain/offset configurable readout chain because it permits system-level online recalibration. The UMSI chip provides mechanisms to test both the readout block and attached transducers. For readout circuit self test, the embedded DAC can be routed to the analog mux input (Fig. 5) to identify offset and gain drifts. For transducer test, the DAC can be applied to drive external set points or control external actuators on self-testable sensors. Furthermore, the SPI peripheral interface and digital I/O permit application specific test capabilities using an external DAC applied through the voltage readout channel. Once the readout block and/or sensors have gone through a self-test cycle, the microsystem controller can determine any necessary adjustments in the programmable gain and offset settings, or adjust the DAC that sets the reference voltage, implementing a fully automated online recalibration of the sensor node.

In an example self test sequence, the microsystem controller tells the UMSI chip to apply a given DAC output value to the analog mux, sets the gain, and then compares the resulting output with a stored reference value. The procedure can be repeated for a different gain setting, and then the readout configuration parameters can be adjusted to bring the response back to the reference level.

D. Prototype Application Results

The UMSI chip was designed to facilitate the rapid development of multisensor microsystems. This highly adaptive chip provides many general use capabilities while targeting requirements common to environmental sensor systems. Because such systems are often power limited or employed within wireless networks, the UMSI chip supports multiple system-level power management features and permits several hardware configuration (see Section II-B) that allow the user to trade power for advanced features, e.g., self test. To support a next-generation UMSI chip with even lower power dissipation, the circuit topologies are scalable to ∼0.18-μm technology at 1.8-V supply, and power hungry circuits included to drive external loads can be removed.

A prototype multiparameter microsystem was constructed by wire bonding a UMSI die with an all-capacitive MEMS temperature, pressure, and humidity chip [33], as shown in Fig. 14, and connecting the sensor node to a microcontroller using the IM^2 sensor bus protocol. To verify proper operation and programmability of the UMSI chip, a 100-Hz 0.5-V ac signal with 1.65-V bias was applied to different input channels and directed to the voltage readout block. The S/H output results with PGA gain of 1 and 2 V/V are shown in Fig. 15(a) and (b), respectively. Similar tests of the resistive readout block were performed, and results similar to Fig. 13(b) verified proper operation.

In the prototype microsystem, elements of the multiparameter MEMS sensor chip were connected to the UMSI chip, with input

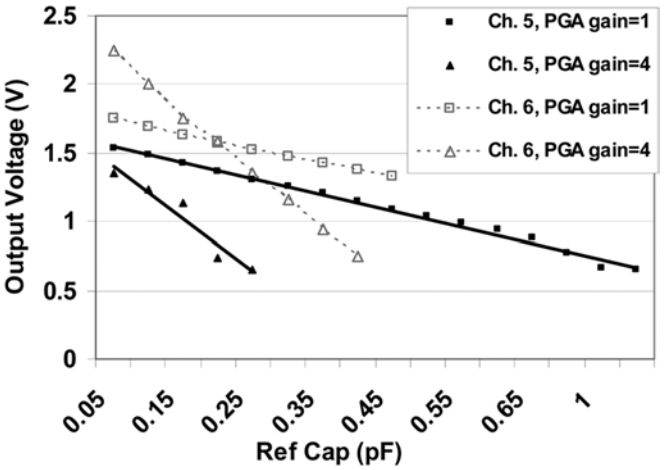


Fig. 16. Measured results with capacitive pressure sensors at input channels 5 and 6 for two gain settings.

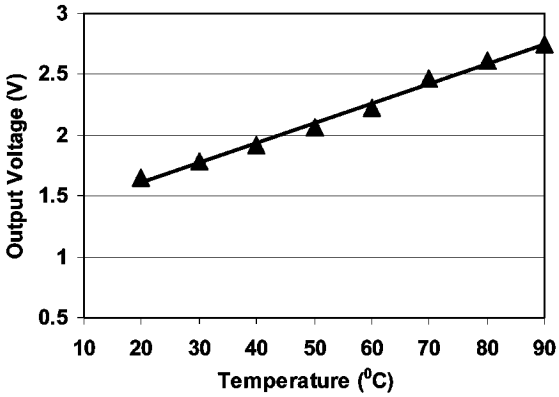


Fig. 17. Response of a temperature sensor measured by the UMSI chip on the prototype microsystem. With PGA gain of 1V/V the sensitivity is about 14.5 mV/°C from 20 to 90 °C.

channels 3 and 4 connected to two temperature sensors, channels 5 and 6 connected to two pressure sensors, and Channel-7 connected to a humidity sensor. To characterize operation of the capacitive readout circuit at fixed sensor outputs, the value of the on-chip reference capacitor was programmably swept in 50-fF steps and results from each sensor input channel were plotted. Fig. 16 shows the results from the pressure sensors at channels 5 and 6 at PGA gains of 1 and 4 V/V with linear response spanning only a portion of the available range of the interface circuit. The Channel-7 humidity sensor input showed a similar response to the Channel-6 pressure sensor at both gain settings. The prototype microsystem was placed in a temperature chamber to record the response of the MEMS temperature sensor, which is plotted in Fig. 17 and shows a linear sensitivity of 14.5 mV/°C at a PGA gain of 1V/V over a 20 °C to 90 °C temperature range. Table IV summarizes the performance of the UMSI chip characterized within the prototype microsystem. Table V compares UMSI performance with several reported generic sensor interfaces and shows that the UMSI provides a significant improvement in signal range. Although most these chips do not report resolution/sensitivity, UMSI performance is comparable to many recently reported sensor-specific (nongeneric) interfaces.

TABLE IV
SUMMARY OF FEATURES PROVIDED BY THE UMSI CIRCUIT

Feature	Performance
Bus Addr Modes	single, multi-node, broadcast
Chip/Node ID	4b or 8b
Chip ID Setting	hardwired or uploaded from external memory
SRAM	32x8b
Digital I/O	8b, bidirectional
Peripheral Intrf.	SPI bus with 4b chip select
Analog Inputs	8-to-4 signal router
Actuator Control	8b digital, 1b analog (6b DAC)
Capacitive Readout	Range: 10fF to 100pF Sensitivity: 1mV/fF (unity gain); 30mV/fF (max gain) Resolution: 1fF at 10Hz bandwidth
Resistive Readout	Single, half-bridge, and full-bridge readout Sensitivity: 2mV/50Ω (unity gain); 18mV/Ω (max gain) @ 22kΩ nominal Resolution: 10Ω at 22kΩ nominal resistance.
Voltage Readout	Range: 0.6 to 10V; Attenuation ratio: 0.125 to 1V/V Resolution: 60μV
Power (@3.3V)	40μW to 10.9mW, 50μW typical

TABLE V
COMPARISON OF INTERFACE CHIP PERFORMANCE

	Key performance	Process	Power
UMSI	C: 10fF to 100pF, Res: 1fF in 10Hz BW Sens: 30mV/fF R: Res: 10Ω at 22kΩ Sens: 18mV/Ω V: 0.6 to 10V Res: 60μV	0.5μm 3M/2P CMOS	2.7 to 3.3V 40μW to 10.9mW 53μW typical
Mackenssen '05 [16]	C: 12 to 200pF R: 82Ω to 2.5KΩ V: 0 to 2.8V I: 58nA to 24μA Res-Sens: N/R	FPAA	5V; 90mW
Chao '04 [14]	C: up to 300pF Res-Sens: N/R	CMOS	N/R: N/R
Kraver '01 [19]	C: 1 to 16pF I: 100nA to 400μA Res-Sens: N/R	0.35μm CMOS	3V; 48mW
Yazdi '00 [4]	C: Res: 1fF in 10 Hz BW	3μm 1M/2P CMOS	5V; 2.2mW
Chavan '00 [5]	C: Sens: 1mV/fF	1μm 2M/2P BiCMOS	5V; 10mW
VDGoes '97 [11]	C: Res: 150aF/0.9fF R: Res: 2μV to 20μV	0.7μm CMOS	3.3 to 5.5V
Wouters '94 [9]	Low power Res-Sens: N/R	2 μm CMOS	3V; N/R

Res = resolution, Sens = sensitivity, N/R = not reported

A modified version of the UMSI chip, wherein some of the configurable analog front-end was replaced by application specific readout circuits, was utilized to develop a chip-scale integrated data gathering microsystem [3]. This 0.15 cm^3 microsystem platform further demonstrates the value of the unique combination of feature provided by the UMSI chip.

VI. CONCLUSION

A highly configurable multiparameter transducer interface suitable for a multidrop intramodule sensor bus was presented. The mixed-signal circuit provides a standard communication

link for intelligent interaction with a central microsystem controller and can interface with actuators and a large variety of capacitive, resistive, current or voltage output sensors. The range of transducers and signal levels accommodated by this chip is significantly larger than previously reported multisensor interfaces. The UMSI chip implements features such as real-time reconfigurability, self test and self calibration, peripheral interface, and plug-n-play operation that are highly desirable in many of the low-power multisensor microsystems. This unique combination of capabilities facilitates the rapid development of new sensory systems, circumventing the need for costly sensor-specific interface circuitry and simplifying the system design and upgrade processes. The chip dissipates 53 μW in a typical four-sensor application from a 3.3-V supply, and it can operate within specification over supply range of 2.7 to 3.3 V. Characterization of a prototype microsystem verifies the interface chip can achieve sensitivities of 30 mV/fF and 18 mV/Ω and can be readily reconfigured to readout a wide range of sensors.

ACKNOWLEDGMENT

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