Highly uniform and low-loss passive silicon photonics devices using a 300mm CMOS platform

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Abstract: Using an advanced 300mm CMOS-platform, we report record-low and highly-uniform propagation loss: 0.45±0.12dB/cm for wires, and 2dB/cm for slot waveguides. For WDM devices, we demonstrate channel variation(3-σ) within-wafer and within-device of 6.1nm and 1.2nm respectively.

OCIS codes: 130.3120, 230.7370, 230.7390, 140.4780, 060.1810

1 INTRODUCTION

Next-generation silicon photonics transceivers will require the integration of ultra-low-power active devices with ultra-low-loss passive devices enabling wavelength-division multiplexing (WDM). A major challenge in the manufacturing of such devices is the extreme sensitivity of the device and waveguide properties (phase and amplitude transfer control) on the cross-sectional dimensions and sidewall quality of the employed photonic wire and rib structures, which results in poor device uniformity across a die or a wafer [1].

In this paper, we report on a significant improvement in propagation loss well below 1dB/cm with a 1-σ variation of 0.12dB/cm across a 300mm for a single-mode 400nm x 220nm wire waveguide. For WDM devices, an absolute channel wavelength 3-σ variation of 6.1nm is demonstrated across a wafer, as well as a channel-spacing 3-σ variation of 1.2nm. Furthermore, for the first time we verify the wide belief that silicon photonic device and circuit performance and variability will be greatly improved with advanced CMOS processes and substrate technology.

2. FABRICATION TECHNOLOGY

For the device fabrication, we used a 300mm Silicon-On-Insulator (SOI) wafer with 220nm of crystalline Si top layer and 2000nm buried oxide (BOX). The SOI wafers were manufactured by Soitec using SmartCut™ technology. Fig.1 depicts a typical Si thickness distribution. The wafers show a high degree of uniformity with 3-σ variation of 1.65nm (0.75%) and a wafer range of 2.5nm (1.1%). For the device patterning, we used a modified 28-nm shallow-trench isolation (STI) process [2]. The pattern on the photomask is transferred into silicon using 193nm immersion lithography and a dry etch process. We use two etch levels, a 220nm deep level for waveguide definition and 70nm shallow level for fiber-chip grating coupler definition. After dry etch and resist removal, the waveguides were covered with silicon dioxide and planarized. After planarization the wafers are tested optically.

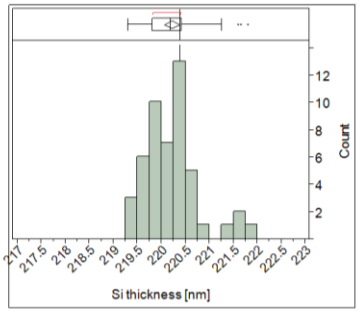

Fig. 1 Si thickness distribution over a 300mm SOI wafer.

3. LOW-LOSS WAVEGUIDES

We use two types of waveguides to demonstrate the loss performance: (1) single-mode photonic full-depth etched wires and (2) slot waveguide. The propagation loss in these waveguides is mainly attributed to light scattering off the etched sidewalls. Therefore, losses are a direct qualification of the patterning process quality. It has been shown in [3] that low roughness patterning can be achieved by using 193immersion lithography and an optimized dry etch

process. To assess the propagation loss, we fabricated spiral photonic wire waveguides of three different widths (400, 450 and 500nm) and slot waveguide (260nm rail width, 100nm slot width). Each waveguide comes in 4 lengths (1, 2, 4 and 7cm) from which the propagation loss is extracted by a linear fit. The bend radius of wires and slot waveguides was 10µm and 20µm respectively.

In the C band, we measure an average propagation loss of 0.8, 0.74 and 0.5dB/cm for 400, 450 and 500nm wide wire waveguides respectively over a 300mm wafer (Fig.2). The error margin on individual data point is <0.02dB. To our knowledge, this is the lowest loss reported for fully etched single-mode silicon wire. The waveguide losses are verified across the 300mm wafer with 3-σ variation of 0.12dB/cm and a range of 0.12dB/cm (Fig. 3). This represents over 50% improvement as compared to the best single-mode waveguide reported loss on a 200mm platform.

For slot waveguides, we measure a propagation loss of 2dB/cm at 1550nm (Fig. 4), while with the 200mm platform, a similar type of waveguide geometry yields a loss of between 10-15dB/cm.

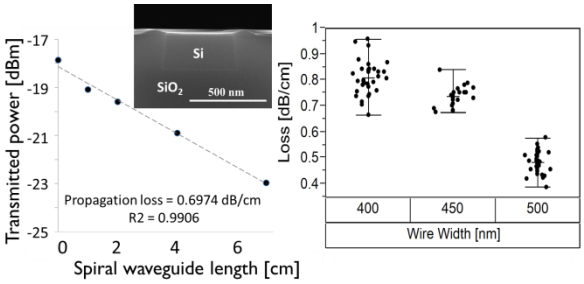

Fig. 2. Propagation loss extraction of a 450nm photonic wire. Loss of different waveguide widths. Inset shows a typical cross-section of a 450nm wide wire.

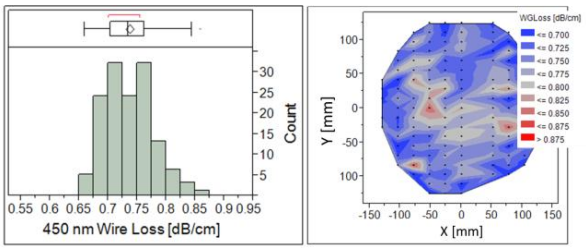

Fig. 3. Within wafer propagation loss uniformity of a 450nm wire waveguide.

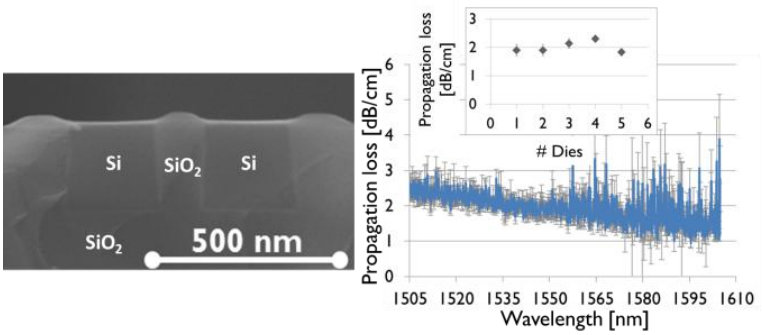

Fig. 4 (left)Cross-section SEM image of a slot waveguide and (right) typical transmission spectrum and loss spectrum.

Fig. 6 shows the distribution of the drop wavelength of the first channel across the 300mm wafer. We observe a within-wafer 3σ variation of 6.1 nm, which agrees well with the waveguide width variability over the wafer, where 3-σ variation of 7.65nm is observed.

Fig. 7 shows the variability (1-σ) of the CS error for all channels across a 200mm and a 300mm wafer, as a function of the average CS. By using the 300mm platform the 1-σ variability of the CS error is reduced to 0.4nm (at an average CS of 2.5nm) from 0.7nm in the 200mm platform (at an average CS of 2.55nm) [4].

4. CONCLUSION

We presented a highly uniform and low-loss silicon photonics platform using advanced 300mm CMOS fabrication technology. The substantial improvement in propagation loss and WDM device matching over the wafer is an important step for realizing next-generation low-power and high-density silicon photonics devices and systems.

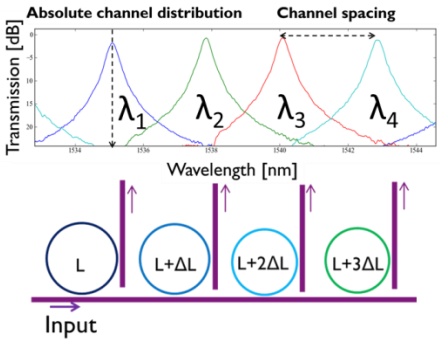

Fig. 5 (left)Schematic of 1x4 single-ring de-multiplexer. Right) Typical spectral response and the parameters studied.

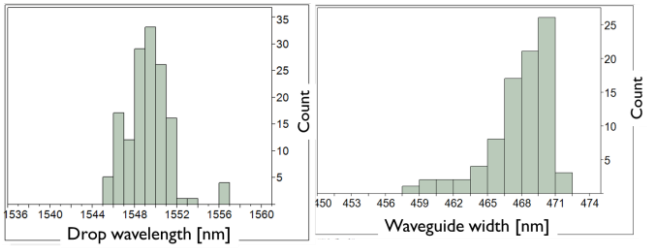

Fig. 6 (left) Absolute channel variability of one of the channels, (right) 450nm photonic wire distribution over a 300 mm wafer

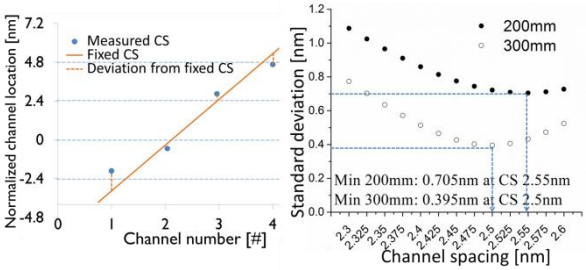

Fig. 7 (Left)Schematic of channel spacing and deviation analysis. (Right) Variability of channels spacing between 200mm and 300mm platform.

5. ACKNOWLEDGEMENT

The authors wish to thank the imec p-line for the fabrication of the silicon photonics wafers. This work was supported by imec's Core Partner Program and the ERC-project ULPPIC. The research leading to these results has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 318178-PLAT4M.

6. REFERENCE

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