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# HLS-based Optimization of Tau Triggering Algorithm for LHC: a case study

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Abstract-With the current increase in the data produced by the Large Hadron Collider (LHC) at CERN, it becomes important to process this data in a corresponding manner. To begin with, to efficiently select events that contain relevant information from a massive flow of data. This is the task of the tau lepton decay triggering algorithm. The implementation is based on the High-Level Synthesis (HLS) approach that allows generating a hardware description of the design from the algorithm written in a high-level programming language like C++. HLS tools are intended to decrease the time and complexity of hardware design development, however, their capabilities are limited. The development of an efficient application requires substantial knowledge of the hardware design and HLS specifics. This paper presents the optimizations introduced to the algorithm that improved latency and area and more importantly solved the problems with the routing, making it possible to implement the algorithm on the FPGA fabric.

Index Terms—HLS, algorithm optimization

## I. INTRODUCTION

With the current increase in the data produced by the Large Hadron Collider (LHC) at CERN, it becomes important to process this data in a corresponding manner. Firstly, to efficiently select events that contain relevant information from a massive flow of data. This is the main objective of the tau lepton decay triggering algorithm.

Tau lepton is an important particle for analysis of the physical processes happening in LHC, it "plays an important role in both precise measurement of Standard Model physics and search for physics beyond the Standard Model" [1]. However, it has a short lifetime and short decay length and can be found and reconstructed only by its decay products. The tau triggering algorithm is designed to identify the events that have hadronically decaying tau leptons [1].

The algorithm consists of 3 major steps. In the first step, the event data is buffered, and the 16 objects (seeds) with the highest pT (transverse momentum) value are selected. Selected seeds and buffered data from the whole event are then passed to the select candidates step. The task of this step is to select up to 30 tau candidates from the neighborhood of each seed.

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Then, selected candidates are analyzed to find information that can be used to reconstruct tau objects.

The implementation of the algorithm is based on the High-Level Synthesis (HLS) approach that allows generating a hardware description from the algorithm written in a highlevel programming language like C++. HLS tools are intended to decrease the time and complexity of hardware design development, which is especially useful in the case of computeand data-intensive applications. However, the capabilities of HLS tools are limited. Proper optimization of the algorithm requires knowledge of the hardware design and HLS specifics.

The algorithm is developed using Vivado HLS targeting Xilinx Virtex UltraScale+ FPGA VCU118 Evaluation Kit.

The task of the case study was to optimize the critical parts of the algorithm in order to solve problems with timing, area, and routing. Considering the selected development approach, in order to optimize the algorithm two tasks should be solved: first, optimized design development and, second, its implementation in a correct way so that Vivado HLS can synthesize it accordingly.

The paper is organized in the following way. Section 2 presents the main concepts of high-level synthesis and its current state. Section 3 presents the sorting algorithm developed for the project. Section 4 provides an overview of the candidates selection task optimization. Conclusions are given in Section 5.

## **II. HIGH-LEVEL SYNTHESIS**

With the increased popularity of the FPGAs (Field-Programmable Gate Array) and heterogeneous systems combining processor units and programming logic on one platform, there arises the necessity to introduce new programming methods for the FPGAs that will make them more accessible to the broader public.

FPGAs have certain benefits over traditional computational platforms like CPU and GPU. Due to their natural parallel computing capabilities, they are faster than the CPU. While GPUs are capable of parallel computing as well, FPGAs are characterized by lower cost and much lower power consumption.

However, the complexity of programming that requires substantial knowledge of the underlying architecture and hardware specifics and increased time to develop the product makes FPGA platforms less accessible to the broader public. Using

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IP (Intellectual Property) cores, ready-to-use functional blocks, is one way to solve the problem; they allow building an application in a Lego-like fashion by combining needed blocks together. Nevertheless, not every functionality can be implemented using IPs. More complex algorithms require tailored solutions designed specifically for the application.

A better way to solve the problem is the High-Level Synthesis (HLS) tools that introduce a higher level of abstraction for the hardware programming, namely they allow developers to write algorithms in high-level languages like C and C++ that will be automatically translated by the tool into HDL specification considering characteristics of the selected board. This way, HLS tools allow non-hardware specialists to program FPGAs. Additionally, they increase the portability and maintainability of the application, code written in C/C++ can be easily re-synthesized for different target platforms, debugged, and changed in case there is a need. Since the input code for HLS describes the algorithm, what the program does, rather than how exactly it is implemented on the target platform.

However, HLS is not a panacea. It still requires domainspecific knowledge to write well-optimized code. HLS tools suggest different pragma directives for hardware-specific optimization of the algorithm. Nevertheless, those directives alone are not enough to synthesize optimal RTL implementation. They will not be able to improve the algorithm not suitable for the hardware implementation. In order to produce an efficient hardware description, the input code should be restructured accordingly. Licht et al. [2] states that naive unoptimized HLS implementations show worse performance than naive software implementations. Matai et al. [3] present a case study for insertion sort optimization, showing how properly written code can increase the performance of the algorithm, reducing the latency and resource usage. Restructured code shows the best result time- and area-wise compared to the software version of the algorithm optimized with different pragma directives.

Huang et al. [4] compare the HLS-based development process to embedded systems development. Even though companies like STM and Arduino producing development boards provide great support for their products including frameworks for automated settings and board-specific libraries in order to make the programming of the devices easier, it still requires domain-specific knowledge to write efficient applications and solve arising problems.

The main difference is that high-level languages used in HLS for input code are not designed to describe hardware specifications, they are designed to describe software instructions executed sequentially, which introduces a challenge of describing hardware constructs with software languages.

Additionally, it requires the knowledge of how HLS tools themselves work, in what order they implement directives, how they represent the algorithm internally, and how they synthesize different constructs in order to restructure the design of the application in a way that will produce a desirable result. Several works report that the quality of results (QoR) of the HLS generated hardware description is far behind that of manually written RTL design [2], [4]–[7]. On the contrary, [8] shows an HLS-generated design that reduces resource usage by 11-13 % compared to the design written by an RTL expert, proving that HLS can produce competitive results. The case study presented in [9] shows comparable results as well.

A serious limitation of HLS tools is that physical layout and routing estimation is difficult on the HLS level and therefore require again logic synthesis and implementation in order to identify whether synthesized design has routing problems and congestions. Reported congested areas should then be mapped to the original code, which is a problem on its own since the generated hardware description of the design differs drastically from the input code.

Nevertheless, the complex nature of the algorithm which is both compute-intensive and data-intensive calls for the HLSbased development process. And therefore, the aforementioned specifics of the HLS should be addressed and solved during the work on the project.

## A. Vivado HLS overview

Vivado HLS [10] is the commercial tool provided by Xilinx. It accepts code written in C, C++, and SystemC as input and synthesizes hardware description in VHDL, Verilog, and SystemC. The tool includes a variety of pragma directives for design optimization and libraries for hardware-specific features, such as arbitrary precision data types, Xilinx IP (Intellectual Property) functions for streams, shift registers, etc. Additionally, it provides automatic test-bench creation, C and RTL co-simulation, and support for floating-point and fixed-point arithmetics.

After synthesis, Vivado HLS creates a report describing the performance metrics of the generated design, including the maximum frequency of the design based on the longest combinational delay, latency of the design, initiation interval (number of clock cycles before the application can accept new input), number of utilized resources based on the number of resources available on the target platform, types of interfaces used for input and output signals. The same information is presented for every function and loop instantiated in the design.

In order to guarantee the synthesizability of the design, Vivado HLS does not accept some C/C++ language constructs, including recursion, dynamic memory allocation, function pointers, and operating system calls.

#### III. SORTING

The first step of the algorithm is dedicated to buffering the input data and selecting 16 seeds out of 144 candidates with the highest pT (transverse momentum) value. The candidates are sorted, and 16 elements from the top are saved into the Seeds array for further analysis.

Input data is a continuous stream of particle events. The event data includes data from 36 regions that come one region at a time. Every region contains 22 charged tracks, 13 photon

tracks, and 10 tracks from neutral particles. First 4 tracks from every region form an array of seed candidates  $(36 \times 4 = 144)$ . Later an array of seed candidates is sorted to find the 16 best seeds based on their pT value since a high pT value can be an indication of decaying tau leptons.

### A. Original algorithm

The original sorting algorithm was a hardware-optimized version of bubble sort that was taking too many resources causing problems with the routing of the whole algorithm. The task was to develop a new sorting algorithm that will significantly decrease the number of utilized resources and potentially decrease the latency of the first step since the total latency of the algorithm is very strict. The latency of the first step can be defined as max(B, S), where B is the latency of the sorting. Buffering takes 56 clock cycles, the original sorting solution takes 57 clock cycles. Therefore, an optimized solution should take the same amount of clock cycles or less than the buffering.

In the beginning, it was decided to try some modifications of the original algorithm to explore possible optimizations without introducing a completely new sorting algorithm. Each seed candidate object is represented by a structure with 6 members. During the sorting, seed candidates are read and written numerous times. The idea was to use a smaller structure containing the pT value and index of the candidate for the sorting and then write the 16 best seeds using obtained indices. Another idea was instead of a smaller structure use a temporary array of 8 + 16 bit integers that will hold both the index of the candidate (8 bits) and its pT value (16 bits). Both approaches only slightly reduced the resource usage of the function, did not reduce the latency and introduced the problem of using many multiplexers at the stage when the selected seeds should be written to the output array based on their indices in the seed candidates array. The results are presented in Table I.

 TABLE I

 Results of the original algorithm modifications

Algorithm	Latency, cycles	FF	LUT
Original	57	151,287 (6%)	262,690 (22%)
Smaller struct	58	132,448 (5%)	208,487 (17%)
8 + 16 bit integer	72	146,627 (6%)	238,428 (20%)

Eventually, it was decided to try a different sorting algorithm. The algorithm should consider the streaming nature of incoming data, the fact that it comes in chunks of 4, and that only 16 elements out of 144 should be saved for further processing. The straightforward approach to use some hardware-optimized sorting architecture to sort all 144 elements would not be applicable, because even sorting algorithms with time complexity O(n) would take much more clock cycles than desired.

## B. Streaming merge sort

At first, it was decided to implement a merge sorter tree that at every level will leave only the 16 best elements, discarding the others.

On the first level, there are 16 arrays, 9 elements each  $(16 \times 9 = 144)$ . On the second level, they are merged into 8 arrays of size 16, and so on until there is only one array left with the best seeds. 16 arrays on the first level were sorted in an insertion sort manner: a new coming element would traverse through the array to find its place, then if needed elements greater than the new one will be shifted, and a new element inserted. To parallelize the process, each seed candidate from one region would be inserted into a different array. This way, a new element is inserted in the array on the first level every third cycle, giving the previous element 2 clock cycles to find its place, which was proved sufficient during the runs of the algorithm.

Three different variants of the merge sorter were tried: OUT arrays implemented as BRAMs, OUT arrays partitioned and implemented as separate registers, and finally OUT arrays implemented as FIFO streams. The results prove that streams are the best solution for the merge sorter as they decrease the latency of the merge stage. However, they have a certain drawback: all elements from the previous level that are not passed to the next level should anyway be read from the stream. The results are presented in Table II.

TABLE II Results for merge sort implementations

OUT arrays	Latency, c	BRAM	FF	LUT
As BRAM	104	48	35,333 (1%)	146,998 (12%)
Partitioned	84	0	63,552 (2%)	439,358 (37%)
As streams	72	0	41,117 (1%)	391,176 (33%)

It can be seen that the implemented merge sort does not fit into defined latency and does not decrease the number of resources used and therefore does not satisfy the task description. The increased latency is attributed to the fact that it was required to divide the buffering process and the merge sorter between different functions. Buffering requires a pipeline directive in order to read new region data every clock cycle and start processing new event data every 36 cycles. Merge sorter though requires a dataflow directive to make all merge levels work in parallel, and Vivado HLS cannot instantiate the dataflow region from pipelined function. Therefore, the merge sorter waits until the buffering stage is over and starts to work only after.

#### C. Spatial insertion sort

The first algorithm developed that improved the timing and the resource usage was a modification of insertion sort. A spatial sorter was built that included 16 insertion cells. The sorting architecture is presented in Figure 1.

The sorting algorithm considers that 4 inputs from each region are already sorted and, therefore, 4 elements are used



Fig. 1. Spatial sorter architecture

as an input for each insertion cell, unlike traditional implementation that has 1 new coming element as an input.

Each insertion cell works on one element of the Seeds array. First, the insertion cell gets 4 elements from the new region and compares it to the first element of the Seeds array. The biggest element is saved to the CURR\_REG variable. Since it is known that elements in the IN array are sorted, the biggest element is either CURR\_REG or IN[0]. If it is not CURR\_REG, IN[0] is saved into the CURR\_REG, the previous value of CURR\_REG is inserted in the appropriate place in the OUT array. The OUT array is then passed to the next sorting cell. The work of the insertion cell is presented in Figure 2.



Fig. 2. Sorting cell architecture

In order to make Vivado HLS implement 16 different instantiations of the insertion cell function, so each of them will use its own static variable CURR\_REG, the function is defined as a template with an integer parameter that acts as an ID number. Otherwise, Vivado HLS will generate the design, in which all insertion cells will share the same CURR\_REG variable.

Generally, the complexity of a spatial sorter is O(2n), but in our case, the complexity is O(n/4 + m), where n is the number of seed candidates and m is the number of top seeds.

With this approach, sorting takes 36 + 1 + 16 (53 cycles), because the first region elements are passed to the first sorting cell on the second cycle and the elements from the last region take 16 cycles to pass through all sorting cells. Since the latency of the first step function is determined by either buffering or sorting, depending on which operation takes more clock cycles, the total latency of the function with the described sorting algorithm is 56 clock cycles.

It was possible to modify the created algorithm to decrease the timing of the sorting part even more. Instead of working on 1 element from the Seeds array, new sorting cells work on 2 elements from the Seeds array. Graphically, a modified sorter is presented in Figure 3.

The architecture of the insertion cell has changed as well. The solution for the modified insertion cell was inspired by [11] that presents a single-stage N sorter based on a comparison counting matrix. The suggested N-sorter does not require calculating the rank of each element, it is built according to the equations derived from the comparison counting result.

Since it is known that the IN array is sorted and REG0 and REG1 are sorted, several simple rules were deducted to sort those elements. 6 elements should be sorted into 6 output positions: out1, out2, out3, out4, out5, and out6. out1 and out2 are saved into REG0 and REG1, and out3–out6 are saved into the OUT array.

The examples of the rules are presented below:

- 1) Only two elements can go to the out1: REG0 or IN[0]. The biggest one goes to the out1.
- 2) Four elements can go to the out2: REG0, REG1, IN[0], or IN[1]. If REG1 is bigger than IN[0], then it goes to the out2. If IN[0] is smaller than REG0 but greater than REG1, then it goes to the out2. If IN[1] is bigger than REG0, then it goes to the out2. Else, REG0 goes to the out2.



Fig. 3. Modified spatial sorter

3) The rules for the other output positions are depicted in the same way.

The latency of the modified sorting algorithm is 36+1+8 (45) cycles. The resource usage for the spatial sorter modifications is presented in Table III.

 TABLE III

 Results for spatial insertion sorter versus original algorithm

Algorithm	Latency, c	FF	LUT
Original	57 (57)*	151,287 (6%)	262,690 (22%)
Spatial sorter	56 (53)	104,749 (4%)	33,822 (2%)
Modified spatial sorter	56 (45)	103,783 (4%)	22,987 (1%)

\* The latency of the sorting process is given in the brackets.

It can be seen that a developed spatial sorter significantly decreases the usage of the resources and provide an opportunity to decrease the latency of the first step function if it will be possible to decrease the latency of the buffering process.

# IV. CANDIDATES SELECTION

During the second step of the algorithm, for each seed, the data from four neighboring regions (the region where the seed was found plus three adjacent ones based on the seed's location in the region) should be saved into candidate arrays. However, there was a problem with the way data from the selected regions was read from the input buffer and written to the candidate arrays. Regions were referred by their indices (from 0 to 35), but access through non-sequential indices created huge multiplexers and caused serious routing problems. A new representation of selected regions and a new way to write the data from the buffered arrays were required.

A new way to represent the selected regions by the row and column according to Figure 4 was suggested.

Every row and column was marked as either odd or even, and every odd-even pair was numbered. This way, the seed's

odd ever odd ever					
odd	0	1	2	3	0
even	4	5	6	7	0
odd	8	9	10	11	1
even	12	13	14	15	1
odd	16	17	18	19	2
even	20	21	22	23	2
odd	24	25	26	27	3
even	28	29	30	31	3
odd	32	33	34	35	4
	0	0	1	1	

Fig. 4. New regions representation

neighborhood is defined by one even and one odd row and one even and one odd column. For example, the neighborhood including regions 4, 5, 8, and 9 is defined by even row 0 and odd row 1, even column 0 and odd column 0. Since the first row and the last row are both odd, two additional parameters were added to indicate whether the last row is used or not, and if it is used then whether it is considered even or odd. The grid represents an unfolded torus, and the first and the last rows are connected, e.g., region 0 has five adjacent regions: 1, 4, 5, 32, and 33.

It was thought that changes in the selected region's representation should result in 8-to-1 MUXs (multiplexers) for row selection, 2-to-1 MUXs for last row selection, and 2-to-1 MUXs for column selection instead of the previous 36-to-1 MUXs. The problem was to make Vivado HLS infer it from the design.

A function that reads the data from the input buffer and writes it to the candidate arrays was redesigned in the following way. First, two rows should be selected: one even and one odd. Since the number of rows is uneven, the last row is considered as a special case. This way, if the candidate row is not the last one, then the selection is done from only four rows: 0, 2, 4, 6 for the even row and 1, 3, 5, and 7 for the odd. Then, from those two rows, two columns should be selected. Again, one even and one odd, therefore, in each case the selection is done from two columns: 0 and 2 for the even column and 1 and 3 for the odd.

In order to make Vivado HLS synthesize appropriate MUXs, the following idea was implemented (presented in the example of tracks.) Tracks were saved in two arrays:  $2D \ 4 \times 8$  track array for the first 8 rows and 1D trackLastRow array for the last row. Each row in the track array contains two rows from the original grid. This way, all even rows are on the left and all odd rows are on the right. Selected rows are copied to two  $2D \ 2 \times 2$  arrays: tRowEven and tRowOdd. This way, even columns end up in the first column and odd columns in the second column.

Described architecture is presented in Figure 5. Those shapes make it clear for Vivado HLS which elements are valid for each selection. This design gives 2-to-1 MUXs for the last row selection, 4-to-1 MUXs for row selection, and 2-to-1 for column selection, which is even better than predicted.



32	33	34	35
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Fig. 5. Preselect candidates selection process

This task made it clear that creating a well-optimized algorithm using HLS tools requires solving two problems: first, designing an efficient architecture and, second, writing an implementation that Vivado HLS will be able to synthesize according to the idea.

## V. CONCLUSION

For the first step of the algorithm, two different sorting algorithms were implemented and compared with the original solution: streaming merge sort and spatial insertion sort. The merge sort solution has shown that not every design can be implemented using HLS due to the limitations of the tools. It was not possible to write the code in a way that Vivado HLS can schedule merge sorter with streaming data in parallel with the buffer process.

Insertion sort solution, on the other hand, was able to reduce the resource usage of the function drastically (7× fewer LUTs for the first version and  $11\times$  fewer LUTs for the modified version compared to the original algorithm) as well as decrease the latency of the sorting part (21 % for the modified version) and solve the problem with the routing. The suggested insertion sort algorithm considers the properties of the input data (new data comes presorted in blocks of 4) and the task specification (only 16 best elements out of 144 should be selected), proving that a solution tailored to the task provides a better design.

For the candidates selection task, a new way was introduced to select 4 regions for each seed and access the data from those regions in order to avoid huge multiplexers in the RTL design that originally caused problems with routing as well. The new design instead of 36-to-1 MUXs uses 4-to-1 and 2to-1 MUXs, which take less area and do not cause problems with implementation on FPGA.

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