Holey Silicon as Efficient Thermoelectric Material

Jinyao Tang[1, 3*], Hung-Ta Wang[1*], Dong Hyun Lee[4], Melissa Fardy[1], Ziyang Huo[1], Thomas P. Russell[4], Peidong Yang[1, 2, 3†]

[1] Department of Chemistry, [2] Department of Materials Science and Engineering, University of California, Berkeley, California 94720, USA.

[3] Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, USA.

[4] Department of Polymer Science and Engineering, University of Massachusetts, Amherst, MA 01003, USA.

* These authors contributed equally to this work.

† To whom correspondence should be addressed. E-mail: p_yang@berkeley.edu

Abstract: This work investigated the thermoelectric properties of thin silicon membranes which have been decorated with high density of nanoscopic holes. These "holey silicon" (HS) structures were fabricated by either nanosphere or block-copolymer lithography, both of which are scalable for practical device application. By reducing the pitch of the hexagonal holey pattern down to 55 nm with 35% porosity, the thermal conductivity of HS is consistently reduced by two orders of magnitude and approaches the amorphous limit. With a value of ~0.4 at room temperature, the thermoelectric performance of HS is comparable with the best value recorded in silicon nanowire system.

Keywords: silicon, thermoelectric, thermal conductivity, necking, nanostructure

DISCLAIMER

Solid state thermoelectric (TE) modules convert heat to electricity and are commonly used for cooling and refrigeration purposes. [1-4] Current research has been directed towards nanoscale materials due to the potential of enhancing the Seebeck coefficient and suppressing the thermal conductivity. [5-8] The most widely used thermoelectric material, Bi_2Te_3, has the figure of merit $ZT(=S^2\sigma T/\kappa)$ ~1 at room temperature, where S is Seebeck coefficient, σ is electrical conductivity, T is the absolute temperature, and κ is thermal conductivity. Its application in energy generation is limited, however, mainly due to the materials limited availability, low material stability, and high manufacturing cost. Bulk silicon, which is abundant and well-engineered, has never been considered for TE applications due to its high lattice thermal conductivity (150 W/m·K). [9]Porous silicon, on the other hand, with randomly distributed and intertwined pores, could achieve extremely low thermal conductivity down to 0.1 W/m·K.[10] However, the electronic structure of this disordered porous silicon is severely deteriorated, which yields very poor electrical conductivity and thus a low ZT. [11] Recent work has shown that by either using nanowires with diameters much smaller than the bulk phonon mean free path (MFP) or roughening the nanowire surface, a near 100-fold suppression in lattice thermal conductivity is observed, resulting in a ZT that is dramatically enhanced from 0.01 for the bulk to 0.4~0.6[12, 13]. However, Si nanowires' weak mechanical strength and strong dependence on both diameter and detailed surface morphology remain as big challenges for large scale implementation. The thermal transport properties of silicon nanowires not only highly depend on its diameter/size, [12, 14, 15] but also on their nanoscopic surface morphology. [12] Thus, the synthesis of high density and highly uniform nanostructures is a key challenge for realizing high performance silicon nanowire based TE modules.

To overcome these problems inherent to the nanowire system, we report the enhanced thermoelectric performance of a new type of nanostructure, holey silicon (HS), where high density nanoscopic holes are created in thin, single-crystalline silicon membranes. These HS nanostructures exhibit good mechanical strength and reproducibly low thermal conductivity while maintaining sufficient electrical quality. These characteristics make them viable candidates for TE applications. HS was prepared using either nanosphere lithography (NSL) or block copolymer (BCP) lithography, yielding holes with pitches of 350 nm, 140 nm and 55 nm. Our results show that the thermal conductivity of 55 nm-pitch HS can be as low as 1.14-2.03 W/m·K. In the HS system reported here, we propose that a "necking effect" is the main mechanism of reducing thermal conductivity based on our experiments and previously reported simulation. [16] Without significantly sacrificing the thermoelectric power factor, $S^2\sigma$, we demonstrate that HS behaves as a phonon glass and electron crystal[17] with ZT ~0.4 at room temperature. Additional improvement could be achieved by further optimization of the electrical doping, as well as the pitch and porosity of the holes. The scalability of the BCP lithography process and the promising thermoelectric properties make HS superior for practical thermoelectric power generation.

The preparation of large scale HS films is based on deep reactive ion etching (DRIE) of silicon-on-insulator (SOI) substrates (100 nm device layer, confirmed by SEM cross section) masked by thin chromium masks templated by either NSL or self-assembled BCP film (details in SI). This method yields uniform 55 nm, 140 nm, or 350 nm pitch HS with porosity of ~35%. Specifically for 55 nm pitch HS, the self-assembled BCP holey pattern (Figure 1a) is transferred to the HS film through DRIE.

For transport measurements and SEM/TEM characterization, all HS films were tailored into individual ribbons (1-3 μm x 20-50 μm) by standard photolithography, then released from the SOI substrate by etching the buried oxide layer in hydrofluoric acid vapor. The TEM image (Figure 1b) shows that the HS ribbon has uniform hole size and separation distance with ordered hexagonal packing. As shown in Figure 1b inset, the selected area electron diffraction (SAED) pattern recorded along the [100] zone axis confirms the single-crystallinity of the entire HS ribbon, which is consistent with the starting SOI device layer. The sidewalls of the holes have a layer of 1-2 nm native oxide, as shown in Figure 1c.

The thermal transport properties of the HS ribbon were characterized by microelectromechanical systems (MEMS) devices, [18] which consist of two suspended silicon nitride (SiN_x) membranes patterned with platinum heating/sensing coils and separated by 10-30 μm. The HS ribbons were placed between the two membranes using a micromanipulator, then anchored to the membrane by a ~300 nm thick Ni bonding patch that was evaporated through a SiN_x stencil mask (Figure 1d). The thermal contact resistance was estimated by comparing the thermal conductance of Ni bonded silicon ribbon to monolithically integrated silicon ribbon (Figure S4, SI) and was confirmed to be less than 10% of total resistance for all the HS ribbons measured (Figure 2a-c).

Figure 2d shows the temperature dependent thermal conductivity of HS with different pitches in comparison to a non-holey ribbon and amorphous silica. [19] The room temperature thermal conductivities of all silicon ribbons are also summarized in table1 for comparison. With similar porosity (φ~35%), the HS ribbons show a clear trend of thermal conductivity reduction as a function of pitch size. This dependency deviates from

the classic Eucken model, [20] $\kappa_{porous}/\kappa_{solid}=(1-\varphi)/(1+\varphi/2)$, indicating κ should be 42W/m·K for all 35% HS which is only valid when the material dimensions are much larger than the phonon MFP. The dramatic discrepancy to the Eucken model across the entire temperature range demonstrates that phonon size effect is very important among these HS dimensions and will be discussed latter. In addition, the peak of the thermal conductivity vs. temperature curve (Umklapp peak) is shifted to higher temperature as the pitch size decreases, suggesting phonon-phonon scattering contributes minimally in limiting the thermal transport in these structure ($T_{U\text{-}peak}$ ~130 K for nonholey ribbon, $T_{U\text{-}peak}$ ~200 K for 350 nm pitch HS, and $T_{U\text{-}peak}$ >300 K for both 140nm and 55nm pitch HS.). In Figure 2e, we further compare the temperature dependent thermal conductivity at low temperature region (30-60K), and a clear trend on temperature power rule (T^3 for bulk) is also observed indicating specific scattering effect is decreasing the temperature power to ~1.1 for 55nm HS. [15] These intriguing thermal properties imply that the phonon size effect in the holey structure presented here is quite important and can effectively suppress thermal conductivity beneficial for TE application.

It can be seen that the thermal conductivity of the 55 nm pitch HS is comparable to that of amorphous silica. [19] To verify the reproducibility of the low thermal conductivity in HS, multiple samples are prepared in different batches, and consistently low values, ranging from 1.14 to 2.03 W/m·K at room temperature, are routinely recorded (see Figure S5, Table S1 in SI for detail). The cause of variation is mainly due to the slight difference in porosity among samples, resulting from the block copolymer quality and etching conditions. Also, no dependence of the thermal conductivity on ribbon width, ranging from 0.79 μm to 2.35 μm, is observed, suggesting that the phonon transport is

dominated by the HS morphology. This represents a distinct advantage of HS over nanowire systems, in which the performance varies significantly with diameter and detailed surface morphology. [12, 13]

Compared with silicon nanowires, one key feature of the HS structure is that the width of thinnest part, or neck (n), is considerably less than the pitch size (p), such that n/p~0.42 for samples with 35% porosity. This geometry is very different to nanowires, wherein the surface roughness (h) is much less than its diameter (d), making h/d <0.1. [12] For 55nm pitch HS with 35% porosity, the neck is approximately 20nm in width. However, this 55 nm pitch HS gives significantly lower thermal conductivity than that of 22nm silicon nanowire, reported previously as ~7 W/m·K. [14, 15] In our HS system where n/p is much larger, phonons can experience more backscattering by reflecting from the nanohole sidewalls. We propose that this feature plays an extremely important role in dramatically decreasing the thermal conductivity.

Several theoretical studies have been reported on similar porous structure. [8, 16, 21] In particular, Hao *et al.* reported a Monte Carlo simulation of phonon transport in silicon with square arrays of holes considering frequency dependent phonon MFP, which increased the accuracy of their model. [16] The trend of pitch dependent thermal conductivity reduction experimentally shown in the HS system is similar to the model result, yet the experimental value is smaller than the prediction. We attribute the difference to the surface scattering in 100nm thick film, porosity difference, small surface roughness created by the DRIE, and the difference between square array and hexagonal array (see details in Figure S6 and SI). Their simulation observed that when the distance of adjacent holes is smaller than phonon MFP, a phonon can be "trapped" behind

the hole, which creates a local negative temperature gradient opposing the linear temperature gradient along a free channel. We address this phenomenon as a "necking effect" which requires necking morphology with pitch size be smaller than the phonon MFP. Additionally, it raises two distinguishing thermal behaviors observed in our experiment. Firstly, as the HS pitch size gets smaller, the percentage of phonons with MFP (frequency dependent) greater than the pitch will increase, which should result in a stronger necking effect and lower overall κ, as is the trend observed in Figure 2. Secondly, the necking effect should become more significant as the "neck" become thinner while maintaining a fixed pitch. To verify this effect, 350nm pitched HS was prepared with differing neck widths, ranging from 160nm to 40nm, by change porosity from 13% to 40%. After normalizing the porosity, the results clearly show that the thermal conductivity decreases with neck width. (see also Figure S6, compared in parallel with theoretical prediction). It is also worth mentioning that the imperfection of holes packing in our HS could introduce additional scattering on broader range of phonon spectra, which is beneficial for κ reduction.

Since the electron MFP in highly doped silicon (~$1x10^{19}$ cm^{-3}, optimal for thermoelectric application) is ~ 1-10 nm which is smaller than the 55nm pitch, there is no analogous necking effect on the electrical properties. Therefore, the power factor (S^2/ρ) of HS should not be degraded, resulting in a net increase in ZT. To this end, we measured all the thermoelectric properties (S, ρ, and κ) of the 55nm pitch HS to evaluate its ZT. The SOI were doped with Boron at 830°C for 1 hour in a customized BCl_3 doping furnace to achieve a doping level ~$5x10^{19}$ cm^{-3} (confirmed by hall measurement), then 55nm pitch HS ribbon was prepared as described previously. Four probe electrical

contacts parallel to a platinum heating coil were patterned using photolithography for both ρ and S measurements (device details are shown in Figure S7 and SI; the result is shown in Figure 4a). The post-doped HS showed a thermal conductivity of ~1.73 W/m·K at room temperature, not significantly different from the un-doped holey ribbons (Table 1). With this doping concentration, the electronic contribution of thermal conductivity, $\kappa_e = L \cdot T \cdot \sigma$ is about 0.21 W/m·K (Lorenz number, $L = 2.2 \times 10^{-8}$ $J^2K^{-2}C^{-2}$, is defined by Wiedemann–Franz law for degenerate doping), leading to a lattice thermal conductivity, κ_{ph} of 1.52 W/m·K.

For comparison, Figure 3b shows the ratios of the thermal conductivity κ and thermoelectric power factor S^2/ρ for holey and non-holey controls as a function of temperature. The HS shows 34 times suppression of thermal conductivity compared with the non-holey silicon ribbons, and 85 times suppression compared with bulk silicon at room temperature, with greater decreases observed at lower temperature in both cases. A moderate deterioration of the thermoelectric power factor is also observed as compared with optimally doped non-holey Si ribbons (Note both κ and ρ of HS are normalized by porosity). The lower thermoelectric power factor is mainly due to the decreased electrical conductivity from carrier depletion by surface states. This is confirmed experimentally as the electrical conductivity enhancement is observed by surface passivation with atomic layer deposition of Al_2O_3, and is currently under investigation for additional ZT enhancement.

Over the entire temperature range of our measurements, the ZT enhancement factor remains ~50 times in comparison to non-holey silicon of the same thickness (Figure 3c). From 150K to 300K, the ZT of HS increases with temperature and is 0.4 at

300K. Comparing with thin and rough silicon nanowire systems, these HS nanostructures exhibit reliable thermoelectric performance due to the necking effect while having much better mechanical strength. As mentioned above, the thermoelectric properties of these holey silicon nanostructures have no dependence on ribbons width, making them even more amenable for TE module integration. Higher ZT values than the one reported here can be obtained by further optimization of the doping level, the pitch/neck ratio, and effective surface passivation. Because of the scalability of this process, an immediate application for these holey silicon nanostructures could be on-chip thermal management for solid state devices, while large scale waste heat recovery is also conceivable by extension to bulk materials system.

Acknowledgements

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Figure legends:

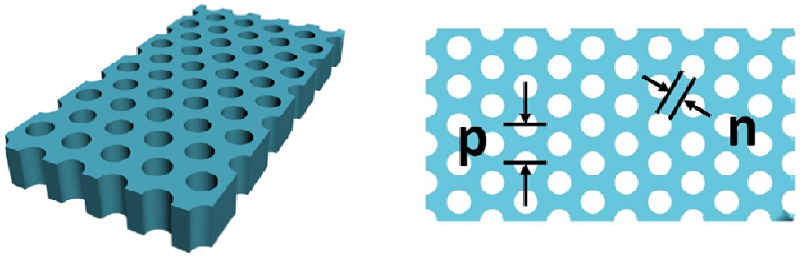
Figure 1 | Structural characterization of 55nm pitch HS ribbon. a, AFM topography image of BCP holey pattern with Fourier-transform pattern (inset) indicating the long range order. **b,** Bright field TEM image of a section of HS ribbon. The porosity is estimated as ~35% through the entire ribbon. SAED pattern (inset) indicates its single crystalline nature. **c,** High-resolution TEM of the edge of a hole showing ~2 nm thick surface native oxide. **d,** SEM image of the thermal measurement device. Between two suspended SiN_x membranes, a 55nm-pitch HS ribbon is bonded by 300nm Ni. Scale bars for **a** and **b** are 1 μm, **c** is 5 nm, and d is 10 μm.

Figure 2 | Thermal conductivity of HS ribbons with different pitch. SEM images of **a,** 350 nm pitch, **b,** 140 nm pitch, and **c,** 55 nm pitch HS ribbon for thermal measurement. All scale bars are 1μm. **d,** Temperature dependent κ of non-holey (black squares), 350 nm (red squares), 140 nm (green squares), 55 nm pitch (blue squares) HS ribbon, and amorphous silica (empty squares from **ref 19**). Error bars for all three holey ribbons are smaller than the data points. **e,** Low temperature data on a logarithmic scale with T^3, T^2, and T^1 curves for comparison guidelines.

Figure 3 | Thermoelectric properties and ZT calculation for 55 nm pitch HS ribbon. a, Temperature-dependent ρ (black squares) and S (red squares) of a boron doped 55 nm pitch HS ribbon. (hole concentration ~$5x10^{19}$ cm^{-3} from hall measurement). The room temperature S^2/ρ= 2.28±0.59 mW/m·K **b,** κ comparison of doped 55 nm pitch HS ribbon with doped non-holey silicon ribbon (black squares), or bulk silicon (open squares, 1.7x 10^{19} cm^{-3}, As-doped, from **ref 9**); S^2/ρ comparison (red squares) of doped 55 nm pitch HS ribbon with non-holey silicon ribbon. **c,** ZT of 55 nm pitch HS ribbon (red squares) compared with non-holey ribbon (blue squares) shows ~50 times enhancement. With consideration of measurement error from both ρ (4.7%), S (3%) and κ (6%), the ZT shows 16.7% uncertainty at 95% confidence.

Table legends:

Table 1 | Summary of the HS geometry and the thermal conductivity at 300K. Note: All ribbons are 100nm in thickness. All κ are normalized by φ. Samples are all intrinsic (phosphorus doped, ~$3x10^{14}$ cm^{-3}), except of *****(boron doped, ~$5x10^{19}$ cm^{-3}) used for ZT.



	avg. pitch, p (nm)	avg. neck, n (nm)	avg. porosity, φ (%)	κ ($Wm^{-1}K^{-1}$)
non-holey	—	—	0	50.9 ± 2.0
non-holey*	—	—	0	47.6 ± 1.7
350-pitch	350	152	~35	10.23 ± 0.44
140-pitch	140	59	~35	6.96 ± 0.34
55-pitch	55	23	~35	2.03 ± 0.07
55-pitch*	55	23	~35	1.73 ± 0.06

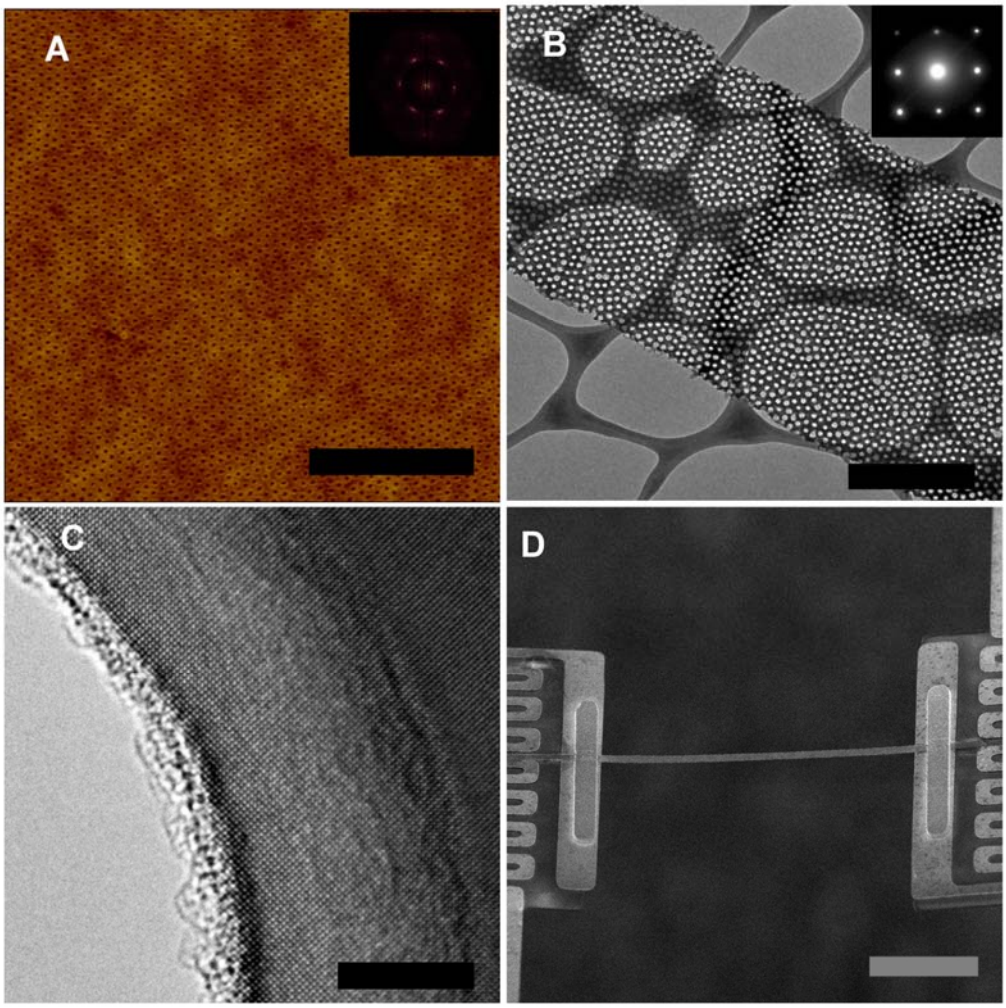


Figure01

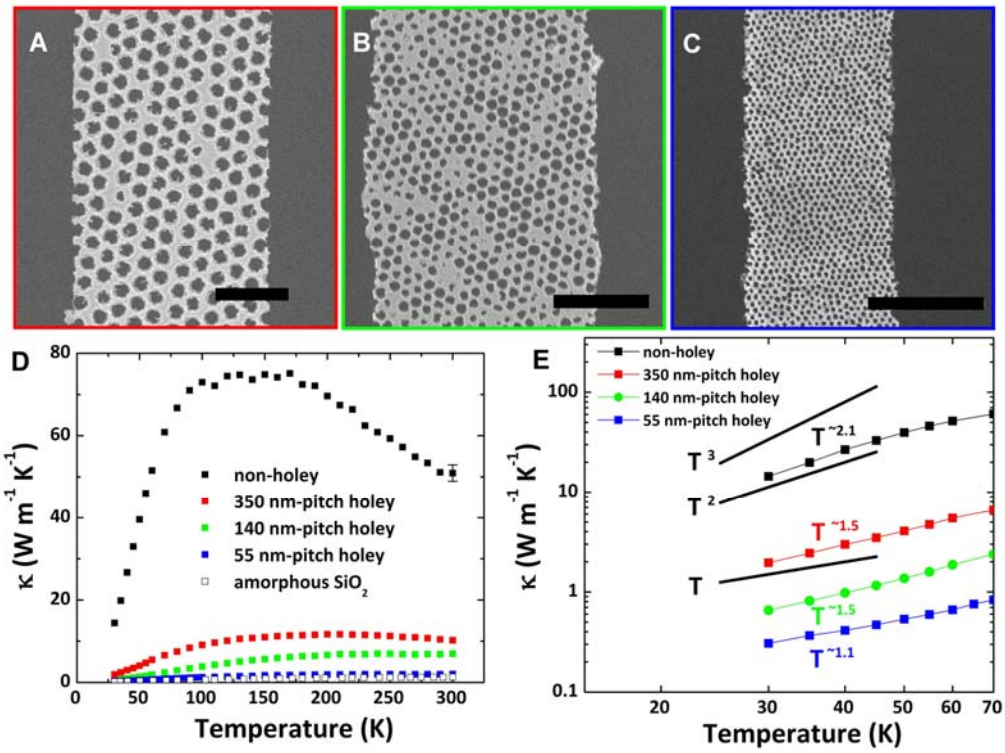
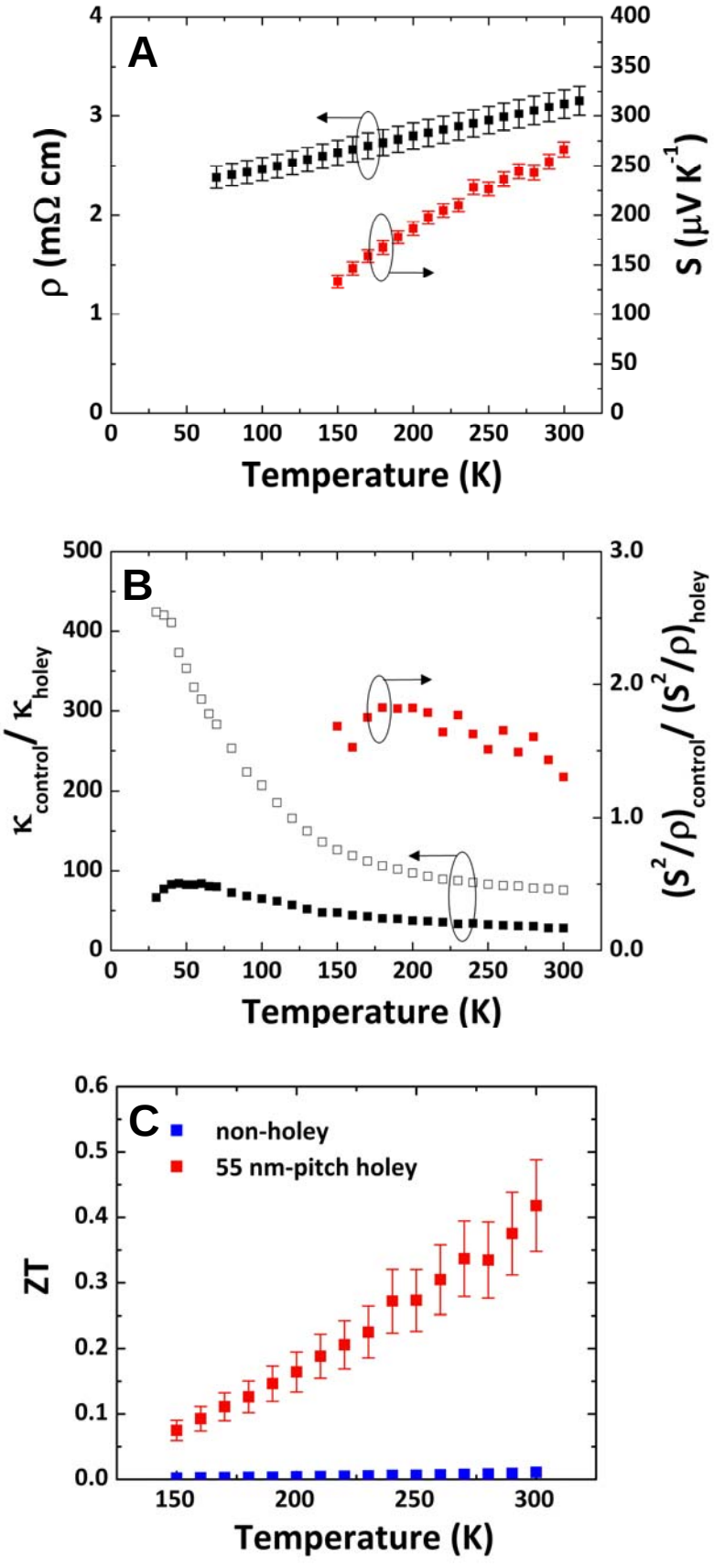

A
B
C
D
κ (W m-1 K-1)
non-holey
350 nm-pitch holey
140 nm-pitch holey
55 nm-pitch holey
amorphous SiO2
Temperature (K)
E
non-holey
350 nm-pitch holey
140 nm-pitch holey
55 nm-pitch holey
T3
T2
T
T~2.1
T~1.5
T~1.5
T~1.1
κ (W m-1 K-1)
Temperature (K)

Figure02


A
ρ (mΩ cm)
S (μV K-1)
Temperature (K)
B
κcontrol / κholey
(S2/ρ)control / (S2/ρ)holey
Temperature (K)
C
non-holey
55 nm-pitch holey
ZT
Temperature (K)

Figuer03