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Homo-Junction Bottom-Gate Amorphous In–Ga–Zn–O TFTs With Metal-Induced Source/Drain Regions

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ABSTRACT A fabrication process for homo-junction bottom-gate (HJBG) amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs) is proposed, in which the a-IGZO section as source/drain (S/D) regions is induced into a low resistance state by coating a thin metal Al film and then performing a thermal annealing in oxygen, with the channel region protected from back etching by depositing and patterning a protective layer. The experimental results show that with a 5 nm Al film and annealing at 200 °C, the sheet resistance of the S/D a-IGZO is reduced to 803 Ω/□, and keeps stable during a subsequent thermal treatment. In addition, the thin Al_2O_3 film generated by the annealing contributes to an improved thermal stability and ambient atmosphere immunity for the fabricated HJBG TFTs.

INDEX TERMS Amorphous indium–gallium–zinc oxide, thin-film transistors, homo-junction, aluminum reaction.

I. INTRODUCTION

Amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs) have been intensively investigated since being reported in 2004 by Nomura *et al.* [1]. Such transistors exhibit superior performances compared to conventional silicon-based TFTs and are thereby considered a promising active device for next-generation display applications [1]–[4]. In particular, their fabrication process is potentially comparable to existing amorphous silicon (a-Si) TFT production technology in terms of manufacturing cost and simplicity [5].

A TFT can either have a top-gate or bottom-gate structure. For a bottom-gate structure, two processes are mainly used for the fabrication of a-IGZO TFTs at present: back channel etching (BCE) process and etch stop layer (ESL) process [6], [7]. The BCE process is usually preferable due to the fewer photolithographic masks and fabrication steps [6], [7]. However, the back channel etching step turns out to be very difficult to handle and usually substantially degrades the device performances [8]–[10]. The ESL-based process produces a channel layer that is free of back etching, enabling a high device performance [8], [9], [11]. However, it usually requires more masks, leading to a highly increased production cost [6], [7]. In particular, this process also induces a large parasitic capacitance and makes it difficult to shrink the TFT channel length [6]–[8]. These factors largely limit its application in high-end products.

Recently, an alternative process called a homo-junction bottom-gate (HJBG) process was proposed to address the issues associated with the BCE and ESL processes mentioned above [12]–[14]. In the HJBG structure, both source/drain (S/D) and channel sections are composed of the same oxide semiconductor layer such as a-IGZO, and the S/D section is heavily doped to be highly conductive. This is different from the BCE and ESL cases, where the S/D section is a stack of metal and oxide films. The methods proposed thus far for the forming of the homo-junction S/D regions include Ar [14], [15] or H_2 plasma treatments [14]

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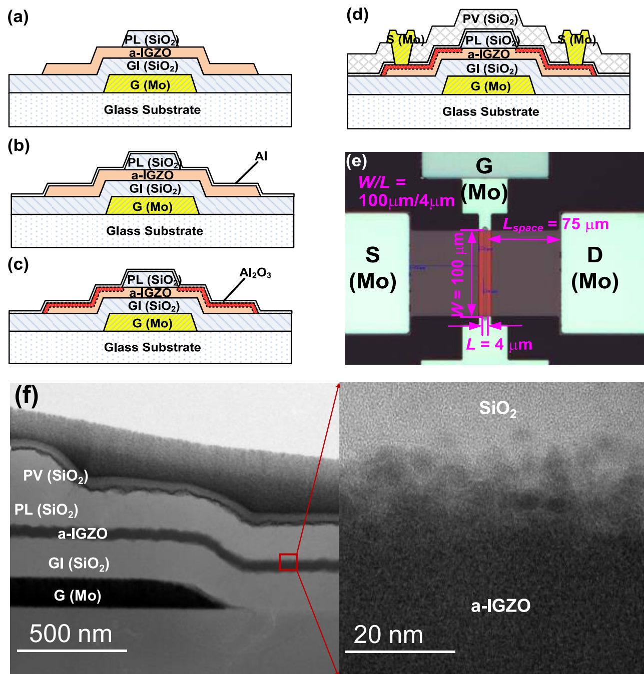

FIGURE 1. (a)–(d) Schematic fabrication steps for a homo-junction bottom-gate a-IGZO TFT, (e) top view of a fabricated a-IGZO TFT, (f) TEM image of a fabricated a-IGZO TFT.

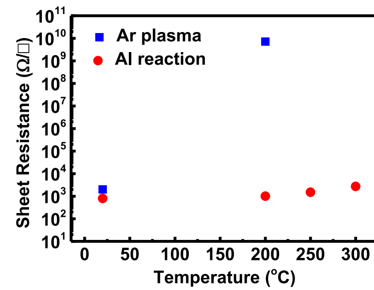

FIGURE 2. Sheet resistance of the source/drain regions treated by Ar plasma or Al reaction versus the post thermal treatment temperature.

and hydrogen diffusion from SiN_x [12], [13], [16]. For the Ar plasma approach, the initially induced low resistance S/D regions could not be well maintained since the oxygen vacancies induced by ion bombardment are largely reduced during the subsequent thermal process [17], [18]. Although the thermal stability of the Ar plasma treated S/D regions could be improved by applying an appropriate substrate bias power during the plasma treating process, a narrow process window was resulted [19]. For the hydrogen-related doping methods, the stability and uniformity, as well as the scalability of the fabricated devices, are the main concerns due to the high diffusivity of hydrogen atoms [20]–[23]. Therefore, the HJBG processes proposed thus far are unlikely to be applicable for mass production. Recently, a metallic S/D forming method was proposed for the fabrication of self-aligned top-gate oxide TFTs [18], [24]–[26]. Though top-gate technology is able to minimize the parasitic capacitance, it needs a back light shielding layer for the channel region, leading to a complex process.

In this work, we propose a new HJBG fabrication process for a-IGZO TFTs. The metal Al reaction is employed to form the high conductive S/D regions of the bottom gate TFT. It will be demonstrated that the fabricated HJBG a-IGZO TFTs in this process have a high electrical performance, strong channel-length scalability, excellent thermal stability in S/D resistance, and high immunity to ambient-atmosphere.

II. EXPERIMENTAL DETAILS

Fig. 1 (a)–(d) show cross-sectional schematic fabrication steps for the proposed HJBG a-IGZO TFTs. First, a 120 nm Mo film was deposited as the gate electrode (GE) by direct-current (DC) sputtering. Then, a 200 nm SiO_2 film was deposited as the gate insulator (GI) at 300 °C by plasma-enhanced chemical vapor deposition (PECVD). Then, a 50 nm a-IGZO film was deposited by DC sputtering at room temperature and patterned to form the active island by wet etching. Next, PECVD was used to deposit a 200 nm SiO_2film at 150 °C as the protection layer (PL), followed by removal of the PL section on the S/D regions by dry etching (Fig. 1(a)). Then, a 5 nm Al film was sputtered onto the exposed a-IGZO layer as the S/D regions (Fig. 1(b)) before thermal annealing in oxygen ambient at 200 °C for 1.5 hours. During the annealing process, the Al reacted with the underlying a-IGZO, generating the Al_2O_3 film on the surface and oxygen vacancies in the a-IGZO (Fig. 1(c)). Thus, the S/D a-IGZO section was highly conductive and self-aligned to the SiO_2 PL. Afterwards, 200 nm of SiO_2 was deposited as the passivation layer at 150 °C by PECVD. Finally, S/D electrodes were formed by Mo via contact holes (Fig. 1(d)). It is seen from the process that the active layer does not encounter any etching step, similar to the case of the ESL process, with the channel length (L) defined by the PL length and the parasitic capacitance determined by the underlap length between the GE and PL, similar to the case of the BCE process. Therefore, the proposed process has the advantages of both BCE and ESL processes.

For comparison, a-IGZO TFTs with S/D regions treated by Ar plasma instead of the Al reaction were also fabricated. The Ar plasma treatment was performed immediately after dry etching the SiO_2 PL. The treatment time was 90 s at room temperature with a radio frequency power of 50 W.

The electrical characteristics of the TFTs were measured using an Agilent B1500 semiconductor parameter analyzer at room temperature in the dark.

III. RESULTS AND DISCUSSION

Fig. 2 shows the sheet resistance of Al- and Ar plasma-treated a-IGZO films versus the post thermal annealing temperature. The annealing was carried out in oxygen ambient for 1 hour. It is seen that the sheet resistance of the Al-treated a-IGZO increased slightly from 803 Ω/□ to 2724 Ω/□. In contrast, the sheet resistance of the Ar plasma treated a-IGZO

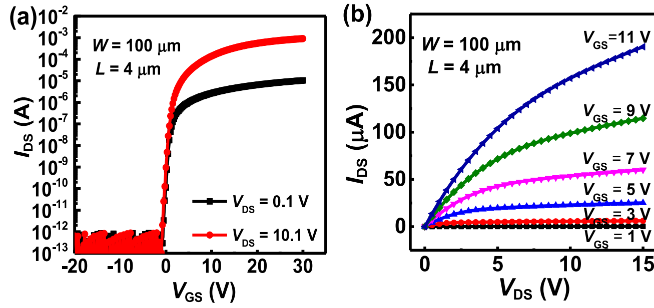

FIGURE 3. Current–voltage (*I* − *V*) characteristics of a TFT fabricated using the proposed Al reacted HJBG process, with (a) transfer and (b) output characteristics shown.

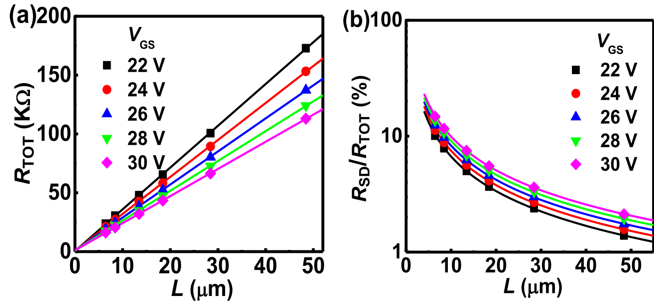

FIGURE 4. (a) Total resistance (R_{TOT}) and (b) ratio of source/drain parasitic resistance to the total resistance (R_{SD}/R_{TOT}) versus channel length for varying gate voltages.

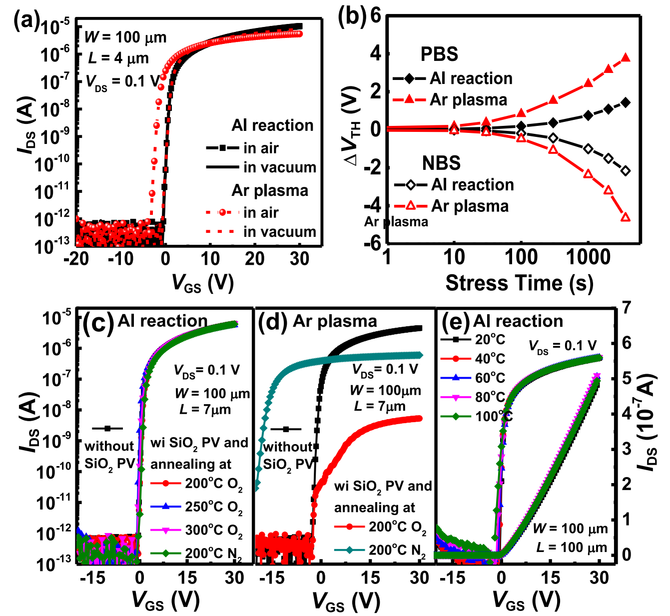

FIGURE 5. (a) Transfer characteristics of the Al- and Ar plasma-treated a-IGZO TFTs without passivation measured in air and in vacuum, (b) time-dependent threshold voltage shifts (ΔV_{TH}) of the Al- and Ar plasma-treated a-IGZO TFTs without passivation under both 20 V positive-bias stress (PBS) and −20 V negative-bias stress (NBS) for 3600 s measured in air, (c) and (d) transfer characteristics evolutions of the Al- and Ar plasma-treated a-IGZO TFTs respectively after passivation and annealing, and (e) transfer characteristics evolution of the Al-treated a-IGZO TFTs under different working temperatures.

increased drastically by more than six orders of magnitude, from 1994 Ω/□ to 7.14 × 10^9Ω/□, after the thermal annealing at 200 °C. The depth profile analysis by secondary ion mass spectrometry (SIMS) revealed that Al diffused into the a-IGZO layer by a depth of approximately 13 nm after the one hour annealing (data not shown here), which is similar to the result reported by Morosawa *et al.* [18].

Fig. 3 shows the current–voltage (*I* − *V*) characteristics of a HJBG TFT fabricated using the proposed process, with (a) the transfer and (b) output characteristics. The a-IGZO TFT with a channel length of 4 μm shows a subthreshold swing (*SS*) of 0.26 V/decade, a field-effect mobility (μ_{FET}) of 9.24 cm^2/V·s, a threshold voltage (V_{TH}) of 2.11 V, and an on-to-off current ratio (I_{ON}/I_{OFF}) exceeding 1 × 10^9 at V_{DS} = 10.1 V. From the output characteristics, no current crowding phenomenon is observed in the linear region, indicating that the source/drain parasitic resistance (R_{SD}) is low.

Fig. 4 shows (a) the total resistance (R_{TOT}) and (b) the ratio of R_{SD} to R_{TOT} versus channel length at different V_{GS}. R_{TOT} is calculated from the transfer characteristics at $V_{DS} = 0.1$ V with various channel lengths. The width normalized R_{SD} ($R_{SD}W$) can be extracted from the intercept of the fitting lines by the transfer length method (TLM), and is evaluated to be 24 Ω·cm, which is comparable to that (10.4 Ω·cm) of BCE-type a-IGZO TFT with Al-doped ZnO S/D electrodes in our previous work [10]. For a conventional ES-type a-IGZO TFT with metal S/D electrodes, the typical $R_{SD}W$ value was about 100 Ω·cm [11]. Moreover, as shown in Fig. 4(b), the R_{SD}/R_{TOT} ratio is about 23 % at V_{GS} = 30 V for the device with $L = 4$ μm. The ratio is slightly large. It is worth mentioning that the R_{SD} in this work was surely overestimated due to the non-optimized layout design. Note that the distance from the metal contact to the a-IGZO channel is approximately 75 μm, which is much longer than what is necessary, as shown in Fig. 1(e). With an optimal layout, the R_{SD} could be definitely further reduced. In addition, the shrinkage of the channel length ΔL is evaluated to be around 0.5 μm, much smaller than that for S/D regions formed by H doping [12]. This result implies that the incorporation of hydrogen into the S/D regions during PECVD of the SiO_2 layer can be effectively blocked by the generated Al_2O_3 film.

For comparison, Ar plasma-treated TFTs with and without a passivation layer were also fabricated. For the passivated device, following the Ar plasma treatment, a 200 nm SiO_2 passivation layer was deposited, and a thermal annealing was subsequently performed at 200 °C in oxygen for 1.5 hours. For the device without passivation, Mo contact electrodes were formed immediately after the Ar plasma treatment, without subsequent thermal treatment. Fig. 5 (a) shows the transfer characteristics measured in air and in vacuum for the Al- and Ar plasma treated a-IGZO TFTs without passivation, respectively. While the Ar plasma-treated TFT shows a lower V_{TH} in air, the Al-treated TFT shows nearly identical characteristics in both cases. The lower V_{TH} for the Ar

plasma-treated TFT in air can be explained by the adsorption of water molecules on the a-IGZO back channel surface [27]. This result implies that the SiO_2 PL alone cannot protect a-IGZO TFTs from the invasion of water molecules. For the Al-treated TFT, the thin Al_2O_3 layer formed by thermal oxidation of the thin Al film enhances the passivation effect, leading to excellent environmental stability. In addition, it is seen that the Al-treated TFT shows a higher on-current compared to the Ar plasma-treated TFT. The extracted $R_{SD}W$ values for Al- and Ar plasma-treated TFTs are 24 Ω·cm and 124 Ω·cm, respectively. The lower R_{SD} for the Al-treated TFT is responsible for the higher on-current.

Fig. 5(b) shows the time-dependent threshold voltage shifts (ΔV_{TH}) of the Al- and Ar plasma treated a-IGZO TFTs without passivation measured in air under both the positive-bias stress (PBS) and the negative-bias stress (NBS). As shown, the Al-treated a-IGZO TFT shows better stability under both the PBS and NBS. The stability improvement in the Al-treated devices can also be explained by the prevention of the ambient effect due to the effective protection of the channel layer by the thin Al_2O_3 layer [28].

Fig. 5(c) and (d) show the evolutions of the transfer characteristics of the Al- and Ar plasma treated a-IGZO TFTs after deposition of the SiO_2 passivation layer and annealing in O_2 or N_2 for 1.5 hours. For the Al-treated TFT, no noticeable change in the transfer curves is observed after passivation and annealing. In contrast, for the Ar plasma-treated TFT, the on-current is significantly lowered after passivation and annealing, which results from a remarkably increased S/D resistance. This result suggests that the annealing induces a significant reduction of the oxygen vacancies previously generated in the source and drain regions by the Ar plasma treatment. Fig. 5(e) shows the transfer characteristics evolution of the Al treated a-IGZO TFTs under different temperatures. A slight increase in subthreshold current with temperature is observed, which can be ascribed to the thermally activated carriers from traps in the band gap of a-IGZO. The evolution is similar to that observed in a-IGZO TFTs with metal S/D electrodes [29], [30], implying that the Al-treated S/D regions do not bring about additional temperature instability issue.

IV. CONCLUSION

We have demonstrated a novel process for fabricating homojunction bottom-gate a-IGZO TFTs. By coating a thin Al film and then performing thermal annealing, the fabricated HJBG TFTs have been demonstrated to exhibit a low S/D sheet resistance, which is comparable to or even lower than that obtained for TFTs fabricated using a conventional ES process. In addition, the thermally oxidized thin Al_2O_3 film can block hydrogen diffusion and H_2O invasion and can thus enhance the passivation effect. As a result, the HJBG TFTs fabricated using the proposed process show excellent electrical performance, high thermal stability, and strong immunity to ambient atmosphere.

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