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Keywords

Virtual prototyping, Silicon Carbide (SiC), Transformer, Converter control, ZVS converters

Abstract

A 100 kW, isolated dc–dc converter was built over the course of one year, starting from a blank page. This paper details the design and manufacturing process, and reflects in particular on the strengths and weaknesses of computer-based modelling and simulation tools.

1 Introduction

Many research articles have been dedicated to the optimal design of converters [1, 2, 3]. It may appear that nowadays, building a new converter is only a matter of writing down some specifications, and then applying a design procedure. However, as we designed and built a new converter (i.e starting from a "blank page" instead of improving upon an existing design) in a limited time (12 months), we found that we had to rely heavily on assumptions and arbitrary decisions. This paper presents an overview of the design procedure which led to a working converter, with the objective of identifying the strengths and weaknesses of the process.

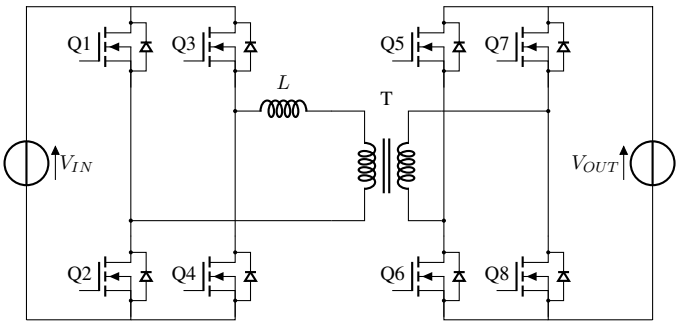
As a power converter is a complex system which requires multi-physics simulations (electrical, electromagnetic, thermal, mechanical...), several modelling approaches have been proposed in the literature: [4] describes a set of design tools mainly based on finite-elements (FE) modelling (associated with a circuit simulator), to take advantage of its accuracy. On the contrary, [5] introduces a method to generate analytical models, which are much faster to solve than finite-elements. In some cases, a single, accurate FE simulation can be used to identify the parameters of fast compact models, allowing faster subsequent runs [6].

System simulation of a power converter can be performed using dedicated system modelling language such as VHDL-AMS [7] or Modellica, or using circuit simulators (Saber, SPICE, Simplorer, PSIM...), with non-electrical quantities (such as temperature) calculated using equivalent circuit models. In any case, as the system becomes more complex, simulation time increases drastically. This is particularly true for time domain simulations of power electronic converters, which require a sub-nanosecond resolution (for switching transients) over milliseconds periods (to capture the fundamental frequency of signals), and ideally even minutes (to reach thermal equilibrium).

In this paper, we describe the design of a complete converter from the bottom up, including custom power electronic modules rather than off-the-shelf components. This is mainly justified by the lack of suitable components at the time, but also by the objective of evaluating the performance of the commercial design tools.

Parameter	Value
Function	dc–dc converter
Power flow	Bi-directional
Input voltage (V_{IN}) range	900 – 1200 V
Output voltage (V_{OUT}) range	450 – 600 V
Conversion Ratio at full load (a)	0.5 $\pm$10 %
Nominal Power (P_{dc})	100 kW
Conversion efficiency (η) at a=0.5	$\geq$ 98 %
Switching Frequency (f_S)	20 kHz
Switches technology	SiC MOSFETs
Max. volume	200 L
Ambient temperature	30 °C
Cooling system	air-cooled

(a)



(b)

Figure 1: (a): List of specifications and arbitrary design choices used as an input to the design process. (b): Circuit diagram of the chosen converter topology: a Dual Active Bridge (DAB). The transformer has an input/output ratio of 2. The input and output capacitors are not depicted here.

An isolated dc–dc converter, the central part of a solid-state transformer (SST, [8]), was chosen as the application case. Such converters have applications in traction [9], wind turbines [10], etc. Here, we focused on a 100 kW, 1200 V/600 V bidirectional, isolated dc–dc converter.

Silicon IGBTs are commonly used as the power switches in this power/voltage range [11]. As recent improvements in SiC technology [12] have resulted in the commercial availability of 1200 V and 1700 V MOSFETs and Schottky Barrier Diodes (SBDs), we focused on SiC power switches in this paper. Indeed, replacing Si IGBTs and diodes with SiC MOSFETs and SBDs in a comparable 100 kW dc–dc converter was shown in [13] to result in a clear improvement in efficiency: 96.9 % at 60 kW max. output power for Si vs 97.9 % at 100 kW max. output power for SiC, while at the same time allowing a much higher switching frequency (20 kHz for SiC and 4 kHz for Si).

The next section briefly introduces the specifications of the converter, and the preliminary design stage which resulted in the selection of the converter topology (as well as some other general design parameters). Section 3 then details the design process all the way up to the physical implementation. The manufacturing and test of the converter are described in Section 4. The design process and its outcome are then discussed in section 5 and a conclusion is given in section 6

2 Pre-design

The specifications of the converter described in this paper are given in Fig. 1a. Some of them are purely functional (input/output voltage, nominal power, target efficiency…), and some are arbitrary design choices (switches technology, switching frequency). These specifications are then used to assess the many dc–dc converter topologies available [10] (Dual Active Bridge – DAB – with or without resonance, resonant converter…). This process of evaluating the topologies is conducted with theoretical analysis and circuit simulations (using ideal components). It is described in more details in [10], and is beyond the scope of this paper. The selection of the most suitable topology is based on the expected efficiency (transformer and power electronics), technical complexity and cost. Regarding the transformer, since its technology and geometry are not yet selected at this stage, the level of each current harmonic is used as a criterion for the losses estimation [14]. For the power electronic switches, conduction and switching losses are estimated based on the datasheets of the SiC dies [15] (on-state resistance and switching energy). The list of possible SiC dies is limited to only two references from Wolfspeed (one 1700 V and one 1200 V-rated MOSFET, along with the corresponding SBDs), because they are the only devices readily available at the time of the pre-design (2014). At this stage of the design, the number of dies to be used per switch position is simply based on their recommended RMS current (as quoted in their datasheet), without any thermal consideration.

As a result of this pre-design stage, a non-resonant DAB topology [16] is selected (Fig. 1b). The leakage inductance L of the Medium Frequency Transformer (MFT) is a key element for the performance of the DAB converter, as it dictates the phase shift between the primary and secondary inverters: if too

Table I: Outcome of the pre-design stage.

Parameter	Value	Comment
General		
Topology	Non-resonant DAB	
Minimum power transfer	1 kW	(arbitrary) 1 % of the nominal power
Transformer		
Apparent power	180 kVA	
Primary nominal voltage range	900-1200 V	specifications from Tab. 1a
Maximal RMS current on primary	150 A	calculated from the ideal waveforms
Operating frequency range	17-23 kHz	arbitrary: $\pm$ 15 % frequency variation allowed for control
Turns ratio (N2/N1)	0.5	specifications from Tab. 1a
Leakage Inductance	$< 10\,\mu$H	final objective 10 – 25 µH, to be adjusted using a series inductor if needed
SiC switches		
# of MOSFETs and diodes per switch position	5 (1700 V rating)	cf. datasheet for chips CPM2-1700-0040B and CPW5-1700-Z050B

large, this phase shift would limit the transmitted power; if too low, it would make the control too complex [13]. Considering a maximum phase shift range of 10 – 25° (so the power factor is higher than 0.9 in nominal conditions) yields a leakage inductance in the 10 – 25 µH range. Without more information (in particular regarding the control system timing constraints), it is decided to aim for the smallest value; an additional inductor would be connected in series to reach a higher leakage inductance value if needed. This allows to retain some freedom in the design process.

Tab. I presents the main results of the pre-design stage.

3 Detailed Design and Implementation

Once the topology and is main parameters have been selected, the detailed design of the converter can begin. As presented in Fig. 2, the design is broken into three main tasks (transformer, power electronics and control), each managed by a different team using the specifications in Fig. 1a and Tab I.

3.1 Transformer design

The details of the transformer design are given in [17]. Because of the short development time, the magnetic material is chosen *a priori*: among the possible candidates [18], ferrite is selected because of its availability, despite its low maximum induction level ($\approx$ 0.2 T). Amorphous materials are discarded because of their strong magnetostrictive coefficients (risk of acoustic noise); nanocrystalline cores are only available in a limited range of sizes, with long lead times. In particular, 3C90 ferrite material is used because of its suitable performances.

3.1.1 Analytical design

The analytical design allows to quickly compare many configurations, especially regarding copper and core losses. The copper losses in the winding are estimated using Dowell's equations [19]. These equations consider the current harmonics and estimate the AC resistance of the winding taking into account proximity and skin effects in the conductors [17]. Foil winding is preferred because of its lower cost, lower AC resistance compared to wire, and because it is well suited to the small number of turns being considered here (2 windings with 14 turns per column). The leakage inductance is calculated using [20] at 3.38 µH, a value compatible with the specifications (note that this value does not include the inductance of the connecting cables).

For the core losses, the improved General Steinmetz Equations (iGSE) are used [21]. IGSE requires detailed data regarding the Ferrite material. These data are extracted from the material's datasheet [22], as we do not have experimental characterization data at this stage.

At the end of the analytical design, it is decided to have the transformer made, because of the long lead time (more than 8 weeks for manufacturing only). The main parameters (number of turns and dimensions of the foils, magnetic material reference) are given to the transformer manufacturer. The mechanical structure (required to hold together the various ferrite parts, the winding and the transformer terminals) is directly proposed by the manufacturer (it is reused from one of their former projects). Many parameters (in particular the location of the terminals of the transformer) are left to the discretion of the manufacturer.

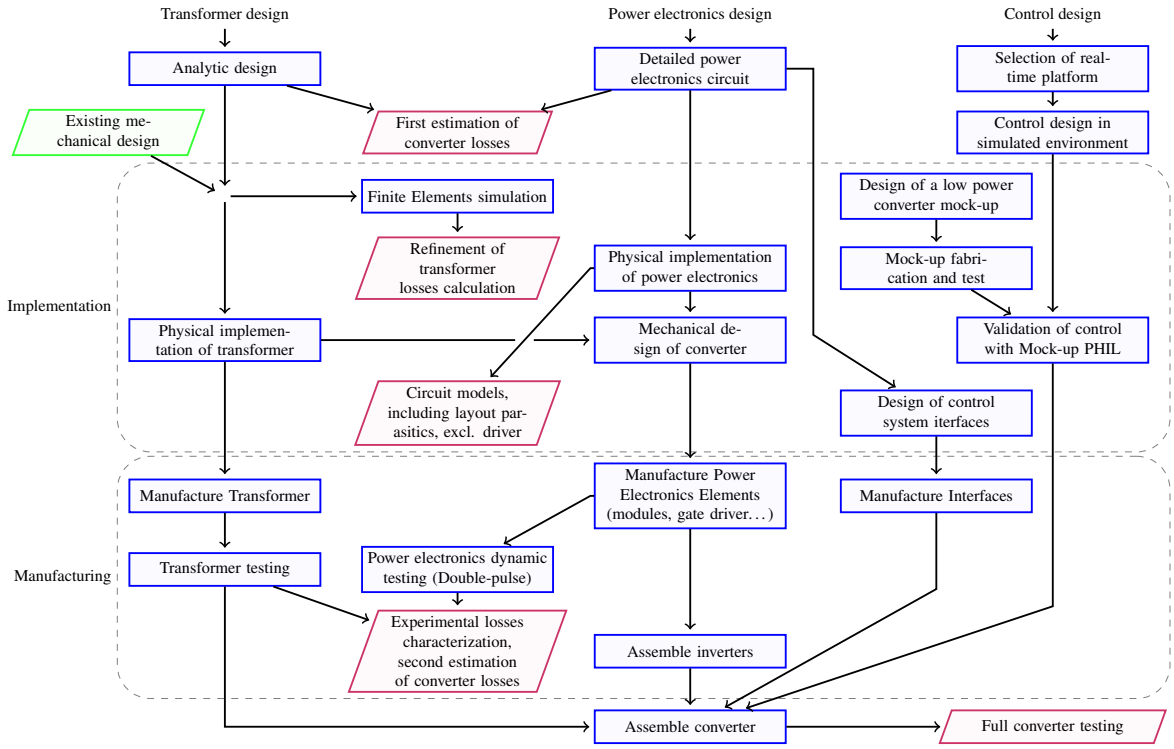


Figure 2: Flowchart of the detailed design procedure (the corresponding timeline is discussed in the article).

3.1.2 Finite element simulations

While the transformer is being built, Finite Elements (FE) simulations are run. They allow to get a more accurate estimation of the losses (especially for the copper losses). They also allow to perform thermal simulations (temperature distribution over the transformer), electrostatic simulations (to calculate parasitic capacitance and check dielectric strength). All calculations are performed using Ansys software: Maxwell for the magnetic and electrostatic simulations, Ansys Mechanical for heat conduction, ICEpak for simulations which mix heat conduction and convection.

The magnetic simulations confirm the leakage inductance value which was calculated analytically (3.38 µH vs. 3.39 µH for FE). They are performed in 3D to represent effects such as current crowding around the power connections. Indeed, these connections are found to represent a large share of the transformer's ac resistance (up to 60 % [17]). 3D FE offers a much more accurate model of the current distribution in the copper conductors, which unfortunately results in a much greater ac resistance compared to the analytical model (Fig. 6a). 3D FE predicts that the ac resistance at 20 kHz is more than twice the dc resistance. At the time of these findings, the transformer is being manufactured, so it is decided to manage the increased losses through additional cooling fans, relying on ICEpak simulations for airflow calculations.

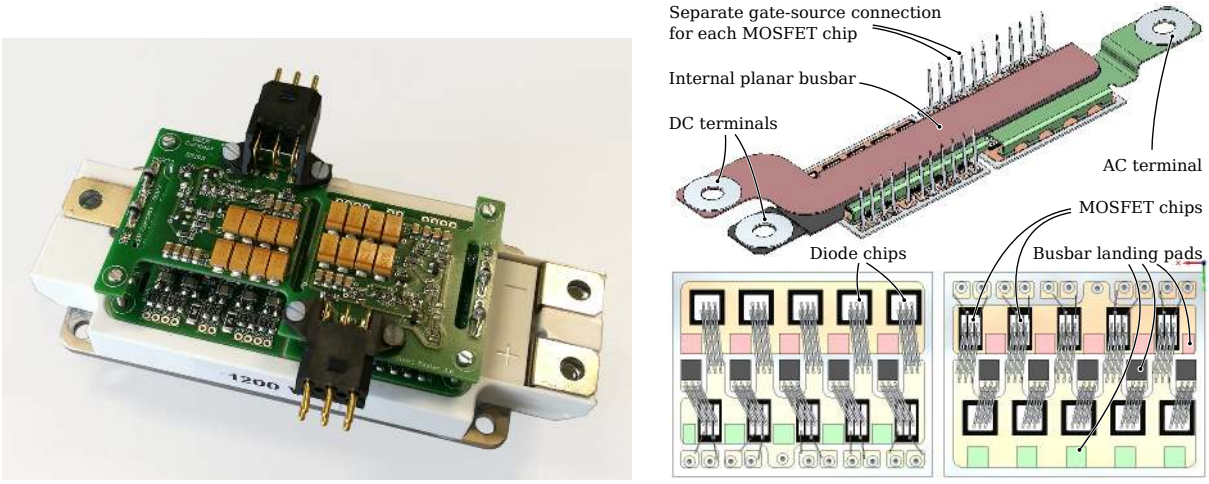
3.2 Power Electronics design

This task refers to the design and implementation of the two inverters of the DAB topology. It also addresses the mechanical structure of the whole converter.

3.2.1 Detailed power electronics circuit

At the time the design is initiated, 1700 V-SiC MOSFETs and Diodes are available on the market as bare dies or discrete, but not in module package [23]. Given the power rating of the converter, a discrete-based circuit is not considered desirable, so we decide to develop a custom power module.

Some simple thermal calculations are performed. First, the switching losses are estimated using the turn-off energy data given in the datasheet of the devices (as we assume Zero-Voltage Switching – ZVS –, turn-on losses are considered negligible). For the conduction losses, the evolution of $R_{DS_{on}}$ with the temperature is non-negligible (it doubles between 25 and 150 °C for 1700 V MOSFETs), so it is considered in our calculations, assuming an (arbitrary) baseplate temperature of 70 °C and a module thermal



(a) (b)

Figure 3: (a) Photograph of the custom power module with the output stage of the gate driver mounted. Length/width of the power module: 152/62 mm. (b) CAD view of the internal interconnects of the power module (top) and layout of the ceramic substrates (where the MOSFETs are located in close proximity with the diode of the opposite switch).

resistance identical to that of the EconoDUAL package from Infineon (which is chosen as the outline for our module). These data confirm that for power modules with 5 MOSFET dies per switch position, the junction temperature remains below the maximum allowed value. On the secondary (600 V side), 1200 V MOSFETs (CPM2-1200-0025B, 25 mΩ $R_{DS_{on}}$) and diodes (CPW5-1200-Z050B) are used instead of 1700 V devices. This way, the primary and secondary inverters remain geometrically equivalent, and their losses are comparable [24]. An existing gate driver circuit is used here. It was designed for IGBT modules, and is based on discrete components.

Finally, the last elements to be selected are the input/output capacitors. In the absence of any specification regarding input/output ripple voltage, we set it to an arbitrary value of 5 %, and we consider that the input and output capacitors manage the full ac currents of the converter. In the worst case (maximum voltage – 1200 V – on the primary and the minimum conversion ratio – 0.45) the current values is expected to reach 211 A. Because of the high switching frequency, the required capacitance remains relatively low (22 µF). The closest commercially available capacitors are found to be 40 µF capacitors which can sustain 57 A (AVX FFVS6U0406K). 4 such capacitors are then connected in parallel to provide sufficient current capability, and much higher capacitance value than initially required. For modularity and cost aspects, the same capacitors are used for the primary and secondary sides.

At this stage, by combining the estimation of losses from the power semiconductor devices and from the transformer (as calculated using the analytical model), we reach a first milestone where the efficiency of the converter ("first estimate" line, in Fig. 8b) can be compared to the target efficiency in the specifications (98 %, see Fig. 1a)

3.2.2 Physical implementation of the power electronics

At this point, the detailed circuit diagram of the converter has been drawn, and the exact references of all components are known. The most specific components (SiC MOSFETs and diodes, capacitors) are ordered, as they have relatively long lead times (more than 8 weeks).

As mentioned above, a custom power module is designed with the "EconoDUAL" outline (Fig. 3a). Although the SiC MOSFETs have an internal body diode, we are not sure we can use it reliably. As a consequence, we decide to use antiparallel SiC SBDs. To satisfy the current ratings of the diodes, 5 chips are used per switch position (i.e our module contains as many diodes as MOSFETs). This is probably far from optimal, but reflects the lacks of reliability data at the time the decision is taken (end 2014). Regarding the internal routing of the power module, various configurations are compared with regard to their parasitic inductances. The models are first designed with a 3D mechanical CAD software (CREO

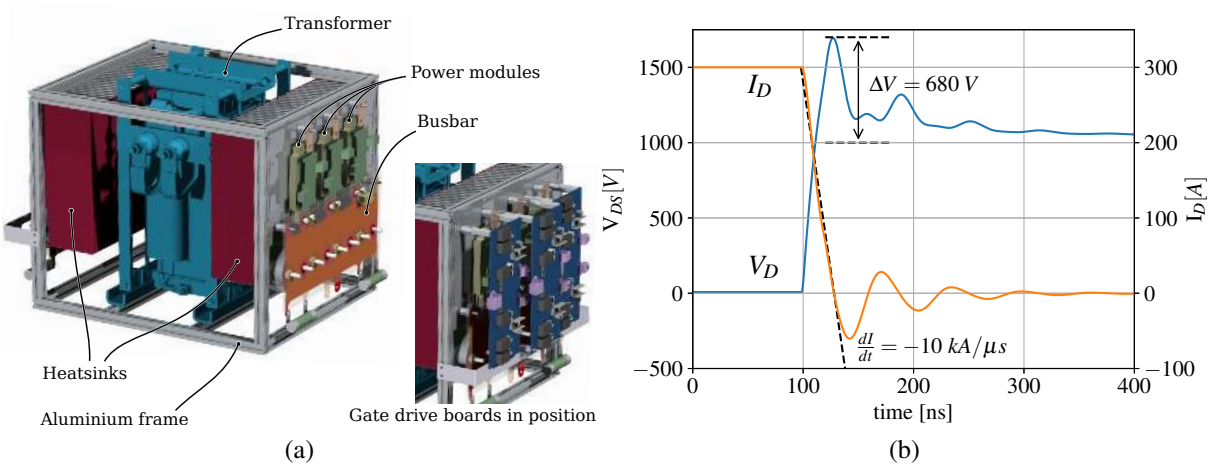


Figure 4: (a): CAD view of the complete converter (without cables). (b): Time-domain simulation result for the turn-off (V = 1000 V ; I = 300 A ; di/dt = -10 kA/us), including the modelling of the interconnects (especially the inductive behaviour), in a double-pulse configuration (hard switching).

Parametric, Fig. 3b), then the parasitic inductances are calculated using Ansys Q3D Extractor. The gate and source connections of each die are routed independently, to keep some flexibility in case issues are encountered in the parallel operation of the MOSFETs: all transistors can be connected in parallel, or they can be driven through individual gate resistors, depending on the layout of the gate driver board. In our case, 5 Ω resistors are connected between the output stage of the gate driver and each gate terminal of the power module .

3.2.3 Mechanical design of converter

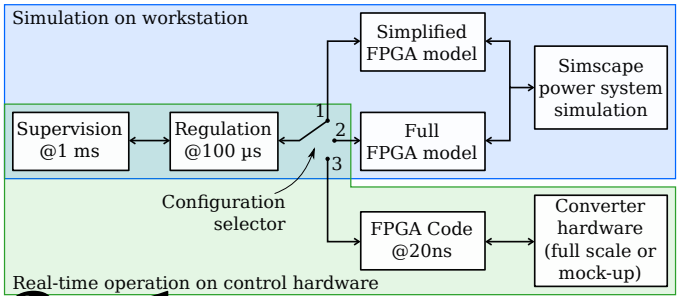
Based on the thermal calculations performed previously, plus some safety margins (we consider each module dissipates 500 W, has a baseplate temperature of 70 °C and shall operate at a maximum junction temperature of 120 °C so as not to degrade its $R_{DS_{on}}$ too much), we select an aluminium heatsink with embedded copper heatpipes for better heat spreading (Mersen, 205×300×120 mm^3), with three 92 mm axial fans (Papst). This heatsink is used as the support to mount all the components of each inverter. A 3D implementation of the inverters is done using mechanical CAD software, with a custom laminated busbar used to connect the power modules. Inverters and transformer are then secured to an aluminium frame (Fig. 4a).

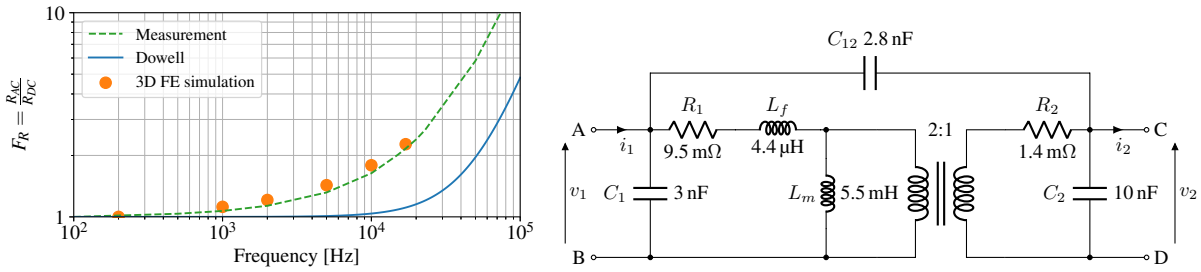
3.2.4 Circuit models

Electromagnetic simulations are performed using the Ansys Electromagnetic suite [25]: parasitic inductances, capacitances and resistances are calculated (using Q3D Extractor) from the 3D geometry of the inverters. An equivalent circuit model is automatically generated, and included in a time-domain simulation (Simplorer). As no models are available for the MOSFETs, we use the simplified macro model proposed in [26]. However, even this simplified model is found to be too complex for the converter simulation to run in a reasonable time (we have 20 dies per power module, and 4 power modules total). Finally, we end up using ideal switch and diode models with capacitors in parallel. These capacitors are important as, together with the inductors in the circuit, they set the switching transients. Fig. 4b presents a simulation result during turn-off.

From the simulated voltage and current waveforms (Fig. 4b), the global parasitic inductance of the commutation loop (capacitor, busbar and power module.) is evaluated at 68 nH [27]. Finally, more detailed electromagnetic simulations are performed using Ansys Maxwell to analyze the current density distribution in the interconnects (wirebonds, busbar…). However, these cannot be conducted using the complex current waveforms produced by the circuit simulation, and must be limited to dc. This limits their relevance (skin and proximity effects are not taken into account in the resulting current distribution

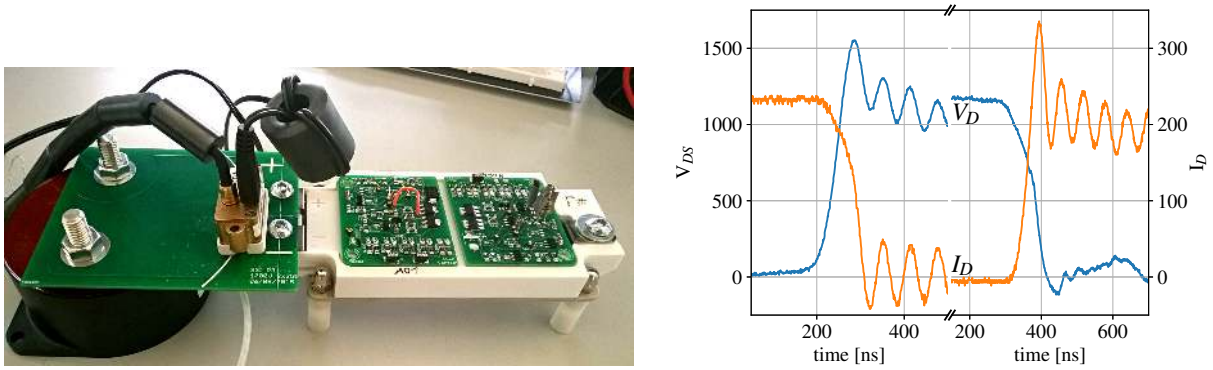
As no obvious issue is identified through the simulation, the design stage is considered finished for the power electronics, and manufacturing can start.


Simulation on workstation
Simplified FPGA model
Simscape power system simulation
Supervision @1 ms
Regulation @100 µs
1
2
3
Full FPGA model
Configuration selector
FPGA Code @20ns
Converter hardware (full scale or mock-up)
Real-time operation on control hardware



(a) (b)

Figure 6: (a):Evolution of the ac resistance (relative to the dc resistance), as forecast by various analytical models, by FEM simulation, and as measured. (b): Equivalent model of the medium frequency transformer identified from measurements.



(a) (b)

Figure 7: (a) dc connections used for double-pulse tests on the power module, including a film capacitor, a custom busbar made out of printed circuit board, and a high bandwidth Rogowski-coil current sensor (Fraunhofer IZM). (b): corresponding waveforms measured on the power modules, used to refine the losses model and to adjust the output impedance of the gate driver. Note that the interconnects used here are different from the complete busbar used for the simulations in Fig. 4b, hence the different over-voltage.

losses, especially as the frequency increases. It also confirms that the 3DFE modelling offers as satisfying level of precision. An analysis of these differences is available in [17].

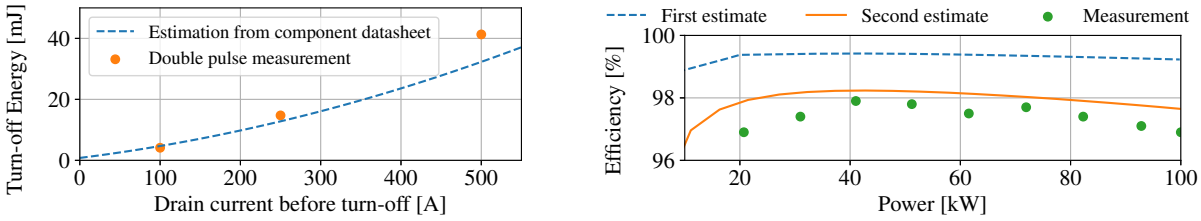
In order to check the interactions between the transformer and the other components (switches, busbar. . .), an equivalent model of the transformer is required. The circuit diagram of this equivalent model is depicted in Fig. 6b, after identification with the measurements.

4.2 Power electronics dynamic testing

The power modules are manufactured first (DeepConcept, Tarbes, France). They are characterized using a double pulse test circuit (Fig. 7a, principle described in [26]), which allows the measurements of the hard-switching losses. An example of measured waveforms is given in Fig. 7b. Thanks to such measurements, we can adjust the switching energy losses (turn-off losses only, as turn-on losses occur under zero voltage switching conditions) used in our estimation. As it can be seen in Fig. 8a, the use of the coefficients calculated from the datasheet of the dies causes an underestimation of the turn-off energy loss of up to 15–20 %. Together with the experimental characterization of the transformer, these results are used to produce the “second estimate” line in Fig. 8b. The double-pulse test circuit is also used to adjust the output impedance of the gate driver (a small capacitor is added to increase the gate-to-source capacitance of the MOSFETs). In parallel, the complete converter is assembled according to the CAD plans. The result is visible in Fig. 9a.

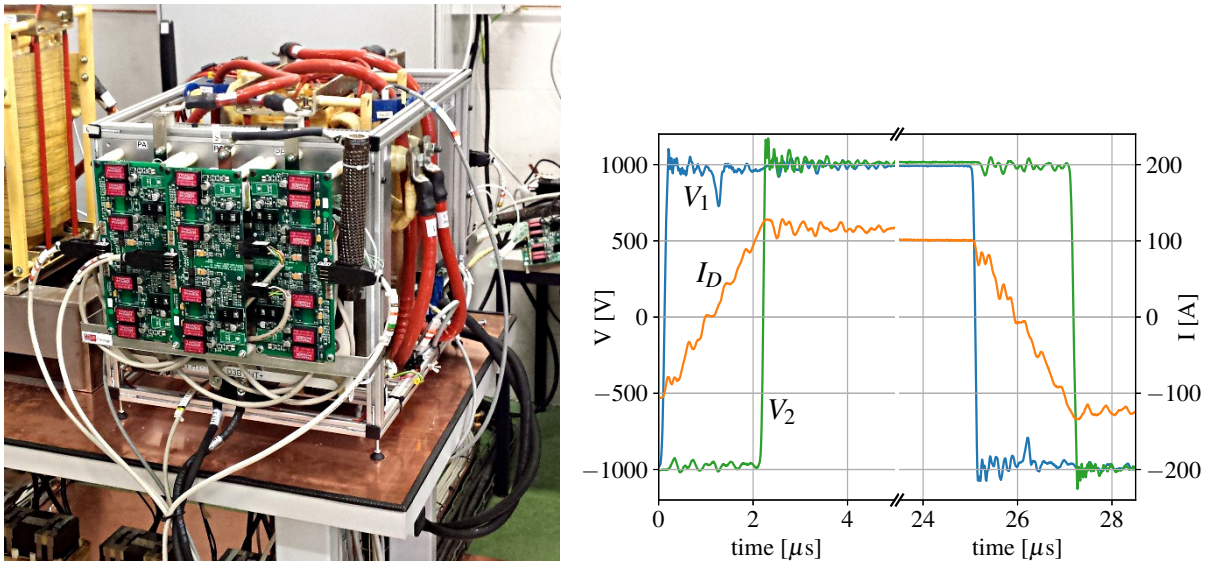
4.3 Full converter testing

Once the test bench has been set-up (a time-consuming task for a converter this size), the actual testing of the power converter is relatively straightforward: the control system is connected to the converter,



(a) (b)

Figure 8: (a): Comparison between the switching losses estimated from the manufacturer's datasheet and from the double-pulse test, for 5 1700 V-SiC MOSFETs and a dc voltage of 1200 V. (b): comparison between the global efficiency as forecast initially, after refinement of the design and the models, and eventually measured.



(a) (b)

Figure 9: (a): Photograph of the final converter. Total dimensions are $43\times46\times71\,\mathrm{cm}^3$ (140 L). (b): Waveforms measured on the converter in operation

and power is gradually increased. A waveform measured at the output of the primary inverter during operation is shown in Fig. 9b. Efficiency measurements are presented in Fig. 8b. The final efficiency is slightly below that predicted by the design, even after the second round of estimation. Note, however, that this efficiency measurement is performed with the voltage/current sensors used for the control of the converter, and therefore has a limited accuracy.

While the converter works, with an efficiency reaching almost 98% (the objective in Fig. 1a) over a large part of the power range, some issues must be highlighted (and will be discussed in the next section):

- EMC issues are encountered, causing a malfunction of the control system (the internal FPGA is reset by EMI above 50 kW). This is solved by re-routing the cables of the test bench (many were overlapping), by adding ferrite beads on auxiliary power supplies and driving signal cables, and by providing earth connection of all metal screen on one point only. The control software is also made more robust to EMI transients by filtering outliers from the I/Os.

- At 1200 V, two power modules are found to fail, because of arcing between the internal busbars (the black and red metal sheets in Fig. 3b). This is attributed to an insufficient clearance between the parts, and possibly to a bubble in the silicone encapsulant. The other modules do not seem to be affected.

5 Discussion

A 100 kW converter was entirely designed and built over the course of one year. Its final performance, although not fully in line with the specifications (the efficiency, in particular, is slightly below 98%), are remarkably close. The converter can operate continuously, indicating that the thermal management system is able to absorb the higher losses level.

As explained in the introduction, the objective of this article is to reflect upon the design process. As the converter was essentially "built from scratch", the design was not based on incremental improvements of an existing converter. This means that in many cases, questions were asked in absolute terms (will it work?) rather than in relative terms (will it work better?). This is an essential difference, in particular for computer simulation, as in the "absolute" case, no reference data are available. Therefore, the accuracy of the modelling is unknown at the design stage.

When looking back on the design process, summarized in Fig. 2, one striking fact emerges: despite the effort which was put in the modelling and simulation, almost none of the simulation results were actually fed back in the process: in Fig. 2, simulation results are outputs (red boxes), mere "milestones" used to check that the converter meets its specifications. In no occasion did the simulation results led to changes in the design, which was finally mainly based on simple analytical approaches and on the datasheets of the components. However, this observation masks fundamental differences between models, which we will discuss now.

For the transformer design, the numerical modeling is found to be remarkably accurate, capable to identify issues such as an increase in ac resistance caused by the geometry of the terminals. 3D FE simulations are not simply a refinement of the analytical calculations: they offer a very different picture, which may have resulted in changes in the design of the transformer, had we not sent it to manufacturing beforehand. The main issue here is that simulations take time: one week for the electromagnetic calculations, not including the preparation of the model, the analysis of the results, and the subsequent thermal simulations. It is, however, a worthwhile effort, and the simulation time could be reduced by using more powerful computing hardware.

Regarding the design of the control system, the RCP provides a very efficient way to (almost) seamlessly transfer from a block-diagram description to real-time code. An intermediary test using a small-scale mock-up remains valuable, as it helps capturing issues which might not be detected in simulation (typically the overflow of a register which occurs over a long period). This is especially important, as the debugging capabilities are limited for the FPGA circuit. All designs we currently work on include such small-scale mock-up stage, with three major improvements: the mock-ups are now made on PCBs (as opposed to breadboard, which was found not to be reliable enough), they now use exactly the same interface as the final converter, and are designed to have the same dynamics, so the transfer to the full-scale converter is even more straightforward.

The power electronics simulations present a completely different picture: over the course of the project, we have never been able to perform a complete circuit simulation of the converter (i.e including accurate models of the switches, their gate drive circuits, as well as the circuit parasitics and the transformer model). This level of complexity is too demanding for the circuit simulator. Ideal switches (on/off behaviour) with a linear capacitor in parallel were used as a model for the SiC MOSFETs instead. A second (and related issue) is that SiC MOSFETs models are not available for all simulation platforms (Wolfspeed provides SPICE models, and we use Ansys Simplorer). This required the adjustment of a compatible model using a dedicated tool (in Simplorer) and the datasheet of the MOSFET. Generating a model this way is convenient, but does not give any information about its level of accuracy, or about its domain of validity.

Even if we had been able to simulate the power circuit of the converter, this would probably have been insufficient to predict the EMC issues we encountered during the tests (spurious resets of the control systems above a certain power level). This would have required to take into consideration the entire converter, including models of the gate drivers, the auxiliary power supplies, the low power wiring, the grounding configuration, etc. Not only would such approach require tremendous computing power, but it would also require models for these elements. Another approach could be to perform model reduction, to adapt the models to the analyses (i.e. to use a different model to predict EMI or power losses). This,

however, requires considerable expertise, time, and data. Some of these data being not available, it requires experimental characterization, and therefore advance purchase of some elements [29]. Finally, for subsequent designs, we use a more protective approach regarding EMC, for example using fiber optics as a link between the control system and the converter (for driving signals as well as for measurements). While it provides an ideal barrier to EMI, it comes at a certain cost.

As for the other issue encountered (arcing inside one power module), preventing it through simulation, if possible at all, would have required a totally different modelling. It is not clear yet if the issue was related to thermo-mechanical effects (deformation of the internal leadframe as a consequence of heating), manufacturing issues (inaccuracy in the forming of the metal parts, in their alignment, bubble in the silicone encapsulant), design issue (insufficient clearance between the parts), or (more probably) a combination of the three. The multiplicity of the possible causes makes modelling quite complicated, and one can consider that hardware prototyping is unavoidable here. This is, however, a specific case: custom modules were required as no 1700 V SiC power modules were available at the time. With "off-the-shelf" modules, any such design issue would have been addressed beforehand by the manufacturer.

6 Conclusion

A 100 kW converter was designed "from scratch", over a relatively short time-frame (1 year from beginning of design to test), with the objective of assessing the design methodology. The design process was separated between three main elements: transformer, power electronics, and control system.

Thanks to RCP techniques, which rely on seamless transition from computer model to firmware generation, the control was developed independently from the transformer and the converter. This is not so true for hardware elements such as the transformer and the power electronic circuits, for which computer simulation was found to be less straightforward.

For the transformer, 3D-FE simulation was found to be accurate, but requires a lot of effort and time to set the model up, run the simulation, and analyze the results. However, it is worth the effort, and new transformer designs we have made since have relied heavily on 3D-FE simulation.

For the power electronics, on the contrary, no complete simulation could be run, because of the complexity of the model. Simplifications were required which, together with un-verified models for the semiconductor devices, produced simulation results of unknown validity. As a consequence, the power electronics design was mainly based on datasheet information, safety margin, or designer expertise.

More importantly, the lack of complete circuit simulation did not allow us to identify EMC issues, which required fixing the converter on the test bench. Here, the solutions rely more on EMI-safe approaches (such as fiber optics data transfer) than on computer simulation.

This does not mean that simulation is useless. For incremental changes (e.g. improving a prototype before moving to production), a reference is available to check the validity of the models. In this case, simulation gives an invaluable analysis tool. Simulation is also quite useful for optimization or to evaluate the consequences of changing a design parameter. But in the case of a relatively large converter such as the one presented here, electrical simulation does not currently allow the generation of a complete "virtual prototype" which could replace a hardware prototype.

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