HP Memristor Mathematical Model for Periodic Signals and DC

A. G. Radwan[1,2], M. Affan Zidan[1] and K. N. Salama[1]

[1]Electrical Engineering Department
King Abdullah University of Science and Technology
Thuwal, Kingdom of Saudi Arabia 23955-6900
Email: {ahmed.radwan, mohammed.zidan, khaled.salama}@kaust.edu.sa
[2]Department of Engineering Mathematics
Faculty of Engineering, Cairo University, Egypt

Abstract— **In this paper mathematical models of the HP Memristor for DC and periodic signal inputs are provided. The need for a rigid model for the Memristor using conventional current and voltage quantities is essential for the development of many promising Memristors' applications. Unlike the previous works, which focuses on the sinusoidal input waveform, we derived rules for any periodic signals in general in terms of voltage and current. Square and triangle waveforms are studied explicitly, extending the formulas for any general square wave. The limiting conditions for saturation are also provided in case of either DC or periodic signals. The derived equations are compared to the SPICE model of the Memristor showing a perfect match.**

I. INTRODUCTION

Memristor (M) is believed to be the fourth fundamental two terminals passive element, beside the Resistor (R), the Capacitor (C) and the Inductor (L). The existence of such element was postulated by Leon Chua in 1971[1], but without finding its passive realization. In 1978 Chua and Kang extends the idea to memristive devices and systems [2]. The real Memristor was not found until 2008, when a team in Hewlett-Packard labs had built the first electronic passive Memristor [3]. This Memristor is based on partially doped T_iO_2 as shown in Fig 1, where $w \in (0, D)$.

Since its realization many applications are proposed for the Memristor, memory [4], biology [5], and spintronic [6]. Recently the Memristor response for a sinusoidal input was modeled using a linearized model of the pinched i-v hysteresis as in [7] or qualitatively as in [8], [9].

In this paper we provide a mathematical model for the DC input and symmetric periodic signals inputs. Unlike [7], [8], [9] works, which focuses on the sinusoidal input wave form, we derived rules for any periodic signals in general in terms of voltage and current. Square and triangle wave forms are studied explicitly. An extended rules for for any general square wave are also provided. The limiting conditions for saturation in case of either DC or periodic signals are also introduced. We compare our derived equations with the SPICE model of the Memristor [10] showing a perfect match.

II. HP MEMRISTOR

There are four fundamental circuit variables, the current i, the voltage v, the charge q and the flux ϕ. Chua [1] realized
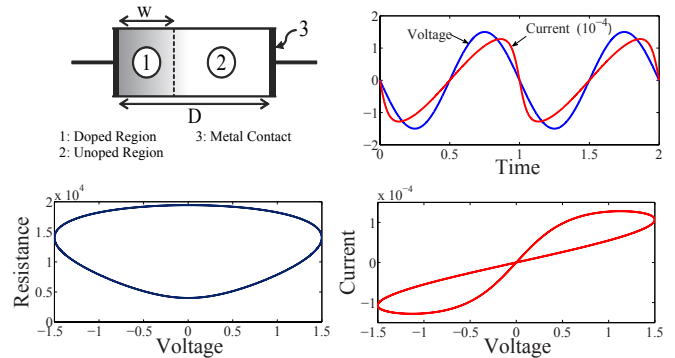

Fig. 1. Memristor current versus time, and current and resistance versus input voltage, for sinusoidal wave input voltage of 1Hz frequency and -1.5V peak voltage. Memristor Parameters: $R_{off} = 16k\Omega$, $R_{on} = 100\Omega$, $R_o = 4k\Omega$. The abstract structure of the HP Memristor is also given.

that only five of the six possible combinations are used, so he defines the missing combination to be the memristive one,

$$R(w) = \frac{dq}{d\phi} = \frac{v(t)}{i(t)} \tag{1}$$

where R is the instantaneous resistance and w is the state variable of the Memristor.

The HP Memristor [3] was built on drifting the dopant between doped and undoped potion of the material, which models the memristive property. As shown in Fig.(1) w is modeled by the length of the doped region, which is bounded between 0 and device length D. The instantaneous resistance of the Memristor is written as [3],

$$R = x \cdot R_{on} + (1 - x) R_{off} \tag{2}$$

where $x = w/D$, R_{on} is the resistance of the completely doped Memristor, and R_{off} is for the completely undoped.

The Memristor resistance as a function of time is drived in [8], [9]. We can generalize the resistance for linear dopant drift as,

$$R^2 = R_o^2 - 2kR_d\phi(t), \ R \in (R_{on}, R_{off}) \tag{3}$$

where $k = \mu_v \cdot R_{on}/D^2$, μ_v is dopant drift mobility, $\phi(t) = \int_0^t v(\tau)\, d\tau$ is the flux at time t, $R_d = R_{off} - R_{on}$ which is the difference between the boundary resistances, and $R_o = R(x_o)$ is the initial resistance at $t = 0$.

Fig. 1 shows the Memristor's response for sinusoid input voltage, using Eq.(3). The figure shows the Memristor's current versus both of time and voltage, and the Memristor's resistance versus voltage.

III. MODEL FOR THE DC VOLTAGE

For a Memristor with a DC input, the dopant boundary will move in one direction towards 0 or D limits, depending on the sign of the input voltage. After w reaches one of its two limits, the Memristor will act as a constant resistance tends to R_{on} or R_{off}. By evaluating the flux (ϕ) in Eq.(3), the resistance as a function of time can be calculated as,

$$R^2 = R_o^2 - 2kR_d V_{DC} t, \ R \in (R_{on}, R_{off}) \quad (4)$$

where V_{DC} is the value of the DC voltage. The time required for resistance saturation t_{sat}, in which R reaches either R_{on} or R_{off} can be calculated using Eq. (4), such that ,

$$t_{sat} = \begin{cases} \dfrac{R_o^2 - R_{off}^2}{2V_{DC}kR_d} & , V_{DC} < 0 \\[3mm] \dfrac{R_o^2 - R_{on}^2}{2V_{DC}kR_d} & , V_{DC} > 0 \end{cases} \quad (5)$$

where the saturation direction depends on the sign of V_{DC}. Fig. 2(a) shows the required saturation time versus the amplitude of the DC input voltage. This figure shows that more saturation time is required for smaller input voltages.

The maximum required saturation time regardless the initial value of the Memristor resistance is given by,

$$(t_{sat})_{max} = \frac{R_{off} + R_{on}}{2\,|V_{DC}|\,k} \quad (6)$$

which can be approximated as $\left(D^2 R_{off}/(2\mu_v R_{on} V_{DC})\right)$ as observed before by HP experiments in [3]. Fig. 2(b) shows the maximum saturation time required by the Memristor for different values of R_{off}. It appears from the figure that more saturation time is required in case of higher off-resistance.
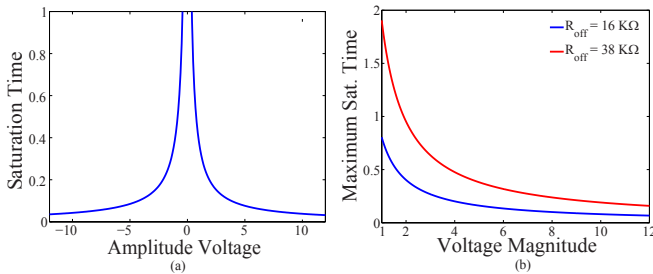

Fig. 2. (a)Saturation time versus the amplitude voltage, where $R_{off} = 16k\Omega$. (b) Maximum saturation time for a DC input versus the voltage magnitude for different R_{off}. Memristor's parameters: $R_{on} = 100\Omega$ and $R_o = 11k\Omega$
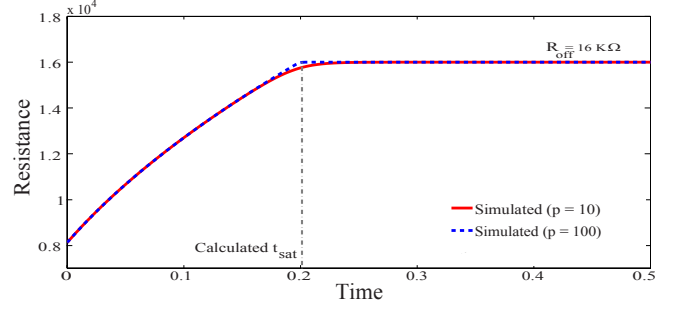

Fig. 3. Calculated saturation time compared to SPICE simulations for nonlinear dopant drift ($p = 10$) and almost linear drift ($p = 100$) at $3V$ DC. Memristor's parameters: $R_{on} = 100\Omega$, $R_{off} = 16k\Omega$ and $R_o = 8k\Omega$

The initial resistance for symmetric saturation times, $t_{sat} = 0.5\,(t_{sat})_{max}$, in case of equal magnitude positive and negative voltage is given by,

$$R_o^* = \sqrt{\frac{R_{on}^2 + R_{off}^2}{2}} \approx \frac{R_{off}}{\sqrt{2}} \quad (7)$$

which is greater than the average value $(R_{on} + R_{off})/2$, and the difference increases as R_d increases.

Fig. 3 shows the SPICE simulations results for two different p, which models the effect of nonlinear dopant drift [10], and the calculated saturation time. The calculated saturation time is identical with SPICE simulation at $p = 100$ which matches the linear dopant case. Also comparing with the nonlinear output, at $p = 10$, shows a neglected error.

IV. GENERAL MODEL FOR PERIODIC SIGNALS

For any periodic signal with zero area under the curve and starting with zero voltage, the Memristor's resistance reaches its maximum or minimum value, at $t = (n + \alpha)T$, where $n = 0, 1, 2, ...$, such that,

$$R_M^2 = R_o^2 - 2kR_d A_\alpha, \ R_M \in (R_{on}, R_{off}) \quad (8)$$

where A_α is the area of the first half cycle $[0, \alpha T]$. The nature of this value either maximum (R_{max}) or minimum (R_{min}) depending on the sign of A_α. Again, at $t = \{0, T, 2T, ...\}$ the resistance returns to its initial value, such that, $R = R_o$, since the total net-area at these instances equals to zero.

Unsaturated resistance limiting net-areas (flux)

Both of the resistance range and the rotation of the pinched i-v hysteresis are affected with the area by the voltage curve (flux). Generally, the boundaries for non-saturating resistance can be calculated by substituting R_M with R_{off} and R_{on} in Eq. (8), such that,

$$A_{off} = \frac{1}{2k}\left(\frac{R_{off}^2 - R_o^2}{R_{on} - R_{off}}\right) < 0 \quad (9)$$

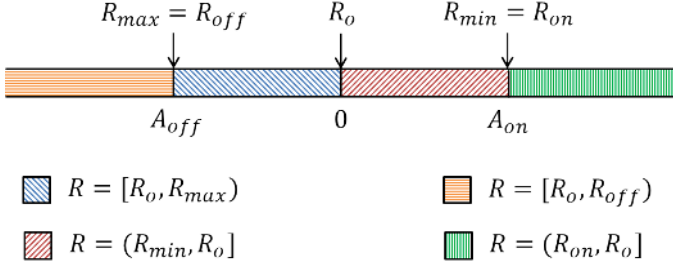$$A_{on} = \frac{1}{2k}\left(\frac{R_{on}^2 - R_o^2}{R_{on} - R_{off}}\right) > 0 \quad (10)$$

Fig. 4. Intervals of the Memristor's resistance versus the area under the voltage curve (flux).
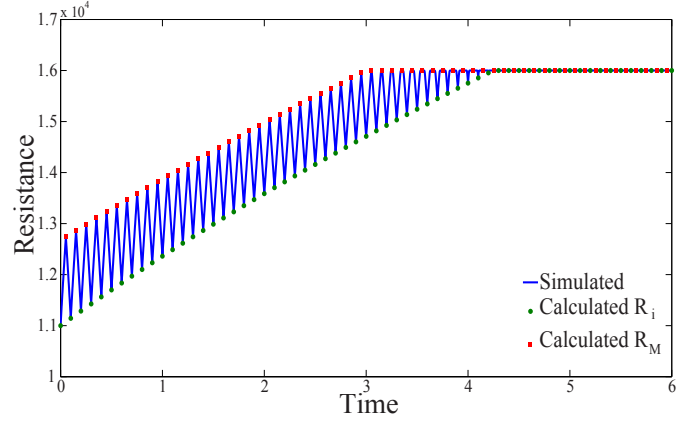

Fig. 5. Simulated Memristor resistance versus time and calculated R_M and R_i, for non-symmetric square wave input voltage. $V_{o1} = -2.5V$, $V_{o2} = 2.5V$, $\alpha = 0.52$ and frequency $= 10$Hz. Memristor parameters: $R_{on} = 100\Omega$, $R_{off} = 16k\Omega$ and $R_o = 11k\Omega$. Simulation parameter $p = 40$.

where A_{off} and A_{on} are the limiting first half cycles area for just reaching saturation at R_{off} and R_{on} respectively. The difference between these boundaries is given by,

$$|A_{sat}| = \frac{R_{off} + R_{on}}{2k} \quad (11)$$

which is independent of R_o. This value considered as the minimax required half cycle area by the Memristor's resistance to reach saturation, either R_{off} or R_{on}, when R_o equals to R_{on} or R_{off} respectively.

Fig. 4 shows the interval range of the resistance, which is limited by A_{off} and A_{on}

V. SQUARE WAVEFORMS

A. Non-zero net-area waveform

In general for any non-zero net-area square wave the resistance with increase or decrease gradually, with or without oscillation , until completely saturated at either R_{off} or R_{on}. The direction of saturation depends on the sign of total area under the curve and the grade of the change depends on the total area magnitude. For zero net-area signal resistance will continually oscillates returning to R_o at the end of each cycle.

The value of the resistance at start of each cycle, $t = nT$ where $n = 0, 1, 2, ...$, is given by,

$$R_i^2(n) = R_i^2(n-1) - \frac{2kR_d}{f}(V_{o1}\alpha + V_{o2}(1-\alpha))$$

$$= R_o^2 - \frac{2nkR_d}{f}[V_{o1}\alpha + V_{o2}(1-\alpha)] \quad (12)$$

where $R_i(n) \in (R_{on}, R_{off})$, $R_i(0) = R_o$, and f is the frequency. Where $[V_{o1}\alpha + V_{o2}(1-\alpha)]$ denotes to is total total area under the curve, α is the duty cycle , and V_{o1} and V_{o2} are the amplitude voltage at the first and second parts of the cycle respectively

The Memristor's resistance reaches its maximum or minimum value, at $t = (n + \alpha)T$, where $n = 0, 1, 2, ...$, as,

$$R_M^2(n) = R_i^2(n) - \frac{2\alpha V_{o1}kR_d}{f}$$

$$= R_o^2 - \frac{2kR_d}{f}[(n+1)V_{o1}\alpha + V_{o2}(1-\alpha)] \quad (13)$$

where $R_i(n) \in (R_{on}, R_{off})$. Fig. 5 shows a perfect matching between the calculated R_i and R_M for a non-zero net-area

waveform and the SPICE simulation. This figure also illustrates the effect of the non-zero net-area on the Memristor's resistance steady state, when the duty cycle increases from 50% up to 52%.

B. Zero net-area waveform

Square wave will have a zero net-area under the curve if,

$$\frac{V_{o1}}{V_{o2}} = \frac{\alpha - 1}{\alpha} \quad (14)$$

in this case, the resistance with respect to time can be derived from Eq. (3), such that,

$$R^2 = \begin{cases} R_o^2 - 2V_{o1}kR_dt, & (a) \\ R_o^2 - 2V_{o2}kR_d(T - t), & (b) \end{cases} \quad (15)$$

where $R \in (R_{on}, R_{off})$, V_o is amplitude voltage and T is the period time. Part (a) of the equation is applied in the first half cycle and part (b) in the second one. Due to symmetry the calculated values for resistance are repeated every cycle.
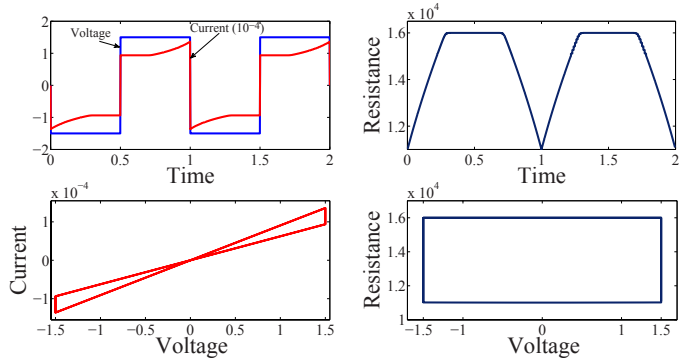

Fig. 6. SPICE simulation results for Memristor current and resistance versus time and voltage for square wave input voltage, with -1.5 amplitude voltage and frequency of 1Hz. $R_{on} = 100\Omega$, $R_{off} = 16k\Omega$, $R_o = 11k\Omega$ and $p = 40$.

By substituting Eq. (14) in Eq. (13), the maximum or minimum resistance, reached at $t = (n + \alpha) T$ where $n = 0, 1, 2, ...$, is derived by,

$$R_M^2 = R_o^2 - \frac{2\alpha V_o k R_d}{f}, \ R_M \in (R_{on}, R_{off}) \qquad (16)$$

Fig. 6 shows the Memristor's current and resistance versus both time and voltage for symmetric zero net-area input waveform. While Fig. 7(a) shows the matching between the calculated resistance versus the SPICE simulated one, in case of saturating resistance at R_{off}, since the first half cycle area A_α is greater than A_{off} as given in Eq. (9).

VI. TRIANGLE WAVEFORMS

For symmetric zero-net area triangle waveform input voltage the resistance with respect to time can be derived from Eq. (3),

$$R^2 = \begin{cases} R_o^2 - 4V_o f K R_d t^2, & (a) \\ R_o^2 - \frac{V_o k R_d}{2f}\left(1 - 8f^2 \left(T/2 - t\right)^2\right), & (b) \\ R_o^2 - 4V_o f K R_d \left(T - t\right)^2, & (c) \end{cases} \qquad (17)$$

where $R \in (R_{on}, R_{off})$ and T is the period time. Part (a) of the equation is applied in the first quarter cycle, part (b) in the second and third quarters and part (c) for the fourth quarter. Due to symmetry the calculated values for resistance are repeated every cycle. Fig. 7(b) shows the matching between the calculated and SPICE simulated resistance versus time, in case of saturating resistance at R_{off}, since the first half cycle area A_α is greater than A_{off} as given in Eq. (9).

Using Eq. (8) the maximum or the minimum resistance of the Memristor, at $t = (n + 1/2) T$ where $n = 0, 1, 2, ...$, is,

$$R_M^2 = R_o^2 - \frac{V_o k R_d}{2f}, \ R_M \in (R_{on}, R_{off}) \qquad (18)$$

where V_o is the amplitude voltage of the input signal. Fig. 8 shows the matching between the calculated and SPICE results for zero net-area input waveform.
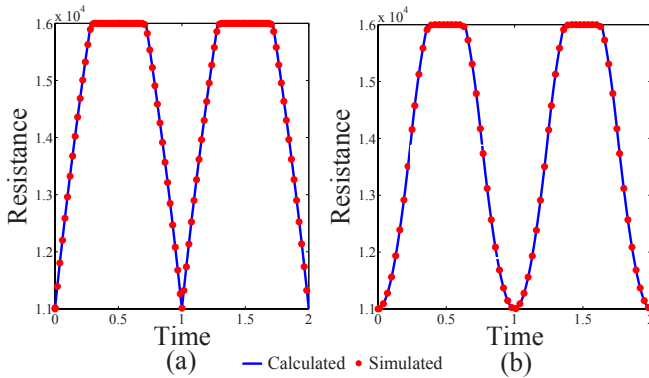

Fig. 7. Memristor resistance versus time for, (a) square wave input vantage with -1.5 amplitude voltage and frequency of 1Hz, (b) triangle wave input vantage with -2 amplitude voltage and frequency of 1Hz.. Memristor parameters: $R_{on} = 100\Omega$, $R_{off} = 16k\Omega$ and $R_o = 11k\Omega$. Simulation parameter $p = 40$.
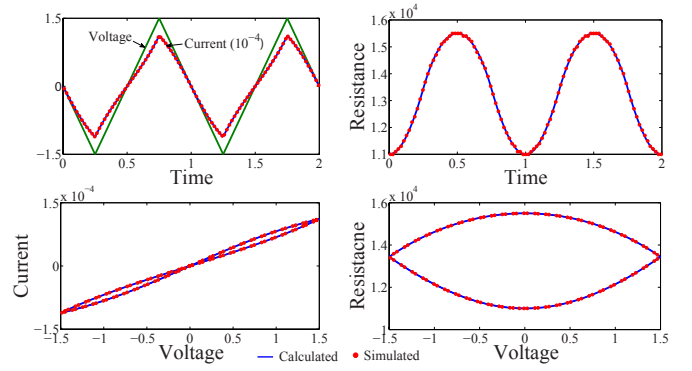

Fig. 8. Calculated and SPICE simulation ($p = 100$) results for Memristor current and resistance versus time and voltage for triangle wave input voltage, with -1.5 amplitude voltage and frequency of 1Hz. $R_{on} = 100\Omega$, $R_{off} = 16k\Omega$ and $R_o = 11k\Omega$.

VII. CONCLUSION

In this paper, many mathematical models of the HP Memristor for DC and periodic waveforms input voltage are derived. The Memristors resistance as function of time, saturation time, maximum saturation time, and also the value of the initial resistance for equal saturation times are discussed. General boundary conditions for the net-flux per cycle and the saturation cases, showing the range of the Memristors resistance in each interval are introduced. Memristors resistance maxima and minima for any periodic input voltage either for zero and nonzero net-flux per cycle are mathematically derived. Time domain equations for the Memristors resistance, current and power in case of zero net-flux per cycle are easily derived. All mathematical equations are compared to the SPICE model of the HP Memristor showing a perfect match.

REFERENCES

[1] L. Chua, "Memristor-the missing circuit element," *Circuit Theory, IEEE Transactions on*, vol. 18, no. 5, pp. 507 – 519, Sep 1971.
[2] S. M. K. Chua, L.O., "Memristive devices and systems," *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209 – 223, Feb. 1976.
[3] D. B. Strukov, G. S. Snider, and D. R. Stewart, "The missing memristor found," *Nature*, vol. 435, pp. 80–83, 5 2008.
[4] P. O. Vontobel, W. Robinett, P. J. Kuekes, D. R. Stewart, J. Straznicky, and R. S. Williams, "Writing to and reading from a nano-scale crossbar memory based on memristors," *Nanotechnology*, vol. 20, no. 42, 2009.
[5] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, "Memristive model of amoeba learning," *Phys. Rev. E*, vol. 80, no. 2, p. 021926, Aug 2009.
[6] Y. V. Pershin and M. Di Ventra, "Spin memristive systems: Spin memory effects in semiconductor spintronics," *Phys. Rev. B*, vol. 78, no. 11, p. 113309, Sep 2008.
[7] D. Wang, Z. Hu, X. Yu, and J. Yu, "A pwl model of memristor and its application example," *Communications, Circuits and Systems, 2009. ICCCAS 2009. International Conference on*, pp. 932 –934, 2009.
[8] F. Y. Wang, "Memristor for intrductory physics," *Physics. class-ph*, pp. 1–4, 2008.
[9] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *EUROPEAN JOURNAL OF PHYSICS*, vol. 30, pp. 661–675, 2009.
[10] Z. Biolek, D. Biolek, and V. Biolkova, "Spice model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009.