Hybrid Analytical Modeling Method for Split Power Bus in Multilayered Package

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***Abstract*—As multiple chips are being integrated into a single package with increased operating frequency, switching noise coupling on power buses has become an important design issue. To reduce the noise coupling, a split power bus structure has been generally used in package substrates having multilayered power and ground planes. Consequently, there is an increasing need for an efficient method to analyze a split power bus in a multilayered package. This paper introduces a hybrid analytical modeling method for characterizing a split power bus in a multilayered package. The proposed method uses a resonant cavity model combined with a segmentation method. Furthermore, a port assignment technique and an associated calculation method for the equivalent circuit model parameter of the split gap are proposed. The proposed port assignment technique and the analytical equation make it possible to analyze a split power bus, especially in a multilayered package. To verify the proposed method, multilayered test packages are fabricated and tested by means of frequency-domain measurements. In addition, an optimal power bus design method was successfully demonstrated for suppressing noise coupling between chips on a single package. Finally, the proposed method and optimal power bus design method was verified using a series of frequency-domain and time-domain measurements.**

***Index Terms*—Multilayered package substrate, resonant cavity model, segmentation method, simultaneous switching noise (SSN), split power bus.**

I. Introduction

RECENTLY, increases in the clock speed and power consumption of circuits and chips in high-performance systems have lead to occurrences of large and sudden current surges on power buses and to a significant amount of noise on power buses. This noise, known as simultaneous switching noise (SSN), has become a major source of electromagnetic interference, which severely degrades system performance [1]. Moreover, continuing demand for integration of different technologies and for reduction of total product cost has driven use of system on a package (SOP) [2], noise sensitive circuits [such as phase-locked loops (PLL)] placed close to noisy high-speed digital circuits. Therefore, reduction and isolation of the SSN on packages has become a very critical design issue, with regard to improving system reliability and suppressing electromagnetic interference (EMI) [3]–[6].

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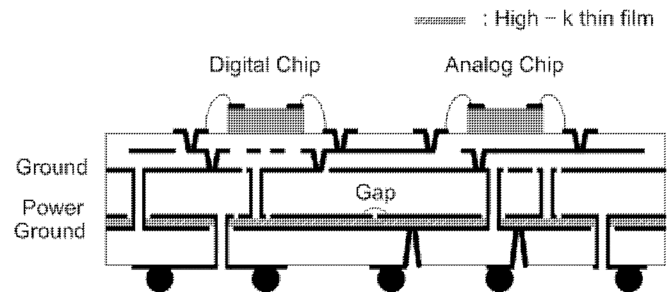

Fig. 1. Example of SOP. A digital chip and an analog chip are mounted on a single package, and a pair of power/ground planes with high-k thin film is used as an embedded decoupling capacitor. The power plane is split into two separate planes by a gap to isolate the simultaneous switching noise from the noisy digital chip to the noise sensitive analog chip.

For example, Fig. 1 illustrates an example of SOP, in which a digital chip and an analog chip are mounted together on a single package. In this package, additional ground and power planes are employed with a high- k dielectric thin film to implement a high-frequency embedded decoupling capacitor into the SOP substrate. In addition, the power plane is split into two separate planes by a gap to isolate a power bus of noise sensitive analog circuits or chips from a power bus of noisy digital circuits or chips. The switching noise of a noisy digital circuit coupled with a noise sensitive analog circuit, such as a PLL or an analog-to-digital converter (ADC), can cause significant timing jitter [7], [8].

As implied in the SOP structure of Fig. 1, several design elements, such as the decoupling capacitor, via, and gap, determine the various characteristics of the power bus, including its impedance, switching noise generation, and switching noise isolation in the multilayered package. Among the design elements, the split power bus in the multilayered package is essential for noise isolation because it is the most cost-effective method for the reduction of the noise coupling. Accordingly, analysis of the split power bus in the multilayered package should precede package design.

Several methods have been used to analyze split power buses in multilayered packages similar to that shown in Fig. 1; these methods include transmission-line modeling methods [9], [10] and two-dimensional (2-D) or three-dimensional (3-D) full-wave numerical methods, such as FDTD, FEM, and MOM [11], [12]. However, a uniform grid step in the transmission-line modeling method causes simulation errors when components or sources are connected to the model [13] and the full-wave

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numerical methods are relatively complex and require significant simulation time and resources. Although there are many analytical modeling methods to analyze solid power buses in multilayered packages [14], [15], it is difficult to apply them directly to a split power bus in the multilayered package structure.

In this paper, we present a hybrid analytical modeling method to analyze a split power bus in a multilayered package by combining a resonant cavity model [14]–[16] and a segmentation method [17]–[20]. Although hybrid modeling methods based on a resonant cavity model and a segmentation method for isolation structures of a power bus in a two-layered PCB were successfully demonstrated in [21], [22], in this paper, the isolation structures of a power bus consisting of multilayered power and ground planes are analyzed using the hybrid modeling method for the first time. For the analysis of a multilayered structure, a port assignment technique and an analytical equation to model the split gap in multilayered package are proposed. The proposed port assignment technique and the analytical equation make it possible to apply the resonant cavity model and the segmentation method to the analysis of a split power bus in a multilayered package. Thus, we can accurately calculate the impedances (Z_{ii}, Z_{ij}) of a split power bus in a multilayered package with the port assignment technique.

To verify the proposed method, we fabricated a series of multilayered test package substrates with embedded capacitor and two separated power planes. Then, the proposed hybrid analytical modeling method was successfully verified by means of impedance measurements in the frequency domain. In addition, the calculated self-impendence and transfer impedances (Z_{ii}, Z_{ij}) show good agreement with the measured impedances. The proposed hybrid analytical modeling method is a gridless equation-based approach and so it is possible to calculate the impedances of the power buses at any port location. Finally, we demonstrate an optimal power bus design method based on the proposed modeling method for a split power bus with an embedded capacitor. We can accurately determine an optimal power bus configuration in a short time and with modest resource consumption. For example, we precisely calculated optimal via positions within 4 min, in contrast with the 2 h needed to complete the calculations using commercial 3-D full wave simulators.

Section II describes the proposed hybrid analytical modeling method for calculating the self-impedance (Z_{ii}) and the transfer impedance (Z_{ij}) of the split power bus in the multilayered package. We introduce the resonant cavity model and the segmentation method, and we propose the port assignment technique and the analytical equation to calculate the equivalent circuit model parameter of the split gap embedded between the two ground planes. Then, a split power bus in the multilayered package is analyzed using the proposed hybrid analytical modeling method. In Section III, we compare the self-impedance (Z_{ii}) and the transfer impedance (Z_{ij}) obtained from the hybrid analytical modeling method and impedance measurement to demonstrate the validity of the model. Finally, we present a power bus design method based on an optimal via position technique to reduce the transfer impedance (Z_{ij}) of the split power bus with the embedded capacitor. The calculation results are well verified by a series of experiments involving frequency- and time-domain measurements.

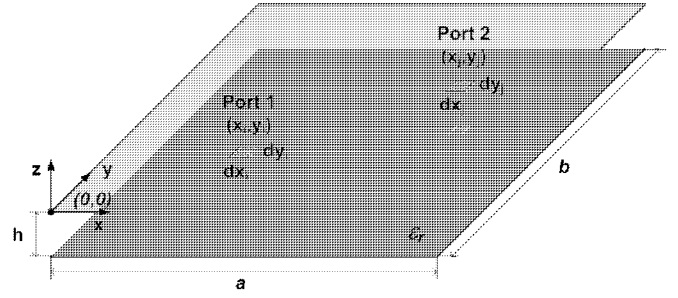


Fig. 2. Geometry of a rectangular power/ground plane structure. Port 1 and Port 2 are defined between the power plane and the ground plane, and are located at (x_i, y_i) and (x_j, y_j), respectively.

II. Hybrid Analytical Modeling Method for Analysis of Split Power Bus in Multilayered Package

In this section, we introduce the resonant cavity model and the segmentation method that are used in the proposed hybrid analytical modeling method. In addition, a port assignment technique and an analytical equation for the split gap model are proposed to analyze a split power bus in a multilayered package. With the port assignment technique and the analytical equation, it is possible to apply the resonant cavity model and the segmentation method to an analysis of a split power bus in a multilayered package.

A. Resonant Cavity Model and Segmentation Method

As shown in Fig. 2, the most common power bus structure in a multilayered package is a rectangular cavity formed by a pair of power and ground planes. The impedance matrix elements of the rectangular power/ground planes can be obtained from a resonant cavity model described in [14]–[16], as shown in

$$\begin{aligned} Z_{ij} = j\omega\mu h \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} & \frac{C_m^2 C_n^2}{ab(k_{xm}^2 + k_{yn}^2 - k^2)} \\ & \times \cos(k_{xm}x_i)\cos(k_{yn}y_i)\cos(k_{xm}x_j)\cos(k_{yn}y_j) \\ & \times \sin c\left(\frac{k_{xm}dx_i}{2}\right)\sin c\left(\frac{k_{yn}dy_i}{2}\right)\sin c\left(\frac{k_{xm}dx_j}{2}\right) \\ & \times \sin c\left(\frac{k_{yn}dy_j}{2}\right) \end{aligned} \quad (1)$$

where the mode number m represents an mth mode associated with the x dimension and the mode number n represents an nth mode associated with the y dimension. The terms a and b are the metal plane widths in the x and y directions, respectively, and two ports are located at (x_i, y_i) and (x_j, y_j) with an electrically small size (dx_i, dy_i) and (dx_j, dy_j), respectively. The constant $C_m^2 C_n^2 = 1$, for $m = n = 0$; $C_m^2 C_n^2 = 2$, for $m = 0, n \neq 0$ or $m \neq 0, n = 0$; and $C_m^2 C_n^2 = 4$, for $m \neq 0, n \neq 0$. When considering a low-loss case, $k = k_r - jk_i$ and $k_i = (k_r/2)(\tan(\delta) + (r/d))$, where k_r is $\omega\sqrt{\mu\varepsilon}$, $\tan(\delta)$ is the loss tangent in the dielectric, and r and d are the skin depth in the metal plane and the thickness of the metal plane, respectively.

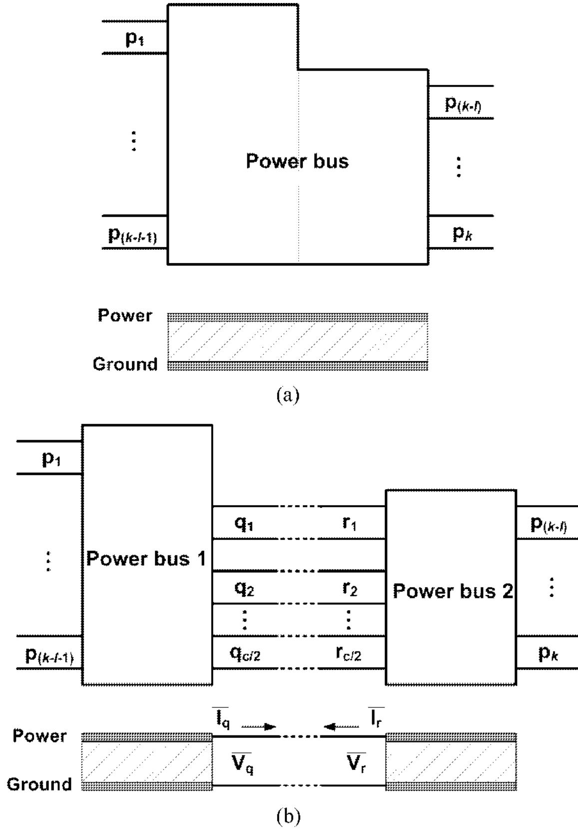


Fig. 3. Concept of the segmentation method using impedance matrices. (a) Irregular power bus including k external ports ($p_1 \sim p_k$). (b) Equivalent representation of the irregular power bus using two rectangular power buses with internal c ports ($q_1 \sim q_{c/2}$ and $r_1 \sim r_{c/2}$).

The function $\sin c(x) = 1$, for $x = 0$, and $\sin c(x) = \sin(x)/x$, for $x \neq 0$. For $(x_i, y_i) \neq (x_j, y_j)$, the term Z_{ij} in (1) represents the transfer impedance between the two ports,and Z_{ii} represents the self-impedance at port (x_i, y_i).

The impedance expression in (1) is very useful when characterizing a power bus consisting of a single rectangular power/ground cavity. However, in practical packages, a power bus will contain many rectangular power/ground plane cavities in a substrate. Furthermore, a power plane is often split into two planes by a gap to reduce noise coupling, as described in Fig. 1. Therefore, in this study, to analyze the split power bus in the multilayered package, we combined the resonant cavity model of (1) with a segmentation method, which was introduced in previous papers [17]–[20].

The segmentation method was originally proposed to analyze 2-D microwave planar circuits and to calculate the impedance, even when the power bus is a power/ground plane of an arbitrary shape. In the segmentation method, the power bus is segmented into rectangular power buses and the interconnections between the rectangular power buses are represented by a finite number of internal ports. The accuracy of the segmentation method is then determined by the number of ports used for the interconnections between the rectangular power buses.

Fig. 3 illustrates the concept of the segmentation method. When there is a power bus consisting of power/ground planes of arbitrary shape, like in Fig. 3(a), the power bus can be represented by a combination of two rectangular power buses and c internal ports, as shown in Fig. 3(b). When the c internal connected ports are divided into two groups, q and r, Z matrices can be written for all ports as in

$$\begin{bmatrix} \bar{V}_p \\ \bar{V}_q \\ \bar{V}_r \end{bmatrix} = \begin{bmatrix} \tilde{Z}_{pp} & \tilde{Z}_{pq} & \tilde{Z}_{pr} \\ \tilde{Z}_{qp} & \tilde{Z}_{qq} & \tilde{Z}_{qr} \\ \tilde{Z}_{rp} & \tilde{Z}_{rq} & \tilde{Z}_{rr} \end{bmatrix} \begin{bmatrix} \bar{I}_p \\ \bar{I}_q \\ \bar{I}_r \end{bmatrix} \tag{2}$$

where $\bar{V}_p$ and $\bar{I}_p$ are the voltages and currents at the k external ports. In addition, $\bar{V}_q, \bar{V}_r, \bar{I}_q$, and $\bar{I}_r$ are the voltages and currents at the c internal ports. The impedance matrices in (2) represent impedances between the voltages and the currents at the external ports and the internal ports.

The voltage and the current relation in (3) represents voltage and current conditions applied when the two rectangular power buses in Fig. 3(b) are connected to each other by the internal ports

$$\begin{aligned} \bar{V}_q &= \bar{V}_r \\ \bar{I}_q + \bar{I}_r &= 0. \end{aligned} \tag{3}$$

Then, by substituting equations of (3) into (2) and by eliminating the internal ports $\bar{V}_q, \bar{V}_r, \bar{I}_q$, and $\bar{I}_r$, the external impedance matrix of the overall network is expressed as

$$\begin{aligned} \tilde{Z}_p = \tilde{Z}_{pp} &+ (\tilde{Z}_{pq} - \tilde{Z}_{pr})(\tilde{Z}_{qq} - \tilde{Z}_{qr} - \tilde{Z}_{rq} + \tilde{Z}_{rr})^{-1} \\ &\times (\tilde{Z}_{rp} - \tilde{Z}_{qp}). \end{aligned} \tag{4}$$

The term $\tilde{Z}_p$ in (4) describes the impedances between the voltages and the currents at the external ports when the internal ports q and r are connected. Then, the expression of (4) can be applied to an analysis of a power bus shaped like that shown in Fig. 3(a). The accuracy of the segmentation method has been demonstrated by showing close agreement between the calculated and the measured results in previous papers [17]–[20]. The expression for the impedance matrices of (4) is useful for the analysis of arbitrary power/ground planes and can be applied further to analyze a split power bus.

For example, a ground plane is shared by power bus 1 and power bus 2, and the two power planes are connected by c internal ports and by an impedance matrix $\tilde{Z}_{\rm int}$, as shown in Fig. 4. The voltage and the current relations (3) are then modified to

$$\begin{aligned} \bar{V}_q &= \bar{V}_r + \tilde{Z}_{\rm int}\overline{I_q} \\ \bar{I}_q &= -\bar{I}_r \end{aligned} \tag{5}$$

where

$$\tilde{Z}_{\rm int} = \begin{bmatrix} Z_{\rm int} & 0 & \cdots & 0 \\ 0 & Z_{\rm int} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & 0 & Z_{\rm int} \end{bmatrix} \quad (c/2 \text{ by } c/2 \text{ matrix}).$$

Now substituting (5) into (4), we obtain the Z matrix as

$$\begin{aligned} \tilde{Z}_p = \tilde{Z}_{pp} &+ (\tilde{Z}_{pq} - \tilde{Z}_{pr})(\tilde{Z}_{qq} - \tilde{Z}_{qr} - \tilde{Z}_{rq} + \tilde{Z}_{rr} + \tilde{Z}_{\rm int})^{-1} \\ &\times (\tilde{Z}_{rp} - \tilde{Z}_{qp}). \end{aligned} \tag{6}$$

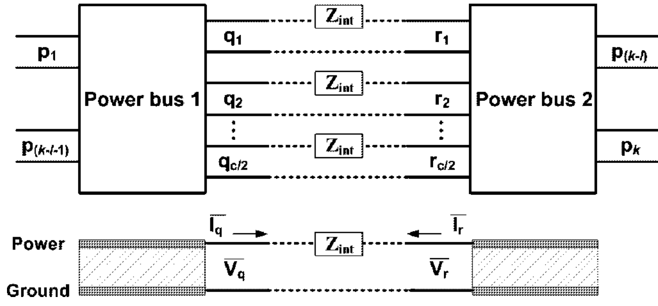


Fig. 4. Concept of enhanced segmentation method using impedance matrices. When the power plane includes a discontinuity modeled by the impedance matrix $\tilde{Z}_{\rm int}$, the overall impedances of the power bus can be calculated based on the current and the voltage relations at the internal ports $q_1 \sim q_{c/2}$ and $r_1 \sim r_{c/2}$.

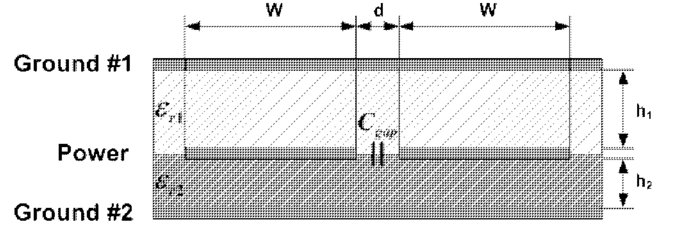


Fig. 5. Modeling of a gap between the power planes embedded in an inhomogeneous dielectric insulator with different thicknesses (h_1 and h_2) and different dielectric constants (ε_{r1} and ε_{r2}). Because the capacitive coupling is the dominant noise coupling path in the split power bus, the gap can be modeled by a capacitor $C_{\rm gap}$ (in farads per meter).

When a gap in a split power bus is modeled by an impedance matrix $\tilde{Z}_{\rm int}$ we can calculate the self-impedance (Z_{ii}) and the transfer impedance (Z_{ij}) of the split power bus.

In the next section, we will derive an analytical equation to calculate the model parameter of the split gap that is embedded between two ground planes. The analytical equation is to be applied to the analysis of a split power bus in a multilayered package.

B. Lumped Circuit Modeling of Gap on Split Power Bus in Multilayered Package

In the previous section, we introduced the resonant cavity model and the segmentation method for calculating the impedances of arbitrary power bus structures. To apply the methods to the analysis of a split power bus in a multilayered package, a gap is modeled using an equivalent lumped circuit model and an analytical equation for the model is derived.

The split power bus has been used as a low-cost structure to prevent noise propagation from noise sources to susceptible devices. When there is no other conductive connection between the two power planes, capacitive coupling across the gap is the primary noise coupling mechanism between the two power planes. Therefore, a split power bus can be modeled by the coupling capacitance at the gap and two pairs of the power/ground planes.

In this paper, we analyze a split power bus, the split power planes of which are embedded between two ground planes with dielectric insulators of different thicknesses (h_1 and h_2) and different dielectric constants (ε_{r1} and ε_{r2}), as shown in Fig. 5. We considered the two power planes embedded in the multilayered package as a parallel-coupled stripline and the capacitances ($C_{\rm gap1}$ and $C_{\rm gap2}$) are segmented as shown in Fig. 6 in order to derive an analytical equation for the capacitance $(C_{\rm gap})$ of Fig. 5. The capacitance $(C_{\rm gap})$ is for a unit length of the gap.

The even-mode and odd-mode capacitances of the parallel-coupled striplines shown in Fig. 6 are provided by (7) and (8) [23]

$$C_{\rm even} = 4\varepsilon_r \frac{K(k_e)}{K(k_e')}\ ({\rm F/m}) \tag{7}$$

where $k_e = \tanh(\pi w/4h)\tanh(\pi/4(w+d/h))$ and $k_e' = \sqrt{1-k_e^2}$, and

$$C_{\rm odd} = 4\varepsilon_r \frac{K(k_o)}{K(k_o')}\ ({\rm F/m}) \tag{8}$$

where $k_o = (\tanh(\pi w/4h))/(\tanh(\pi/4(w+d/h)))$ and $k_o' = \sqrt{1-k_o^2}$.

Here, $K(k)$ is a complete elliptical integral of the first kind

$$K(k) = \frac{\pi}{2}\sum_{n=0}^{\infty}\left[\frac{(2n-1)!!}{2n!!}\right]^2 k^{2n}. \tag{9}$$

By the definition of the odd-mode and the even-mode capacitances in parallel-coupled stripline [24], the capacitance of the split gap is the difference between the odd-mode capacitance and the even-mode capacitance, as described in (10)

$$\begin{aligned} C_{\rm gap1} &= C_{\rm odd1} - C_{\rm even1} \\ &= 2\varepsilon_{r1}\left(\frac{K(k_{o1})}{K(k_{o1}')} - \frac{K(k_{e1})}{K(k_{e1}')}\right)\ ({\rm F/m}) \\ C_{\rm gap2} &= C_{\rm odd2} - C_{\rm even2} \\ &= 2\varepsilon_{r2}\left(\frac{K(k_{o2})}{K(k_{o2}')} - \frac{K(k_{e2})}{K(k_{e2}')}\right)\ ({\rm F/m}) \end{aligned} \tag{10}$$

where

$$\begin{aligned} k_{e1} &= \tanh\left(\frac{\pi w}{4h_1}\right)\tanh\left(\frac{\pi}{4}\left(\frac{w+d}{h_1}\right)\right) \\ k_{e1}' &= \sqrt{1-k_{e1}^2} \\ k_{o1} &= \frac{\tanh\left(\frac{\pi w}{4h_1}\right)}{\tanh\left(\frac{\pi}{4}\left(\frac{w+d}{h_1}\right)\right)}, \quad k_{o1}' = \sqrt{1-k_{o1}^2} \\ k_{e2} &= \tanh\left(\frac{\pi w}{4h_2}\right)\tanh\left(\frac{\pi}{4}\left(\frac{w+d}{h_2}\right)\right) \\ k_{e2}' &= \sqrt{1-k_{e2}^2} \\ k_{o2} &= \frac{\tanh\left(\frac{\pi w}{4h_2}\right)}{\tanh\left(\frac{\pi}{4}\left(\frac{w+d}{h_2}\right)\right)}, \quad k_{o2}' = \sqrt{1-k_{o2}^2} \\ k_{o2}' &= \sqrt{1-k_{o2}^2}. \end{aligned}$$

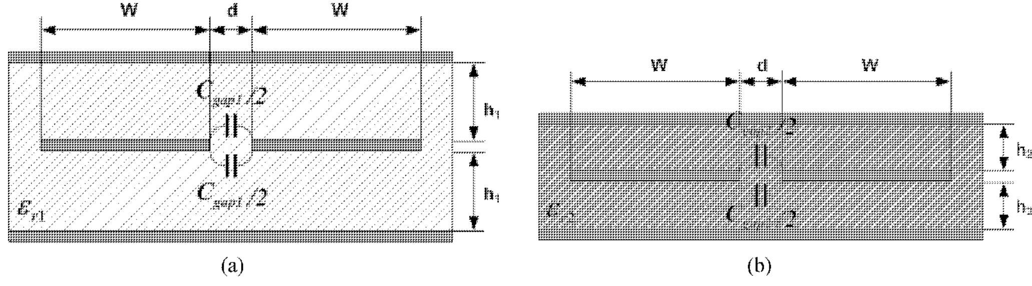


Fig. 6. Modeling of the gap capacitance between two split power planes embedded in a substrate with a homogeneous dielectric insulator. The capacitance representing the model of the gap (C_{gap1} and C_{gap2}) comprises two respective capacitors ($C_{\text{gap1}}/2$ and $C_{\text{gap2}}/2$).

Because the capacitance C_{gap} in Fig. 5 can be approximated by the sum of $C_{\text{gap1}}/2$ and $C_{\text{gap2}}/2$ shown in Fig. 6, the capacitance of the gap is given by

$$\begin{aligned} C_{\text{gap}} &\cong \frac{C_{\text{gap1}} + C_{\text{gap2}}}{2} \\ &= \varepsilon_{r1}\left(\frac{K(k_{o1})}{K(k'_{o1})} - \frac{K(k_{e1})}{K(k'_{e1})}\right) \\ &\quad + \varepsilon_{r2}\left(\frac{K(k_{o2})}{K(k'_{o2})} - \frac{K(k_{e2})}{K(k'_{e2})}\right)\ (\text{F/m}). \end{aligned} \tag{11}$$

Using (11), we can calculate the capacitance representing the model of the gap C'_{gap} and the impedance matrix $\tilde{Z}_{\text{int}}$ for an analysis of a split power bus in a multilayered package, resulting in

$$\tilde{Z}_{\text{int}} = \begin{bmatrix} \frac{1}{j\omega C'_{\text{gap}}} & 0 & \cdots & 0 \\ 0 & \frac{1}{j\omega C'_{\text{gap}}} & \cdots & 0 \\ \vdots & \vdots & \ddots & 0 \\ 0 & 0 & 0 & \frac{1}{j\omega C'_{\text{gap}}} \end{bmatrix} \quad (c/2 \text{ by } c/2 \text{ matrix}). \tag{12}$$

C. Analysis of Split Power Bus in Multilayered Package

In this section, we propose a port assignment technique for a split power bus in a multilayered package, and we combine this technique with the hybrid analytical modeling method, including the resonant cavity model and the segmentation method presented in the previous section.

As the system-switching frequency increases, the frequency of interest in the power bus design also increases and then skin effect becomes evident, causing the surface current at the plane to decay rapidly as it penetrates a conductor surface. This skin-effect approximation makes it possible to divide the multilayered power bus into multiple pairs of vertically two-layered power buses. Analytical modeling methods based on the skin-effect approximation for a multilayered solid power bus have been developed, and these modeling methods have been found to be experimentally valid when the conductor thickness $t \geq 3\delta$, where δ is the skin depth [25].

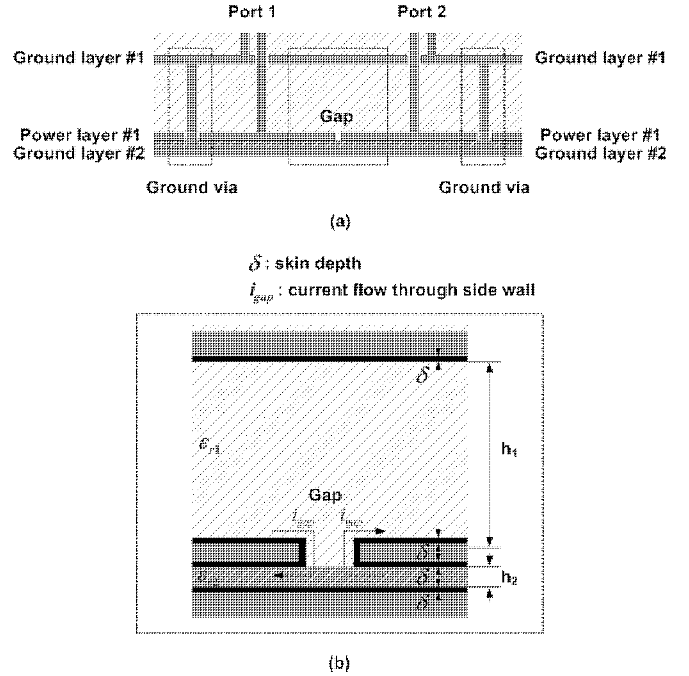


Fig. 7. Cross section of a split power bus structure in a multilayered package, with the skin effect in the gap. (a) The power bus consists of three layers: two ground layers and one power layer. The power plane is split into two separate planes, which are embedded in inhomogeneous dielectric insulators with different thicknesses (h_1 and h_2) and different dielectric constants (ε_{r1} and ε_{r2}), and two ports (Port 1 and Port 2) for impedance measurements are connected to each split power plane referenced to the upper common ground plane of ground layer 1. (b) The surface current at the power plane decays rapidly as it penetrates at high frequency because of skin effect; nevertheless, the current can be conducted vertically through the side wall of the gap in the split power planes embedded between two ground planes.

It is impossible to analyze the split power bus in the multilayered package with the same analysis assumptions used for a solid power bus. As shown in Fig. 7(a) and (b), the current can be conducted from the upper power plane of power layer 1 to the lower power plane of power layer 1 through the sidewall of the gap. Therefore, we cannot separate a split power bus in a multilayered package simply into two pairs of power buses with the skin-effect approximation of [25]. Hence, in this paper, we define virtual ports (Port 3, Port 4, Port 5, and Port 6) between ground layer 1 and ground layer 2, as shown in Fig. 8(a), so that the virtual ports enable the segmentation method to analyze the split power bus in the multilayered package by considering

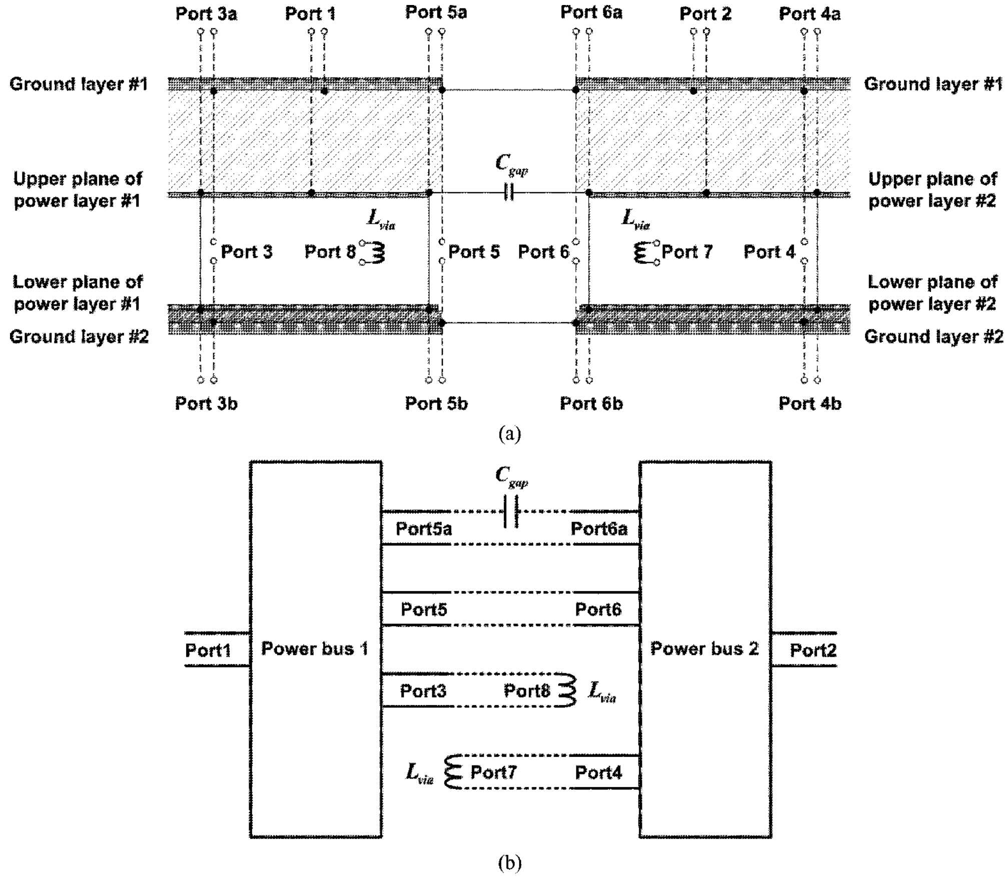


Fig. 8. Model and ports assignment of a split power bus in a multilayered package. (a) Equivalent circuit model for a split power bus in a multilayered package; four virtual ports (Port 3, Port 4, Port 5, and Port 6) are assigned additionally to consider current flow. (b) Ports assignment for segmentation method.

the current flow through the sidewall of the gap. Of the virtual ports, Port 5 and Port 6 are defined for the slot, while Port 3 and Port 4 are defined to consider the ground via connecting the two ground layers, 1 and 2, because current can be conducted through the sidewall of the via void between the upper plane and bottom plane of power layer 1.

Fig. 8(b) shows the port assignments, including the virtual ports by which to apply the segmentation method to analyze a split power bus in a multilayered package. Using the proposed segmentation method and the impedance matrices at the ports described in Fig. 8(b), we can calculate the self-impedance (Z_{ii}) and the transfer impedance (Z_{ij}) at Port 1 and Port 2. When the internal connected ports are the same as group q (Port 3, Port 5a, Port 5, and Port 7) and group r (Port 4, Port 6a, Port 6, and Port 8), the Z matrices of all ports can be written as follows:

$$\begin{bmatrix}\bar{V}_p\\ \bar{V}_q\\ \bar{V}_r\end{bmatrix} = \begin{bmatrix}\tilde{Z}_{pp} & \tilde{Z}_{pq} & \tilde{Z}_{pr}\\ \tilde{Z}_{qp} & \tilde{Z}_{qq} & \tilde{Z}_{qr}\\ \tilde{Z}_{rp} & \tilde{Z}_{rq} & \tilde{Z}_{rr}\end{bmatrix}\begin{bmatrix}\bar{I}_p\\ \bar{I}_q\\ \bar{I}_r\end{bmatrix} \tag{13}$$

where

$$\bar{V}_p = \begin{bmatrix}V_1\\ V_2\end{bmatrix}, \quad \bar{V}_q = \begin{bmatrix}V_3\\ V_7\\ V_{5\mathrm{a}}\\ V_5\end{bmatrix}, \quad \bar{V}_r = \begin{bmatrix}V_8\\ V_4\\ V_{6\mathrm{a}}\\ V_6\end{bmatrix}$$

$$\bar{I}_p = \begin{bmatrix}I_1\\ I_2\end{bmatrix}, \quad \bar{I}_q = \begin{bmatrix}I_3\\ I_7\\ I_{5\mathrm{a}}\\ I_5\end{bmatrix}, \quad \bar{I}_r = \begin{bmatrix}I_8\\ I_4\\ I_{6\mathrm{a}}\\ I_6\end{bmatrix}$$

$$\tilde{Z}_{pp} = \begin{bmatrix}Z_{11} & 0\\ 0 & Z_{22}\end{bmatrix}, \quad \tilde{Z}_{pq} = \begin{bmatrix}Z_{11} & 0 & Z_{15\mathrm{a}} & Z_{15}\\ 0 & 0 & 0 & 0\end{bmatrix}$$

$$\tilde{Z}_{pr} = \begin{bmatrix}0 & 0 & 0 & 0\\ 0 & Z_{24} & Z_{26\mathrm{a}} & Z_{26}\end{bmatrix}$$

$$\tilde{Z}_{qp} = \begin{bmatrix}Z_{31} & 0\\ 0 & 0\\ Z_{5\mathrm{a}1} & 0\\ Z_{51} & 0\end{bmatrix}, \quad \tilde{Z}_{rp} = \begin{bmatrix}0 & 0\\ 0 & Z_{42}\\ 0 & Z_{6\mathrm{a}2}\\ 0 & Z_{62}\end{bmatrix}$$

$$\tilde{Z}_{qr} = \tilde{Z}_{rq} = \begin{bmatrix}0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\end{bmatrix}$$

$$\tilde{Z}_{qq} = \begin{bmatrix}Z_{33} & 0 & Z_{35\mathrm{a}} & Z_{35}\\ 0 & j\omega L_{\mathrm{via}} & 0 & 0\\ Z_{5\mathrm{a}3} & 0 & Z_{5\mathrm{a}5\mathrm{a}} & Z_{5\mathrm{a}5}\\ Z_{53} & 0 & Z_{55\mathrm{a}} & Z_{55}\end{bmatrix}$$

$$\tilde{Z}_{rr} = \begin{bmatrix}j\omega L_{\mathrm{via}} & 0 & 0 & 0\\ 0 & Z_{44} & Z_{46\mathrm{a}} & Z_{46}\\ 0 & Z_{6\mathrm{a}4} & Z_{6\mathrm{a}6\mathrm{a}} & Z_{6\mathrm{a}6}\\ 0 & Z_{64} & Z_{66\mathrm{a}} & Z_{66}\end{bmatrix}.$$

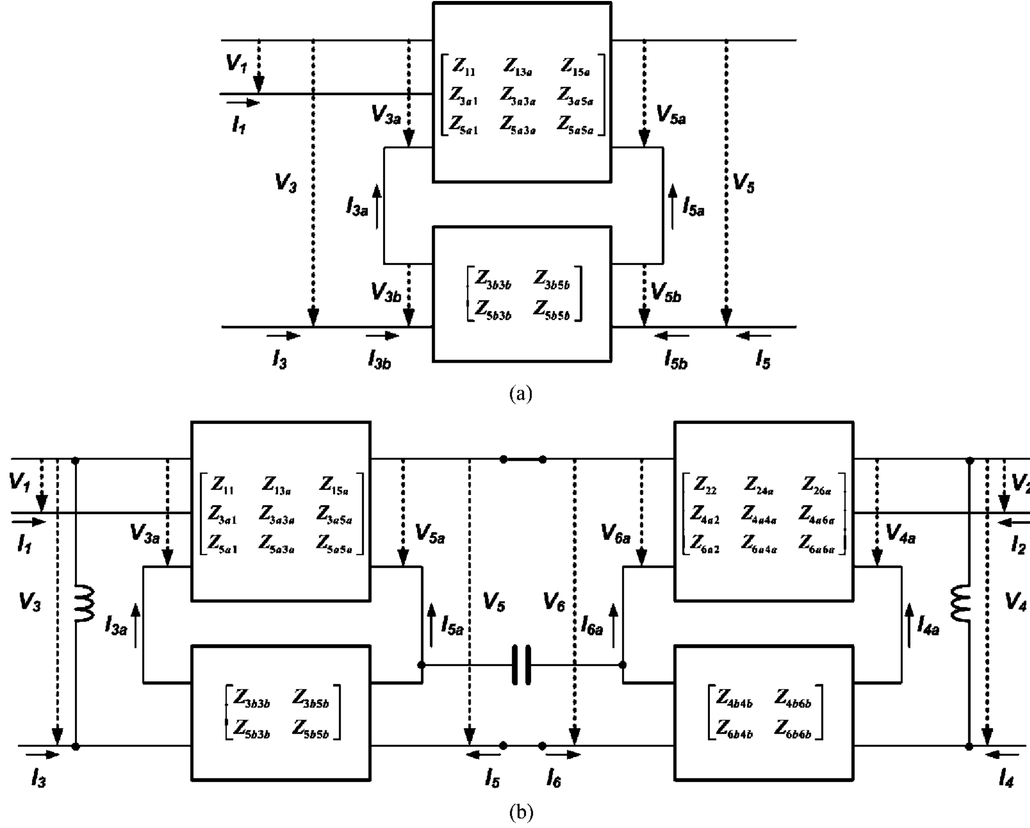


Fig. 9. Equivalent network representation for a split power bus in a multilayered package. (a) Equivalent network representation of the left half on the split power bus. (b) Equivalent network representation of the split power bus, including via and gap model.

Then the overall impedance matrix is calculated by

$$\begin{aligned}\tilde{Z}_p &= \begin{bmatrix} Z_{11_\text{overall}} & Z_{12_\text{overall}} \\ Z_{21_\text{overall}} & Z_{22_\text{overall}} \end{bmatrix} \\ &= \tilde{Z}_{pp} + (\tilde{Z}_{pq} - \tilde{Z}_{pr})(\tilde{Z}_{qq} - \tilde{Z}_{qr} - \tilde{Z}_{rq} + \tilde{Z}_{rr} + \tilde{Z}_{\text{int}})^{-1} \\ &\quad \times (\tilde{Z}_{rp} - \tilde{Z}_{qp}) \end{aligned} \tag{14}$$

where

$$\tilde{Z}_{\text{int}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 1/j\omega C_{\text{gap}} & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

As a result, we can calculate the self-impedance (Z_{ii}) and the transfer impedance (Z_{ij}) at ports 1 and 2 on the split power bus in the multilayered package using (14) after we calculate the impedances in (14). Among the impedances in (14), we can calculate the self-impedances and the transfer impedances at all ports, except the virtual ports, using the resonant cavity model (1). Then, the impedance of the virtual ports (Port 3, Port 4, Port 5, and Port 6) should be calculated.

To calculate the impedance relating to the virtual ports, consider the left section of the power bus, including Port 1, in Fig. 8(a). The impedances for Port 1, Port 3a, and Port 5a are computed for the plane pair consisting of ground layer 1 and the upper plane of power layer 1 as

$$\begin{bmatrix} V_1 \\ V_{3\text{a}} \\ V_{5\text{a}} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{13\text{a}} & Z_{15\text{a}} \\ Z_{3\text{a}1} & Z_{3\text{a}3\text{a}} & Z_{3\text{a}5\text{a}} \\ Z_{5\text{a}1} & Z_{5\text{a}3\text{a}} & Z_{5\text{a}5\text{a}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_{3\text{a}} \\ I_{5\text{a}} \end{bmatrix}. \tag{15}$$

In addition, the impedance matrix for Port 3b and Port 5b for the plane pair composed of ground layer 2 and the lower plane of power layer 1 can be computed as

$$\begin{bmatrix} V_{3\text{b}} \\ V_{5\text{b}} \end{bmatrix} = \begin{bmatrix} Z_{3\text{b}3\text{b}} & Z_{3\text{b}5\text{b}} \\ Z_{5\text{b}3\text{b}} & Z_{5\text{b}5\text{b}} \end{bmatrix} \begin{bmatrix} I_{3\text{b}} \\ I_{5\text{b}} \end{bmatrix}. \tag{16}$$

In (15) and (16), we can calculate the impedances using the resonant cavity model.

The equivalent circuit representation for the left section of the power bus in Fig. 8(a) is shown in Fig. 9(a) [25]. From Fig. 9(a), the current-voltage relations for the plane structure are given as follows:

$$\begin{aligned} &i_3 = i_{3\text{a}} = i_{3\text{b}}, \quad i_5 = i_{5\text{a}} = i_{5\text{b}} \\ &V_3 = V_{3\text{a}} + V_{3\text{b}}, \quad V_5 = V_{5\text{a}} + V_{5\text{b}}. \end{aligned} \tag{17}$$

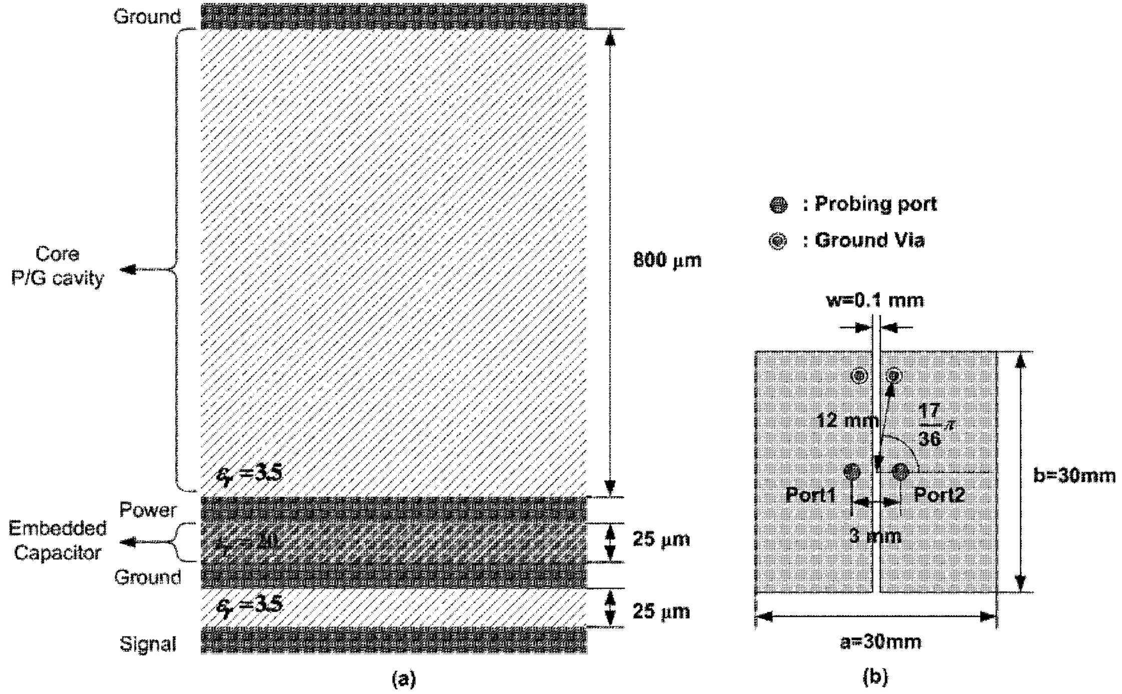


Fig. 10. Test package substrate structure with embedded capacitor. (a) Cross section of the test package substrate, where the thicknesses of the core substrate and the high-k thin film are 800 and 25 μm, respectively, and their permittivities are 3.5 and 20, respectively. (b) The power plane is split into two power planes by a gap with dimensions of $w = 0.1$ mm and $b = 30$ mm.

Based on these relations, the impedance matrices (15) and (16) can be combined, resulting in an impedance matrix

$$\begin{bmatrix} Z_{11} & Z_{13} & Z_{15} & Z_{15a} \\ Z_{31} & Z_{33} & Z_{35} & Z_{35a} \\ Z_{51} & Z_{53} & Z_{55} & Z_{55a} \\ Z_{5a1} & Z_{5a3} & Z_{5a5} & Z_{5a5a} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{13a} & Z_{15a} & Z_{15a} \\ Z_{3a1} & Z_{3a3a} + Z_{3b3b} & Z_{3a5a} + Z_{3b5b} & Z_{3a5a} \\ Z_{5a1} & Z_{5a3a} + Z_{5b3b} & Z_{5a5a} + Z_{5b5b} & Z_{5a5a} \\ Z_{5a1} & Z_{5a3a} & Z_{5a5a} & Z_{5a5a} \end{bmatrix}. \quad (18)$$

For example, we can obtain $Z_{15} = V_1/I_5 = V_1/I_{5b} = V_1/I_{5a} = Z_{15a}$ using (17) and $Z_{51} = Z_{15} = Z_{15a} = Z_{5a1}$ with reciprocal network assumption, and we can also obtain $Z_{35} = V_3/I_5 = V_{3a} + V_{3b}/I_5 = V_{3a}/I_5 + V_{3b}/I_5 = V_{3a}/I_{5a} + V_{3b}/I_{5b} = Z_{3a5a} + Z_{3b5b}$ using (17) and $Z_{35} = Z_{53} = Z_{3a5a} + Z_{3b5b} = Z_{5a3a} + Z_{5b3b}$ with reciprocal network assumption.

From (18), the impedances between Port 1, Port 3, Port 5, and Port 5a can be calculated. For example, the transfer impedance Z_{13} between Port 1 and virtual Port 3 is equal to the transfer impedance Z_{13a} between Port 1 and Port 3a, and the transfer impedance Z_{35} between virtual Port 3 and virtual Port 5 is equal to sum of transfer impedance Z_{3a5a} and transfer impedance Z_{3b5b}. In addition, we can calculate the impedance matrix relating to Port 2, Port 4, Port 6, and Port 6a on the right section of the split power bus in Fig. 8(a), as follows:

$$\begin{bmatrix} Z_{22} & Z_{24} & Z_{26} & Z_{26a} \\ Z_{42} & Z_{44} & Z_{46} & Z_{46a} \\ Z_{62} & Z_{64} & Z_{66} & Z_{66a} \\ Z_{6a2} & Z_{6a4} & Z_{6a6} & Z_{6a6a} \end{bmatrix} = \begin{bmatrix} Z_{22} & Z_{24a} & Z_{26a} & Z_{26a} \\ Z_{4a2} & Z_{4a4a} + Z_{4b4b} & Z_{4a6a} + Z_{4b6b} & Z_{4a6a} \\ Z_{6a2} & Z_{6a4a} + Z_{6b4b} & Z_{6a6a} + Z_{6b6b} & Z_{6a6a} \\ Z_{6a2} & Z_{6a4a} & Z_{6a6a} & Z_{6a6a} \end{bmatrix}. \quad (19)$$

Fig. 9(b) shows the equivalent network representation for the split power bus in the multilayered package shown in Fig. 8(a), including the right-hand section of the split power bus and the lumped circuit models for the vias and the split gap. The impedance parameters in the boxes can be computed using the methods previously described. Then, the external impedance parameters $(Z_{11}, Z_{12}, Z_{21}, Z_{22})$ of Port 1 and Port 2 are calculated from these impedances, using the proposed enhanced segmentation method.

III. Verification and Application of Hybrid Analytical Modeling Method

A. *Verification of Hybrid Analytical Modeling Method*

To verify the proposed hybrid analytical modeling method, test package substrates were designed and fabricated for Z-parameter measurement, and the measured results were compared with the calculated results to verify the accuracy of the model. Fig. 10 illustrates the layout and the cross-section of the test package substrate.

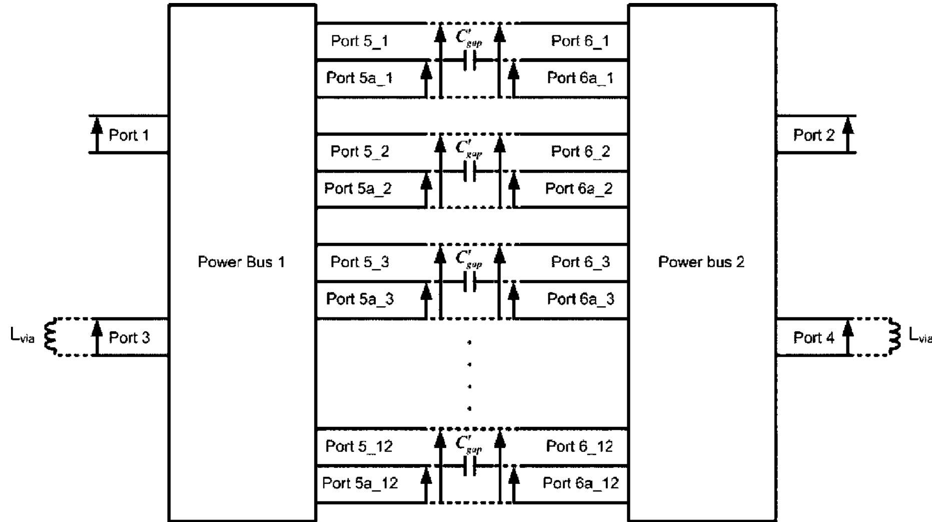
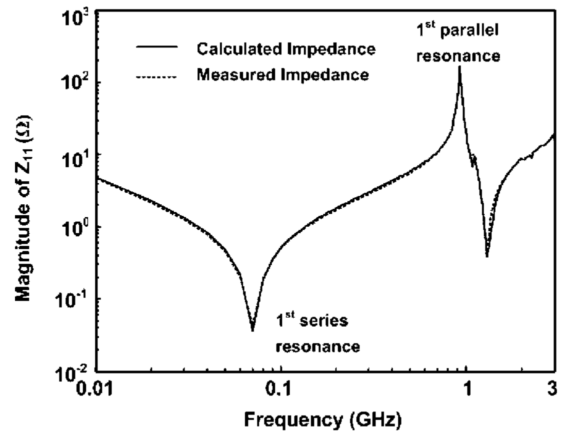


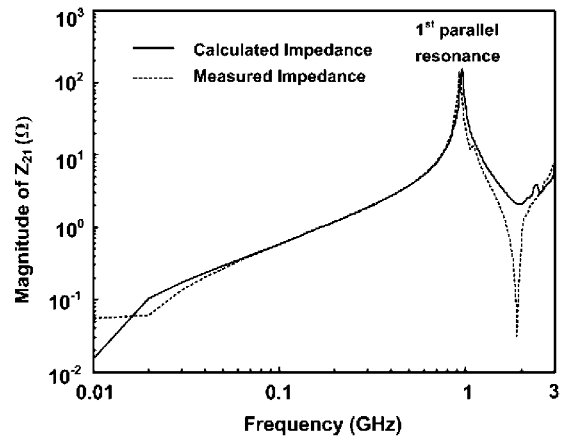
Fig. 11. Ports assignment and equivalent circuit model of the split power bus with the embedded capacitor. Port 5_1–Port 5_12, Port 5a_1–Port 5a_12, and Port 6_1—Port 6_12, Port 6a_1—Port 6a_12 are assigned for internal connections with the gap model; Port 3 and Port 4 are assigned for the via connection.

As shown in Fig. 10(a), the test package substrate comprises four conductor layers with dimensions $a = 30$ mm and $b = 30$ mm. BT resin was used as the dielectric material of the core substrates with permittivity $\varepsilon_r = 3.5$ and thickness $d = 0.8$ mm. In addition, a high-k thin film with permittivity $\varepsilon_r = 20$ and thickness $d = 0.02$ mm with a pair of power/ground planes was used for the embedded capacitor, which reduces switching noise on the power bus as a decoupling capacitor. When we set the origin at the center of the test package substrate in Fig. 10(b), two probing ports are located at $(-1.5, 0\text{ mm})$ and $(1.5, 0\text{ mm})$, and two vias connecting the two ground planes are located at (0.5, 12 mm) and $(-0.5, -12\text{ mm})$. The power plane is split into two planes by a gap with dimensions of $w = 0.1$ mm and $b = 30$ mm. An Agilent vector network analyzer 8753ES and a Cascade GS type microprobe with 400 μm pitch were used to measure the S parameter for a frequency range from 10 MHz to 3 GHz; then, the measured S parameters were converted to Z parameters by the conversion relation [26].

The basic analytical modeling method was described in the previous section, and it was explained that the gap is modeled using a single capacitor. However, to apply this method to the calculation of the impedance for the test package substrate, the gap should be modeled as an array of capacitors, and the number of capacitors (C'_{gap}) in the array is dependent upon the maximum frequency of interest, which affects the accuracy of the model. In this study, because the maximum frequency was 3 GHz and the length of the gap was 30 mm, the split power bus was modeled using 12 internal ports per plane and 12 capacitors $C'_{\text{gap}} = (C_{\text{gap}} \times 30\,\text{mm})/12$ (Farad). Then, the total ports were defined as shown in Fig. 11, and the impedance for each port was calculated by means of the methods described in the previous sections. In Fig. 11, the inductances representing the equivalent circuit models of the vias are analytically calculated [27] and the values are approximately 0.5 nH; the capacitance representing the equivalent circuit model of the slot is calculated by (11) and the value is 0.06 pF for each capacitor of the array.



(a)



(b)

Fig. 12. Comparison of the calculated and the measured results. The solid line represents the impedances calculated using the proposed hybrid analytical modeling method, whereas the dotted line represents the impedances obtained from the measured S parameters. (a) Comparison of the calculation and the measurement of Z_{11} up to 3 GHz. (b) Comparison of the calculation and the measurement of Z_{21} up to 3 GHz.

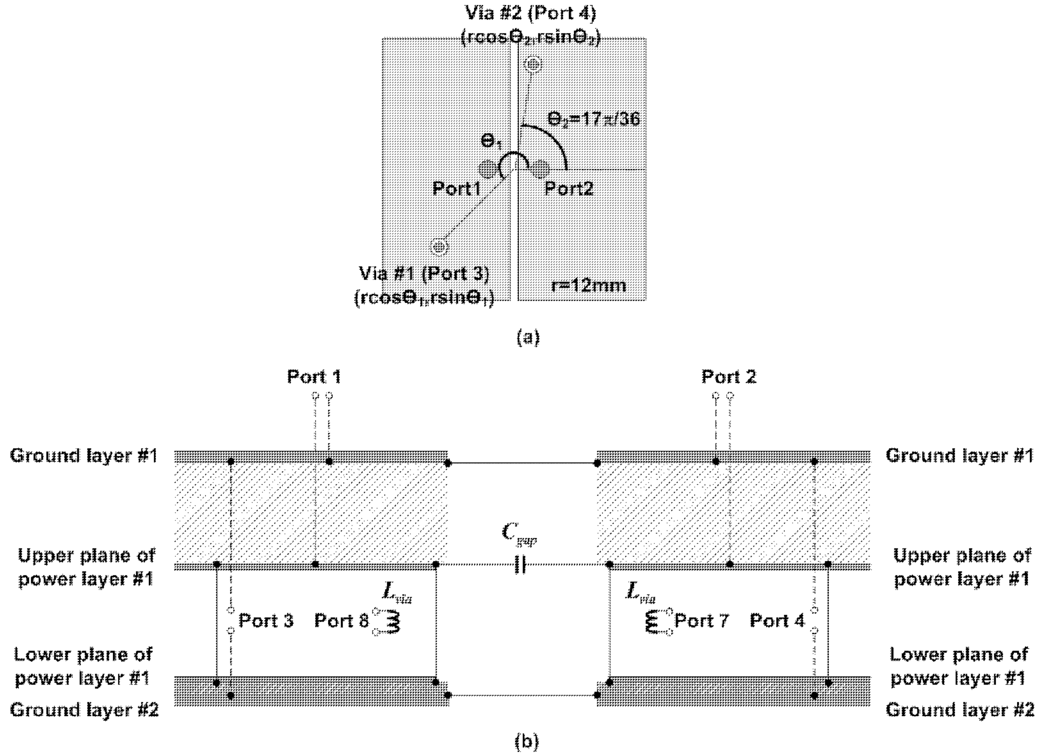


Fig. 13. Dimensions and cross section of a test package substrate to demonstrate the optimal position of the via on the split power bus with an embedded capacitor. (a) Top view of the split power plane. (b) Cross section of the test package substrate and ports assignment.

Fig. 12 shows the self-impedance and the transfer impedances of the test package substrate shown in Fig. 10(b) obtained by both measurement and calculation. The calculated impedances show a good correlation with the measured impedances. In Fig. 12(a), the self-impedance (Z_{11}) shows a series resonance at 70 MHz because of the capacitance of the embedded capacitor ($\approx$3.47 nF) and the effective inductance of the planes ($\approx$1.49 nH). In addition, the self-impedance (Z_{11}) in Fig. 12(a) and the transfer impedance (Z_{21}) in Fig. 12(b) show a parallel resonance at 1 GHz because of the effective inductance of the core plane cavity and the capacitance of the core plane cavity.

Fig. 12 illustrates that we can use the proposed hybrid analytical modeling method to characterize and analyze a split power bus in a multilayered package with high accuracy.

B. Optimal Via Positioning for Suppression of Switching Noise Coupling on Split Power Bus With an Embedded Capacitor

In this section, we describe an optimal power bus design methodology based on the proposed hybrid modeling method to demonstrate the usefulness of the proposed modeling method. The resultant calculation results are verified by means of frequency and time-domain measurements.

Positioning of the ground via that connects the two ground planes is a power bus design element for the test package substrate, shown in Fig. 13, used to verify the proposed hybrid analytical modeling method. We can minimize the magnitude of the transfer impedance Z_{21} by optimally positioning the via.

In Fig. 13, we assume that via 1 and via 2 are located at $(r\cos\theta_1, r\sin\theta_1)$ and $(r\cos\theta_2, r\sin\theta_2)$ respectively. To simplify the optimization, θ_2 and r are fixed at $17\pi/36$ and 12 mm, respectively. When θ_1 varies from $\pi/2$ to $3\pi/2$, the transfer impedance Z_{21} between Port 1 and Port 2 changes. Therefore, the optimal position of via 1 can be found by scanning the calculated transfer impedances at a target frequency, using the hybrid analytical modeling method described in the previous section. Once the optimal positioning is chosen, when the target frequency is set below the first parallel resonance frequency, the impedance is minimized for a broad frequency range below the first parallel resonance frequency, because the power bus shows inductive characteristics for the broad frequency range below the first parallel resonance frequency.

This is an efficient scheme to determine the optimal position of design elements such as the via, and it is often used in the other analysis methods, such as full-wave simulation. However, in full-wave simulation, an excessive amount of time is required to complete the calculation, because the mesh must be reconstructed and the impedance needs to be repeatedly calculated for varied port locations. In contrast, using the proposed analytical modeling method, only the impedances relating to Port 3 need to be updated to calculate the transfer impedances between Port 1 and Port 2, thereby greatly reducing the calculation time, while Port 3 indicates the position of via 1. For example, when θ_1 is changed from $\pi/2$ to $3\pi/2$ in 18 steps, it takes approximately four minutes to complete the computation using the proposed analytical modeling method; in contrast, the same computation takes two hours using the 3-D full-wave simulation.

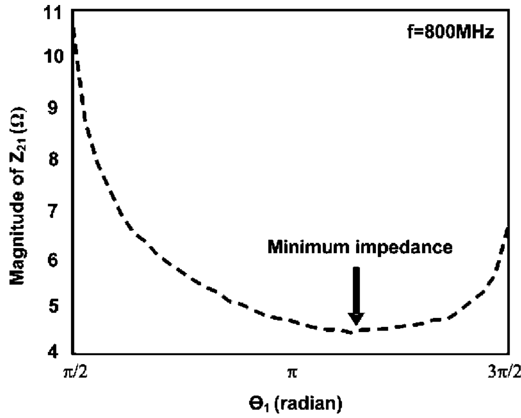


Fig. 14. Calculated transfer impedance corresponding to the via 1 position at $f = 800$ MHz. From this graph, the optimized position of the via 1 can be obtained.

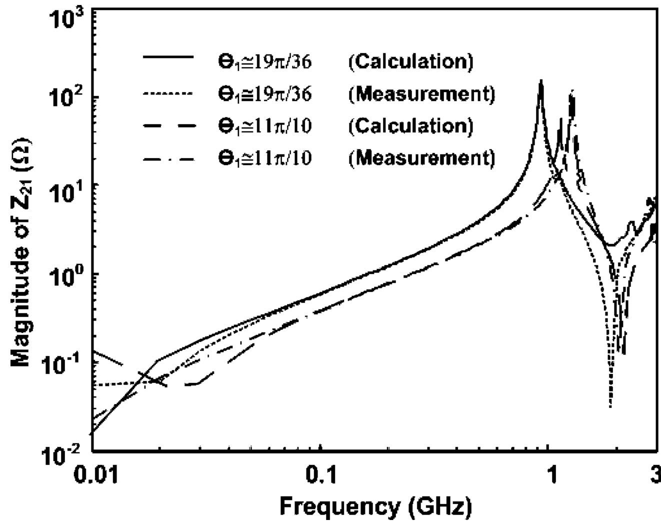


Fig. 15. Comparison of the calculation and the measurement of Z_{21} up to 3 GHz corresponding to the position of via 1. The transfer impedance is minimized at the optimized via position up to the first parallel resonance frequency when the target frequency is set at 800 MHz.

The transfer impedance was calculated using the method explained in the previous section, and Fig. 14 shows the calculated transfer impedance Z_{21} corresponding to the position of via 1 at $f = 800$ MHz. It was found that the transfer impedance is minimized at $\theta_1 = 11\pi/10$.

In Fig. 15, the measured transfer impedance (Z_{21}) and the calculated transfer impedance (Z_{21}) are compared when the via 1 is located at the worst position $(\theta_1 = 19\pi/36)$ and at the optimal position $(\theta_1 = 11\pi/10)$. As shown in the graph, the results confirm the validity of the proposed design methodology, and it is well verified that the optimal via position reduces the magnitude of the transfer impedance Z_{21}, while Z_{21} represents the degree of switching noise coupling on the split power bus in the multilayered package. Furthermore, it is found that the first parallel resonance frequency is shifted to a higher frequency when the position of via 1 is optimized, because the optimized position of via 1 reduces the effective inductance of the plane.

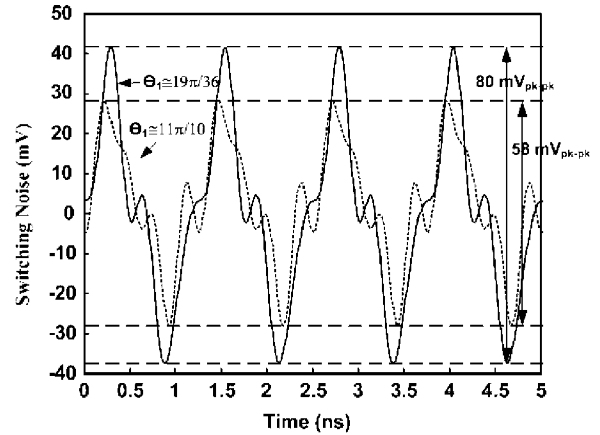


Fig. 16. Calculated switching noise waveforms at Port 2 on the split power bus with an embedded capacitor. With the optimal via position $(\theta_1 = 11\pi/10)$, the switching noise at Port 2 was reduced from 80 to 53 $\mathrm{mV_{pk-pk}}$.

To verify the power bus design methodology using the proposed hybrid analytical modeling method in time domain, we have measured switching noise waveforms and have compared them with both the time-domain calculation data at the worst via position $(\theta_1 = 19\pi/36)$ and that at the optimal via position $(\theta_1 = 11\pi/10)$. For the time-domain calculation, a current profile on the power bus was extracted via a spice simulation, and the current spectrum was calculated using a fast Fourier transform. Subsequently, the noise voltage spectrum at Port 2 was obtained using the product of the current spectrum at port 1 and the transfer impedance of the power bus Z_{21}. Finally, the switching noise at Port 2 was calculated from the noise voltage spectrum at Port 2 using an inverse fast Fourier transform.

In this experiment, a commercial clock driver (TI CDCVLP110) was mounted on the test package substrate as a noise source at Port 1 with 800 MHz differential clock inputs from a pulse pattern generator, and the noise was measured with an oscilloscope fitted with a high-impedance probe. Because the clock driver has differential I/O circuits, its switching noise is relatively low; therefore, we used 25-Ω and 75-Ω resistors to produce unbalanced termination conditions at differential outputs. Unbalanced termination increases the switching noise on the power bus.

The calculated switching noise waveforms are shown in Fig. 16. The chip is assumed to be located at Port 1 and the noise is calculated at Port 2 in the split power bus with an embedded capacitor. In this noise waveform, the voltage was reduced from 80 to 53 $\mathrm{mV_{pk-pk}}$ by optimizing the position of via 2. Fig. 17 shows the measured switching noise waveforms, which are slightly different from the calculated result, because a commercial clock driver is used as the noise source, and it is infeasible to model the driver precisely. If a precise driver model could be provided, the switching noise could be calculated accurately from the current profile. In the measured result, the switching noise was reduced from 77 to 60 mV, and it is found that the optimization of via 1 reduces the switching noise efficiently.

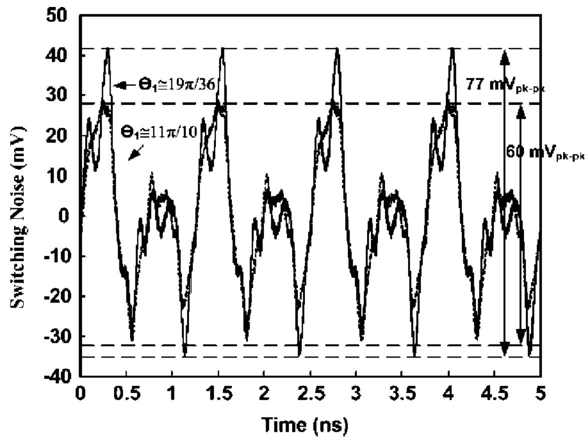


Fig. 17. Measured switching noise waveforms at Port 2 on the split power bus with an embedded capacitor. With the optimal via position ($\theta_1 = 11\pi/10$), the switching noise at Port 2 was reduced from 77 to 60 mV_{pk-pk}.

IV. Conclusion

In this paper, a hybrid analytical modeling method for calculating the impedance of a split power bus in a multi-layered package was demonstrated, and the method was verified using fabricated test package substrates that included an embedded capacitor. The hybrid analytical modeling method used to analyze a split power bus in a multilayered package combines a resonant cavity model and a segmentation method. Especially for the analysis of a multilayered package, a port assignment technique considering vertical current flowing in the gap and an analytical equation to model the split gap were proposed. The proposed port assignment technique and the analytical equation make it possible to apply the resonant cavity model and the segmentation method to an analysis of a split power bus in a multilayered package. Subsequently, we can accurately calculate impedances of a split power bus in a multilayered package with the proposed port assignment technique. The calculated impedance shows a good correlation up to 3 GHz, and it is possible to increase the accuracy of the model when precise models of the non planar structures, such as the via and the gap, are given. Finally, the power bus design methodology was demonstrated using the hybrid analytical modeling method, and it was verified by means of frequency-domain and time-domain measurements. The measurement results show that we can effectively reduce the switching noise by means of optimal via distribution based on the proposed hybrid analytical modeling method. Using the proposed hybrid analytical modeling method, it is possible both to accurately characterize a split power bus in a multilayered package and to efficiently design a package to include a split power bus with low impedance.

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