Hybrid Cascaded H-bridges Multilevel Motor Drive Control for Electric Vehicles

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***Abstract* — This paper presents a hybrid cascaded H-bridge multilevel motor drive control scheme for electric/hybrid electric vehicles where each phase of a three-phase cascaded multilevel converter can be implemented using only a single DC source and capacitors for the other DC sources. Traditionally, each phase of a three-phase cascaded multilevel converter requires *n* DC sources for 2*n* + 1 output voltage levels. In this paper, a scheme is proposed that allows the use of a single DC source as the first DC source with the remaining *n* - 1 DC sources being capacitors. It is shown that a simple 7-level equal step output voltage switching control can simultaneously maintain the balance of DC voltage levels of the capacitors, eliminate specified low order non-triplen harmonics, and produce a nearly sinusoidal three-phase output voltage. This scheme therefore provides the capability to produce higher voltages at higher speeds (where they are needed) with a low switching frequency method for motor drive application, which has inherent low switching losses and high conversion efficiency. This control scheme especially fits fuel cell electric vehicle motor drive applications and hybrid electric vehicle motor drive applications.**

Keywords: hybrid cascaded H-bridge multilevel converter, DC voltage balance control, multilevel motor drive, electric/hybrid electric vehicle application.

I. Introduction

The multilevel converter is a promising power electronics topology for high power motor drive applications because of its low electromagnetic interference (EMI) and high efficiency using a fundamental switching scheme. The cascaded multilevel converter with separate DC sources can fit many of the needs of all-electric vehicles because it can use onboard batteries or fuel cells to generate a nearly sinusoidal voltage waveform to drive the main vehicle traction motor [1]-[3].

Traditionally, each phase of a cascaded multilevel converter requires *n* DC sources for 2*n* + 1 levels [1]-[3]. For many applications, to get many separate DC sources is difficult, and too many DC sources will require many long cables and could lead to voltage unbalance among the DC sources. To reduce the number of DC sources required when the cascaded H-bridge multilevel converter is applied to a motor drive, a scheme is proposed in this paper that allows the use of a single DC source (such as battery or fuel cell) as the first DC source with the remaining *n*–1 DC sources being capacitors in the cascaded H-bridges multilevel converter. The control goal here is to maintain the balance of the DC voltage level of each of the capacitors while simultaneously producing a nearly sinusoidal three-phase output voltage with a low switching frequency control method. This scheme therefore provides the capability to produce higher voltages at higher speeds (where they are needed) with a low switching frequency, which has inherent low switching losses and high conversion efficiency. This kind of multilevel converter motor drive is referred to as a hybrid multilevel motor drive in this paper. For electric/hybrid electric vehicle motor drive applications, two or three H-bridges for each phase is a good tradeoff between performance and cost.

The work presented here is based on the previous work by the authors in [4]. However, after this paper was accepted for publication, the authors were made aware of the prior work [5], which is essentially the same method.

II. Working Principle of Hybrid Cascaded H-bridge Multilevel Motor Drive

To operate a cascaded multilevel converter using a single DC source, it is proposed to use capacitors as the DC sources for all but the first source. To simplify this problem, consider a cascaded multilevel converter with two H-bridges as shown in Fig. 1. The DC source for the first H-bridge (H_1) is a battery or fuel cell with an output voltage of V_{dc}, and the DC source for the second H-bridge (H_2) is the capacitor voltage to be held at V_c. The output voltage of the first H-bridge is denoted by v_1, and the output of the second H-bridge is denoted by v_2 so that the output voltage of the cascaded multilevel converter is

$$v(t) = v_1(t) + v_2(t) \tag{1}$$

By opening and closing the switches of H_1 appropriately, the output voltage v_1 can be made equal to $-V_{dc}$, 0, or V_{dc} while the output voltage of H_2 can be made equal to $-V_c$, 0, or V_c by opening and closing its switches appropriately. Therefore, the

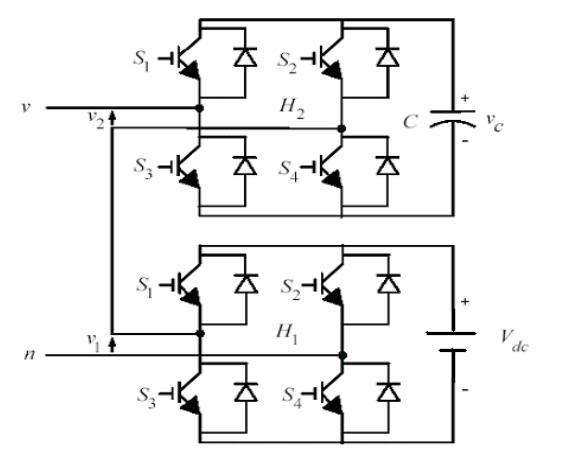

Fig. 1. Topology of a single phase of the proposed multilevel converter with a single DC source for first level and capacitors for other levels.

output voltage of the converter can have the values $-(V_{dc}+V_c)$, $-V_{dc}$, $-(V_{dc}-V_c)$, $-V_c$, 0, V_c,, $(V_{dc}-V_c)$, V_{dc}, and $(V_{dc}+V_c)$, which are 9 possible output levels. For the 9 possible levels used in a cycle, $-(V_{dc}-V_c)$ and $(V_{dc}-V_c)$ can be used to charge the capacitors; $-(V_{dc}+V_c)$, $-V_c$, V_c and $(V_{dc}+V_c)$ can be used to discharge the capacitors.

Not all the possible voltage levels must be used in a cycle. A simple 7-level output voltage case is illustrated in Fig. 2 where $V_c = V_{dc}/2$. This waveform can be achieved using two distinct switching patterns.

One possible cycle is to output $-(V_{dc}+V_c)$, $-V_{dc}$, $-(V_{dc}-V_c)$, 0, $(V_{dc}-V_c)$, V_{dc}, $(V_{dc}+V_c)$. *This is illustrated in Fig. 3 with* $V_c = V_{dc}/2$.

Another possible cycle is to output $-(V_{dc}+V_c)$, $-V_{dc}$, $-V_c$, 0, V_c, V_{dc}, $(V_{dc}+V_c)$. *This is illustrated in Fig. 4 with* $V_c = V_{dc}/2$.

To charge the capacitor, then choose the switching scheme with $v_1 = V_{dc}$, $v_2 = -(V_{dc}-V_c)$ *if* $i > 0$. *Otherwise, if* $i < 0$, *the switching scheme with* $v_1 = 0$, $v_2 = V_c$ *is chosen to charge the capacitor.*

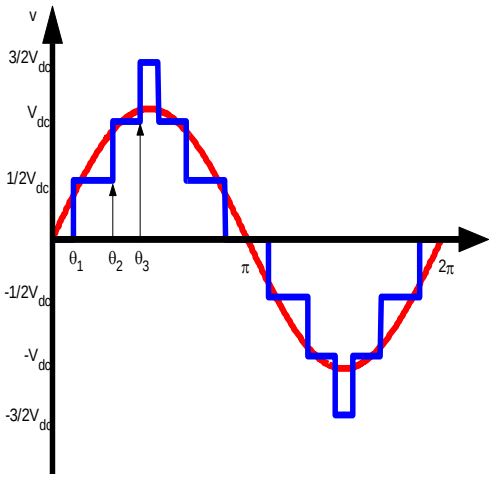

Fig. 2. 7-level equal step output voltage waveform.

For the two possibilities, the output voltage waveforms are identical thus they have the same harmonic content.

In the 7-level equal step output voltage example, the fact that the output voltage level $V_{dc}/2$ can be achieved in two different ways is exploited to keep the capacitor voltage balanced (see [4] and [5]). The voltage on the capacitor is regulated when the desired output voltage is $V_{dc}/2$. For practical applications, the capacitor voltage V_c needs to be measured. Fig. 3 shows how the waveform of Fig. 2 is generated if for $\theta_1 \le \theta < \theta_2$, $v_1 = V_{dc}$ and $v_2 = -V_{dc}/2$ is chosen. In contrast, Fig. 4 shows how the waveform of Fig. 2 is generated if, for $\theta_1 \le \theta < \theta_2$, $v_1 = 0$ and $v_2 = V_{dc}/2$ is chosen.

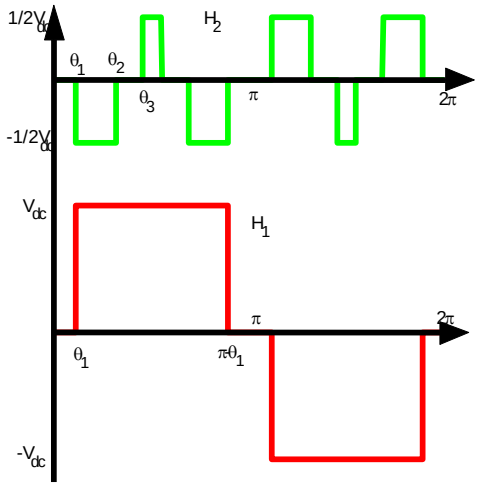

Fig. 3. Capacitor charging cycle for H-bridges H_1 and H_2.

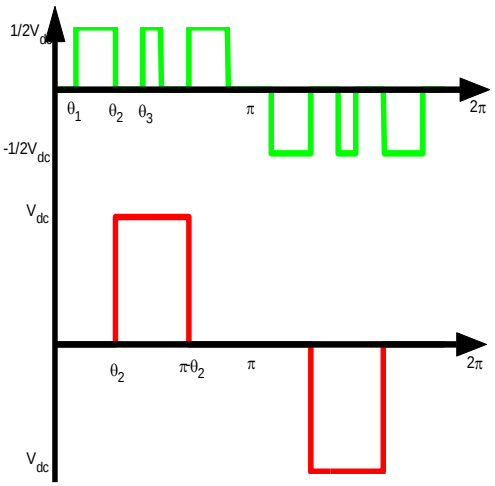

Fig. 4. Capacitor discharging cycle for H-bridges H_1 and H_2.

By choosing the nominal value of the capacitor voltage to be one half that of the DC source, the nominal values of the levels are equally spaced. However, this is not required. The criteria for this capacitor balancing scheme is that (1) the desired capacitor voltage is less than the DC source voltage, (2)

the capacitance value is chosen large enough so that the variation of its voltage around its nominal value is small (generally, one can choose the capacitor-load time constant to be greater than 10 times of the fundamental cycle time), and (3) the capacitor charging energy is greater than or equal to the capacitor discharge energy in a cycle.

III. Modulation Control

Generally, traditional PWM control methods and space vector PWM methods are applied to multilevel converter modulation control. The disadvantage of the traditional PWM methods is the power loss in the switches due to the high switching frequency [6]-[15]. For these reasons, low switching frequency control methods, such as a fundamental frequency method [16], and the active harmonic elimination method [17] have been proposed for motor drive applications.

If the nominal capacitor voltage is chosen as $V_{dc}/2$, then the fundamental frequency switching scheme angles for equal DC sources can be used in the hybrid multilevel motor drive control. This is the simplest switching control method for the proposed hybrid multilevel motor drive. It also is an effective modulation control method for the proposed hybrid cascaded multilevel converter motor drive.

A. 7-level Equal Step Output Voltage Switching Control

The Fourier series expansion of the 7-level equal step output voltage waveform is

$$V(\omega t) = \sum_{n=1,3,5\Lambda}^{\infty} \frac{4V_{dc}}{n\pi}(\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3))\sin(n\omega t) \tag{2}$$

where n is the harmonic number of the output voltage of the multilevel converter. Given a desired fundamental voltage V_1, one wants to determine the switching angles θ_1, θ_2, θ_3 so that $V(\omega t) = V_1 sin(\omega t)$, and specific higher harmonics of $V(n\omega t)$ are eliminated [18]-[20]. For three-phase motor drive applications, the triplen harmonics in each phase need not be canceled as they automatically cancel in the line-to-line voltages. In this paper, the goal is to eliminate the 5th and 7th harmonics. Mathematically, this can be formulated as the solution to the following equations:

$$\begin{aligned} \cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) &= m \\ \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) &= 0 \\ \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) &= 0 \end{aligned} \tag{3}$$

This is a system of three transcendental equations in the three unknowns θ_1, θ_2 and θ_3. There are many ways one can solve for the angles (see, for example, [17], [21] - [23]). Here the resultant method (see [14] and [20]) was used to find the switching angles. The modulation index m is defined as

$$m = \frac{\pi V_1}{2V_{dc}}, \tag{4}$$

and the total harmonic distortion (THD) up to the 50th harmonic (odd, non-triplen) is computed as

$$THD = \frac{\sqrt{V_5^2 + V_7^2 + \ldots + V_{49}^2}}{V_1}. \tag{5}$$

B. Hybrid Electric Vehicle Application Considerations

One possible application for the hybrid cascaded multilevel motor drive is an electric/hybrid vehicle. Electric/hybrid vehicles use batteries to run an electric motor. Presently, a three-phase full bridge PWM converter is used for electric/hybrid electric vehicles. The instantaneous output power is limited by the battery voltage, and a high power DC-DC boost converter is required to utilize braking energy to charge the batteries. The proposed hybrid cascaded H-bridge multilevel motor drive has two advantages over this traditional topology. The proposed hybrid multilevel motor drive can inherently produce a larger output voltage than a traditional three-level motor drive. The hybrid cascaded multilevel motor drive also can be used to absorb braking energy at low speeds because one or several of the capacitors can be charged based on the charging voltage without the need for a high power DC-DC boost converter.

IV. Experimental Results

To experimentally validate the proposed hybrid cascaded H-bridge multilevel motor drive control scheme, a prototype three-phase cascaded H-bridge multilevel converter has been built using MOSFETs as the switching devices. Three DC power supplies (one for each phase) feed the motor drive. A real-time variable output voltage, variable frequency three-phase motor drive controller based on Altera FLEX 10K field programmable gate array (FPGA) is used to implement the control algorithm with 8 μs control resolution. For convenience of operation, the FPGA controller was designed as a card to be plugged into a personal computer, which used a peripheral component interconnect (PCI) bus to communicate with the microcomputer. To maintain the capacitor's voltage balance, a comparator using operational amplifier is used to detect the capacitor's voltage and feed the voltage signal into the FPGA controller. A 1/3 hp induction motor is connected to the motor drive as its load.

In the experimental implementation, to simplify the switching control issue, the 7-level equal step output voltage switching method is used. The capacitors' voltages are regulated to $V_{dc}/2$ (24 V).

Two 7-level equal step output voltage cases are implemented: 1) with the modulation index m = 0.82 and the output frequency equal to 30 Hz, and 2) with m = 1.32 and the output frequency equal to 60 Hz. Fig. 5 shows the output phase voltage waveform for m = 0.82 and f = 30Hz. Fig. 6 shows the normalized FFT analysis of its line-line voltage. From the FFT analysis, it can be seen that the 5th and 7th harmonics are near

zero, and the first non-zero harmonic is the 11th. Here, the 5th and 7th harmonics are not exactly zero because the capacitor's voltage is not constant, but varying with time. This can be seen from the voltage waveforms. The output voltages are not constant for each level, because of the effect of charging and discharging of the capacitors.

Also, transients appeared in the output voltage waveforms at some of the step changes. This is because the dead time for each H-bridge is not exactly the same. The combination of several H-bridges will produce these transients.

The phase current waveform for m = 0.82 and f = 30 Hz and its normalized FFT analysis are shown in Fig. 7 and 8, respectively. The high frequency current harmonics are lower than that of its corresponding voltage harmonics because the induction motor acts as a low-pass filter. For example, the 11th voltage harmonic is more than 20%; however, its corresponding current harmonic is less than 20%.

For the Case 2 experiment, the modulation index is 1.32 and the fundamental frequency is 60 Hz. The phase voltage waveform is shown in Fig. 9, and its corresponding normalized FFT analysis of line-line voltage is shown in Fig. 10. The phase current waveform is shown in Fig. 11, and its corresponding normalized FFT analysis of phase current is shown in Fig. 12. Also, it can be derived that the normalized current harmonic contents are less than its corresponding normalized voltage harmonic contents because the induction motor acts as a low-pass filter.

V. Conclusions

This paper developed a new hybrid cascaded H-bridges multilevel motor drive control scheme that required only one power source for each phase. A 7-level equal step output voltage switching control method has been applied to the motor drive. It can be derived from the computational results and experimental results that this motor drive scheme can maintain its capacitors' voltage balance using a low switching frequency control method and eliminate the specified low order harmonics.

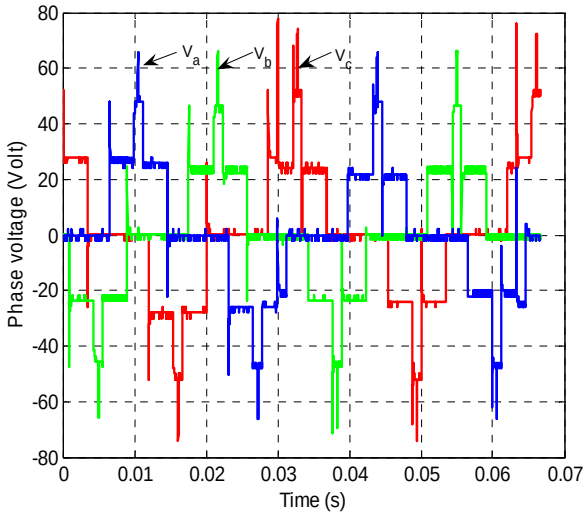

Fig. 5. Output voltage waveform for m=0.82, f=30 Hz.

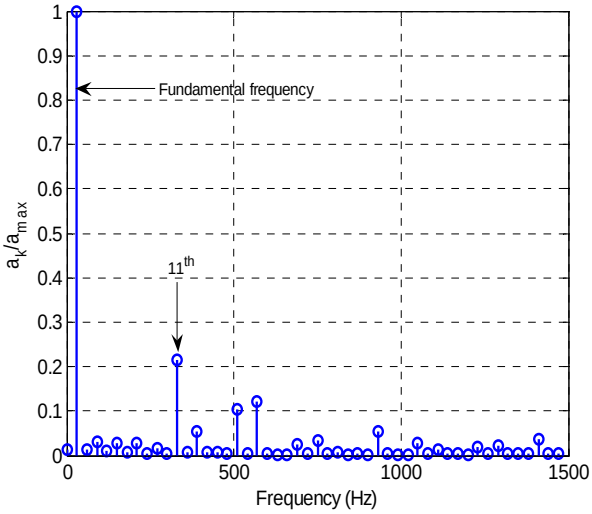

Fig. 6. Normalized FFT analysis of line-line voltage for m=0.82, f=30 Hz.

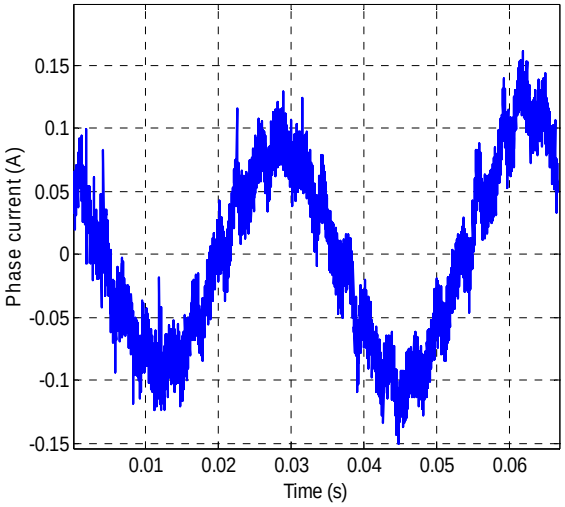

Fig. 7. Output current waveform for m=0.82, f=30 Hz.

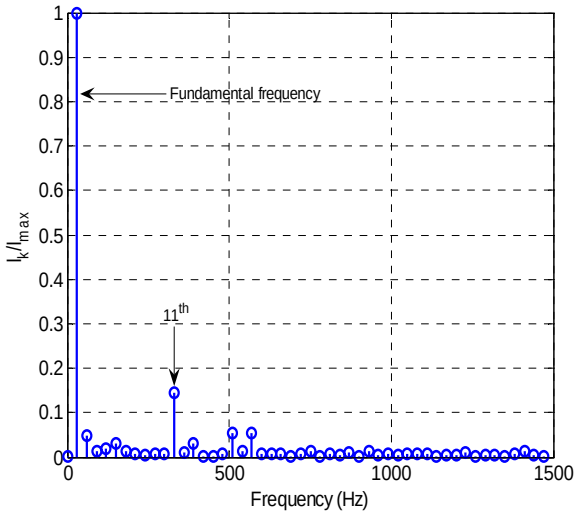

Fig. 8. Normalized FFT analysis of phase current for m=0.82, f=30 Hz.

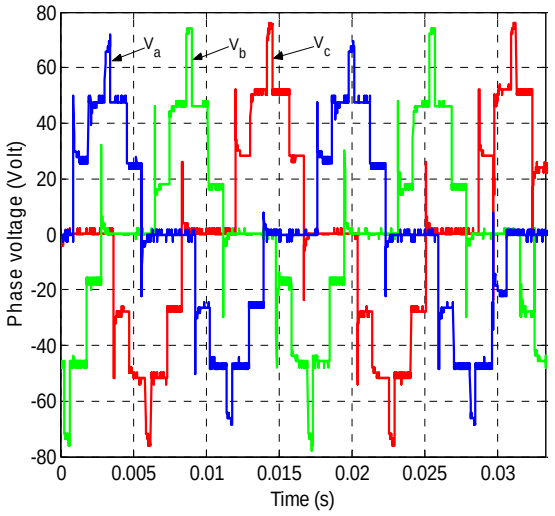

Fig. 9. Output phase voltage waveform for m = 1.32, f = 60 Hz.

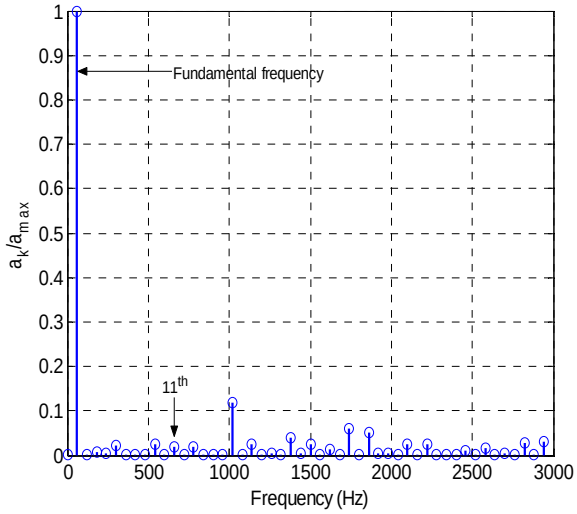

Fig. 10. Normalized FFT analysis of line-line voltage for m = 1.32, f = 60 Hz.

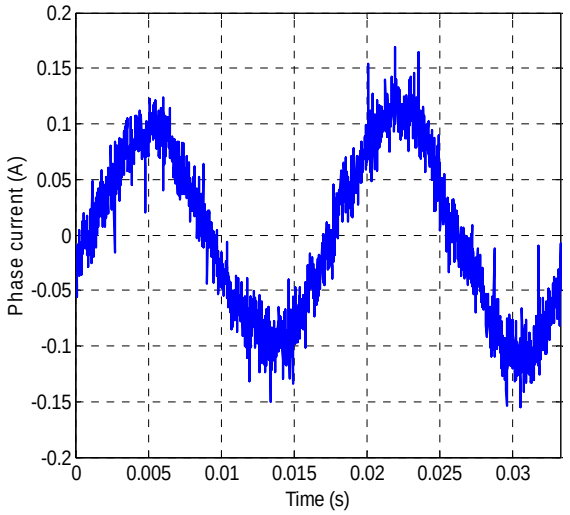

Fig. 11. Output current waveform for m = 1.32, f = 60 Hz.

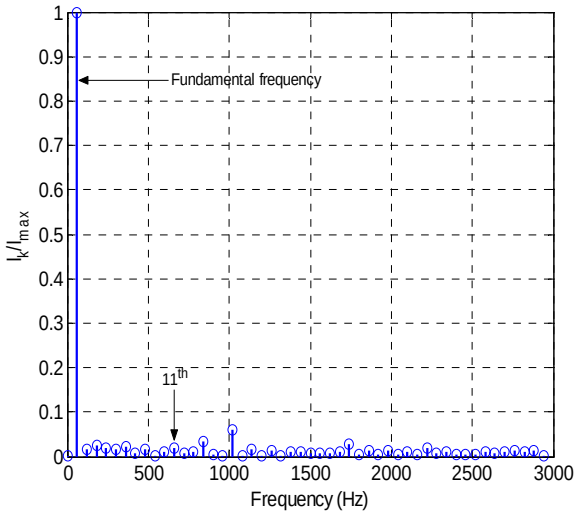

Fig. 12. Normalized FFT analysis of phase current for m = 1.32, f = 60 Hz.

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