

# Hybrid Cascaded Modular Multilevel Converter with DC Fault Ride-Through Capability for HVDC Transmission System

Rui Li, Grain Philip Adam, Derrick Holliday, John E. Fletcher and Barry W. Williams

**Abstract**--A new hybrid cascaded modular multilevel converter for high-voltage dc (HVDC) transmission system is presented. The half-bridge (HB) cells are used on the main power stage and the cascade full-bridge (FB) cells are connected to its ac terminals. The main power stage generates the fundamental voltages with quite low switching frequency, resulting relatively low losses. The cascaded FB cells only attenuate the harmonics generated by the main power stage, without contribution to the power transfer. Thus, the energy storage requirement of the cascaded FB cells is low and the capacitance of FB cells is reduced significantly. Due to the dc fault reverse blocking capability of the cascaded FB cells, the proposed topology can ride-through the pole-to-pole dc fault. In addition the soft restart is achieved after the fault eliminates, without exposing the system to significant inrush current. Besides, the average-value model of the proposed topology is derived, based on which the control strategy is presented. The results show the feasibility of the proposed converter.

**Index Terms**--dc fault blocking, dc fault tolerant, hybrid cascaded modular multilevel converter (HC-MMC), soft restart, voltage-source-converter high-voltage dc (VSC-HVDC) transmission system.

## I. INTRODUCTION

THE modular multilevel converter (MMC) is a voltage source converter (VSC) for high-voltage dc (HVDC) transmission systems. With a large number of cells per arm, it can generate a staircase voltage that approximates a sinusoidal waveform, with extremely low harmonic distortion; thus no ac filters are needed. Additionally, switching losses are significantly reduced, and low  $dv/dt$  enables the use of transformers with low insulation requirements [1, 2].

The dc fault vulnerability of the MMC is a major issue that constrains its application in HVDC transmission systems. In the event of a short circuit between the dc terminals of the VSC or along the dc cables, even with all IGBTs turned off,

the converter behaves as an uncontrolled diode rectifier connected to a low impedance dc load, thus high ac currents flow through the free-wheeling diodes from the ac grid to the dc side. The low impedance of the short circuit path leads to a steep rise in fault current and that may cause serious damage to the converters, hence the ac or dc circuit breakers are traditionally required to disconnect the VSC from the ac grid or dc fault point. But the response of conventional mechanical circuit breaker is too slow and the semiconductors still endure high current stress during the response time, hence it is unsuitable for dc fault isolation. Presented in [3-5], the bypass elements, typically thyristors, are used to protect the anti-parallel diodes of the half-bridge (HB) cells, due to the slow reaction of ac circuit breaker. But the ac circuit breaker and bypass element have to be rated at the full prospective short circuit currents. The solid-state dc circuit breaker can achieve fast interruption time but at high capital cost and significant on-state operational losses due to the semiconductors in the main current path [6]. The hybrid dc circuit breaker has been proposed where a mechanical path serves as main conduction path with minimal losses during normal operation, and a parallel connected solid-state breaker is used for dc fault isolation [7-9]. However, it has relatively large footprint and its capital cost is still high.

Besides the above dc fault isolation approach, different topologies based on traditional MMC are addressed in [10-12]. Another alternative replaces the HB cells with the full-bridge (FB) cells, thus the capacitors can be inserted into the circuit in either polarity. This feature allows the MMC with FB cells to block dc faults and offers greater controllability [11]. However, this approach requires twice the number of IGBTs in the conduction path, thus higher semiconductor power losses than the equivalent HB arrangement is expected. Based on active controlled power electronic components, the dc transformer is presented in [10, 12]. Although it has been claimed this approach can isolate dc faults rapidly and contribute to dc voltage and power flow control, these added functionalities are achieved at the expense of much higher capital cost and power losses, and a larger footprint compared to that suggested in [11, 13-16].

Recently, the concept of the 'Hybrid Converter' has been proposed which combines different topologies together in order to optimize converter performances. Based on current

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source converters and MMCs with FB cells, the alternate-arm multilevel converter is presented in [2, 17, 18]. This topology can block dc faults with reduced semiconductor losses compared to [13]; however, the direct switches composed of series connected IGBTs are still required. As a result, nearly identical switching characteristics of individual semiconductors with dynamic voltage sharing are required. Reference [13, 16, 19, 20] presents the hybrid multilevel converter which uses the two-level converter in series with cascaded FB cells. It offers ac fault ride-through capability and can block dc faults. However, the active switches of the two-level VSC still suffer high voltage stresses. The dc capacitors of the hybrid multilevel converter are also discharged by a short circuit between the positive and negative dc cables. When the dc side capacitors are charging to reestablish the rated dc link voltage, the inrush current from the ac grid is extremely high and poses a risk of system damage. Additionally, the main power stage of the proposed hybrid converter in [13, 16, 19, 20] can only generate two level output voltages, which contain more harmonics that need to be attenuated by the cascaded FB cells. Furthermore, the use of the two-level converter in the main power stage [13] necessitates the low power stage to track fast change rate of voltage, and this makes synchronization of the two power stages challenging.

Reference [21] proposed the use of hybrid converter that employs a three-level MMC in series with a single FB cell to improve the output voltage quality of the grid side converter for wind turbine generator. Because the FB cell is rated to block  $\frac{1}{4}V_{dc}$ , the proposed hybrid converter is unable to block dc fault and is unsuitable for HVDC transmission system. Also, the extremely large FB cell capacitor is required for the topology presented in [21].

In order to overcome the above problems, the hybrid cascaded VSC is proposed and its dc fault ride-through capability is undergoing extensive research. The detailed topology, operation principle, and dc fault ride-through capability are addressed in Section II. In Section III, the average-value model of the proposed hybrid MMC is presented and its control strategy is thoroughly discussed. The viability of the new hybrid MMC in high-voltage applications is assessed in Section IV, considering point-to-point HVDC links with reduced numbers of cells. In this assessment, the steady state and transient responses of the HVDC link based on the proposed hybrid MMC are examined, and major findings are highlighted. The conclusions drawn from both device and system aspects of the proposed hybrid MMC are summarized in Section V.

## II. HYBRID MMC WITH CASCADED FULL BRIDGE CELLS

### A. Topology of Hybrid MMC with Cascaded FB Cells

Fig. 1 shows a generic version of the proposed MMC-based hybrid converter with ac side cascaded FB chain links. Its main power stage consists of HB based MMC, with  $N_H$  cells

per phase. This stage controls the magnitude and phase of fundamental voltage at the point of common coupling to regulate both active and reactive exchange with the ac grid. The FB chain link in each limb represents the low power stage, which is used as a series active power filter to attenuate the harmonic voltages generated by the main power stage at ( $a_m$ ,  $b_m$  and  $c_m$ ). Due to the ac side cascaded FB chain links, this topology is called a Hybrid Cascaded MMC (HC-MMC).

### B. Operating Principles

For the proposed HC-MMC topology, each arm of the MMC in the main power stage must block full dc link voltage ( $V_{dc}$ ), while the FB chain link of each phase can be configured to block half of the dc link voltage ( $\frac{1}{2}V_{dc}$ ) for dc fault blocking capability. This means the number of FB cells required per phase for the low power stage can be a quarter of the HB cell number for the main power stage, provided the cell capacitors and switching devices of both stages have the same rated voltage. As a result the proposed HC-MMC is expected to have reduced on-state losses compared to hybrid converters presented in [11]. The use of the MMC in the main power stage, instead of a two-level converter or neutral-point clamped (NPC) converter as in [22-24], makes tracking of the voltage possible by sequential switching of the FB cells in and out the power path. For more detailed comparison with the recent state of art multilevel converters, please refer to references [16, 22, 25-27].

Fig. 2 illustrates the terminal voltage of main power stage ( $v_{am}$ ), voltage across FB chain link ( $v_F$ ), and desired output voltage ( $v_{ao}$ ) when a large number of cells are used in both stages. Notice that the proposed hybrid cascaded converter avoids the need for fast tracking of the sharp edges observed in [22] by slowing down the change rate of the output voltage for the main power stage at  $a_m$ ,  $b_m$  and  $c_m$ . In this manner, improved synchronization of the switching instants between high and low power stages is achieved and the output voltage transitions are free from voltage spikes and generally restricted to one voltage level per switching cycle.

For proper operation of the proposed HC-MMC, capacitor voltages of the HB cells and cascaded FB cells must be monitored and maintained around their nominal values. The capacitor voltage balancing of both stages is achieved by rotating the cell capacitors when synthesizing different voltage levels, taking into account arm and limb current polarities, and voltage magnitudes of the cell capacitors. Notice that the HB cell capacitors of the main power stage can only be charged when arm current is positive (unipolar current) or remained constant, and each cell generates two voltage levels. In the contrast, each FB cell of the low power stage can generate three voltage levels (positive, negative and zero voltages), and the cell capacitors can be charged, discharged or kept constant with both positive and negative limb currents. To further ensure the voltages of FB cells remained around  $V_{dc}/(2N_F)$ , a dc voltage loop that injects a small fundamental voltage into the reference signal of FB chain links ( $v_F^*$ ) is incorporated in each phase to compensate for the losses. The proposed HC-

MMC can be controlled using hybrid modulation, where low and main power stages are controlled using two different modulation strategies [13]; or multilevel modulation, where the proposed converter is controlled as one unit using level

shifted disposition carriers [19]. The later approach is adopted in this paper for simplicity of implementation. For more details on the modulation of the hybrid cascaded converters, please refer to references [13, 19, 28, 29].

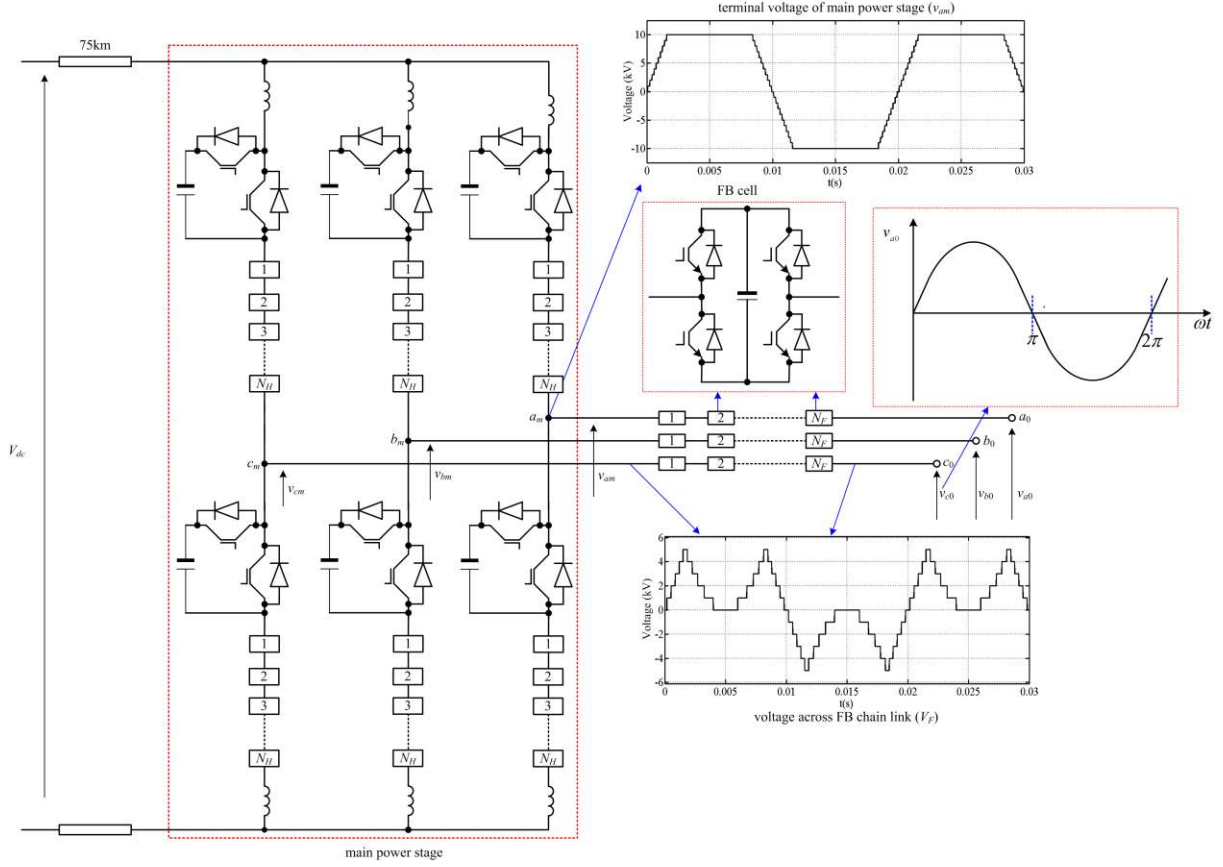


Fig. 1. Proposed HC-MMC topology for HVDC applications.

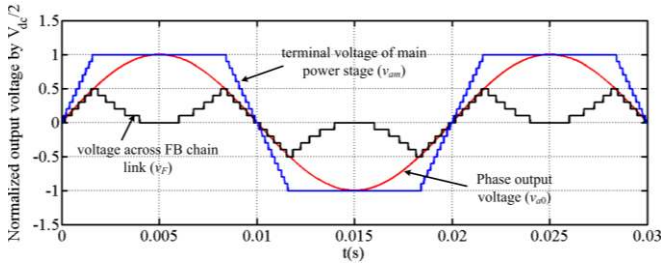


Fig. 2. Waveforms of the main power stage voltage ( $v_{am}$ ), voltage across FB chain link ( $v_f$ ), and desired converter output voltage ( $v_{a0}$ ).

### C. DC Fault Ride-Through

During dc faults, traditional HB based MMCs draw large currents from the ac side through their free-wheeling diodes once the dc voltage drops below the peak of the line ac voltage, and such large currents may damage converter switching devices of the HVDC transmission system [3].

The proposed HC-MMC has inherent dc fault blocking capability, which is necessary to eliminate ac grid contribution to the dc side fault current. Once a dc fault is sensed, all the switching devices of the main power stage and cascade FB cells are blocked, and this presents the capacitors of the cascaded FB cells as a virtual dc link of  $\frac{1}{2}V_{dc}$  per limb or  $V_{dc}$

phase-to-phase. When cascaded FB cells are blocked, their cell capacitors are charged by positive and negative phase currents and this eliminates any possibility of inrush current. During the dc fault period, the freewheeling diodes of the HB cells of the main power stage will experience a decaying current associated with the discharge of the dc cable distributed stray capacitors, and this current will fall to zero when all energy stored in the dc cable capacitors is completely dissipated. In this way, the risk of device failure due to increased current stresses during a dc fault is greatly reduced. Moreover, the capacitor voltages of the main power stage and cascaded FB cells are all retained to be used during soft systems restart when the fault is cleared.

### III. CONTROL OF HC-MMC

This section uses the time average model of the proposed HC-MMC to derive its control systems [30, 31]. Each arm of the main power stage is represented by a controlled voltage source ( $v_{a1}$  and  $v_{a2}$ ;  $v_{b1}$  and  $v_{b2}$ ; and  $v_{c1}$  and  $v_{c2}$ ) in series with arm reactor. Each limb of the cascaded FB cells that operates as an active power filter is also modelled by a controllable voltage source ( $v_{as}$ ,  $v_{bs}$  and  $v_{cs}$ ), see Fig. 3.

According to equivalent circuit in Fig. 3, the differential

equations that describe the dynamics of the HC-MMC arm and output ac currents are:

$$L_s \frac{di_{abc1}}{dt} + R_s i_{abc1} + R_T i_{abc} + L_T \frac{di_{abc}}{dt} = \frac{1}{2} V_{dc} - v_{abc1} - v_{abc0} - v_{abc2} \quad (1)$$

$$L_s \frac{di_{abc2}}{dt} + R_s i_{abc2} - R_T i_{abc} - L_T \frac{di_{abc}}{dt} = \frac{1}{2} V_{dc} - v_{abc2} + v_{abc0} + v_{abc1} \quad (2)$$

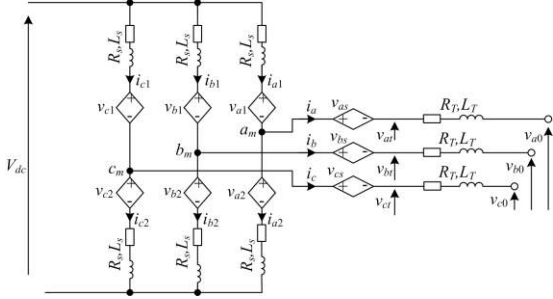


Fig. 3. Equivalent circuit in  $abc$  reference frame.

Recall that  $i_{abc} = i_{abc1} - i_{abc2}$ , and after subtracting equation of the lower arm from that of the upper arm in Fig. 3, the following equation is obtained:

$$\left( L_T + \frac{1}{2} L_s \right) \frac{di_{abc}}{dt} + \left( R_T + \frac{1}{2} R_s \right) i_{abc} = \frac{1}{2} (v_{abc2} - v_{abc1}) - v_{abc0} \quad (3)$$

Equation (3) shows that the fundamental current can be controlled by manipulating the fundamental components of the upper and lower arm voltages for main power stages, and the voltage across the cascaded FB cells. The dynamics of the circulating current at the main power stage of the proposed HC-MMC is described by:

$$L_s \frac{di_{dc}^{abc}}{dt} + R_s i_{dc}^{abc} = \frac{1}{2} V_{dc} - \frac{1}{2} (v_{abc1} + v_{abc2}). \quad (4)$$

where the dc current component of each MMC arm is  $i_{dc}^{abc} = \frac{1}{2} (i_{abc1} + i_{abc2})$ . Equation (4) indicates that the circulating current  $i_{dc}^{abc}$  can be regulated by controlling the average voltage developed across the upper and lower arms.

To facilitate control design, let  $v_{abc} = v_{abc0} + v_{abc1}$  and replace the right hand side of (3) by  $v_{abc}$  (where  $v_{abc} = \frac{1}{2} (v_{abc2} - v_{abc1}) - v_{abc0}$ ), and the resulting equation is transformed to  $d$ - $q$  synchronous reference frame using Park's transformation, assuming the voltage vector at the point of common coupling is aligned with  $d$ -axis:

$$v_d = \left( \frac{1}{2} R_s + R_T \right) i_d + \left( \frac{1}{2} L_s + L_T \right) \frac{di_d}{dt} - \omega \left( \frac{1}{2} L_s + L_T \right) i_q \quad (5)$$

$$v_q = \left( \frac{1}{2} R_s + R_T \right) i_q + \left( \frac{1}{2} L_s + L_T \right) \frac{di_q}{dt} + \omega \left( \frac{1}{2} L_s + L_T \right) i_d \quad (6)$$

The inner current controller is designed based on (5) and (6), by obtaining  $\lambda_d = v_d + \omega (L_T + \frac{1}{2} L_s) i_q$  and  $\lambda_q = v_q - \omega (L_T + \frac{1}{2} L_s) i_d$  from a simple proportional-integral (PI) controller as:

$$\lambda_d = \alpha_p (i_d^* - i_d) + \alpha_i \int (i_d^* - i_d) dt \quad \text{and} \quad \lambda_q = \alpha_p (i_q^* - i_q) + \alpha_i \int (i_q^* - i_q) dt.$$

Afterward,  $v_d$  and  $v_q$  are obtained as:  $v_d = \lambda_d - \omega (L_T + \frac{1}{2} L_s) i_q$  and  $v_q = \lambda_q + \omega (L_T + \frac{1}{2} L_s) i_d$ . After transforming  $v_d$  and  $v_q$  back to  $abc$  reference frame, the modulating signals are obtained as:

$$v_{abc}^* = \frac{1}{2} (v_{abc2} - v_{abc1}) - v_{abc0}.$$

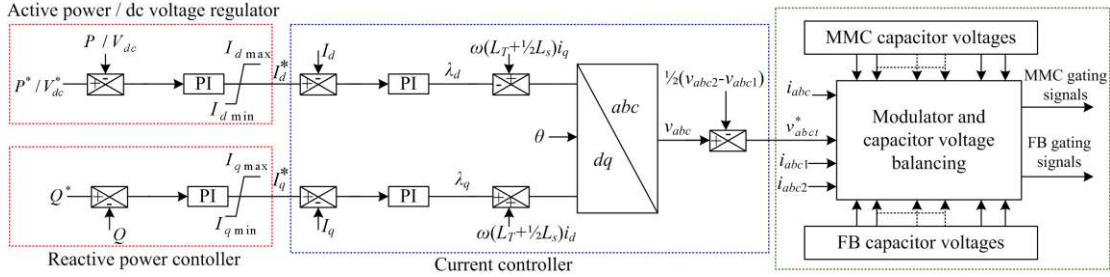


Fig. 4. Generic block diagram for the control systems of the HC-MMC.

On the above basis, the structure of the inner current controller for the HC-MMC in Fig. 4 can be obtained. Notice that the outer loop used in this paper to provide the set-point for the inner current controller of HC-MMC is similar to that of the two-level VSC when operated in dc voltage or active power regulation modes. Minor modifications are introduced to the inner loop to permit incorporation of complex modulator and cell capacitor voltage balancing strategy at main and low power stages. The control system in Fig. 4 contains three loops: the outer loops regulate dc voltage (or active power) and reactive power, and set reference currents ( $i_{dref}$  and  $i_{qref}$ ) for the intermediate loop; the intermediate loop is the current controller which is used to decouple the control of active and reactive powers through  $i_d$  and  $i_q$ , and restrains converter current contribution to the grid during ac network disturbance; and the inner loop is the modulator and cell capacitor voltage balancing strategy of both stages that generates the gating

signals following the modulating signals provided by the intermediate loop. The inner control loop utilizes the phase-disposition (PD) carriers to generate the gating signals. The initial gains for the medium and outer loops in Fig. 4 are selected based on similar approach presented in [13], and then tuned using time domain simulations.

## IV. PERFORMANCE EVALUATION

### A. Simulation Results

Fig. 5 depicts the test system that will be used to assess the capabilities of the presented HC-MMC under normal and dc fault conditions. HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> represent two stations of the long distance HVDC transmission link connected through 75km dc cables, with parameters listed in Table I. For simplicity of illustration, main and low power stages of HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> are modelled with six HB

cells per MMC arm and twelve FB cells in the ac side. In Fig. 5, HC-MMC<sub>1</sub> is configured to regulate the dc link voltage level at 480kV (pole-to-pole) and reactive power exchange with grid G<sub>1</sub>, while HC-MMC<sub>2</sub> controls active and reactive power exchanged with grid G<sub>2</sub>. Unlike the two-level hybrid cascaded converter based HVDC link discussed in [13], a dc link capacitor is not needed for the HC-MMC, and dc cable stray capacitance is sufficient to provide the dc link midpoint to enable operation as  $\pm 240$ kV symmetrical mono-polar.

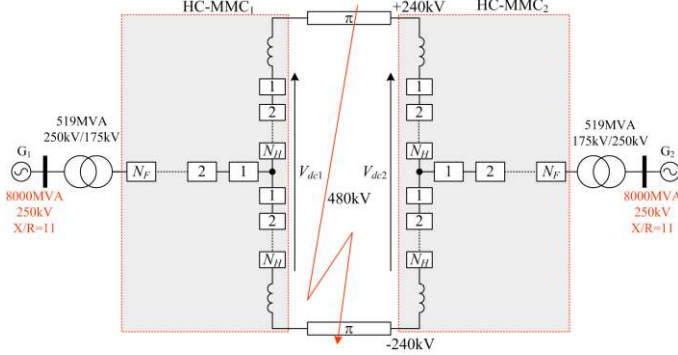


Fig. 5. HVDC transmission system based on novel HC-MMCs.

TABLE I  
Test System Nominal Parameters.

| PARAMETER  | Nominal value     |
|--|-------------------|
| dc link voltage  | 480kV             |
| capacitor voltage of HB cell                                     | 80kV              |
| capacitor voltage of FB cell                                     | 20kV              |
| HB cell number per arm   | 6                 |
| cascaded FB cell number  | 12                |
| capacitance of HB cell   | 380 $\mu$ F       |
| capacitance of FB cell   | 270 $\mu$ F       |
| arm inductance   | 36mH              |
| phase-to-phase peak voltage of G <sub>1</sub> and G <sub>2</sub> | 245kV             |
| carrier frequency  | 1.35kHz           |
| dc transmission line length                                      | 75km              |
| $\pi$ section number of dc transmission line                     | 20                |
| dc transmission line resistance                                  | 9.7m $\Omega$ /km |
| dc transmission line inductance                                  | 0.8mH/km          |
| dc transmission line capacitance                                 | 0.25 $\mu$ F/km   |

### 1) Four-quadrant operation

To demonstrate four quadrant operation of the proposed HC-MMC based HVDC link in Fig. 5, HC-MMC<sub>2</sub> is initially commanded to import 320MW from G<sub>1</sub> to G<sub>2</sub> and the power flow direction is reversed at time  $t=2.75$ s to export 320MW from G<sub>2</sub> to G<sub>1</sub>. The change rate of active power is restrained to -1.6MW/ms. The reactive power of HC-MMC<sub>1</sub> is reversed from 150MVar to -150MVar at  $t=2.75$ s, while that of HC-MMC<sub>2</sub> is kept at zero during the entire simulation period.

Fig. 6 presents simulation results for the four-quadrant operation of the test system. Observe that the power reversal is achieved with minimum transient effects in the active and reactive powers and ac currents of the HC-MMC<sub>1</sub>, see Fig. 6 (a) and (c), and no overshoot in the active and reactive powers and ac currents of the HC-MMC<sub>2</sub>. Notice that during active

power reversal, as commanded by HC-MMC<sub>2</sub>, the dc current reverses accordingly as expected from all VSC-HVDC links, with limited overshoot due to dynamics associated with arm and dc cable inductances. Furthermore, it can be seen that during active power reversal as commanded by HC-MMC<sub>2</sub>, a limited drop in the dc link and cell capacitor voltages of both converter stations are observed, see Fig. 6 (f), (g) and (h). Following the power reversal, the HVDC transmission system being studied returns quickly to steady state.

One of the significant characteristics of the presented HC-MMC is the low capacitance requirements of the ac side cascaded FB cells. Fig. 6 (i) and (j) show the capacitor voltages of the cascaded FB cells remain balanced around 20kV, with less than 3% peak-to-peak voltage ripple. This low ripple is achieved with cell capacitance of 270 $\mu$ F, which is smaller than that of main power stage. Such a low voltage ripple indicates that the capacitance of the cascaded FB cell can be further reduced to give  $\pm 10\%$  ripple, which is a widely accepted figure for MMCs. The results presented in Fig. 6 have shown that the proposed HC-MMC is able to operate satisfactorily in the illustrative HVDC link over the entire operating range, with voltage and current stresses in the active and passive devices fully controlled.

### 2) DC fault ride-through

This section assesses the performance of the proposed HC-MMC during pole-to-pole dc short circuit fault, considering the test system in Fig. 5. The simulated scenario assumes the test system is subjected to a solid pole-to-pole dc fault at the middle of dc cable at  $t=2$ s, and cleared after 280ms. Both HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> are blocked during dc fault period. In the pre-fault condition, HC-MMC<sub>2</sub> exports -210MW active power from G<sub>2</sub> to G<sub>1</sub>, and also exchanges 85MVar with its the ac side at G<sub>2</sub>, while HC-MMC<sub>1</sub> is set to maintain the dc voltage constant at 480kV, with unity input power factor. The actions of HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> after dc fault depend on their pre-fault control modes. After dc fault is cleared, the gating signals to the main power stage of the HC-MMC<sub>1</sub> that operates in dc voltage control mode will be restored to build up the dc voltage to its rated and charge the dc cable, utilizing the soft restart control in order to minimize any potential oscillations in the dc link current and voltage. Once the dc voltage of the HC-MMC<sub>1</sub> has recovered to rated value, its cascaded FB cells are de-blocked to allow HC-MMC<sub>1</sub> to operate in dc voltage control and provide reactive power support to the ac grid G<sub>1</sub>. Subsequently, the gating signals to both stages of HC-MMC<sub>2</sub> can be restored, thus allowing its active and reactive powers to be ramped gradually from zero to their pre-fault values.

Simulation results obtained from this test are displayed in Fig. 7. When the dc fault occurs at  $t=2$ s, the dc link voltage drops to zero, and three-phase ac currents of both stations HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> drop to zero as their gating signals are inhibited, Fig. 7 (c) and (d). Immediate blocking of both converter stations activates their inherent dc fault reverse blocking capability, resulting in zero reactive and active power exchange between HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> and their

corresponding ac grids, Fig. 7 (a) and (b). When the dc fault is cleared at  $t=2.28s$ , the main power stage of HC-MMC<sub>1</sub> is de-blocked as previously stated to re-energize the dc cables gradually, benefiting from the large stored energy in its cell capacitors. During the dc link voltage restoration, only the high-voltage part of HC-MMC<sub>1</sub> must be operated, while both stages of HC-MMC<sub>2</sub> remain blocked. When the low power

stage of the HC-MMC<sub>1</sub> is de-blocked at 2.4s, relatively small inrush currents are observed at the HC-MMC<sub>1</sub> ac side as the dc voltage regulator restores the dc link voltage to the rated value, Fig. 7 (c). When HC-MMC<sub>2</sub> is de-blocked at  $t=2.9s$  and power transfer is restarted, relatively small inrush currents are observed in the ac side for short periods of time, see Fig. 7 (d).

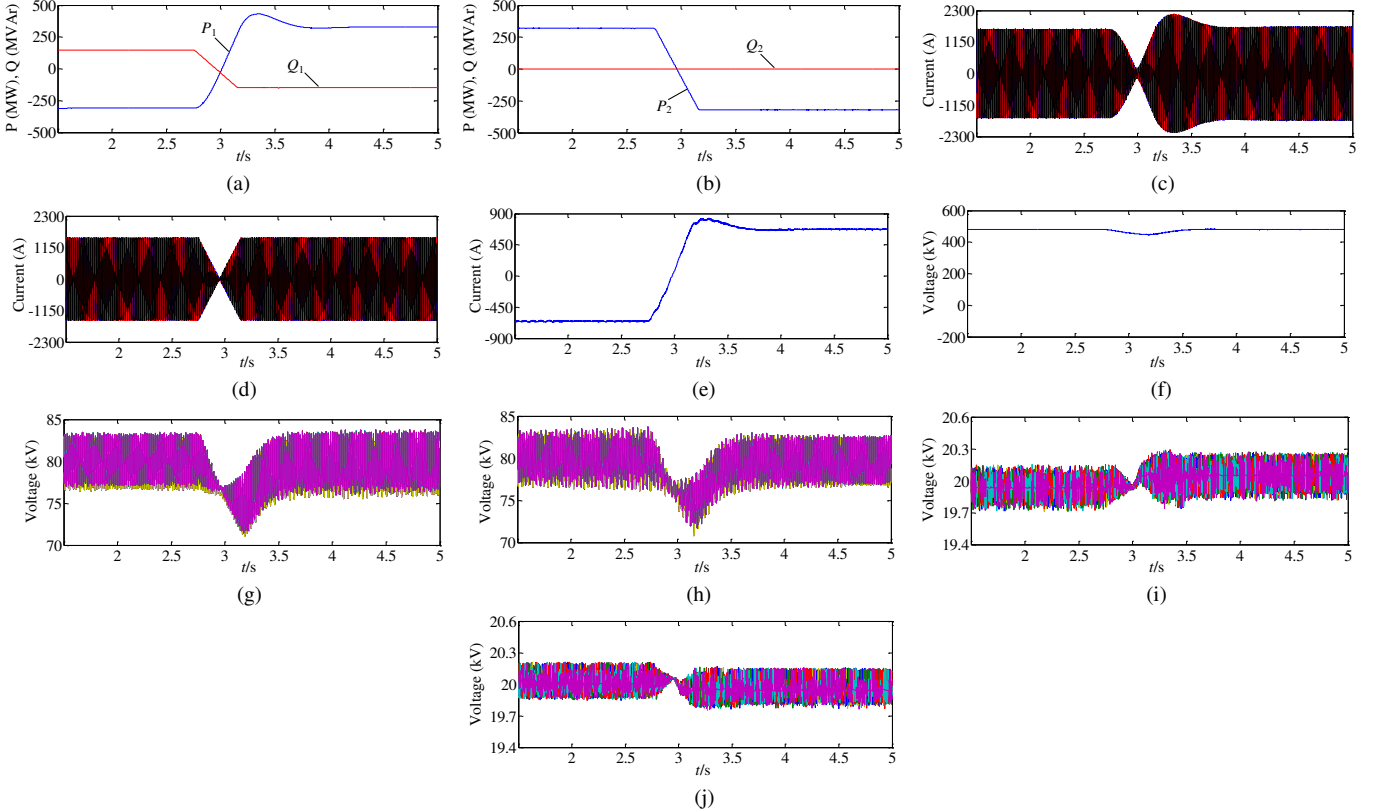


Fig. 6. Four-quadrant operation waveforms. (a) Active and reactive powers of HC-MMC<sub>1</sub>. (b) Active and reactive powers of HC-MMC<sub>2</sub>. (c) Three-phase currents of HC-MMC<sub>1</sub>. (d) Three-phase currents of HC-MMC<sub>2</sub>. (e) DC current. (f) DC voltage. (g) HB cell capacitor voltages of HC-MMC<sub>1</sub>. (h) HB cell capacitor voltages of HC-MMC<sub>2</sub>. (i) Capacitor voltages of cascaded FB cells for HC-MMC<sub>1</sub>. (j) Capacitor voltages of cascaded FB cells for HC-MMC<sub>2</sub>.

Observe that after de-blocking both stages of HC-MMC<sub>2</sub>, Fig. 7 (b) shows its active and reactive powers are ramped gradually from zero states to -210MW and -85MVA<sub>r</sub> respectively, over 100ms, with almost no transient oscillations. Besides, the HB cell capacitor voltages of the HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub> remain balanced fluctuating around 80kV, with 8% peak-to-peak voltage ripple, see Fig. 7 (g) and (h). The HB cell capacitor voltages of main power stage exhibit larger variations than that of the FB cells. This is because they have been used during gradual buildup of the dc link voltage and charging of the dc cable stray capacitors, while the FB cells remain blocked.

Reference [13] shows the hybrid cascaded two-level VSC exhibits large inrush currents that may damage converter switches when converter is de-blocked, and this large current is associated with the uncontrolled charging of the two-level converter dc link and dc cables capacitors. For the presented HC-MMC, only the dc cable distributed capacitance is discharged through anti-parallel diodes of the MMC parts, due to the distributed cell capacitors of main power stage instead of concentrated dc link capacitor as in two-level and neutral-

point clamped converter. As a result, the peak fault current for the case being considered in this paper is 4.3kA, which is only 7.2% of that of hybrid cascaded two-level converter.

Fig. 7 (k) to (n) presents arm currents of the main power stage of HC-MMC<sub>1</sub> and HC-MMC<sub>2</sub>. These arm currents briefly exhibit over-currents as the dc cable capacitance discharges during the initial period of the dc fault and then subsides to zero as previously explained. It should be noted that the arm currents of HC-MMC<sub>1</sub> experience limited over current when soft restart is initiated at  $t=2.4s$ , see Fig. 7 (k) and (m).

Although the test system is subjected to the most severe type of dc fault, the system is fully recovers and continues to contribute to the power transfer between G<sub>1</sub> and G<sub>2</sub>. The results presented in Fig. 7 have shown that the dc fault blocking and soft restart capabilities of the proposed HC-MMC can allow the HVDC transmission system to ride-through a dc fault, avoiding using the solid-state dc circuit breakers. This distinct feature may facilitate practical implementation of HVDC transmission system and multi-terminal dc grids. The following part summarises the soft

restart strategy of the HC-MMC discussed earlier, including its main objectives:

In the hybrid cascaded converter discussed in [13] and all other multilevel converters with dc fault reverse blocking capability [25], converter switching devices tend to experience extremely high current stresses when a temporary dc fault is suddenly cleared, while ac circuit breakers remain closed. This

is because the dc cables tend to be charged instantly in uncontrolled fashion. This may expose converter switches to extremely high currents (especially, in case of very long HVDC link), and the magnitudes of these currents are only limited by transformer leakage inductances and arm inductances in main power stage.

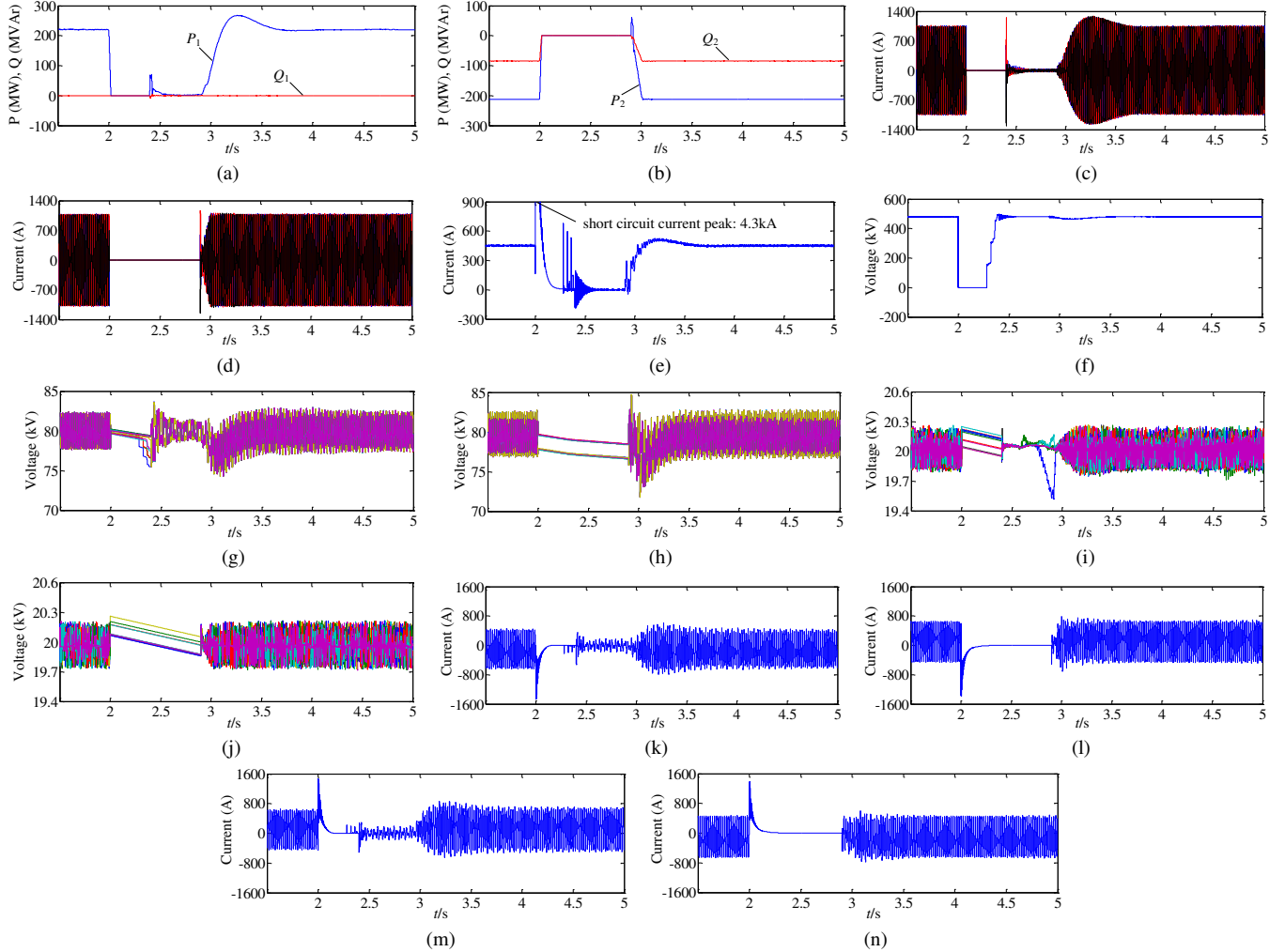


Fig. 7. DC fault ride-through waveforms. (a) Active and reactive powers of HC-MMC<sub>1</sub>. (b) Active and reactive powers of HC-MMC<sub>2</sub>. (c) Three-phase currents of HC-MMC<sub>1</sub>. (d) Three-phase currents of HC-MMC<sub>2</sub>. (e) DC current. (f) DC voltage. (g) HB cell capacitor voltages of HC-MMC<sub>1</sub>. (h) HB cell capacitor voltages of HC-MMC<sub>2</sub>. (i) Capacitor voltages of cascaded FB cells for HC-MMC<sub>1</sub>. (j) Capacitor voltages of cascaded FB cells for HC-MMC<sub>2</sub>. (k) Upper arm currents of HC-MMC<sub>1</sub>. (l) Upper arm currents of HC-MMC<sub>2</sub>. (m) Lower arm currents of HC-MMC<sub>1</sub>. (n) Lower arm currents of HC-MMC<sub>2</sub>.

TABLE II  
Comparison between FB-MMC and HC-MMC, where  $N$  is the cell number per arm.

| ITEM   | FB-MMC     | HC-MMC     | Remarks  |
|--|------------|------------|--|
| Number of IGBTs per phase                    | $8N$       | $6N$       | HC-MMC has lower cost of semiconductors  |
| Number of IGBTs in conduction path per phase | $4N$       | $3N$       | HC-MMC has lower on-state losses   |
| Number of cell capacitors per phase          | $2N$       | $2.5N$     | HC-MMC uses more capacitors, thus it expected to have larger footprint than FB-MMC |
| Semiconductor losses                         | High       | Moderate   |  |
| AC filters                                   | Not needed | Not needed |  |
| AC and DC fault ride-through capability      | Yes        | Yes        |  |
| Soft restart                                 | No         | Yes        |  |

This paper proposes a soft restart that exploits the cascaded FB cells of both converter stations as fast acting ac and dc

circuit breakers to stop the uncontrolled inrush currents from ac side toward dc side when dc link voltage collapses during

dc fault (elimination of ac grid contribution to dc fault current). Also, the cascaded FB cells of both stations mimicked operation of ac circuit breakers by preventing instantaneous charging of the dc cables when a temporary dc fault is suddenly cleared; thus, the uncontrolled inrush currents from the ac side toward dc side through converter switches are avoided. The proposed soft restart uses the energy stored in HB cell capacitors of the main power stage and voltage of these cells to build up the dc link voltage gradually from zero to nearly rated in discrete fashion. This is achieved by sequential de-blocking of the HB cells of the converter that controls dc link voltage, while the cascaded FB cells of both stations remain in blocking state (acting as opened ac circuit breakers). In this period, the dc cable stray capacitors are charged gradually as the dc link voltage is building up.

After the dc link voltage of the station that regulates dc voltage is restored to near its rated voltage, its cascaded FB cells are de-blocked to lift up the dc link voltage of this station to its rated. When this stage is achieved, both main and low power stages of the converter that controls active power are de-blocked simultaneously to allow equalization of dc link voltages of both stations as dc power is maintained zero. Afterward, power transmission can be restarted.

The results presented in this paper have shown that the proposed restart strategy has minimized transient oscillations normally associated with the system re-energization following sudden clearance of the dc short circuit fault, without exposing converters to high currents that may damage their switching devices.

### B. Comparison between HC-MMC and FB-MMC

For ease of comparison between the proposed HC-MMC and FB-MMC, the FB and HB cells in both converters and both stages of HC-MMC are rated to be  $V_{dc}/N$ ; where ' $V_{dc}$ ' is the dc link voltage and ' $N$ ' is number of cells per MMC arm. This means both the HC-MMC and FB-MMC are operated from the same dc link voltage and connected to the same ac side voltage. The detailed comparison between FB-MMC and HC-MMC is summarized in Table II. This table confirms that HC-MMC has lower switches in conduction path than FB-MMC; therefore, it is expected to have lower conduction loss.

The following part presents a high level switching loss comparison between HC-MMC and FB-MMC. Sequential switching of the IGBT as in Fig. 1 does not mean high switching losses (or high switching frequency). For example, in typical full-scale HVDC systems with 480kV dc link, where the voltage across each cell capacitor and its IGBTs during normal operation is assumed to be 2kV, the number of cells per arm is  $480\text{kV}/2\text{kV}=240$  cells. This means the numbers of cell capacitors and IGBTs from upper arm plus that from lower arm of the main power stage are 480 and 960 respectively (with 480 IGBTs in conduction path at each instant). By controlling the measurement rate of the cell capacitor voltages and other means, the number of times each IGBT can switch on and off during transition from  $-1/2V_{dc}$  to  $+1/2V_{dc}$  and vice versa can be restrained to 3 or 4 times per

fundamental period (thus, their average switching frequency will be in range from 150Hz to 200Hz as in typical half-bridge MMC) [32]. Assuming that the low power stage of the HC-MMC uses the same IGBTs as the main power stage, and provided the low power stage must be able to block  $1/2V_{dc}$  for dc fault blocking, the numbers of cell capacitors and IGBTs for the low power stage are 120 and 480 respectively (with 240 IGBTs in conduction path at each instant). With the number of IGBTs in conduction path in both power stages is 720, and assuming the average switching frequency ( $f_{sav}$ ) is the same for both stages as it will be in practical systems, the total switching loss per phase can be approximated as  $f_{sav} \times (E_{on} + E_{off}) \times 720$ , where,  $E_{on}$  and  $E_{off}$  are turn-on and turn-off energies per device. For simplicity, average  $E_{on}$  and  $E_{off}$  are assumed to be the same for all devices over several fundamental periods.

For FB-MMC with the same dc link and ac side voltage as HC-MMC, the number of IGBTs per phase is 1920, with 960 IGBTs in conduction path in each phase. This means, the switching loss can be approximated as:  $f_{sav} \times (E_{on} + E_{off}) \times 960$ . Notice that dc current component only exist in the main power stage of the HC-MMC. This simplified analysis has shown that the HC-MMC is expected to have relatively lower switching loss than FB-MMC. Using the aforementioned assumptions, HC-MMC and FB-MMC require 1440 and 1920 IGBTs per phase respectively. This shows HC-MMC requires less investment in semiconductor devices than FB-MMC. But the drawback of HC-MMC is that it requires more cell capacitors than FB-MMC, see Table II. For more detailed comparison with the recent state of art multilevel converters, please refer to references [16, 22, 25-27].

## V. CONCLUSION

A new HC-MMC for HVDC transmission systems is proposed where the cascaded FB cells offer dc fault reverse blocking capability. The FBs also act as an ac circuit breaker to virtually eliminate inrush currents from the ac side when the converter is de-blocked during system restart following fault clearance. Controlled recharging of the dc cable capacitance is provided by the HB cells of main power stage while the cascaded FB cells remain blocked. The main power stage of the proposed converter operates at relatively low switching frequency, hence the switching losses are reduced. The cascaded FB cells are only used to compensate the harmonics generated by the main power stage, drastically reducing the FB cell capacitance and dimension. The presented results show that capacitor voltage balancing of both main power stage and cascaded FB cells can be maintained independent of system operating conditions, including dc faults. The synchronization of the main power stage and cascaded FB cells is achieved by slowing down the rate of change of their respective output voltages and by restricting the switching transition to one voltage level per modulation period. When considering the number of devices in the conduction path and the current stresses per device, the proposed converter is expected to be competitive with the hybrid converters in [2, 14, 15, 18].



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