Hybrid Dual Full-Bridge DC-DC Converter with Reduced Circulating Current, Output Filter and Conduction Loss of Rectifier Stage for RF Power Generator Application

Young-Do Kim

Samsung Electro-Mechanics

Su-won, Korea

Il-Oun Lee, In-Ho Cho and Gun-Woo Moon

KAIST

Dae-jeon, Korea

***Abstract*— In this paper, a hybrid dual full-bridge DC-DC converter for radio-frequency (RF) power generator application is proposed to overcome the drawbacks of conventional phase-shift full-bridge (PSFB) converter such as large circulating current of primary side and large output filter size. The proposed converter adopts dual full-bridge hybrid structure with a small series capacitor in the primary side and full-bridge rectifier with two additional low-voltage-rated diodes in the secondary side. With this structure, the proposed converter has advantages of reduction of circulating current, zero-voltage switching (ZVS) operation of all primary switches, size reduction of output inductor, and low conduction loss of rectifier stage. Furthermore, the proposed converter can regulate the output voltage very wide by changing the operational mode according to the output voltage. These advantages result in the improvement of whole load efficiency. The operational principle and analysis of proposed converter are presented and analyzed. A 3kW 40-200V output laboratory prototype is designed and built to verify the feasibility and the effectiveness of the proposed converter.**

***Index Terms*— Hybrid dual full-bridge, Output filter, Circulating current, Zero-voltage switching (ZVS), Wide output voltage applications**

I. INTRODUCTION

Conventional phase-shift full-bridge (PSFB) converter is attractive topology for the high-power and wide-output-voltage applications, since it has some desirable features such as low current/voltage stress, ZVS operation of all primary switches and variable output regulation capability by the phase-shifted control signal [1]

However, the conventional PSFB converter has several problems for wide-output-voltage applications such as RF power generator. Since the operating duty cycle of the conventional PSFB converter extremely varies with the output voltage variation, large circulating current exists on primary side during freewheeling period [3 - 6]. Beside of that, the size of output filter is highly increased due to the small duty operation and it results in low power density and high cost [7-10]. Furthermore, for the high-power and high-output-voltage applications, transformer of the conventional PSFB converter has high turns-ratio so that the primary conduction loss of the conventional PSFB converter is highly increased and the high-voltage-rated diode, which generally has high conduction loss and poor performance such as reverse-recovery property, has to be employed for the secondary side [10].

To solve these problems, a hybrid dual full-bridge converter with reduced circulating current, small output filter, and low conduction loss of rectifier stage for RF power generator applications is proposed in this paper.

II. DESCRIPTION OF PROPOSED CIRCUIT

Fig. 1 shows the circuit diagram of proposed converter. As shown in Fig. 1, the proposed converter is composed of two PSFB converters $PSFB_1$ and $PSFB_2$ which are placed in parallel on primary side. One of PSFB converters $PSFB_1$ consists of switches Q_1, Q_2, Q_3 and Q_4 and a transformer T_1. The other converter $PSFB_2$ consists of switches Q_2, Q_4, Q_5 and Q_6, a small capacitor C_{boost}, and a transformer T_2. Both PSFB converters share switches Q_2 and Q_4. In order to eliminate the circulating current of T_2, C_{boost} is connected in series with T_2 as shown in Fig. 1. Due to the voltage across this capacitor, which is called boost capacitor, the circulating current of T_2 is reset during the freewheeling period. In the secondary side, both main transformers T_1 and T_2 are connected in series and full-bridge rectifier consisting of D_{s1}, D_{s2}, D_{s3} and D_{s4} is employed. Mid-point of both transformers is connected with an additional diode leg having low-voltage-rated diodes D_{a1} and D_{a2}. Since the voltage stress of D_{a1} and D_{a2} is much lower than that of outer diode D_{s1}, D_{s2}, D_{s3} and D_{s4}, diodes that have low forward voltage can be employed for D_{a1} and D_{a2}.

The proposed converter has two operational modes: dual full-bridge mode and single full-bridge mode.

1) *Dual full-bridge mode*: at dual full-bridge operational mode, first full-bridge section has full duty operation which means that diagonal pair of switches Q_1 and Q_2, Q_3 and Q_4 conduct together, and output power is controlled by varying the phase shift among Q_2,Q_4 and Q_5,Q_6 as shown in Fig. 2. Since the circulating current of switches Q_2, Q_4, Q_5 and Q_6 is eliminated by the voltage of C_{boost}, conduction loss of primary side is greatly reduced during the dual full-bridge operation. In spite of reduced circulating current of T_2, since ZVS operation of lagging-leg switches Q_1, Q_2, Q_3 and Q_4 is assisted by the primary current $i_{pri1}(t)$ of T_1, ZVS operation of all six switches can be easily achieved. Furthermore, load current is distributed between additional diode leg and full-bridge diode leg according to the duty ratio. Since the diode that has low forward voltage is employed for the additional diode leg, the secondary conduction loss is greatly

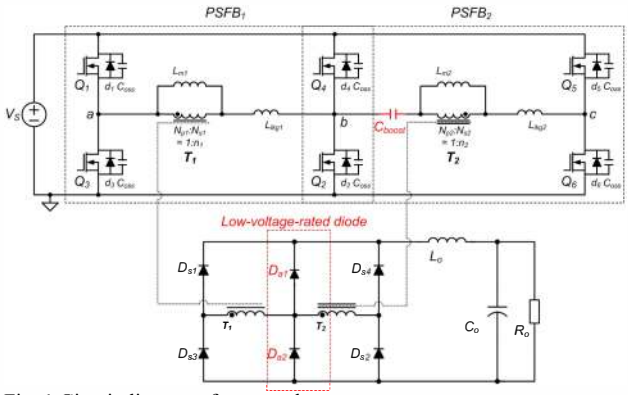

Fig. 1 Circuit diagram of proposed converter

reduced.

2) *Single full-bridge mode*: at single full-bridge operational mode, phase-shifted gate signal is applied to switches Q_1, Q_2, Q_3 and Q_4. , and switches Q_5 and Q_6 are disenabled as shown in Fig 3. Hence, power is mainly delivered to the output stage through Q_1, Q_2, Q_3, Q_4, T_1, D_{s1}, D_{s3}, D_{a1} and D_{a2}. Since T_1 of the proposed converter has lower turns-ratio than that of the conventional PSFB converter, full-bridge stage can be operated with large duty ratio and it results in reduction of conduction loss in primary side. Furthermore, since main power is delivered through D_{a1} and D_{a2}, which have low forward voltage, secondary conduction loss is also reduced during the single full-bridge operation.

Since the proposed converter has to provide variable output voltage according to the output power variation in RF power generator applications, boundary of mode change between single full-bridge operation and dual full-bridge operation can be decided by the design of turns-ratio of both transformers T_1 and T_2.

III. Operational Principle

For the analysis of proposed converter, several assumptions are made as follows:

1) All switches are ideal except for the output capacitor C_{oss} and the internal anti-parallel diode of it.
2) All rectifier diodes are ideal.
3) The output inductor L_o is large enough to be considered as a constant current source I_o during a switching period.
4) The magnetizing inductance L_{m2} of transformer T_2 is large enough to ignore the effect of the
5) Magnetizing current during switching period, while the magnetizing inductance L_{m1} of transformer T_1 is designed with small value.
6) Two transformers T_1 and T_2 have same turns-ratio of $n_1=N_{s1}/N_{p1}=n_2=N_{s2}/N_{p2}$ and $n=n_1+n_2$.

As shown in Fig. 2 and Fig. 3, each switching period can be subdivided into 16 modes and 12 modes, respectively. The proposed converter has symmetrical operation so that only half cycle is explained.

A. Dual full-bridge operation

Mode 1 [t_0-t_1]*:* Mode 1 begins when commutation of D_{s1} and D_{a1} is finished. Q_1, Q_2 and Q_5 are conducting and input power is transferred to the secondary side. During mode 1, positive input voltage V_s is applied to the primary voltage $v_{pri1}(t)$ of T_1 and V_s-$v_{Cb}(t)$ is applied to the primary voltage $v_{pri2}(t)$ of T_2, respectively. Therefore, primary currents $i_{pri1}(t)$ is linearly increased. However, the magnetizing inductance L_{m2} of T_2 is very large so that the effect of magnetizing inductor current $i_{Lm2}(t)$ can be ignored. Then, $i_{pri2}(t)$ is almost same value with reflected load current. Since $i_{pri2}(t)$ charges the boost capacitor C_{boost}, the voltage $v_{cboost}(t)$ of C_{boost} is linearly increased in this mode. The energy stored in transformer T_1 and T_2 is transferred to the output through D_{s1} and D_{s2}. The output voltage of rectifier stage $v_{rec}(t)$ is sum of reflected voltage $v_{sec1}(t)$ of T_1 and reflected voltage $v_{sec2}(t)$ of T_2. The currents and the voltages are represented as follows:

$$i_{pri1}(t) = 0.5nI_o + \frac{V_s}{L_{m1}+L_{lkg1}}(t-t_0) + i_{pri1}(t_o) \quad (1)$$

$$i_{pri2}(t) = 0.5nI_o + \frac{V_s - v_{C_{boost}}(t)}{L_{m2}+L_{lkg2}}(t-t_0) \simeq 0.5nI_o + i_{pri2}(t_o) \quad (2)$$

$$v_{C_{boost}}(t) = v_{C_{boost}}(t_0) + \frac{0.5nI_o}{C_{boost}}(t-t_0) \quad (3)$$

$$v_{rec}(t) = n(V_s - 0.5v_{Cb}(t)) \quad (4)$$

$$v_{Ds1,3}(t) = n(V_s - 0.5v_{Cb}(t)),\ v_{Da2}(t) = 0.5n(V_s - v_{Cb}(t)),$$
$$v_{Da1}(t) = 0.5nV_s \quad (5)$$

Mode 2 [t_1-t_2]*:* At time t_1, Q_5 is turned off and mode 2 begins. The output capacitors C_{oss} of switches Q_5 and Q_6 are linearly charged and discharged respectively by the energy stored in the output inductor L_o. $v_{pri2}(t)$ is linearly decreased to zero and the primary $v_{pri1}(t)$ is continuously maintained at V_s. Hence, $v_{sec2}(t)$ is decreased from $n(V_s$-$v_{Cboost}(t))$ to zero voltage. Then, $v_{rec}(t)$ falls from $n(V_s$-$0.5v_{Cboost}(t))$ to $0.5nV_s$.

Mode 3 [t_2-t_3]*:* After $v_{pri2}(t)$ reaches zero, anti-parallel diode D_6 of Q_6 starts to conduct. When Q_6 is turned on at this time, ZVS operation of Q_6 is achieved. During mode 3, since the commutation between D_{s2} and D_{a2} is progressed, total $v_{Cboost}(t)$ is applied to L_{lkg2} and $i_{pri2}(t)$ starts to decrease rapidly. $v_{pri1}(t)$ is still maintained at V_s during this mode. Hence $v_{rec}(t)$ is maintained at $0.5nV_s$ and $i_{pri1}(t)$ is continuously increased. The currents and secondary voltages are represented as follows:

$$i_{pri1}(t) = 0.5nI_o + \frac{V_s}{L_{m1}+L_{lkg1}}(t-t_2) + i_{pri1}(t_2) \quad (6)$$

$$i_{pri2}(t) = i_{pri2}(t_2) - \frac{1}{L_{lkg2}}\int v_{Cboost}(t)dt \quad (7)$$

$$v_{C_{boost}}(t) = v_{C_{boost}}(t_2) + \frac{1}{C_{boost}}\int i_{pri2}(t) \quad (8)$$

$$v_{rec}(t) = 0.5nV_s \quad (9)$$

Mode 4 [t_3-t_4]*:* When commutation between D_{s2} and D_{a2} is completed, mode 4 begins. Since $i_{pri2}(t)$ is in zero state, the input power is transferred to the output stage through only T_1 ,D_{s1} and D_{a2}. The voltage of boost capacitor $v_{cboost}(t)$ remains its maximum value $V_{cboost,max}$ and the secondary voltage $v_{sec2}(t)$ of T_2 is decreased to $0.5nV_{Cboost,max}$.

Mode 5 [t_4-t_5]*:* At time t_4, Q_1 and Q_2 are turned off and mode 6 begins. Since $v_{sec1}(t)$ remains in positive side, output current still flows through T_1 , D_{s1} and D_{a2} during

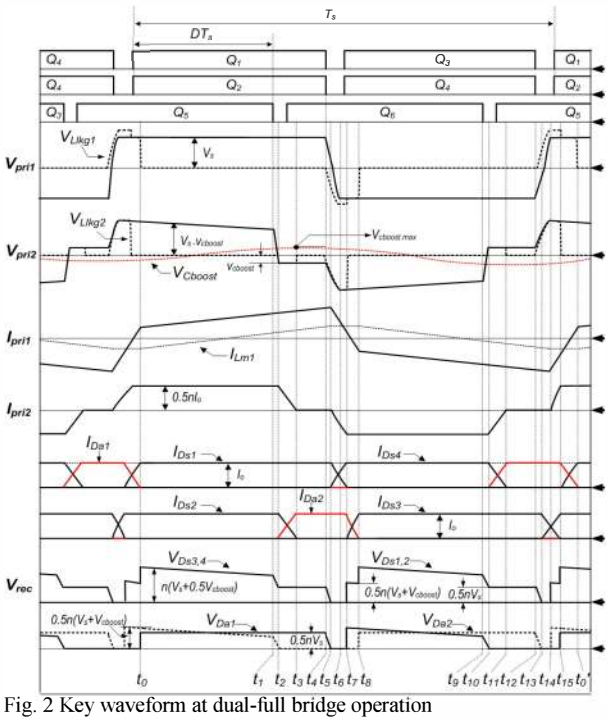

Fig. 2 Key waveform at dual-full bridge operation

this mode. Hence, C_{oss} of Q_1, Q_2, Q_3 and Q_4 are linearly charged and discharged respectively by the reflected load current of T_1 and the current of magnetizing inductor L_{m1}. The voltages and currents are represented as follows:

$$i_{pri1}(t) = 0.5nI_o + I_{Lm1}(t_4) \tag{10}$$

$$v_{Q3}(t) = v_{Q4}(t) = V_s - \frac{0.5nI_o + I_{Lm1}(t_4)}{4C_{oss}}(t-t_4) \tag{11}$$

$$v_{pri1}(t) = V_s - \frac{0.5nI_o + I_{Lm1}(t_4)}{2C_{oss}}(t-t_4) \tag{12}$$

$$v_{pri2}(t) = -V_{Cboost.\max} - \frac{0.5nI_O + I_{Lm1}(t_4)}{4C_{oss}}(t-t_4) \tag{13}$$

Mode 6 [t_5-t_6]: When the sum of $v_{sec1}(t)$ and $v_{sec2}(t)$ reaches at zero voltage, mode 6 starts. At time t_5, D_{s4} starts to conduct and commutation between D_{s1} and D_{s4} is progressed. The C_{oss} of Q_1, Q_2, Q_3 and Q_4 are charged and discharged, respectively in a resonance manner with L_{lkg1}+L_{lkg2}. The voltages and currents are represented as follows:

$$v_{pri1}(t) = v_{pri1}(t_5) - 2i_{pri1}(t_5)Z_o \sin(\omega_o(t-t_5)) \tag{14}$$

$$v_{pri1}(t) = v_{pri1}(t_5) - 2i_{pri1}(t_5)Z_o \sin(\omega_o(t-t_5)) \tag{15}$$

$$i_{pri1}(t) = i_{pri1}(t_5)(1 - Z_o \cos(\omega_o(t-t_5)) \tag{16}$$

$$i_{pri2}(t) = -i_{pri1}(t_5)Z_o \cos(\omega_o(t-t_5)) \tag{17}$$

, $i_{pri1}(t_5) = 0.5nI_o + \frac{V_s T_s}{4L_{m1}}$, $Z_o = \sqrt{\frac{L_{lkg1}+L_{lkg2}}{4C_{oss}}}$, $\omega_o = \frac{1}{\sqrt{4(L_{lkg1}+L_{lkg2})C_{oss}}}$

Mode 7 [t_6-t_7]: After $v_{pri1}(t)$ and $v_{pri2}(t)$ reach -V_s, anti-parallel diode D_3 of Q_3 and anti-parallel diode D_4 of Q_4 start to conduct. When Q_3 and Q_4 are turned on at this time, ZVS operation of Q_3 and Q_4 is achieved. During this mode, the commutation between D_{s1} and D_{s4} is still progressed. The sum of the input voltage V_s and divided voltage of $V_{cboost.max}$ is applied to both leakage inductor L_{lkg1} of T_1 and leakage inductor L_{lkg2} of T_2 so that $i_{pri1}(t)$ and $i_{pri2}(t)$ is rapidly decreased to negative side. The voltages and currents are represented as follows:

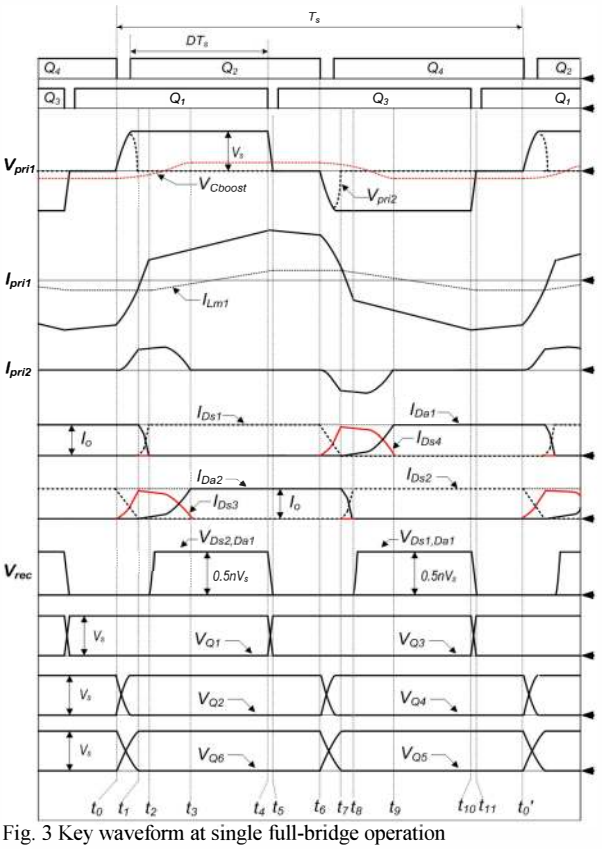

Fig. 3 Key waveform at single full-bridge operation

$$V_{l_{lkg1}} = V_s + v_{Cboost.\max}\frac{L_{lkg1}}{L_{lkg1}+L_{lkg2}} \tag{18}$$

$$V_{l_{lkg2}} = V_s + v_{Cboost.\max}\frac{L_{lkg2}}{L_{lkg1}+L_{lkg2}} \tag{19}$$

$$i_{pri1}(t) = i_{pri1}(t_6) - \frac{V_{l_{lkg1}}}{L_{lkg1}}(t-t_6) \tag{20}$$

$$i_{pri2}(t) = -\frac{V_{l_{lkg2}}}{L_{lkg2}}(t-t_2) \tag{21}$$

Mode 8 [t_7-t_8]: When commutation between D_{s1} and D_{s4} is finished, mode 8 begins. At this time, since commutation between D_{s3} and D_{a2} is progressed, V_s is applied to the L_{lkg1} and $i_{pri1}(t)$ is continuously decreased to the negative side. The negative voltage $-V_s$+$v_{cboost}(t)$ is applied to $v_{pri2}(t)$, then $v_{rec}(t)$ is increased to $0.5n(V_s+v_{cboost}(t))$ and input energy is transferred to the output through T_2, Q_4, Q_6, D_{a2} and D_{s4}. The voltages and currents are represented as follows:

$$i_{pri1}(t) = i_{pri1}(t_7) - \frac{V_S}{L_{lkg1}}(t-t_7) \tag{22}$$

$$i_{pri2}(t) = -0.5nI_O \tag{23}$$

$$v_{pri2}(t) = -V_s + v_{Cboost}(t) \tag{24}$$

$$v_{C_{boost}}(t) = V_{C_{boost}.\max} - \frac{1}{C_{boost}}\int i_{pri2}(t) \tag{25}$$

B. Single full-bridge operation

The operation of the proposed converter at single full-bridge operation is almost same with conventional PSFB converter except Mode 1, 2 and 3. Hence, only Mode 1, 2 and 3 are explained and the explanation of other modes is omitted.

Mode 1 [t_0-t_1]: At t_o, after Q_4 is turned off and mode 1

begins. The output capacitors C_{oss} of Q_2 and Q_4 are charged and discharged, respectively in a resonance manner with equivalent leakage inductor (L_{lkg1}//L_{lkg2}) and the voltage of Q_2 starts to decrease. Hence, the difference between V_{Q2} and V_{Q5}+$v_{cboost}(t)$ is applied to $v_{pri2}(t)$ and $i_{pri2}(t)$ is start to increase. From this operation, the voltage transition between Q_5 and Q_6 is occurred and commutation between D_{s2} and D_{s3} is progressed. C_{boost} is charged by $i_{pri2}(t)$. The voltages and current are represented as follows:

$$v_{Q2}(t) = i_{pri1}(t_0)Z_L \sin(\omega_L(t-t_0)) \quad (26)$$

$$v_{Q5}(t) = V_s - i_{pri1}(t_0)Z_L \sin(\omega_L(t-t_0)) \quad (27)$$

$$i_{pri1}(t) = i_{pri1}(t_0)(1+Z_L \cos(\omega_L(t-t_0)) \quad (28)$$

$$i_{pri2}(t) = i_{pri1}(t_0)Z_L \cos(\omega_L(t-t_0)) \quad (29)$$

$$, i_{pri1}(t_5) = 0.5nI_o + \frac{V_s DT_s}{2L_{m1}}, \quad Z_L = \sqrt{\frac{L_{lkg1} \,||\, L_{lkg2}}{2C_{oss}}}, \omega_L = \frac{1}{\sqrt{2(L_{lkg1} \,||\, L_{lkg2})C_{oss}}}$$

Mode 2 [t_1-t_2]*:* After commutation between D_{s2} and D_{s3} is finished, mode 2 begins. The anti-parallel diode d_6 of Q_6 and Q_2 are conducted. The commutation between D_{s2} and D_{a2}, D_{a1} and D_{s1} is progressed and V_s is applied to L_{lkg1} and $v_{cboost}(t)$ is applied to l_{lkg2}. Therefore, $i_{pri1}(t)$ and $i_{pri2}(t)$ is increased.

Mode 3 [t_2-t_3]*:* At t_2, the commutation between D_{s1} and D_{a1} is finished and mode 3 begins. During this mode, the commutation between D_{s2} and D_{a2} is still progressed and input energy is mainly transferred to the secondary side through T_1, D_{s1} and D_{a2}. When $v_{cboost}(t)$ is increased to the positive side, $i_{pri2}(t)$ start to decrease. When $i_{pri2}(t)$ reaches to zero current, mode 3 is ended.

IV. Analysis of Proposed Circuit

A. Voltage conversion ratio, M

Fig. 4 shows the output voltage of rectifier stage for both the conventional PSFB converter and the proposed converter. Since the duration of mode 6, 7 and 8 is relatively narrow at dual full-bridge operation of the proposed converter, and the voltage of boost capacitor is also practically small, duration of mode 6,7 and 8 is ignored for the analysis of rectifier output voltage. The voltage conversion ratio is given by averaging the rectifier output voltage so that the voltage conversion ratio of proposed converter at dual full-bridge mode without considering the effect of boost capacitor can be expressed as follows:

$$M_{proposed.dual} = \frac{V_o}{V_s} = n(0.5 + D) \quad (30)$$

The voltage conversion ratio of conventional PSFB converter is expressed as follows:

$$M_{conv\ PSFB} = \frac{V_o}{V_s} = 2nD \quad (31)$$

Fig. 5 shows the normalized voltage conversion ratio of both the proposed converter and the conventional PSFB converter according to the duty variation. As shown in Fig. 5, the proposed converter has higher gain than the conventional PSFB converter so that transformer of the proposed converter can be designed to have small turns-ratio with same duty cycle.

The voltage conversion ratio of proposed converter at dual full-bridge mode without considering the effect of boost capacitor is same with that of circuit in [20]. However, when considering the effect of boost capacitor, turns-ratio of transformer T2 can be slightly changed. As explained in section II, the voltage of boost capacitor appears on the rectifier output voltage, and then the waveform of rectifier output can be changed as dotted line in Fig. 4-(a). Therefore, the voltage conversion ratio of the proposed converter can be slightly increased and turns-ratio of transformer T2 can be designed as smaller value [10].

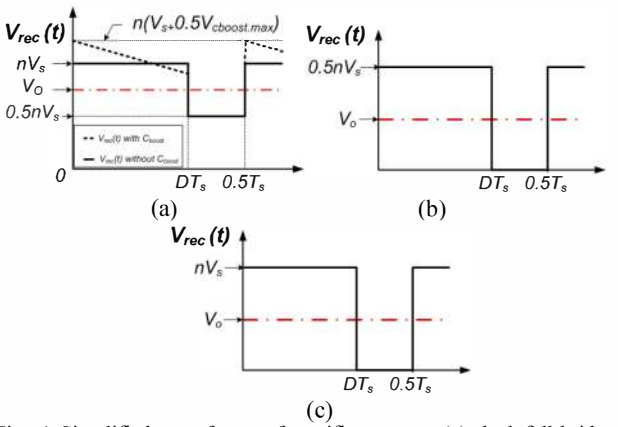

Fig. 4 Simplified waveforms of rectifier output: (a) dual full-bridge mode of proposed converter (b) single full-bridge mode of proposed converter (c) conventional PSFB converter

When it is assumed that the duration of mode 3 is relatively narrow than that of mode 1, average primary current $i_{pri2}(t)$ of T_2 during a half cycle is estimated to $0.5nDI_o$. Therefore, the maximum voltage of boost capacitor $V_{cboost,max}$ can be estimated as follows:

$$0.5\Delta v_{C_{boost.max}} = V_{C_{boost.max}} \approx \frac{nDI_O T_s}{4C_{boost}} \quad (32)$$

From (32), it is noted that the maximum voltage of boost capacitor is inversely proportional to C_{boost}. Hence, the voltage conversion ratio of proposed converter is more increased with smaller C_{boost}. However, when $V_{cboot,max}$ is greater than V_s, the proposed converter is placed in an abnormal condition. Considering this condition, the minimum value of C_{boost} is given as follows:

$$C_{boost} \geq \frac{nDI_O T_s}{4V_s} \quad (33)$$

The voltage conversion ratio of proposed converter at single full-bridge operation is given as follows:

$$M_{proposed.single} = \frac{V_o}{V_s} = nD \quad (34)$$

Since the proposed converter at single full-bridge mode has same rectifier waveform compared to the conventional PSFB converter, the voltage conversion ratio of proposed converter at single full-bridge mode is same expression with that of the conventional PSFB converter. Hence, the operating duty cycle of proposed converter at single full-bridge mode can be larger than that of conventional PSFB converter due to the small turns-ratio of transformer in the proposed converter.

B. Conduction loss of rectifier stage

Since the output of DC/DC stage in RF power generator has high output voltage (V_o: 40V~200V), full-bridge rectifier is employed for the rectifier stage due to

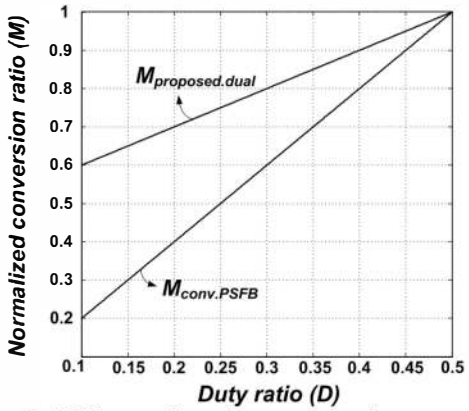

Fig. 5 Normalized DC conversion ratio versus duty ratio

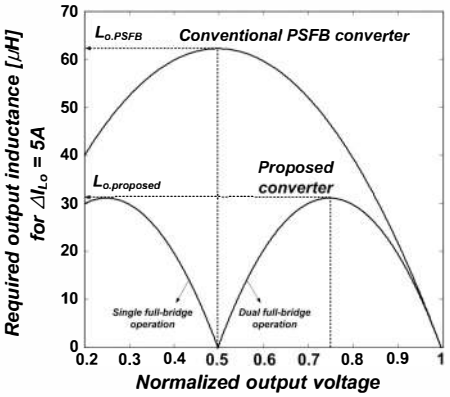

Fig. 6 Required inductance versus output voltage variation

the voltage stress of rectifier diode. However, although full-bridge type rectifier is applied, the rectifier diodes still suffer from high voltage stress coming from the oscillation of parasitic circuit elements [12]. Therefore, high-voltage-rated diode has to be used for the rectifier stage. High-voltage-rated diode typically has large forward voltage so that it results in large conduction loss of secondary side.

In the rectifier stage of proposed converter, the additional diodes D_{a1}, D_{a2} are placed in the midpoint of both transformer T_1 and T_2 with full-bridge rectifier. As shown in table I, the additional diodes have much lower voltage stress than other rectifier diodes. Therefore, the low-voltage-rated diodes that have low forward voltage can be employed for the additional diodes. As explained in mode analysis of dual full-bridge mode, conduction path of load current is distributed between D_{a1}, D_{a2} and D_{s3}, D_{s4} during the switching cycle so that the conduction loss of rectifier diodes is decreased. Since the average current of additional diode is inversely proportional to duty cycle as shown in table I, the conduction loss of rectifier stage is getting lower as the output power decreases.

Since the voltage stress of rectifier diodes is related with the voltage of boost capacitor as shown in table I, the selection of C_{boost} is restricted to guarantee the designed maximum voltage stress of rectifier diode as well as the normal operation of converter and it is expressed as follows:

$$C_{boost} \geq \frac{n^2 D I_O T_s}{8(V_{diode.\max} - nV_s)} \tag{35}$$

C. Conduction loss of primary side

As explained in section II, since the voltage of boost capacitor C_{boost} reset the primary current $i_{pri2}(t)$ of T_2 during the freewheeling period at dual full-bridge operation, the circulating current of $i_{pri2}(t)$ is reduced and smaller C_{boost} results in more reduction of conduction loss. On the other hand, the conventional PSFB converter has circulating current that results in large conduction loss of both primary switches and primary side of transformer. For wide output application, especially RF power generator application, the output voltage and output current vary widely according to the output power requirement so that the duty ratio is also widely changed. In this case, the circulating current of conventional PSFB converter is highly increased as required output power is decreased, and the conversion efficiency of conventional PSFB converter becomes poor.

Although the proposed converter has the circulating current at single full-bridge operation, it still has lower RMS current stress as shown in Table I, due to smaller turns-ratio of transformer T_1 than that of the conventional PSFB converter.

D. Output filter Requirement

As shown in Fig. 4, the rectifier voltage of proposed converter has improved waveform than conventional PSFB converter. Hence, output filter can be designed as small value in the proposed converter.

The output inductor both of the proposed converter and the conventional PSFB converter can be designed from the rectifier output voltage as shown in Fig. 4, and it can be approximated as follows, respectively.

For the dual full-bridge operation of proposed converter,

$$L_{o.proposed} = \frac{(nV_s - V_o)}{\Delta I_{Lo}}\left(\frac{V_o}{nV_s} - 0.5\right)T_s \tag{36}$$

For the single full-bridge operation of proposed converter,

Table I The voltage and current stress of semiconductor components

	Proposed Converter				Conventional PSFB converter
	Dual full-bridge mode		Single full-bridge mode		
Primary switches RMS current	Q_1,Q_3	$0.35nI_o$	$0.35nI_o$		$0.7nI_o$
	Q_5,Q_6	$0.5nI_o\sqrt{D}$	N/A		N/A
	Q_2,Q_4	$nI_o\sqrt{0.76D+0.126}$	$0.35nI_o$		$0.7nI_o$
Rectifier diode voltage stress	$n(V_s+0.5V_{scboost.max})\approx nV_s$		$0.5nV_s$		nV_s
Rectifier diode AVG. current	D_{s1},D_{s3}	$0.5I_o$	D_{s1},Ds_3	$0.5I_o$	$0.5I_o$
	D_{s2},D_{s4}	DI_o	D_{s2},D_{s4}	N/A	
Additional diode voltage stress	$0.5n(V_s+V_{scboost.max})\approx 0.5nV_s$		$0.5nV_s$		N/A
Additional diode AVG. current	$(0.5-D)I_o$		$0.5I_o$		N/A

For the single full-bridge operation of proposed converter,

$$L_{o.proposed} = \frac{(nV_s - 2V_o)V_o T_s}{2\Delta I_{Lo} nV_s} \quad (37)$$

For the conventional PSFB converter,

$$L_{o.PSFB} = \frac{(nV_s - V_o)V_o T_s}{2\Delta I_{Lo} nV_s} \quad (38)$$

,where ΔI_{Lo} is the peak-to-peak ripple current of output inductor.

Fig. 6 shows the required output inductance according to the output voltage variation for a given ΔI_{Lo}. As shown in Fig. 6, the required output inductance of proposed converter is smaller than that of conventional PSFB converter for a given variation range of output voltage.

V. Experimental Results

To verify the feasibility of the proposed converter, 3kW laboratory prototype converter has been built with following specifications: Input voltage: V_s= 280V, output voltage variation: V_o=40V~200V, switching frequency: f_s=100kHz and maximum output power: P_o=3kW. And components of prototype are shown in table II.

Fig. 7 shows experimental results of primary voltage and primary current for both the conventional PSFB converter and the dual full-bride operation of proposed PSFB converter at full load and half load condition. As shown in Fig. 7, the proposed converter has reduced circulating current and smaller RMS current as discussed in previous section, while the conventional converter has large circulating current due to the small duty operation.

Fig. 8 shows experimental results of primary voltage and primary current for both conventional PSFB converter and single full-bride operation of proposed PSFB converter at 20% load condition. As shown in Fig. 19, the proposed converter has smaller RMS current despite the existence of circulating current because the proposed converter has smaller turns-ratio (n_1=0.44) than turns-ratio (n=0.88) of the conventional PSFB converter. Therefore, it is noted that the proposed converter has lower conduction loss of primary side over whole load condition compared to the conventional PSFB converter.

Table II Component list

Components list	Proposed Converter		Conventional PSFB converter
Primary switches	IPP60R045 (600V/60A)		IPP60R045 (600V/60A)
Transformer	EI5040 x 1		EI5040x2 L_m: 330μH L_{lkg}:2.2uH N_p:N_s=9:8
	T_1 L_m: 302μH L_{lkg}:4.3uH N_p:N_s=18:8	T_2 L_m: 647μH L_{lkg}:2.25uH N_p:N_s=18:7	
Rectifier diode (D_{s1}~D_{s4})	APT75DQ60 (600V/75A/2V)		APT75DQ60 (600V/75A/2V)
Additional diode (D_{a1},D_{a2})	30EPH03 (300V/60A/1.25V)		N/A
Output Inductor (L_o)	CM3580060 x 2 (Φ: 35mm, H: 10.46mm) 28uH		CM400060 x 2 (Φ: 40mm, H: 14.48mm) 58μH
Boost capacitor (C_{boost})	500nF		N/A
Output capacitor (C_o)	750uF/350V		750uF/350V

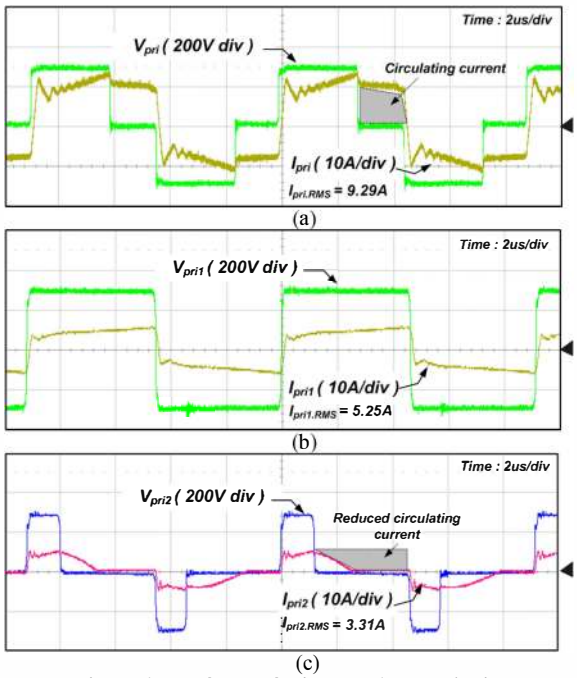

Fig. 7 Experimental waveforms of primary voltage and primary current at half load condition: (a) V_{pri} and I_{pri} of conventional PSFB converter, (b)V_{pri1} and I_{pri1} of proposed converter (c)V_{pri2} and I_{pri2} of proposed converter

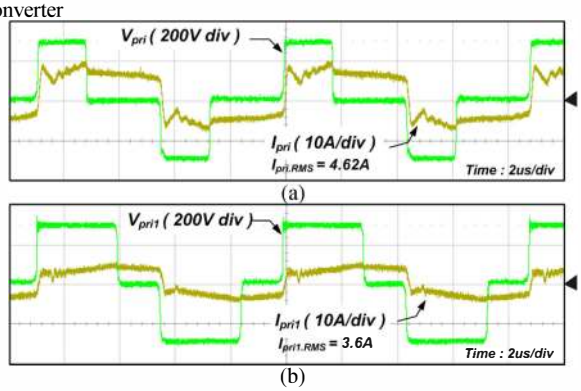

Fig. 8 Experimental waveforms of primary voltage and primary current at 20% load condition: (a) V_{pri} and I_{pri} of conventional PSFB converter, (b)V_{pri1} and I_{pri1} of proposed converter

Fig. 9 shows the experimental results of rectifier-diode voltage for both conventional PSFB converter and proposed PSFB converter. As shown in Fig. 9, the additional diodes have about half voltage stress of rectifier diodes in the conventional PSFB converter. Hence, they are employed with low-voltage-rated and low-forward-voltage diode (300V/1.25V) and it results in reduction of conduction loss in the rectifier stage of proposed converter as analyzed in previous section.

Fig. 10 shows size comparison of designed output inductor between the conventional PSFB converter and the proposed converter. As shown in Fig. 10,
the proposed converter has smaller inductor size than conventional PSFB converter as discussed in section IV.

Fig. 11 represents the comparative efficiency curve between the conventional PSFB converter and the proposed converter as the output power variation. From Fig. 11, it is shown that the proposed converter has higher efficiency over whole output power condition due to the lower RMS current stress of primary side, reduced circulating current and low conduction loss of secondary rectifier.

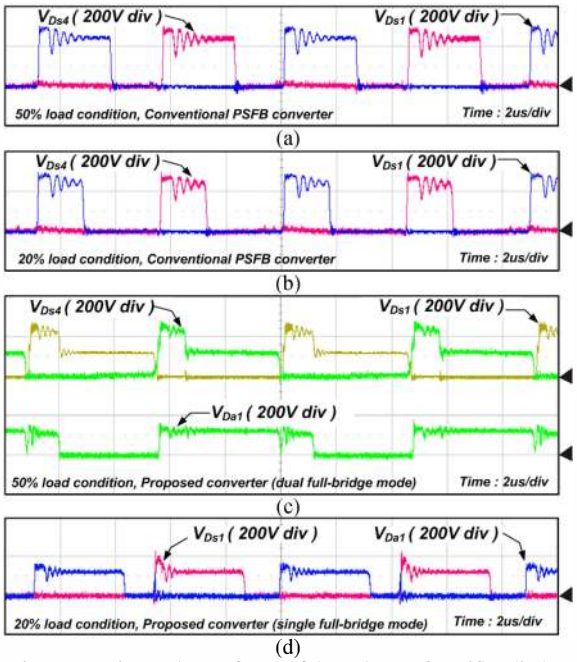

Fig. 9 Experimental waveforms of the voltage of rectifier diodes: (a) 50% load condition of conventional PSFB converter, (b) 20% load condition of conventional PSFB converter, (c) 50% load condition of proposed converter (dual full-bridge mode), (d) 20% load condition of proposed converter (single full-bridge mode)

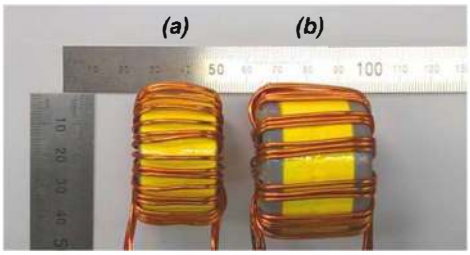

Fig. 10 Size comparison of output inductor: (a) Output inductor of proposed converter, (b) Output inductor of conventional PSFB converter

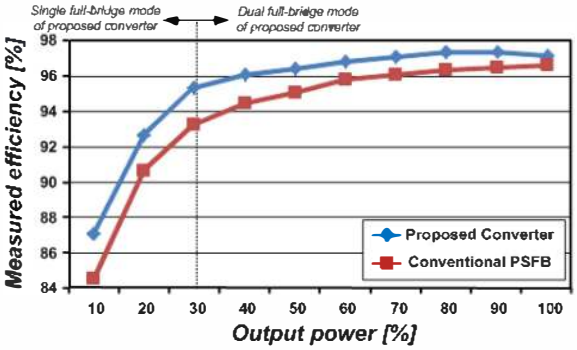

Fig. 11 Efficiency comparison versus output power

VI. Conclusion

A new hybrid dual full-bridge converter with reduced circulating current, small output filter and low conduction loss of rectifier diode for RF power generator application is proposed in this paper. By adopting a small capacitor connected in series with one transformer, the circulating current is greatly reduced. In spite of reduced circulating current, ZVS operation of all switches is well achieved. Furthermore, the energy is transferred to the output stage during the freewheeling period so that the waveform of rectifier output voltage is improved and it results in the size reduction of output inductor compared to the conventional PSFB converter. In addition, since the load current is distributed to the additional low-voltage-rated diode, the secondary conduction loss is also reduced in the proposed converter. These advantages result in the improvement of efficiency over wide output voltage and power ranges. Therefore, it can be said that the proposed converter is very desirable and suitable for high power and high efficiency front-end DC/DC converter of the wide-output-voltage applications such as RF power generator.

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