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Hybrid-Mode SRAM Sense Amplifiers: New Approach on Transistor Sizing

Do Anh-Tuan, Kong Zhi-Hui, and Yeo Kiat-Seng

***Abstract*—A novel high-speed sense amplifier for ultra-low-voltage SRAM applications is presented. It introduces a completely different way of sizing the aspect ratio of the transistors on the data-path, hence realizing a current-voltage hybrid mode Sense Amplifier. Extensive post-layout simulations have proved that the new Sense Amplifier provides both high-speed and low-power properties, with its delay and power reduced to 25.8% and 37.6% of those of the best prior art. It also offers a much better read-effectiveness and robustness against the bit- and data-line capacitances as well as V_{DD} variations. Furthermore, the new Sense Amplifier is able to tolerate a large difference between the parasitic capacitances associated with the complementary DLs. It can operate down to a supply voltage of 0.9 V, the lowest reported for a 0.18 μm CMOS process. A modified cross-coupled amplifier is also introduced, allowing the Sense Amplifier to operate down to 0.55 V.**

***Index Terms*—Low-power SRAM, low-voltage SRAM, sense amplifier (SA).**

I. Introduction

SRAM-BASED cache is one of the most important components of state-of-the-art very large-scale integration (VLSI) systems. Fast SRAM caches are vital to increase the speed of the data flows and, hence, the speed of the system [1]. According to the 2002 International Technology Roadmap for Semiconductors (ITRS 2002) [2], the memory chip will occupy 90% of the chip area by 2013. Therefore, the power dissipated within the on-chip caches will become a dominant part of the total power consumption of the chip. In view of the above, there is inevitably an apparent urgency to address these two often-conflicting power and delay requirements [1], [3], [4]. The current-mode sense amplifier (SA) has the ability to quickly amplify a small differential signal from the bit-lines (BLs) and data-lines (DLs) to full CMOS logic-level outputs without requiring large voltage swings of these capacitive lines (whose parasitic capacitances are normally referred to as C_{BL} and C_{DL}, respectively). It is widely used as one of the most effective ways to reduce both sensing delay and power consumption of the SRAM [5]–[14]. In this work, we extensively studied the operation of existing SAs, analyzed their weaknesses and proposed a new sensing scheme that has a much higher driving force, hence providing faster sensing delay, lower power consumption, and greater reliability.

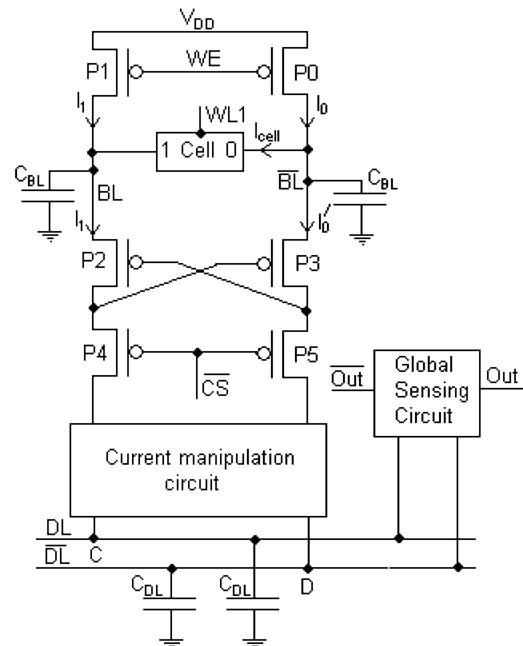

Fig. 1. Current-mode SA with current conveyor incorporated.

This paper is organized as follows. The operations and read effectiveness of the existing current-mode and the proposed SAs are described in Sections II and III, respectively. Sensing delay and power consumption of the new design are graphically presented in Section IV, in comparison with the three best existing designs, namely, the charge-transfer [13], the ultralow-power [9], and the high-speed [8] designs, respectively. In Section V, we describe a modified version of the proposed SA that can operate at a low supply voltage of 0.55 V. Section VI concludes the paper.

II. Current-Mode SA

A. Current-Mode SA and Its Derivatives

The current-mode sensing scheme (Fig. 1) in SRAM applications was first introduced in [5]. The current-mode SAs, marked by the presence of the conventional current-conveyor [5], is insensitive to the C_{BL} and, hence, offers a higher sensing speed and consumes less power compared with the voltage-mode counterparts [5]. Over the last two decades, a number of current-mode SAs have been proposed, aiming at improving the sensing speed and the power consumption in the read operation of the SRAM [7]–[13]. Since all of these SA designs utilize the differential output currents of the current

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TABLE I
SUMMARY OF CURRENTS CONSUMED DURING A READ CYCLE IN A CURRENT-MODE SA. $W_{P0,1} = 15\ \mu M$, $I_{cell} = 92\ \mu A$. $I_0' = I_0 - I_{cell}$. $\Delta I = I_1 - I_0'$

W_{P2-5} (μm)	1	2	3	4	5	6	7
I_0 (μA)	119	146	174	198	221	244	267
I_1 (μA)	38	76	113	143	172	199	226
I_0' (μA)	27	54	82	106	129	152	174
ΔI (μA)	11	22	31	37	43	47	52
% utilization	*7.0*	*9.9*	*10.8*	*10.9*	*10.6*	*10.5*	*10.2*

conveyor, their improvement is only incremental. Reference [5] clearly indicated that the above-mentioned differential current is equal to the current flowing into the cell node where a "0" is stored, i.e., I_{cell}. Our analysis and simulations have proved otherwise. In fact, the differential current is much smaller than the I_{cell}, due to the imperfection of the current conveyor. This issue will be discussed in more detail in the next sections.

B. Imperfections of the Current Conveyor and its Impact on the Current-Mode Sensing Scheme

The current conveyor consists of four identical pMOS transistors P2, P3, P4, and P5 (Fig. 1). Since this configuration is common for all current-mode SAs, its drawback is also their shared weakness. As mentioned in [5], the current conveyor realizes a virtual short circuit across the complementary BLs, i.e., $V_{BL} = V_{\overline{BL}}$ during the read operation. Therefore, the currents I_0 and I_1, which are sourced by the large-sized BL load transistors P0 and P1, respectively, (Fig. 1), are equal, and a current difference of I_{cell} is realized at the inputs of the current conveyor. This is only true in an ideal case where the process variations and short channel-length effect are not present. In deep submicrometer technologies, these effects become significant and there is a slight difference between the BL voltages. For instance, at $V_{DD} = 1.8$ V, $W_{P0,1} = 15\ \mu$m and $W_{P2,3,4,5} = 1\ \mu$m (Fig. 1), then $V_{BL} = 1.79$ V and $V_{\overline{BL}} = 1.77$ V. This 0.02-V difference makes a significant impact on the effectiveness of the read process. It can be explained as follows. Since V_{BL} and $V_{\overline{BL}}$ are close to V_{DD}, both P0 and P1 operate in the triode region. Their drain currents are proportional to their drain-to-source voltages. Thus, by using $V_{DD} = 1.8$ V, $V_{BL} = 1.79$ V, and $V_{\overline{BL}} = 1.77$ V, we have I_0 three times larger than I_1 (see the second column of Table I). Consequently, the effective difference between the BL currents after taking the I_{cell} into account is very small (Δ I in Table I):

$$\text{We use \% utilization} = \frac{\Delta I}{\text{Total current}} = \frac{I_1 - I_0'}{I_0 + I_1} \quad (1)$$

as a figure of merit to measure the effectiveness of the read scheme. In our calculations, we assumed that I_{cell}, which is measured from the standard 6T cell, does not change during the sensing process. As indicated in Table I, at various transistor sizes, *% utilization* of the current-mode SA is only around 10% with Δ I much smaller than I_{cell}. Therefore, it can be concluded that the differential current in the current mode needs to be improved to obtain a more effective read operation, regarding both speed and power consumption.

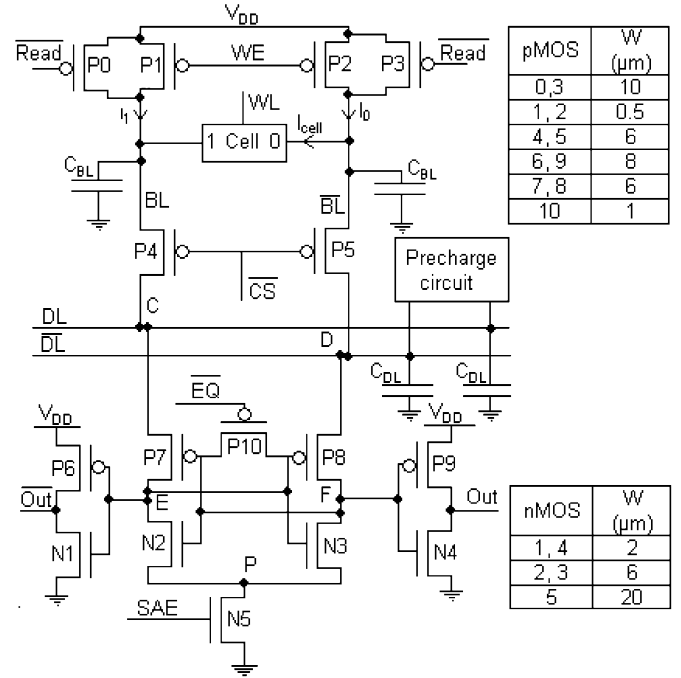

Fig. 2. Proposed SA with a simplified read-cycle-only memory system. Channel lengths of all transistors are 0.18 μm.

III. PROPOSED HYBRID CURRENT-MODE SA

A. Circuit Operation

Our proposed SA is presented in Fig. 2. It consists of 11 pMOS and 5 nMOS transistors (P0 - P10 and N1 - N5). P0 and P3 are responsible for pre-charging the BLs to V_{DD} while P1 and P2 are for holding the BLs at V_{DD} during the read-cycle. P4 and P5 act as a switch to connect the BLs to the DLs. The other 10 transistors (P6 - P10 and N1–N5) form a cross-coupled inverter which amplifies the small voltage difference on the DLs to the full CMOS logic levels [8], [9], [11], [13] and [14]. The new SA is unique in a way that it eliminated the current conveyor and transformed the normally-large BL loads (P0, P1 in Fig. 1) into small sized transistors (P1, P2 in Fig. 2). They serve to hold the BLs at V_{DD} and not to source the BL currents unlike in the conventional designs. P1 and P2 are purposely sized small so that it is not strong enough to keep the BL at V_{DD} if I_{cell} is present. As a result, one of the BLs will drop to a lower level than V_{DD} during a read access.

Before any read cycle, the BLs and DLs are precharged to V_{DD} by (P0, P3) and the pre-charge circuit, respectively (Fig. 2). Meanwhile, the Sense Amplifier Enable (SAE) signal turns off N5 to prevent any dc current from flowing to the ground to save power whilst the Equalization ($\overline{EQ}$) signal turns on P10 to hold the two nodes E and F at the same potential. When a cell is accessed by the Word Line (WL) and Column Select ($\overline{CS}$) signals, the $\overline{Read}$ signal is triggered high to deactivate P0 and P3. The pre-charge circuit is turned off, but P1 and P2 are still on to hold the BLs and the DLs at V_{DD}. Fig. 3 presents the current paths during a read cycle. The Access, Drive, and Load are transistors of the accessed memory cell. We assume that the first cell of the shown column (Fig. 2) is accessed. On the left side, where a "1" is stored, the BL and DL

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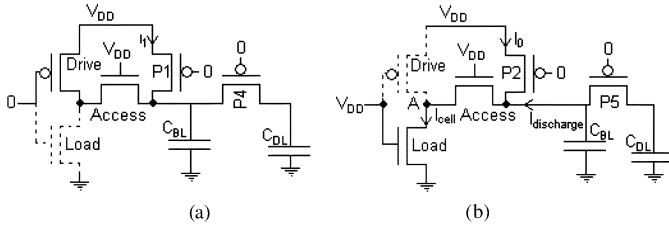

Fig. 3. Current paths during the read cycle in the proposed SA on the side where (a) a "1" is stored or (b) a "0" is stored.

TABLE II
SUMMARY OF CURRENTS CONSUMED DURING A READ CYCLE IN THE PROPOSED SA. $I_{cell} = 92\ \mu A$. $I_0' = I_0 - I_{cell} \cdot \Delta I = I_1 - I_0'$

$W_{P1,2}$ (μm)	0.3	0.5	0.7	0.9	1.1	1.3	1.5
I_0 (μA)	4	6	8	10	13	15	17
I_1 (μA)	3	4	4	4	5	5	5
I_0' (μA)	-88	-86	-84	-82	-79	-77	-75
ΔI (μA)	91	90	88	86	84	82	80
% utilization	1308	900	735	614	467	410	363
% utilization (adjusted)	*96*	*94*	*92*	*89*	*86*	*84*	*82*

remain at V_{DD} since they are held by P1 while no discharge current is available [Fig. 3(a)]. Also, since both DL and BL are kept at V_{DD}, the drain-to-source voltage of P1 is very small and, hence, it only sources a negligible current I_1 during a read, just enough to complement the leakage current along the BL. On the side where a "0" is stored, the cell sinks a current I_{cell}, which is larger than the current I_0 sourced by P2. As a result, a discharge current of $I_{discharge}(I_{discharge} = I_{cell} - I_0)$ is available to discharge the $\overline{BL}$ and $\overline{DL}$. $I_{discharge}$ then discharges both the $\overline{BL}$ and $\overline{DL}$ to lower voltage levels than V_{DD}. The cross-coupled amplifier (P6–P10 and N1–N5) will sense the difference between the DLs and amplify it to a full CMOS logic level. It is worth mentioning here that the $\overline{Read}$ is triggered high during the write cycle to turn off P0 and P3.

B. Read Effectiveness

Similar to the current-mode SA in Fig. 1, *% utilization* is also used to measure the new design's read effectiveness. All simulated results are presented in Table II. It is found that the *% utilization* of the new design is higher than 100%. This can be explained as the total supplied current $(I_1 + I_0)$ is much smaller than I_{cell}. However, during standby, a current equivalent to $I_{discharge}$ mentioned above is used to pre-charge one of the BLs to V_{DD} (the other BL is already at V_{DD} and no charging-up is needed). Therefore, the following equation is used to is used to measure the effectiveness of the read scheme:

$$\% \text{ utilization adjusted} = \frac{\Delta I}{\text{Total current}} = \frac{\Delta I}{I_1 + I_0 + I_{discharge}}.$$

It is shown in Table II that the new design offers a much better % utilization with less power consumption and stronger discharge current than the current-mode scheme.

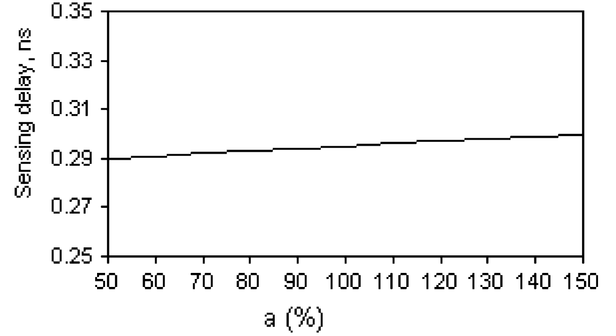

Fig. 4. Sensing delay versus the difference between C_{DL} and $C_{\overline{DL}}$ at $C_{DL} = 3$ pF, $C_{\overline{DL}} = a \times C_{DL}$, $C_{BL} = C_{\overline{BL}} = 3$ pF, $V_{DD} = 1.8$ V.

C. Tolerance to the Difference Between C_{DL} and $C_{\overline{DL}}$

All of the SA designs in the references list are based on the assumption that $C_{DL} = C_{\overline{DL}}$. Therefore, the voltage difference developed on the DLs is governed by

$$\begin{aligned} V_{DL} &= V_o + \frac{I_{BL} * \Delta t}{C_{DL}} \\ V_{\overline{DL}} &= V_o + \frac{I_{\overline{BL}} * \Delta t}{C_{\overline{DL}}} \end{aligned} \tag{2a}$$

$$\begin{aligned} \Delta V &= V_{DL} - V_{\overline{DL}} \\ &= \Delta t * \frac{(I_{BL} - I_{\overline{BL}})}{C_{DL}} = \Delta t * \frac{\Delta I}{C_{DL}} \end{aligned} \tag{2b}$$

When C_{DL} differs from $C_{\overline{DL}}$, the SA works properly only if $(I_{BL})/(C_{DL}) \geq (I_{\overline{BL}})/(C_{\overline{DL}})$. With the BL currents presented in Table I, it can only tolerate up to 10% difference between the two DL capacitances with reasonable sensing delay. The new design in contrast does not rely on the relationship between C_{DL} and $C_{\overline{DL}}$ since only one discharge current is available on one side while on the other side, voltage levels (of both the DL and BL) are kept at V_{DD}. Fig. 4 illustrates how the sensing delay changes with the difference between C_{DL} and $C_{\overline{DL}}$. We varied $C_{\overline{DL}}$ up to ±50% of C_{DL} and the new SA still works with minimum sensing delay variations.

IV. PERFORMANCE COMPARISIONS

The proposed SA and other existing designs [8], [9], and [13] have been optimized and extensively simulated using Cadence's Affirma Spectre circuit simulator based on a 0.18-μm CMOS process from CHRT. All four circuits were simulated using a simplified read-cycle-only two columns, two rows memory system. The standard 6T SRAM memory cells were used. The new SA's active layout area is the smallest among the four (see Table III and Fig. 5). This is due to its simple structure without the current-conveyor and current-mirror pairs. All four designs were tested against C_{BL}, C_{DL}, and V_{DD} variations. In order to gauge the actual behavior of the circuits, a wide range of C_{BL} and C_{DL} (from 1 to 5 pF) have been used to model the actual parasitic capacitances of the memory array. Post-layout simulation results are presented in Figs. 6–8. Fig. 6 evidently shows that only the proposed design can operate down to a V_{DD} of 0.9 V while [13], [9], and [8] cease to work at V_{DD} equal to 1.2, 1.3, and 1.3 V, respectively. Furthermore, at any supply voltage, the new design outperforms the rest with the smallest

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TABLE III
COMPARISON SUMMARY OF FOUR CIRCUITS FOR $C_L = 0.1$ pF, $C_{BL} = 1$ pF, AND $C_{DL} = 1$ pF AT 0.18-μM CMOS TECHNOLOGY AND 50 MHZ FREQUENCY

	Sensing delay, ns	Average power, mW	Layout area, μm^2
Proposed (1.8 V)	0.26	0.244	376
Proposed (0.9 V)	1.6	0.019	376
Charge-transfer (1.8V)	1.01	0.597	568
Ultra low-power (1.8V)	1.28	0.526	579
High-speed (1.8 V)	0.91	0.983	659

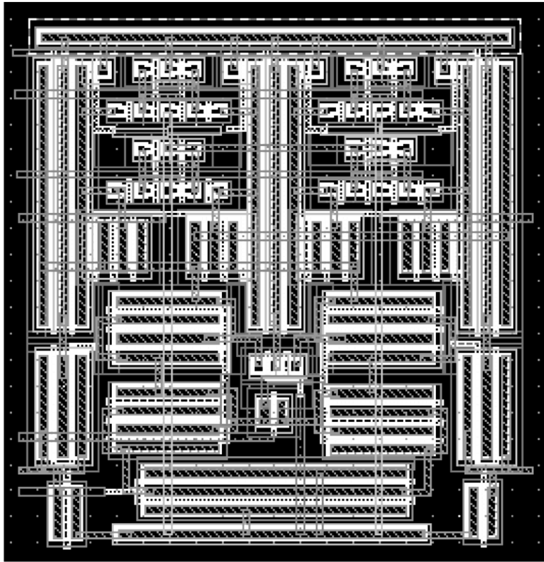

Fig. 5. Layout of the proposed design.

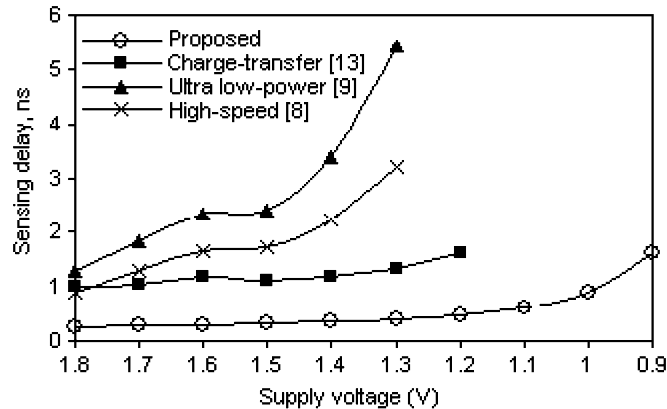

Fig. 6. Sensing delay versus V_{DD} variation for the circuits in comparison at $C_{BL} = 1$ pF, $C_{DL} = 1$ pF, and $C_L = 0.1$ pF.

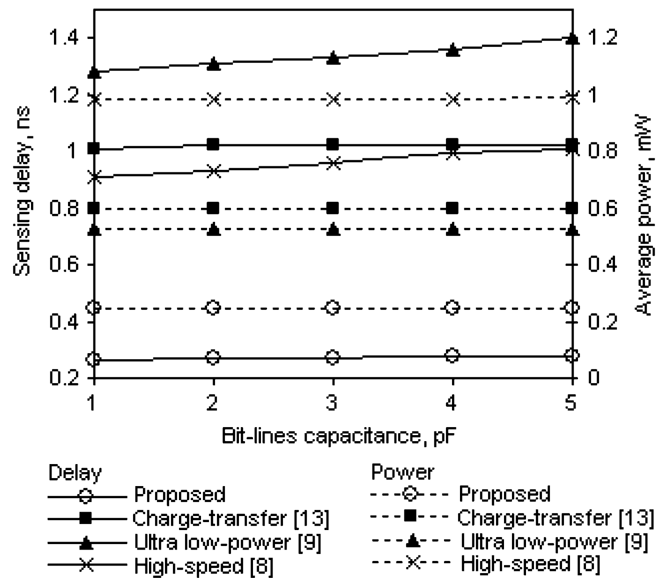

Fig. 7. Sensing delay and average power at 50 MHz versus C_{BL} variation for the circuits in comparison at $C_{DL} = 1$ pF and $C_L = 0.1$ pF.

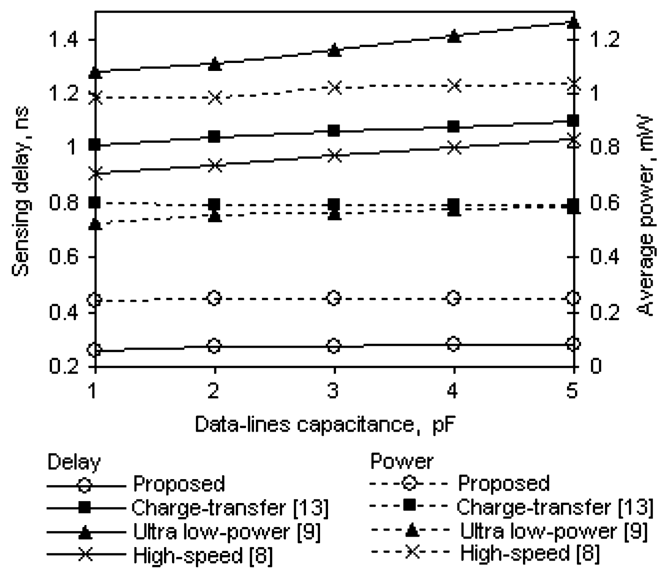

Fig. 8. Sensing delay and average power at 50 MHz versus C_{DL} variation for the circuits in comparison at $C_{BL} = 1$ pF and $C_L = 0.1$ pF.

sensing delay. Figs. 7 and 8 demonstrate the superiority of the proposed design over the other circuits at 1.8-V supply voltage against C_{BL} and C_{DL} variations. For example, at $C_{BL} = 1$ pF, $C_{DL} = 5$ pF and the load capacitor $C_L = 0.1$ pF, its sensing delay is reduced to 25.8%, 20.3%, and 28.6% and its power consumption is decreased to 37.6%, 46.5%, and 24.9% as compared with [13], [9] and [8], respectively. In addition, the new SA offers an enhanced speed robustness against the varying C_{DL}, giving a sensitivity of only 3 ps/pF, which is better than that of the designs in [13], [9], and [8], which are 3.5, 32, and 45 ps/pF, respectively. Table III provides a summary of performance metrics comparisons for all of the SAs working at 1.8 V and the proposed design working at 1.8 and 0.9 V.

V. 0.55-V SENSE AMPLIFIER

In an attempt to reduce the supply voltage to lower than 0.9 V, we proposed a modified cross-coupled inverter which can work at a supply voltage of 0.55 V. Two additional pMOS transistors P11 and P12 were added to the conventional design, as shown in Fig. 9. Furthermore, other transistors were resized so that they are strong enough to work at 0.55 V. P11 and P12 serve as a pre-charge circuit to pre-charge the two nodes E and F to the same potential, i.e., V_{DD}. As a result, a small-sized transistor P10 can be used, thus significantly reducing the switching time of the cross-couple inverter [14]. At 0.55-V supply voltage, its

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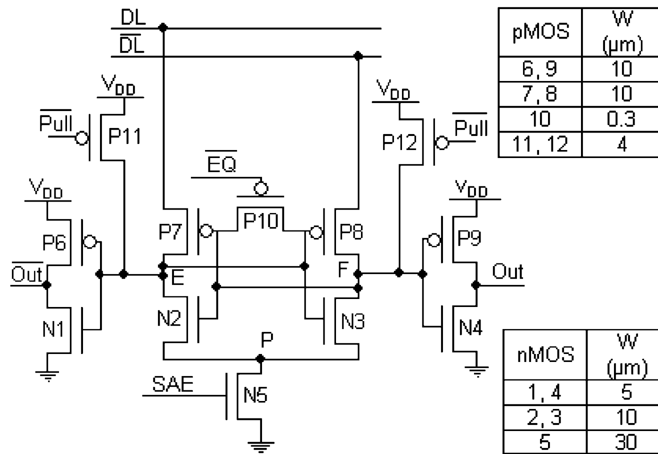

pMOS	W (μm)
6, 9	10
7, 8	10
10	0.3
11, 12	4

nMOS	W (μm)
1, 4	5
2, 3	10
5	30

Fig. 9. Improved version of the cross-coupled amplifier. Channel lengths of all transistors are 0.18 μm.

sensing delay is 4.53 ns and consumes 6.72 μW. For the purpose of this paper, we only optimize the SA for it to work at a very low voltage, rather than over a wide range (from 1.8 to 0.55 V), since large transistors will consume a huge amount of power if it operates at 1.8 V. However, it is enough to prove the superiority of the proposed design over its state-of-the-art counterparts. Transistor sizing for the improved circuit is also shown in Fig. 9.

VI. Conclusion

A robust high-performance SA is presented. It introduces a new read scheme that creatively combines the current- and voltage-sensing schemes to maximize the utilization of I_{cell}, hence offering a much better performance in terms of both sensing speed and power consumption. Since only one of the BLs and one of the DLs are discharged to lower levels than V_{DD} while their complementary lines are kept at V_{DD}, the new SA is insensitive to the difference between C_{DL} and $C_{\overline{DL}}$. This feature helps it to cope with the increasing fluctuation of these parasitic capacitances due to the layout and fabrication processes. The new design can operate in a wide supply voltage range, from 1.8 to 0.9 V with minimum performance degradation. Furthermore, a modified cross-coupled inverter is introduced, which brings down the operating voltage to 0.55 V. Although this modified version needs larger transistor sizing and only work in a small supply voltage range, both versions of the proposed SAs have conclusively proved the robustness and the suitability of the new read scheme for applications where ultralow voltage, ultralow power, and high speed are crucial design considerations.

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