Hybrid single-electron transistor as a source of quantized electric current

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The basis of synchronous manipulation of individual electrons in solid-state devices was laid by the rise of single electronics about two decades ago[1–3]. Ultrasmall structures in a low-temperature environment form an ideal domain for addressing electrons one by one. In the so-called metrological triangle, voltage from the Josephson effect and resistance from the quantum Hall effect would be tested against current via Ohm's law for a consistency check of the fundamental constants of nature, $\hbar$ and e (ref. 4). Several attempts to create a metrological current source that would comply with the demanding criteria of extreme accuracy, high yield and implementation with not too many control parameters have been reported[5–11]. Here, we propose and prove the unexpected concept of a hybrid normal-metal–superconductor turnstile in the form of a one-island single-electron transistor with one gate, which demonstrates robust current plateaux at multiple levels of ef at frequency f.

Synchronized sources, where current I is related to frequency by $I = Nef$ and N is the integer number of electrons injected in one period, are the prime candidates for the devices to define one ampere in quantum metrology. The accuracy of these devices is based on the discreteness of the electron charge and the high accuracy of frequency determined from atomic clocks. Modern methods are replacing classical definitions of electrical quantities; voltage can be derived on the basis of the a.c. Josephson effect of superconductivity[12] and resistance by the quantum Hall effect[13,14], but one ampere still needs to be determined via the mutual force exerted by the leads carrying the current. Early proposals of current pumps for quantum metrology were based on arrays of mesoscopic metallic tunnel junctions[5,6], in which small currents could eventually be pumped at very low error rates[7]. However, these multijunction devices are hard to control and relatively slow[15]. Thus, the quest for feasible implementation with a possibility of parallel architecture for higher yield have led to alternative solutions such as surface-acoustic-wave-driven one-dimensional channels[8], superconducting devices[11,16–21] and semiconducting quantum dots[22]. These do produce large currents in the nano-ampere range but their accuracy is still limited.

Surprisingly, a simple hybrid single-electron transistor, with a small normal-metal (N) island and superconducting (S) leads, has been overlooked in this context. As demonstrated here, an SNS transistor, or alternatively an NSN transistor, see Fig. 1, presents a robust turnstile for electrons showing current plateaux at multiples of ef. We emphasize here that a one-island turnstile does not work even in principle without the hybrid design. An important feature in the present system is that hybrid tunnel junctions suppress tunnelling in an energy range determined by the gap Δ in the density of states of the superconductor, see Fig. 1d bottom inset; current through a junction vanishes as long as $|V_J| \lesssim \Delta/e$.

Figure 1a shows the simple electric configuration to operate a hybrid turnstile. A d.c. bias voltage V is applied between the source and drain of the transistor, and a voltage V_g with d.c. and a.c. components at the gate. In general, a sinusoidal a.c. gate voltage is superposed on the d.c. offset such that the total instantaneous voltage on the gate, normalized into charge in units of e, reads $n_g \equiv C_g V_g/e = n_{g0} + A_g \sin(2\pi f t)$ at frequency f. Here, C_g is the capacitance of the gate electrode to the transistor island. In a basic operation cycle of Fig. 1c, we have chosen the gate offset n_g and amplitude A_g to be $n_{g0} = A_g = 0.5$, and the bias voltage across the transistor is set at $V = \Delta/e$ to suppress tunnelling errors, as will be discussed below. The key point in the operation of the hybrid turnstile is that the charge state locks to a fixed value in any part of the operational cycle except at the moment when a desired tunnelling event occurs. This originates from the interplay of the superconducting gap in the energy spectrum and Coulomb blockade of single-electron tunnelling. It renders this structure to work as an accurate turnstile where errors can be suppressed efficiently by decreasing the temperature and by choosing the bias point properly within the superconducting gap. This locking mechanism is shown and explained in Fig. 1c for one operational cycle. On the contrary, in the biased NNN transistor with Coulomb blockade alone, non-synchronized almost frequency-independent d.c. current through the device is observed. Likewise, a corresponding fully superconducting SSS device is not favourable either, because the inevitable supercurrent of Cooper pairs induces significant leakage errors[23].

Figure 2 shows the current through the SNS turnstile under varying parameters n_{g0}, A_g and V. Figure 2c shows cross-sections of the three-dimensional plot of the type of Fig. 2a along different constant values of n_{g0} against the gate amplitude A_g. The corresponding prediction based on sequential tunnelling theory[1] is shown by the dashed lines in the same plot. The experimental data follow the theoretical prediction very closely with wide flat plateaux at $I = Nef$. The magnitude of the pumped current is robust against fluctuations in relevant parameters. It is not sensitive to the exact

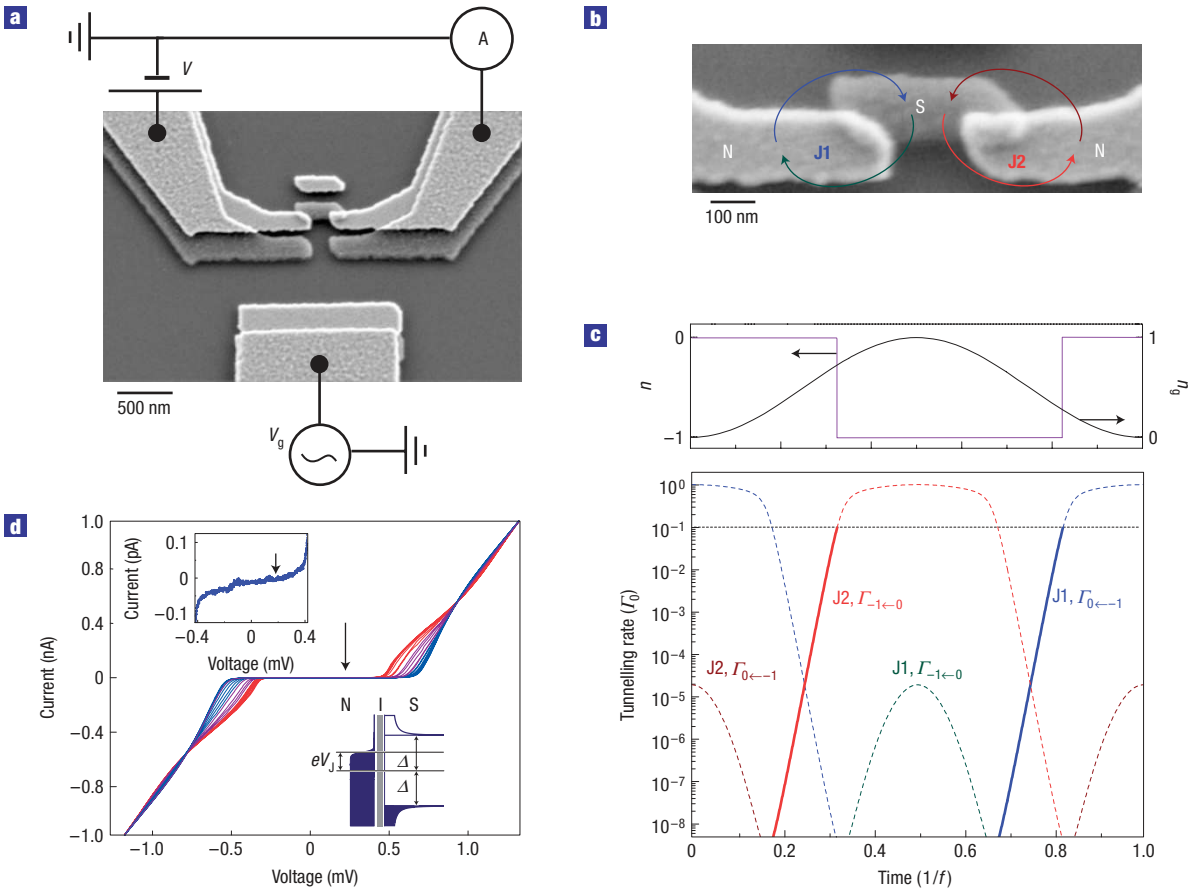

Figure 1 The hybrid turnstile and its basic characteristics. a, An electron micrograph of an NSN turnstile. It is a single-electron transistor fabricated by standard electron beam lithography. The leads are made of copper metal (N) and the island, the small grain in the centre, is superconducting aluminium (S). In the SNS turnstile, the roles of aluminium and copper are swapped, that is the leads are superconducting and the island is normal-state. The measurement configuration is added to this image: d.c. bias voltage V is applied across the transistor, and a voltage composing of d.c. and a.c. components acts on the gate electrode. **b**, A magnified image of the island, indicating notation in **c**. For an equivalent SNS device, the labels N and S are interchanged. **c**, A basic pumping cycle of the turnstile. The normalized gate voltage $n_g \equiv C_g V_g / e$, and the instantaneous charge number n on the island are shown in the top panel against time over one period. The bottom frame shows the relevant tunnelling rates, in units of $\Gamma_0 \equiv \Delta/(e^2 R_T)$ through junctions J1 (left one) and J2 (right one), respectively. Besides the dominant forward processes, the two most important backward rates are shown. The tunnelling occurs when Γ is of order frequency f. Note that when it takes place for instance through junction J2 in the charge state $n = 0$ the island transits into the $n = -1$ state, and the system stays in this state for a while because all of the tunnelling rates for the $n = -1$ state are vanishingly small right after this event. In one full cycle, one electron is transferred through the turnstile from left to right. **d**, Current–voltage (IV) characteristics measured at various values of d.c. gate voltage with no a.c. voltage applied. The separation of the extreme IV curves is a signature of the charging energy $E_C = e^2/(2C_\Sigma)$, where C_Σ is the total capacitance of the island. The arrow marks the working point in the turnstile experiments unless otherwise stated. The top inset shows a magnification of the IV within the gap region demonstrating high subgap resistance of above 10 GΩ. The lower inset shows the energy diagram for one junction biased at a voltage V_J. Normal metal is to the left of the barrier in the centre, and the superconductor to the right, with forbidden states within the energy interval 2Δ around the Fermi level.

dimensions or symmetry of the device, operational temperature, gate offset or its amplitude, or the exact form of the driving signal in general. Some of these dependencies are demonstrated in Fig. 2d based on our present measurements.

Figure 3a shows the IV curves measured for $n_{g0} \simeq A_g \simeq 0.5$ at various frequencies. The frequency dependence of the current corresponding to the first plateau in measurements of the type that were shown in Fig. 2b is plotted in Fig. 3b against ef in the frequency regime up to 80 MHz. The predicted $I = ef$ relation is followed closely within smaller than 1% deviations in absolute current throughout this range. We stress here that in the present measurement, using just a room-temperature current preamplifier, we cannot test the agreement between the prediction and the absolute value of the measured, relatively small current to a higher degree than this.

Next we discuss the choice of the operating conditions of a hybrid turnstile and the potential accuracy of this device. Within the classical model of sequential single-electron tunnelling, the bias voltage V across the turnstile is a trade-off: small bias leads to tunnelling events in the backward direction and large V to errors due to replacement of the tunnelled charge by another one tunnelling in the forward direction through the other junction. Unwanted events of the first type occur at the relative rate of $\simeq \exp(-eV/k_B T_N)$, where T_N is the temperature of the normal-metal electrodes. Errors of the second type occur at the relative rate of $\sim\exp(-(2\Delta - eV)/k_B T_N)$. The prefactor of this expression is of the order of unity in relevant cases of interest. Minimizing these errors thus yields $eV \simeq \Delta$, which is chosen as the operation point in the experiments. At this bias point, the two errors are of the order $\exp(-\Delta/k_B T_N)$. For $\Delta \simeq 200\,\mu$eV (aluminium) and $T_N < 100$ mK,

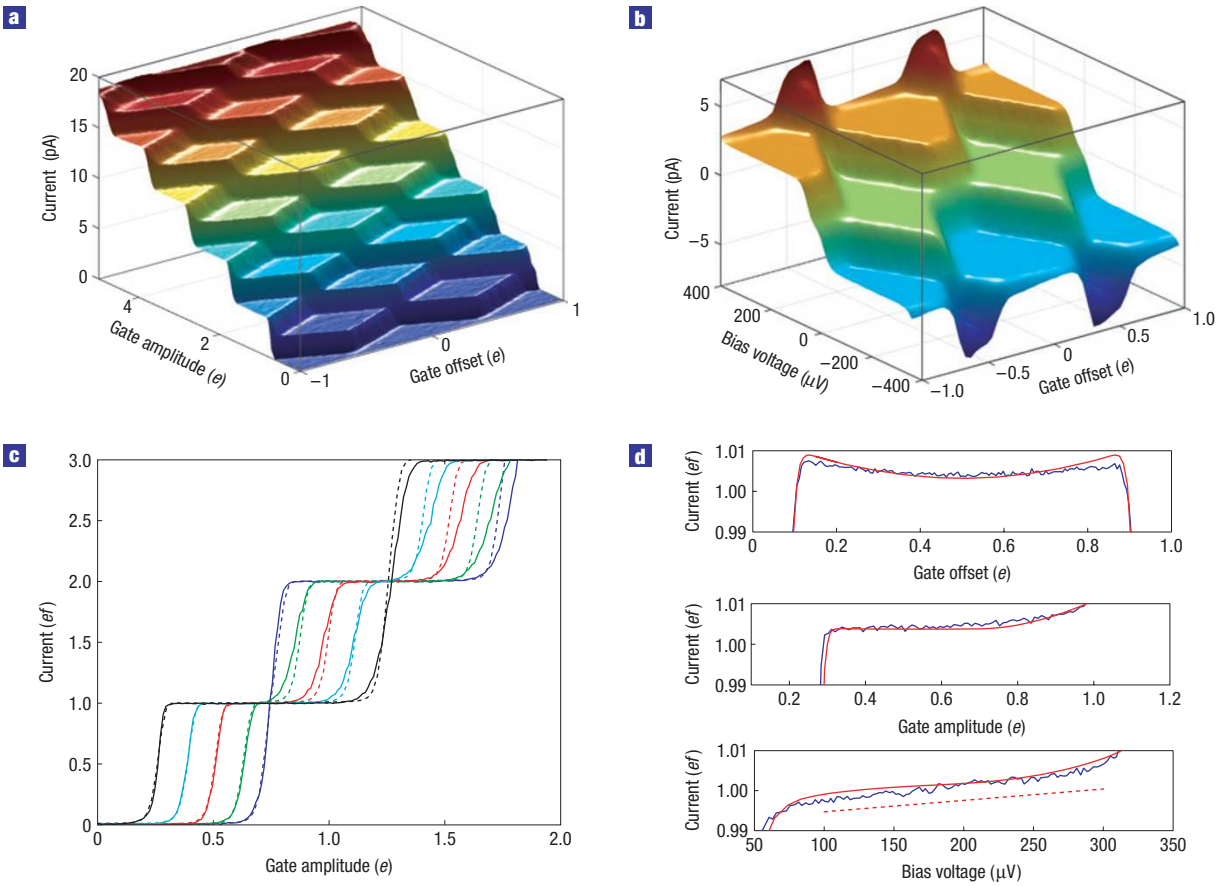

Figure 2 Measured characteristics of the SNS turnstile. **a**, Current plateaux $I = Nef$ at $f = 12.5$ MHz as a function of d.c. gate offset and a.c. gate amplitude. The diamond structure is shown up to $N = 10$ steps. **b**, The plateaux at $f = 20$ MHz as a function of the bias voltage V across the transistor up to the gap threshold of about 400 μV, see Fig. 1d. Current is shown here in a three-dimensional plot at different d.c. gate offset positions with a constant gate amplitude $A_g = 0.5$. **c**, Current at $V = 200$ μV measured at various values of d.c. gate offset and as a function of gate amplitude A_g (solid lines), $f = 20$ MHz. **d**, The $N = 1$ plateau measured at $f = 20$ MHz around the centre of each diamond as a function of d.c. gate offset, a.c. gate amplitude and bias voltage V across the turnstile, respectively, from top to bottom. The dashed lines in **c** and the red solid lines in **d** show the theoretical results according to the sequential tunnelling model. Here, we have used the parameter values $R_T = 350\,\mathrm{k\Omega}$ and $E_C/k_B = 2$ K from the d.c. IV curves (Fig. 1d), and an electron temperature of 80 mK. We further used $\Delta = 185$ μeV and subgap leakage of 2.5×10^{-4} of the asymptotic resistance. The dashed line in the bottom panel of **d** has a slope of 10 GΩ, suggesting that the measured slope here and that of the d.c. IV curve in Fig. 1d have the same origin. All of the measured currents in this letter have been multiplied by the same factor (1.004) for the best consistency with the model: this is well within the ±2% calibration accuracy of the gain of the current preamplifier used.

that is, a standard range of operation temperature, we obtain a thermal error rate of $\sim 10^{-10}$, which is sufficiently small compared with the requested $\sim 10^{-8}$ accuracy of the metrological source[4].

The analysis above neglects several types of error. High operation frequency is one source of error: it leads to missed tunnelling events and to enhanced tunnelling in the wrong direction. For charging energy $E_C \sim \Delta$, these errors are suppressed approximately as $\exp(-\Delta/2\pi f e^2 R_T)$. With typical parameters, Δ for aluminium and $R_T = 50\,\mathrm{k\Omega}$, we then request $f \ll 4$ GHz for accurate operation. Such a small value of R_T seems acceptable because of sufficiently strong suppression of co-tunnelling effects in this system as will be discussed below. With exponential suppression of errors in f, the metrological accuracy limits the frequency to ∼100 MHz for turnstiles with aluminium as the superconductor. A possible way to increase the speed of the device is to use another superconductor with a larger gap, for example, niobium. With ultrasmall junctions, to keep $E_C \sim \Delta$, which is another criterion to satisfy in order not to miss any tunnelling events at the chosen bias point, we would be able to increase the frequency and thus the synchronized current. This is an attractive yet unexplored possibility. Further improvement, about a factor of three increase in frequency, could be achieved by shaping the a.c. gate voltage to have a rectangular waveform.

Another source of potential errors is the co-tunnelling[24], that is, higher-order quantum tunnelling processes, which limit the use of short arrays in normal-metal-based devices[25]. In an SNS turnstile, the lowest-order quasiparticle co-tunnelling errors are, however, suppressed ideally to zero within the superconducting gap. Another process of the same order that is not suppressed by the superconducting gap is the tunnelling of Cooper pairs, also called Andreev reflection. In junctions without pinholes in the barriers, the rate Γ_A of this tunnelling should be quite small, $\Gamma_A/\Gamma_0 \sim \hbar/\mathcal{N} e^2 R_T$, where $\Gamma_0 \equiv \Delta/(e^2 R_T)$ and the effective number of the transport modes in the junction of area A can be estimated to be $\mathcal{N}/A \simeq 10^6 - 10^7\,\mu\mathrm{m}^2$ (refs 26–28). If the charging energy is large, $E_C > \Delta$, it suppresses direct tunnelling of Cooper pairs. Analysis shows that the lowest-order process that limits the accuracy of the hybrid turnstiles with ideal superconducting

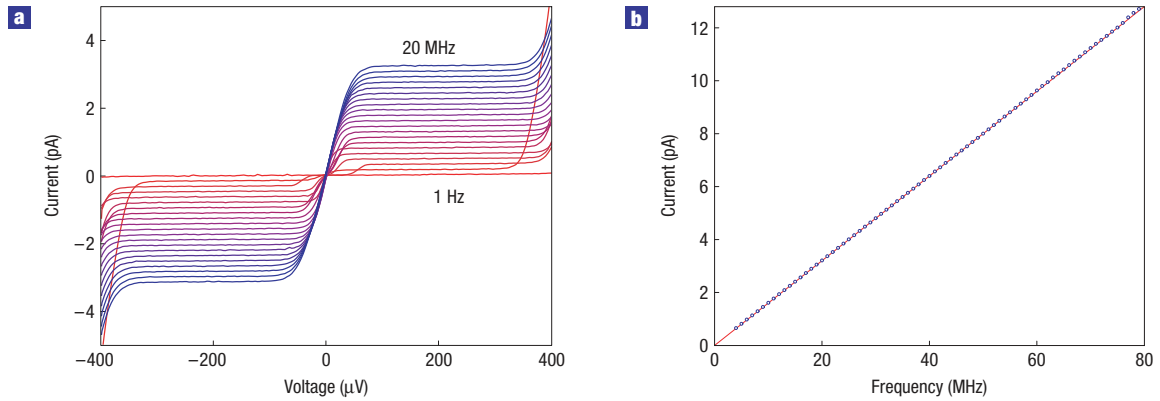

Figure 3 The frequency dependence of the SNS turnstile operation. a, *IV* curves measured at different frequencies ranging from 0 to 20 MHz, at gate settings corresponding to the centre of the first ($N = 1$) current plateau. **b**, The measured current at the centre of the $N = 1$ plateau at the fixed bias of $V = 200\,\mu$V. Linear dependence up to 80 MHz corresponding to $I \simeq 13$ pA can be seen.

electrodes is then the co-tunnelling of one electron and one Cooper pair, the rate Γ_{CPE} of which can be estimated roughly as $\Gamma_{\mathrm{CPE}}/\Gamma_0 \sim (1/\mathcal{N})(\hbar/e^2R_{\mathrm{T}})^2$. These processes can be suppressed efficiently by a proper choice of device parameters.

Subgap leakage, due, for instance, to non-zero density of quasiparticle states within the gap, introduces a material- and fabrication-specific source of errors into our system. This effect is demonstrated by the non-vanishing slope of the IV curve in the top inset of Fig. 1d and by an equal slope in the bias dependence of the bottom panel in Fig. 2d showing the current on the first plateau. The parabolic gate offset dependence around $n_{\mathrm{g0}} = 0.5$ is likewise caused by leakage. Our estimates show that as far as co-tunnelling is concerned, such errors are smaller than those measured in the present devices. For sequential tunnelling, subgap leakage causes a substantial extra contribution to the current, of the order of 10^{-3} in the present device. With high-quality tunnel junctions, possibly by an improved fabrication process, its influence can be suppressed further. Furthermore, the separation of the current plateaux, with only one bias polarity, is in principle not sensitive to this effect, unlike the absolute value of current on a single plateau. Yet the subgap leakage is the main issue to be solved to realize a metrologically compatible turnstile. We would also like to point out that a series connection of a few SN junctions would present an improved version of a multijunction electron pump[6,7] in terms of leakage and co-tunnelling errors, because this device can be operated without external bias voltage.

The charge transport in these systems is associated with non-trivial heat flux: on the basis of the same strategy as discussed here, a single-electron refrigerator can be realized[29]. In this device the superconductor is always heated, but under proper bias conditions heat flows out from the normal metal. Therefore, in a single-island realization, an SNS configuration is more favourable, as compared with the NSN turnstile. With quite realistic parameters it is possible to refrigerate the small, thermally well-isolated N island of an SNS turnstile substantially, and hence the error rates can be further suppressed. For example, with the parameters of the present sample but in the SNS configuration, the island would cool from 100 mK down to 70 mK on the first current plateau when pumping at 20 MHz frequency. The source and drain leads can be thermalized close to the bath temperature by a proper choice of geometry and materials. Another difference between the SNS and NSN structures is the role of the parity effect in the NSN turnstile, in which the pumping cycle leads to unavoidable excitation of at least one odd quasiparticle in the central S electrode, limiting the ultimate turnstile accuracy. Such a limitation should be absent in the SNS case.

One of the key advantages of the single-island turnstile, as compared with multi-island pumps, is that the influence of the background charges[30] can be compensated by adjusting just a single d.c. gate voltage. Therefore, the level of the current can be increased by a relatively straightforward parallelization of several turnstiles. If an enhancement in current by, for example, an order of magnitude is necessary, the d.c.-gate settings of each of the ten turnstiles can be adjusted individually, whereafter their currents can be combined. The whole device can then be operated with common-to-all d.c. bias and a.c. gate drive.

METHODS

Several hybrid turnstiles with aluminium as the superconductor, copper as the normal metal and aluminium oxide as the tunnel barrier in between were fabricated by standard electron beam lithography. Both the aluminium and the copper films were 50 nm thick. The charging energy of the aluminium island is $E_{\mathrm{C}}/k_{\mathrm{B}} \simeq 2$ K. The sum of the tunnel resistances of the two junctions is 700 kΩ, that is, 350 kΩ per junction on average. The current–voltage (IV) characteristics of the transistor are shown in Fig. 1d at various values of the d.c. gate voltage and with no a.c. gate voltage applied. The superconduct gap suppresses the current strongly in the bias region $|V| \lesssim 0.4$ mV. Outside this region, the typical gate modulation pattern shows up[2]. The charging energy of the device was determined on the basis of the envelopes of these IV curves. The turnstile experiments were carried out by voltage biasing the transistor at $V \simeq \Delta/e$, highlighted by an arrow in Fig. 1d.

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CORRIGENDUM

Hybrid single-electron transistor as a source of quantized electric current

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In the version of this Letter originally published, discussions of SNS and NSN transistors were reversed in the captions of Figs 1–3, with concomitant errors in the main text where those figures were referred to. The following text should have been in the caption of Fig. 1: 'In the SNS turnstile, the roles of aluminium and copper are swapped, that is the leads are superconducting and the island is normal-state.' The sentence at the top of the right column on page 123 proclaiming the absence of the parity effect in the measured SNS transistor should not have been included as the parity effect can only manifest in an NSN transistor. These errors have been corrected in the online versions of the Letter.