

# IC Defect Sensitivity for Footprint-Type Spot Defects

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**Abstract**—While it is important to exhaustively verify IC designs for their functional performance, it is equally important to verify their robustness against spot defects, that is, to foresee what will happen to the design when it is exposed to defect conditions in a real manufacturing environment. One such verification is done by extracting the layout sites sensitive to defects. These sites are the places where defects can induce a functional failure of the design. Initial attempts to perform this verification task were based on a “critical area extraction” of one layer at a time. However, this extraction neglects the electrical significance of interrelationships between layers, as could be the case with transistors, vias, etc. In this paper we present a novel method to construct deterministically multilayer critical areas. These critical areas are established on the theoretical basis of defect semantics and on the new concept of “susceptible sites.” Based on these foundations, we developed a system comprising several algorithms which in principle maintain simultaneously as many scan lines as the number of layers, in such a way that it is possible to keep track of the vertical and horizontal effects of defects. The paper also presents experimental timing results and a case study for diagnosing defect-fault information on an IC.

## I. INTRODUCTION

WITH the advent of smaller resolution features and the emergence of new technologies, manufacturing yield becomes a more important issue [25], [42]. The economic viability of a new product is directly related to yield and it is a difficult task to carry out. Spot defects have for a long time been recognized as the main impediment to the successful manufacture of IC's [11], [19], [20], [24], [27], [38], [46]. Consequently, a search for new methods to improve yield, and their automation, has received a high priority [5], [45]. These new methods consider the IC not as a “black box” but as the union of geometrical features that are likely to be affected by defect mechanisms [21], [22].

IC sensitivity to spot defects can better be studied by extracting *critical areas* from layouts. Roughly speaking, a *critical point* in the layout is a point such that if spot defects are centered there a malfunction in the respective

circuit arises. Critical areas are open connected sets of critical points. They naturally are a function of the layout geometry and of the defect size involved. The design's *defect sensitivity* is the ratio of the critical area for a defect size to the total layout area.

Initially, critical areas were applied only to yield prediction but recently several other applications have emerged [6], [12], [29], [36]. A typical example of these other applications is combining the defect sensitivity with a defect size distribution to rank the failure probability of the electrical nodes of a circuit. If a designer had to improve the robustness of a cell library to guarantee a certain yield, this ranking could be used as a guideline for corrective actions. Another example is to rank the probability of occurrence of faults such that a realistic and weighted fault list can be obtained to refine the quality of a test vector set.

The original concept of critical areas appeared in the late 1960's at IBM's Watson Research Center, in Yorktown Heights, NY, where initial attempts were made to evaluate spot defects in FET memories [41]. It was not until 1983 that this concept was first presented in the literature [39]. In the same year a simple geometrical method to extract critical areas from complex layouts was described [26]. Since then, the role of critical areas has been studied in greater detail [7]–[9], [14], [16], [40]. However, most of the analyses have considered very simple layouts, in particular, cases addressing only single-layer conductors and overlapped areas among layers. This comes from the fact that the computation of critical areas is not a trivial task [24]. An attempt to extend the concept of critical areas from single to multiple layers taking into account the electrical significance of the layers was presented in 1989 [31].

A previous approach to extract critical areas was based on a Monte Carlo statistical simulation [35] which essentially consists in throwing dots on the layout and then analyzing their effect. The advantage of this method is that it can find the critical areas in multiple layers; however the big disadvantage is that it is a very large CPU time consumer and consequently unsuitable for analyzing large layouts. A way to overcome this problem was the use of virtual [20] and equivalent layouts [5] that are statistical images of the real layout. They are built as a set of parallel patterns that have the statistical width, length, and space of the patterns. By using these approaches it is possible to analyze large layouts although they have certain shortcomings. For instance, the total critical area computed is an approximation of the actual value; further-

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more, the critical areas cannot be localized in the real layout. Other approaches extract a set of patterns which are likely to fail as a consequence of a determined defect size [10]. However, the area of the patterns or the area between patterns is not the correct critical area and the results tend also to be inaccurate estimations. Recently, a deterministic construction which provides accurate results as well as a visual inspection of the critical areas was presented [32], [33].

Except for the Monte Carlo method, the approaches mentioned above are only capable of extracting critical areas in single layers. However, modeling the patterns only as conductors can be inaccurate in predicting the probability of failure of the circuit. This way of modeling neglects the electrical significance of interrelationships between different layers, as is the case with transistors, and also neglects those defects which do not cause either a short or a break. However if the defect falls in the poly-diffusion area of a transistor it can be fatal even if it does not totally break the geometrical pattern. Although this type of fault is a parametric one, it can introduce glitches which in turn can affect the functional behavior of a design. It is thus not sufficient to extract single-layer critical areas if either an accurate yield prediction or a realistic layout to fault extraction is desired.

We present a system capable of determining and computing critical areas in multiple layers. The extracted critical areas are a function of the geometrical patterns in the layers, of their electrical significance, of their relationship to patterns in the same or other layers, and, of course, of the defect size. In contrast to statistical Monte Carlo simulations, our method is a deterministic construction based on the scan-line principle. This approach results in savings of computational time, especially for large layouts and defect sizes of large magnitudes. Another important advantage of a deterministic method is that defect statistics are not required in the construction of critical areas. With this clear separation of critical areas from defect statistics, defect-sensitivity results are influenced by neither defect size distribution nor defect density.

The system presented in this paper is technology and defect independent; that is, defect mechanisms are not embedded in the programming code. Rather, they are described by the user by appropriately selecting defect conditions that may in turn affect the electrical components of the technology. The system supplies three kinds of results, namely, on-layout visualization of critical areas, computation of critical areas per defect mechanism, and computation of critical areas per individual fault and node.

The organization of the paper is as follows. Section II presents a formal semantic model for microelectronic technologies and process-induced defects. This semantic model is broad enough that i) any technology can be described by means of multivalued state clauses, where a state clause is used to characterize a type of circuit component; ii) defects can also be described by multivalued state clauses, and odd shape defects can be modeled by using the concepts introduced in these semantics; and iii)

the formalism provides a solid mathematical platform for the extraction of multilayer critical areas. Section III presents a theoretical formulation of critical areas for multiple layers. The algorithms of our approach are discussed in Section IV, and two direct applications, namely defect sensitivity per defect mechanism, and IC defect fault analysis, are shown in Section V.

## II. DEFECT SEMANTICS

### A. Microelectronic Technology

A microelectronic technology,  $\mathcal{T} = \{t_k | k = 1, 2, \dots, N_{\text{tech}}\}$ , is an ordered set of process steps which are concerned with changes in matter no more than a few microns above or below the surface of a *carrier*. The carrier is usually referred to as a wafer. Basic process steps in the manufacturing of an IC are [1], [15]:

- 1) oxide growth
- 2) material deposition
- 3) photoresist application
- 4) mask exposure
- 5) developing
- 6) etching
- 7) wash or strip
- 8) photoresist removal
- 9) implantation.

The goal of these steps is to transform an electrical circuit design into an operable device, i.e., the integrated circuit.

Geometrically, an IC can be seen as part of a 3-D Euclidean space with ‘‘lateral’’ coordinates  $(x, y)$  and vertical coordinate  $z$ . In the  $z$  direction a partition into intervals by fixing points on the  $z$  axis,  $z_i$ ,  $i = 1, 2, \dots, N_{\text{layer}}$ , is introduced. These  $z$  points define ‘‘matters’’ as open connected point sets as follows:

$$L_i = \{(x, y, z) \in E^3 | z_{i-1} < z < z_i\}$$

$$L_0 = \{(x, y, z) \in E^3 | -\infty < z < z_0\}$$

$$L_\infty = \{(x, y, z) \in E^3 | z_N < z < \infty\}.$$

$L_0$  is actually the *substrate* with its background doping, whereas  $L_\infty$  is established by the (electrically passive) *air* on the top of the IC. Between these is a set of matters such that each different matter has unique electrical properties. By matter is meant the physical IC materials, such as thick oxide, thin oxide, metal, and polysilicon. Such an arrangement of matter in *layers* is referred to as the silicon layer structure. The set of layers is denoted as  $\mathcal{L} = \{L_i | i = 1, 2, \dots, N_{\text{layer}}\}$ , and the set of matters as  $\mathcal{U} = \{u_k | k = 1, 2, \dots, N_{\text{matter}}\}$ .

Each layer is shaped by a series of process steps such as oxidation, diffusion, and etching. After the ‘‘shaping process’’ some portions of matter disappear and some portions remain. The remaining connected point sets, henceforth called *patterns*, divide the layer in two disjoint regions: *active* and *inactive*. The active region set  $\mathcal{A}_i = \bigcup_{k \geq 1} a_k$ ,  $a_k \subset L_i$ , is the set of patterns to be retained after the shaping process. These patterns are denoted as active

patterns. The inactive region set,  $\bar{\mathcal{A}}_i = L_i - \mathcal{A}_i$ , is the set of empty spaces among active patterns and corresponds to the layer portions that disappear after the shaping process. These empty spaces are denoted as inactive patterns. Generalizing, a shaped layer  $L_i \in \mathcal{L}$  has an *image* given by  $\mathcal{A}_i$ .

Within one layer the inactive patterns may be partially occupied by other matters. For instance, at process step  $t_i$  one may encounter active patterns of thick oxide matter in layer  $L_i$ . A few processing steps further, the inactive patterns of  $L_i$  may now be filled with metal. Thus, it is possible to define a set in terms of an enumerated type of distinct matters contained in  $L_i$  as  $U_i \subset \mathcal{U}$ . For this particular example  $U_i = \{\text{thick oxide, metal}\}$ . Assume that the point  $(x, y, \eta)$ ,  $z_{i-1} < \eta < z_i$  is element of an inactive pattern. Fixing  $z = \eta$  defines a two-dimensional Euclidean space, which in the case of  $z_{i-1} < \eta < z_i$  will be denoted by  $L_i(x, y)$ . Then, for any point  $(x, y) \in E^2$  a function  $W_i(x, y): L_i(x, y) \rightarrow U_i$  is defined, which in fact assigns a value from  $U_i$  to any pair of coordinates. This value is called the state of the layer at  $(x, y)$  and  $U_i$  the state set.

From the above it follows that, given the set of layers  $\mathcal{L}$ , there is an associated set of state sets  $U = \{U_1, U_2, \dots, U_{\text{layer}}\}$ . Now establish the product set of all layers by letting  $L = (L_1, L_2, \dots, L_{N_{\text{layer}}})$  be an  $|N_{\text{layer}}|$ -dimensional vector. The product set  $U = (U_1, U_2, \dots, U_{N_{\text{layer}}})$  is analogously defined. Logically  $W = (W_1, W_2, \dots, W_{N_{\text{layer}}})$  becomes a vector function such that it is possible to write  $W(x, y): L(x, y) \rightarrow U$ .

Consider an NMOS process. Assume the silicon layer structure indicated in Fig. 1. Essentially five layers,  $L_1, L_2, L_3, L_4$ , and  $L_5$ , and five state sets,  $U_1 = (\text{FOX, DDS, DE}), U_2 = (\text{OX, THOX, ME}), U_3 = (\text{OX, POLY, ME}), U_4 = (\text{OX, ME}),$  and  $U_5 = (\text{INS})$ , are defined. For coordinate  $x_1$  (with  $y$  undefined) one can obtain the state vector  $W(x_1) = (\text{DDS, ME, ME, ME, INS})$ . For coordinate  $x_2$  (with  $y$  undefined) the state vector  $W(x_2) = (\text{DE, THOX, POLY, OX, INS})$  is obtained as well.

Obviously the state characterization of silicon layer structures can be applied to identify electrical components by multivalued logic clauses. Adopting  $\mathbf{x}$  as a don't care notation, consider for instance the clause  $\omega(x, y) = (\text{DE, THOX, POLY, } \mathbf{x}, \mathbf{x})$  true for some point in  $(x, y) \in E^2$ . This clause describes a point of an active gate area of an NMOS transistor. The clause  $\omega(x, y) = (\text{DDS, ME} \vee \text{OX, OX, ME} \vee \text{INS, } \mathbf{x})$  indicates that  $(x, y)$  belongs to a source or drain region. These clauses are denoted as state clauses. A technology can be characterized by a set of state clauses  $\Sigma_{\text{tech}} = \{\omega(k) | k \geq 1\}$ . Each of the state clauses identifies a silicon layer structure characterizing a constituent of a set of electrical components. To be able to link the silicon layer structure within a given technology  $\Sigma_{\text{tech}}$  to a circuit schematic, there must be a correspondence between the elements of  $\Sigma_{\text{tech}}$  and the set of constituents of the circuit schematic, say  $\Psi$ .

Assume  $\omega \in \Sigma_{\text{tech}}$ . Consider a point  $(x, y)$  such that  $W(x, y) = \omega$ . Assume now that this point is an inner point of a

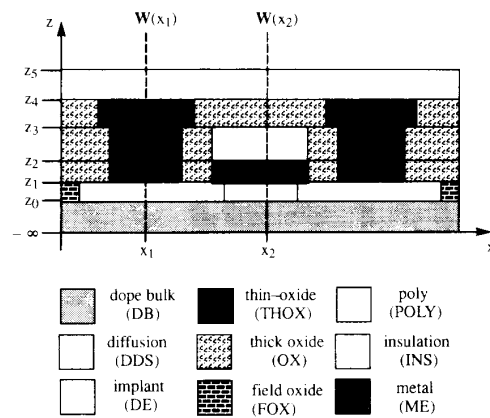


Fig. 1. A silicon layer structure.

closed connected maximal set  $R$  with the property that for any  $(\alpha, \beta) \in R$  the state function  $W(\alpha, \beta) = \omega$  holds. Then  $R(\omega)$  is called a hard structure. Also, for later use, let us denote by  $R(\omega) | L_i$  the partial hard structure, which is obtained from the hard structure  $R(\omega)$  by restricting its argument to the layer  $L_i$ . After elimination of the  $z$  dimension, the IC is considered as a connected rectangular subset of the two-dimensional Euclidean space. There may be many hard structures  $R_r(\omega)$ ,  $r \geq 1$ , on such a chip.

The state clause  $\omega$  characterizes the circuit constituent  $\psi \in \Psi$  (or rather the type of circuit component in question); in addition a hard structure  $R_r(\omega)$  supplies all the geometrical information that completes the description of an instance of the respective circuit constituent. In other words, any  $R_r(\omega)$  corresponds to a circuit element. By circuit element is meant a drain region, a gate region, a via, etc., as opposed to the traditional concept of circuit elements such as resistors, capacitors, and transistors.

The way in which the patterns in the layers are determined is specified by an *IC artwork*. An IC artwork represents the layout of the circuit design to be mapped into hard structures by the processing steps. Formally, an IC artwork is a vector of masks  $M = (M_1, M_2, \dots, M_{N_{\text{mask}}})$  where each mask is defined as a two-dimensional Euclidean space, i.e.,  $M_m = \{(x, y) \in E^2\}$ . Let us denote  $\mathcal{M} = \{M_m | m = 1, 2, \dots, N_{\text{mask}}\}$  as the set of masks.

Within a mask, a connected point set  $o$  is bounded by a finite set of line segments such that every segment extreme is shared by exactly two edges and no subset of edges has the same property. These connected point sets, henceforth called fields, divide the mask in two disjoint regions, *dark* and *light*. The set dark field,  $\mathcal{O} = \{o_k | k \geq 1\}$  contains the regions to be mapped in the silicon layer structure if the lithographic processing step uses positive image projection. On the other hand, if negative image projection is employed, the regions of the set light field,  $\bar{\mathcal{O}}$ , are mapped into the silicon layer structure. Thus, one can create a silicon layer structure by placing the masks on top of each other, correctly aligned to establish a *mask stack* to be processed in sequence.

Very much as in the case of actual silicon layer structures, state clauses for any point  $(x, y)$  of a mask stack can be defined. Any mask of the mask stack may at any point be either dark or light, establishing essentially two sets per mask. In addition let us use  $\mathbf{x}$  as a don't care notion. If  $\Sigma_{\text{artwork}} = \{\mu(k) | k \geq 1\}$  is denoted as the set of state clauses associated with the IC artwork, then with any point  $(x, y) \in E^2$  there exists a Boolean cube  $\mathbf{M}(x, y)$  as a vector of "1," "0," and  $\mathbf{x}$  entries, where "1" stands for dark and "0" indicates light (in the case of positive image projection). As in the case of technology state clauses, these new clauses identify constituents of circuits as well.

Let  $\Omega$  be the subset of all state clauses that identifies the set of constituents of a circuit schematic. Assume some state clause  $\mu \in \Omega$ . Further assume a point  $(x, y) \in E^2$  such that  $\mathbf{M}(x, y) = \mu$ . In general  $\mu$  will be in a connected set of points where one can identify a maximal connected set  $Q(\mu)$  corresponding to one of the constituents from the set  $\Omega$ . Such a set  $Q(\mu)$  will be called a soft structure.

In order to obtain consistency among the circuit schematic, the mask stack, and the silicon structure layers a correspondence between the set of hard structures  $\Sigma_{\text{tech}}$ , the set of soft structures  $\Sigma_{\text{artwork}}$ , and the set of circuit constituents  $\Psi$  must be established. On one hand, this consistency is established by proper definitions of the set  $\Psi$  and the sets  $\Sigma_{\text{tech}}$  and  $\Sigma_{\text{artwork}}$ . The relation between  $\Sigma_{\text{tech}}$  and  $\Sigma_{\text{artwork}}$  is induced of course by a proper interpretation of the effects of the processing steps  $t_i \in \mathcal{T}$ .

### B. Modeling of Process Induced Spot Defects and Faults

Spot defects are local disturbances of the silicon layer structure caused by process variabilities, dust particles, and other contaminations of the fabrication equipment. The general assumption is that spot defects are in essence random phenomena in lithographic processing steps, occurring with a certain stochastic frequency and size and a certain stochastic spatial distribution on the wafers. These defect statistics are obtained from data gathered from special test monitors [28].

The way in which individual process steps are executed is of critical importance to the outcome of the IC. Each of these steps has its own deviations or disturbances from the ideal process which can generate physical changes in the structure of the IC and thus create defects. Therefore, not all defects are due to lithographic process steps. Some derive from process variability such as incomplete step coverages [23], and others from human and equipment contaminations [3], [17], [18], [37], [44].

Although in reality spot defects are three-dimensional objects, the majority of defects found in manufacturing lines have predominantly two-dimensional effects. Hence, spot defects have often been modeled as local disturbances of one layer in the form of small round spots of excess or missing material [19], [20]. The round shape defect model is because by a strange quirk, awkward

shapes of radius  $r'$  thrown randomly onto a wafer can be approximated by a circle of some different smaller radius  $r$ . Furthermore this shape has a solid core with a fuzzy edge to it.

The spot defect semantic model presented in this section is meant to be expressive enough to cover types of substantially more complex character. Defects may hit any combination of layers and on any layer they may be of any shape, and in extremely complex shapes the model may become difficult to handle. An example of an odd defect shape is shown in Fig. 2. This defect cannot be modeled as a square, a circle, or a rectangle. Statistics for this last kind of defect can be obtained from special-purpose defect monitors which can screen different shapes. For this particular example the odd shape is discovered if when on applying an electrical potential across the patterns, the electrical potential is zero only across patterns A, B, and C. The objective of these monitors is, however, to resemble as closely as possible the geometrical features of actual products in order to foresee possible defects in the real production of the IC [4], [30].

Often enough, defects reproduce the silicon layer structure of a hard structure yet cause a deviation of the shape of such structure. These deviations are denoted as failure primitives. Some basic failure primitives are bridges between patterns, broken patterns, the appearance of undesired layers in a silicon layer structure, etc. The impact of a defect on the image of a layer is determined by the effect that the defect has in the functional behavior of the IC; this effect is called a fault. A *fault model*  $\mathcal{F}$  maps the set of altered hard structures,  $R_{\text{def}}$ , onto the fault class  $F$ ,  $\mathcal{F}: R_{\text{def}} \rightarrow F$ . The range of  $\mathcal{F}$  is the set of fault types, that is, equivalent classes of faults including an empty class referring to a fault-free state.

The empty fault class has as its domain the set of hard structures with the property that the IC functional behavior is unaltered. This class of hard structures is insensitive to a given shape deviation; therefore affecting defects of this kind are denoted as benevolent defects. On the other hand, those defects placed in hard structures which are assigned to nonempty fault classes are denoted as catastrophic defects.

Defect mechanisms for spot defects in hard structures can be classified as *protrusions*, *intrusions*, or *isolated spots*. A protrusion defect,  $d^p$ , in some layer  $L_i$  is an undesired active pattern defined as a connected set of points  $(x, y, z)$  such that at least one such point intersects some active pattern(s) in  $L_i$ . An intrusion defect,  $d^i$ , in some structure layer  $L_i$  is an undesired inactive pattern defined as a connected set of points intersecting some active pattern(s) of  $L_i$ . An isolated spot defect,  $d^s$ , in some structure layer  $L_i$  is a connected set of points such that no point of  $d^s$  intersects an active pattern of  $L_i$ . These defect mechanisms are illustrated in Fig. 3.

Protrusion and intrusion defects generated during process step  $t_i$  affect active patterns at the same layer where they occur, and may also have an impact on active patterns at different layers processed at some  $t_j, j \neq i$ . Iso-

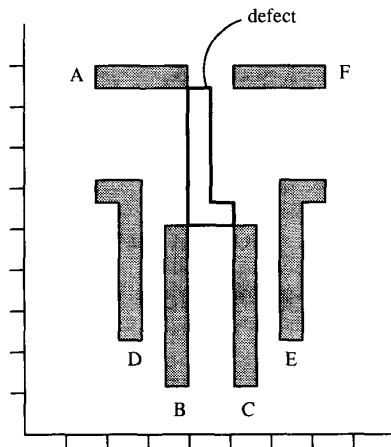


Fig. 2. An odd defect shape.

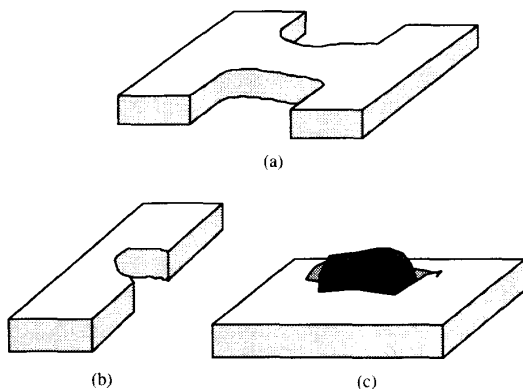


Fig. 3. Defect mechanisms. (a) Protrusion defect. (b) Intrusion defect. (c) Isolated spot defect.

lated spot defects do not affect active patterns in the layer where they originated but may affect active patterns in different layers.

The notation of subsection II-A allows us to define defect mechanisms as an additional set of multivalued state clauses. It may be necessary to extend the set of values for the various coordinates of  $\Omega$ . For instance, an isolated spot defect in the thin oxide layer of an NMOS transistor active gate area most probably will imply the presence of polysilicon in the respective layer, which in a correct structure would not appear. The defect-free state clause, in a four-layer structure, may be  $\omega = (\mathbf{x}, \text{THOX}, \text{POLY}, \text{OX})$  and the presence of the isolated spot would be indicated by some clause, say,  $\omega_{\text{defect}} = (\mathbf{x}, \text{POLY}, \mathbf{x}, \mathbf{x})$ . The shape of the defect would be captured by using the concept of a hard structure.

To consider another example, assume the state clause for the presence of just metal in a four-layer structure to be  $\omega = (\mathbf{x}, \mathbf{x}, \mathbf{x}, \text{ME})$ . Consider two hard structures,  $R_1(\omega)$  and  $R_2(\omega)$ , identifying two different wiring trees in the metal layer. The state clause for a metal spot defect  $\delta$  is of course equal to  $\omega$ . Assume some hard structure  $D(\delta)$

actually modeling the defect. Then if  $R_1(\omega) \cap D(\delta) \neq \emptyset \wedge R_2(\omega) \cap D(\delta) = \emptyset$ ,  $D(\delta)$  acts as a protrusion of  $R_1(\omega)$  if  $D(\delta) - (R_1(\omega) \cap D(\delta)) \neq \emptyset$ ; otherwise  $\delta$  is not a defect because it is actually contained in the metal wire. If, however,  $R_1(\omega) \cap D(\delta) \neq \emptyset \wedge R_2(\omega) \cap D(\delta) \neq \emptyset$ , then the whole point set  $R_1(\omega) \cup D(\delta) \cup R_2(\omega)$  shows a bridge between the two hard structures.

### III. THEORETICAL FOUNDATION OF CRITICAL AREAS

Several defect-sensitivity models can be employed to classify the presence of defects on single or multiple layers inducing single or multiple faults. This classification comprises essentially two categories, *sequential class* and *concurrent class*. The *sequential class* deals with defects causing only one type of failure primitive, while the *concurrent class* deals with defects causing more than one distinct failure primitive at a time. For instance, a spot defect can introduce a bridge and a cut simultaneously.

Both sequential and concurrent classes classify the effect of defects on silicon layer structures, under these two classes it is also possible to classify the nature of defects. That is, whether one or more defects are modeled on one or more layers at the same time. This classification to the nature of defects yields four categories,

- SDSL (single defect, single layer): One defect at a time is modeled in one layer of the silicon layer structure.
- SDML (single defect, multiple layer): Defects are placed per layer, one at a time, and their isolated effect through the entire silicon layer structure is analyzed.
- MDSL (multiple defect, single layer): The simultaneous effect of more than one defect, placed on one layer and possibly occurring at the same place, is modeled through the whole silicon layer structure.
- MDML (multiple defect, multiple layer): The simultaneous effect of more than one defect, placed on more than one layer and possibly occurring at the same place, is modeled through the whole silicon layer structure.

The model to be developed in this section is based on a sequential SDML approach. Defects will be modeled as square objects. This approximation is sufficiently correct and it can be shown that it implies simple and fast algorithms. Through the course of this work only Manhattan layout styles will be assumed.

Before going into detail, definitions that will be used frequently through this section will be introduced first. Let  $(pos(\alpha); l(\alpha), r(\alpha))$  and  $(pos(\beta); l(\beta), r(\beta))$  be two horizontal line segments,  $\alpha$  and  $\beta$ , with ordinate  $pos$  having  $l$  and  $r$  as the left and right abscissas. Both line segments,  $\alpha$  and  $\beta$ , are *comparable* at abscissa  $x$  if there exists a vertical line that intersects them. The relation *above at  $x$*  is defined as follows:  $\alpha$  above  $\beta$  at  $x$  if  $\alpha$  and  $\beta$  are comparable at  $x$  and the intersection of  $\alpha$  with the vertical line lies above the intersection of  $\beta$  with that line [34].

Following the same reasoning it is possible to state that  $\beta$  is below  $\alpha$ . Two more functions are defined,  $x(p)$  and  $y(p)$ , which return the  $x$  and  $y$  coordinates of a point  $p$ , respectively.

The definitions to follow are for horizontal line segments. Analogous definitions can be inferred for vertical line segments.

*A. Susceptible Sites*

Susceptible sites are subsets of active and inactive patterns which provide defect susceptibility information of sections of hard structures where a particular defect mechanism can be meaningful. For the case illustrated in Fig. 4, the space between the two poly patterns is a susceptible site for protrusion defects of poly, but the spaces between the metal and poly patterns are not susceptible sites for protrusion defects of metal; nor are they for protrusion defects of poly. Analogously, the poly patterns are susceptible sites for intrusion defects of poly but not for defects of metal.

Assume three closed connected point sets,  $A$ ,  $B$ , and  $C$ , as shown in Fig. 5(a). Let  $\alpha_1, \alpha_2, \alpha_3$ , and  $\alpha_4$  be four horizontal line segments of  $A$ . And let  $\beta_1$  and  $\beta_2$ , and  $\gamma_1$  and  $\gamma_2$  be the horizontal line segments of  $B$  and  $C$ , respectively. Take any two comparable line segments of the same connected point set, i.e.,  $\alpha_1$  and  $\alpha_3$ . Then, in Fig. 5(b) the open rectangle  $S_1$  ( $\alpha_1, \alpha_3$ ) with corner points ( $s_1, s_2$ ) is called a vertical internal lateral susceptible site, where

$$\begin{cases} s_1 = (\max(l(\alpha_3), l(\alpha_1)), \min(pos(\alpha_3), pos(\alpha_1))) \\ s_2 = (\min(r(\alpha_3), r(\alpha_1)), \max(pos(\alpha_3), pos(\alpha_1))) \end{cases} \quad (1)$$

Take now any two noncomparable line segments of the same connected point set such that the interior of the point set lies above one of the line segments and below the other one, i.e.,  $\alpha_2$  and  $\alpha_3$ . Then, in Fig. 5(b) the open rectangle  $S_4$  ( $\alpha_2, \alpha_3$ ) with corner points ( $r_1, r_2$ ) is called an internal corner susceptible site, where

$$\begin{cases} r_1 = (\min(r(\alpha_3), r(\alpha_2)), \min(pos(\alpha_3), pos(\alpha_2))) \\ r_2 = (\max(l(\alpha_3), l(\alpha_2)), \max(pos(\alpha_3), pos(\alpha_2))) \end{cases} \quad (2)$$

Similarly, two kinds of susceptible sites are identified between different connected point sets. However, these sites are defined as a function of their associated internal ones. Take two susceptible sites such that their line segments are comparable, for instance  $S_1 = (s_1, s_2)$  and  $S_2 = (s'_1, s'_2)$  in Fig. 5(b). Then, in the same figure, the open rectangle  $E_1$  ( $S_1, S_2$ ) with corner points ( $t_1, t_2$ ) is called a vertical external lateral susceptible site, where

$$\begin{cases} t_1 = (\max(x(s_1), x(s'_1)), \min(y(s_2), y(s'_2))) \\ t_2 = (\min(x(s_2), x(s'_2)), \max(y(s_1), y(s'_1))) \end{cases} \quad (3)$$

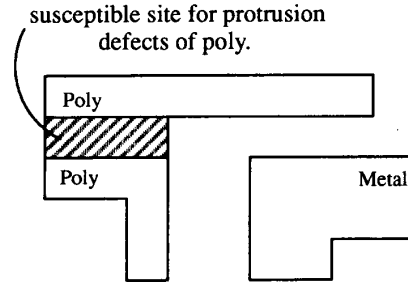


Fig. 4. An example of susceptible sites.

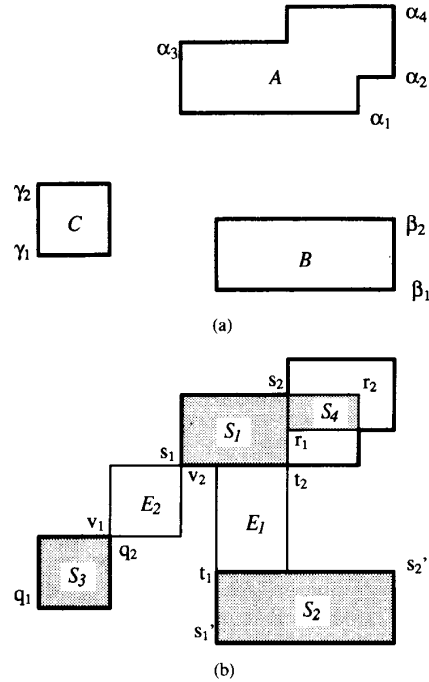


Fig. 5. (a) Three closed connected point sets. (b) Vertical susceptible sites.  $S_1, S_2$ , and  $S_3$  are lateral internal susceptible sites;  $S_4$  is a corner internal susceptible site.  $E_1$  and  $E_2$  are lateral and corner external susceptible sites, respectively.

*External corner susceptible sites* are formed from any two internal sites belonging to different closed connected point sets such that no line segment of one internal susceptible site is comparable to any line segment of the other internal susceptible site. Consider the internal susceptible sites  $S_1 = (s_1, s_2)$  and  $S_3 = (q_1, q_2)$  in Fig. 5(b); then the external corner susceptible site  $E_2$  ( $S_1, S_3$ ), with corner points ( $v_1, v_2$ ) is formed as follows:

$$\begin{cases} v_1 = (\min(x(s_2), x(q_2)), \min(y(s_2), y(q_2))) \\ v_2 = (\max(x(s_1), x(q_1)), \max(y(s_1), y(q_1))) \end{cases} \quad (4)$$

The *magnitude* of any vertical susceptible site  $S = (s_1, s_2)$  is defined as

$$\text{Mag}(S) = |y(s_1) - y(s_2)|. \quad (5)$$

### B. Critical Regions

A critical region is an open connected point set constructed for a defect (of size  $\delta$ ) such that if the center of that defect is placed anywhere on this region, the defect is catastrophic. Critical regions are directly constructed from susceptible sites. Naturally, they are a function of the defect size and of the defect mechanism type.

Since the electrical significance of layer interrelationships is of crucial importance in determining whether a hard structure is catastrophically affected by spot defects, a *failure criterion* specific to the hard structure must be introduced. The failure criterion is a bound represented as a rational number that is used to capture the geometrical situations which determine whether a defect is catastrophic or not. It represents the size of intersection between defect and pattern typical for some defect type. As an example, assume the state clauses  $\mu$  and  $\omega$  for the presence of poly and diffusion in a four-layer structure. Let these clauses be  $\mu = (\mathbf{x}, \text{OXIDE}, \text{POLY}, \mathbf{x})$  and  $\omega = (\mathbf{x}, \text{DIFFUSION}, \text{OXIDE}, \mathbf{x})$ , respectively. Consider three hard structures,  $R_1(\mu)$ ,  $R_2(\mu)$ , and  $R_3(\omega)$ , identifying two wires of poly and one of diffusion, each of them of width  $w$  and spaced a distance  $s$  apart from each other, as depicted in Fig. 6(a). Assume now that there is a protrusion defect in the poly layer. While a minimum defect size  $\delta$  can introduce a bridge between  $R_1(\mu)$  and  $R_2(\mu)$ , the same defect size has no effect between  $R_2(\mu)$  and  $R_3(\omega)$ . However, if the defect size were at least  $\delta + w$ , a parasitic transistor could have been formed (see Fig. 6(b)). In this last situation the extra amount of intersection  $w$  represents the failure criterion of  $R_3(\omega)$  arising from protrusion defects originating in the poly layer. Summarizing, a failure criterion depends on the specific defect mechanism, the specific state clause, and the specific geometrical situation of the hard structure involved in the defect mechanism. The failure criteria for each type of defect mechanism will be examined in detail in the next sections.

Let us first formalize the notion of *critical regions*. Assume now a lateral susceptible site, either internal or external. Take for instance the external susceptible site  $E_1(S_1, S_2) = (t_1, t_2)$  of Fig. 5(b). Assume now a defect of size  $\delta$ . Then, a *vertical lateral critical region*,  $\mathcal{C}_{\text{lat}}(\delta)$ , is established only if

$$y(t_2) - \left(\frac{\delta}{2} + \Phi_{S_1}\right) \leq y(t_1) + \left(\frac{\delta}{2} + \Phi_{S_2}\right) \quad (6)$$

where  $\Phi_{S_1}$  and  $\Phi_{S_2}$  are the failure criteria of the hard structures with which the susceptible site  $E_1(S_1, S_2)$  is associated. If the susceptible site were of an internal type, we would have that  $\Phi_{S_1} = \Phi_{S_2}$  because we are dealing with only one susceptible site.  $\mathcal{C}_{\text{lat}}(\delta)$  is in fact an open rectangle with corner points  $(u_1, u_2)$  given as

$$\begin{aligned} u_1 &= \left(x(t_1) - \left(\frac{\delta}{2} + f\right), y(t_2) - \left(\frac{\delta}{2} + \Phi_{S_1}\right)\right) \\ u_2 &= \left(x(t_2) + \left(\frac{\delta}{2} + f\right), y(t_1) + \left(\frac{\delta}{2} + \Phi_{S_2}\right)\right) \end{aligned} \quad (7)$$

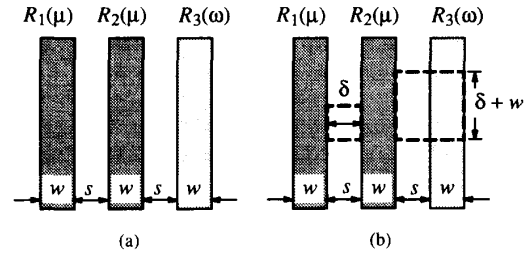


Fig. 6. An illustration of failure criterion. (a) Pattern configuration. (b) Two situations for minimum catastrophic defect sizes.

where  $f$  is an additional horizontal extension of the susceptible site  $E_1$ . This additional extension is dependent on the failure criterion and it is denoted as the end effect of the susceptible site. It appears in cases where the defect's edge can be located some distance  $f$  away from a pattern, without having to physically intersect it, and still be lethal. The extension  $f$  will be treated separately in the next section according to the defect mechanism. As an example, Fig. 7 shows a lateral critical region constructed for a defect size of 3.5 units and  $\Phi_{S_1} = \Phi_{S_2} = 0$ .

*Corner critical regions* are obtained from corner susceptible sites. As with lateral regions, whether the site is external or internal is of no relevance. Take, for instance,  $E_2(S_1, S_3) = (v_1, v_2)$  in Fig. 5(b). The corner critical region is established by the following condition:

$$\begin{aligned} y(v_2) - \left(\frac{\delta}{2} + \Phi_{S_1}\right) &\leq y(v_1) + \left(\frac{\delta}{2} + \Phi_{S_3}\right) \wedge \\ x(v_2) - \left(\frac{\delta}{2} + \Phi_{S_1}\right) &\leq x(v_1) + \left(\frac{\delta}{2} + \Phi_{S_3}\right) \end{aligned} \quad (8)$$

where  $\Phi_{S_1}$  and  $\Phi_{S_3}$  are the failure criteria of the associated hard structures of  $E_2$ . Also, if  $E_2$  were an internal susceptible site,  $\Phi_{S_1} = \Phi_{S_3}$ . The open rectangle  $\mathcal{C}_{\text{cor}}(\delta)$  with corner points  $(o_1, o_2)$  defines the corner critical region, where

$$\begin{aligned} o_1 &= \left(x(v_2) - \left(\frac{\delta}{2} + \Phi_{S_1}\right), y(v_2) - \left(\frac{\delta}{2} + \Phi_{S_3}\right)\right) \\ o_2 &= \left(x(v_1) + \left(\frac{\delta}{2} + \Phi_{S_1}\right), y(v_1) + \left(\frac{\delta}{2} + \Phi_{S_3}\right)\right). \end{aligned} \quad (9)$$

Fig. 7 also shows a corner critical region for a defect size of 3 units and  $\Phi_{S_1} = \Phi_{S_3} = 0$ .

The area enclosed in a critical region is called the critical area. Given  $m$  lateral critical regions and  $n$  corner critical regions, the total critical area for a defect size  $\delta$  is obtained as

$$\text{Area} \left( \bigcup_{i=1}^{i=n} \mathcal{C}_{\text{cor}}(\delta)_i \cup \bigcup_{j=1}^{j=m} \mathcal{C}_{\text{lat}}(\delta)_j \right) \quad (10)$$

where *Area* is a function used to compute the area of a point set.

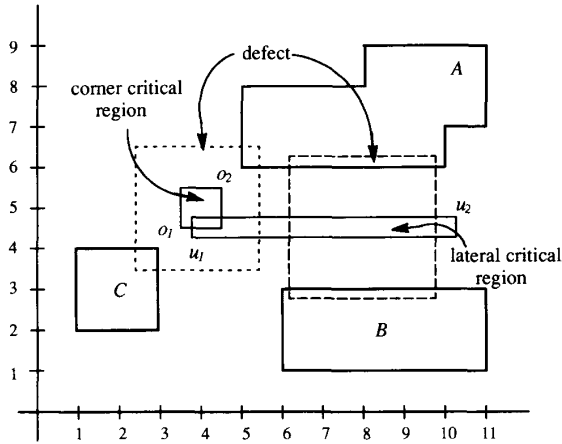


Fig. 7. Construction of critical regions. The corner critical region is for a defect size of 3 units. The lateral critical region is for a defect size of 3.5 units.

### C. Critical Regions for Protrusion Defects

1) *Body Effects*: Consider now two state clauses  $\omega, \mu \in \Sigma_{\text{tech}}$ . Assume three hard structures,  $R_1(\omega)$ ,  $R_2(\omega)$ , and  $R(\mu)$ , mutually nonintersecting, and also that two protrusion defects,  $d_j^p$  and  $d_k^p$ , originating in layers  $L_j$  and  $L_k$ , respectively, are present. Suppose now that we deal with the active patterns  $a \subset L_i$  originating from the partial hard structure  $R_1(\omega) | L_i$ ,  $b \subset L_j$  originating from  $R(\mu) | L_j$ , and  $c \subset L_k$  originating from  $R_2(\omega) | L_k$ . Assume also that the protrusion defect,  $d_j^p$ , affects the functional behavior of  $R_1(\omega)$  and  $R(\mu)$  at  $a$  and  $b$ , respectively, and that the size of such a defect is  $\delta$ .

Let the hard structures be as in Fig. 8(a), and also let the patterns be represented as in Fig. 8(b).  $E_1$ , in Fig. 8(b), represents a *multilayer vertical susceptible site* in  $L_i$  for protrusion defects in  $L_j$ . In a similar way,  $E_2$  is a *multilayer corner susceptible site* for protrusion defects in  $L_k$ .

Before going into detail, let us first study the geometrical conditions under which a protrusion defect of a pattern, say  $a_i$ , can be catastrophic on some other pattern, say  $a_j$ . They are as follows: i) The protrusion of  $a_i$  has to span over pattern  $a_j$ . This case is typically exemplified by a protrusion of polysilicon entirely spanning over a diffusion pattern such that a parasitic transistor is formed. ii) The protrusion of  $a_i$  has to intersect at least the boundary of pattern  $a_j$ . This is the typical case for protrusion defects making a physical bridge between two or more patterns. iii) The defect comes closer than a certain distance to pattern  $a_j$ . This case arises as a consequence of electrical phenomena such as cross talk between patterns.

To be able to consider the situations mentioned above, a *sensitivity factor*,  $\sigma$ , is introduced. In other words,  $\sigma$  determines how much area on  $a_j$  has to be covered by the protrusion, or how close to  $a_j$  the defect must be located. Furthermore,  $\sigma$  is a function of the layers involved in the defect mechanism and of the particular state clause of the hard structure that is affected. In general, for a hard struc-

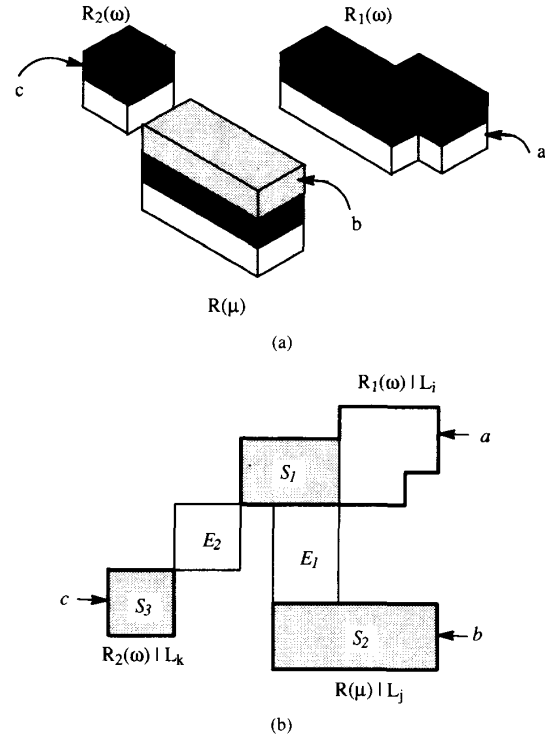


Fig. 8. A multilayer situation is depicted in which three active patterns belonging to three different layers are characterized by two kinds of hard structures. (a) Hard structures. (b) Pattern representation.  $a \subset L_i$  by  $R_1(\omega) | L_i$ ,  $b \subset L_j$  by  $R(\mu) | L_j$ , and  $c \subset L_k$  by  $R_2(\omega) | L_k$ .

ture consisting of, say,  $n$  layers,  $n^n$  different values of  $\sigma$  can be specified. Each of these sensitivity factors determines the conditions of protrusion defects in every layer affecting each one of the layers of the hard structure. A function can now be written, in terms of susceptible sites, defining the *geometrical failure criterion for protrusion defects* as

$$\Phi_{\text{prot}}(E, S, \sigma_{\mu}^{ji}) = \begin{cases} \sigma_{\mu}^{ji} \text{Mag}(E), & 0 \leq \sigma_{\mu}^{ji} \leq 1 \\ \sigma_{\mu}^{ji} \text{Mag}(S), & -1 \leq \sigma_{\mu}^{ji} < 0 \end{cases} \quad (11)$$

where  $\sigma_{\mu}^{ji}$  is the sensitivity factor of layer  $L_j$  given the state clause  $\mu$  and provided that  $L_j$  is affected by protrusion defects originating in  $L_i$ .  $S$  and  $E$  are the internal and external susceptible sites in  $L_j$  where the defect occurs. In this function, negative values of  $\sigma_{\mu}^{ji}$  cover the above-mentioned case i, and positive values cover cases ii and iii.

Replacing  $\Phi_{S_1}$  and  $\Phi_{S_2}$  in (6) and (7) with the corresponding  $\Phi_{\text{prot}}$  of  $a$  and  $b$ , the vertical lateral critical region for protrusion defects in  $L_j$  between patterns  $a$  and  $b$  at lateral susceptible sites  $S_1$ ,  $S_2$ , and  $E_1$  is established if (6) is satisfied, and it is found according to (7).

Similarly, assume that the protrusion defect,  $d_k^p$ , affects  $R_1(\omega)$  and  $R_2(\omega)$  on  $a$  and  $c$ , respectively, and that the size of such defect is  $\Delta$ . Then the *corner critical region* for protrusion defects in layer  $L_k$  between patterns  $a$  and



$c$ , at the corner susceptible site  $E_2$  and the lateral susceptible sites  $S_1$  and  $S_3$  is also found by replacing  $\Phi_{S_1}$  and  $\Phi_{S_3}$  with the corresponding  $\Phi_{\text{prot}}$  in (9) if the conditions of (8) are satisfied.

The critical regions for these two cases are illustrated in Fig. 9 for  $\sigma_{\mu}^{ij} = 0.3$ ,  $\sigma_{\omega}^{ij} = -1$ ,  $\sigma_{\omega}^{ik} = 0.0$ ,  $\sigma_{\omega}^{kk} = 0.0$ ,  $\delta = 4.5$  units, and  $\Delta = 2.5$  units.

2) *End Effects*: For the discussion in this subsection, assume two parallel patterns,  $a \subset L_i$ , originating from the hard structure  $R_1(\omega) | L_i$ , and  $b \subset L_j$ , originating from  $R(\mu) | L_j$ . Assume that both patterns are bridged by a protrusion defect  $d^p$  of size  $\delta$  and layer of origin  $L_i$ . Assume that both  $a$  and  $b$  share the same left and right coordinates. For terminology simplifications, the failure criteria for protrusion defects of patterns  $a$  and  $b$  will be denoted as  $\Phi_a$  and  $\Phi_b$ , respectively. Because of the symmetry at both extremes of the patterns, the explanations to follow are restricted to the right end.

When creating critical regions, besides the pattern extension proportional to  $\delta/2$ , an additional extension, proportional to the failure criterion, has to be considered. The magnitude of this extension is evaluated as follows:

$f(\delta, \Phi_a, \Phi_b, s)$

$$= \begin{cases} 0 & \Phi_a \leq 0 \vee \Phi_b \leq 0 \\ \min(\Phi_a, \Phi_b) & \Phi_a > 0 \wedge \Phi_b > 0 \\ & \wedge \max(\Phi_a, \Phi_b) > s - \delta \\ h(\delta, \Phi_a, \Phi_b, s) & \Phi_a > 0 \wedge \Phi_b > 0 \\ & \wedge \max(\Phi_a, \Phi_b) \leq s - \delta \end{cases} \quad (12)$$

where  $\delta$  is the defect size,  $s$  is the magnitude of the external susceptible site between both patterns, and  $h(\delta, \Phi_a, \Phi_b, s)$  is a function taking values between 0 and  $\min(\Phi_a, \Phi_b)$ . This function will be described later in the context of this subsection. For the rest of this discussion the abbreviations  $f$  and  $h$  will be used instead of  $f(\delta, \Phi_a, \Phi_b, s)$  and  $h(\delta, \Phi_a, \Phi_b, s)$ , respectively. Equation (12) has the following physical interpretation:

a)  $\Phi_a \leq 0 \vee \Phi_b \leq 0$ : When either  $\Phi_a$  or  $\Phi_b$  is zero, the condition to make a bridge begins when the defect intersects the edge of the pattern. Since a defect positioned ahead of  $\delta/2$  never satisfies this condition, the extension is zero. When  $\Phi_a$  or  $\Phi_b$  is negative, the defect has to overlap the pattern by a certain amount of area. Since a defect positioned at a further extension of  $\delta/2$  never overlaps the pattern, the extension is also zero.

b)  $\Phi_a > 0 \wedge \Phi_b > 0$ : When  $\Phi_a$  and  $\Phi_b$  are positive, the condition to make a bridge begins when the edges of the defect are at some distance  $\Phi_a$  from the edge of pattern  $a$  and simultaneously at a distance  $\Phi_b$  from pattern  $b$ . Consider the case where  $\Phi_b > \Phi_a$ . Obviously, the extension  $f$  is not zero and in this case takes the maximum

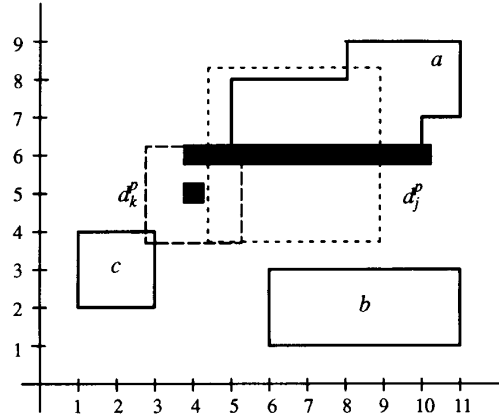


Fig. 9. A corner and a lateral multilayer critical region for two different defect sizes. Critical regions are highlighted in black.

value of  $\Phi_a$  because if the center of the defect is positioned at  $(\delta/2) + \Phi_b$ , its left edge will be at a distance greater than  $\Phi_a$  and will never satisfy the condition for a bridge with  $a$ . Furthermore, the shape of its corresponding subset of the total critical region is not rectangular. It is bounded by two arcs or by two arcs and one line segment, as shown in parts (a) and (b) of Fig. 10. Taking pattern  $b$  as reference, and choosing the center of the bounding arc due to  $\Phi_b$  as the origin (see Fig. 10(a)), this section of the critical region is best described as a set of connected points  $C_{\text{extension}}$ , where

$$C_{\text{extension}} = \left\{ (x, y) \left| \begin{array}{l} 0 < x \leq f \wedge \\ (s - \delta - \Phi_a) < y \leq \Phi_b \wedge \\ (x^2 + y^2 \leq \Phi_b^2 \vee \\ x^2 + (y - (s - \delta))^2 \leq \Phi_a^2) \end{array} \right. \right\}. \quad (13)$$

This follows from the rationale that the distance between the lower left (upper left) corner of the defect and the right corner of  $b(a)$  has to be at most the failure criterion  $\Phi_b(\Phi_a)$ . Since this distance has to be constant, in the extreme case one can draw a circle of radius  $\Phi_b(\Phi_a)$  centered at the right corner point of  $b(a)$  such that any point in the perimeter of this circle corresponds exactly to the coordinates of the lower left (upper left) corner of the defect. Because the corner of the defect moves along the circle, the center of the defect also moves following the same trajectory. With such established critical region, it can be observed that for a defect of size  $\delta > s - \Phi_b$ , the two bounding arcs will intersect at the line  $x = \Phi_a$ , e.g., in order to make a bridge, the extension  $f$  takes the value of  $\Phi_a$ . However, for a defect of size  $\delta \leq s - \Phi_b$ , such as the case of Fig. 10(b), the two bounding arcs will intersect at the line  $x = h$  with  $h < \Phi_a$ . As a result, the extension  $f$  cannot be greater than  $h$  in order to make a

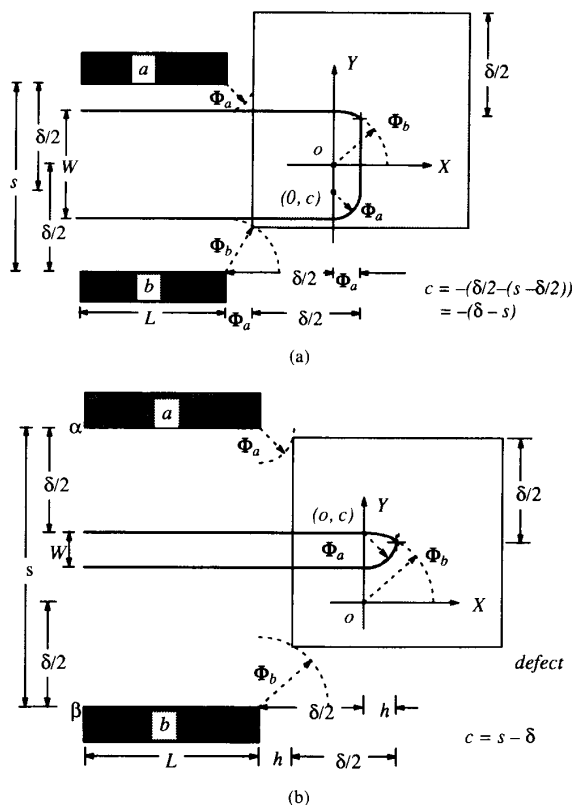


Fig. 10. Critical regions for end effects. (a) Case when  $\delta > s - \Phi_b$ . (b) Case when  $\delta \leq s - \Phi_b$ .

bridge. The exact value of  $h$  can be found by solving the boundary equations in the following equation for the variable  $x$ :

$$\begin{cases} x^2 + y^2 = \Phi_b^2 \\ x^2 + (y - (s - \delta))^2 = \Phi_a^2 \end{cases} \quad (14)$$

For  $\Phi_b < \Phi_a$ , the symmetric conclusions can be drawn, which results in (12).

For ease of modeling and simplification of the algorithms for computing critical areas, the shape of this section can always be approximated as a rectangle with length equal to  $Ramp(\min(\Phi_a, \Phi_b))$  and width equal to  $\delta - s + \Phi_a + \Phi_b$ , where  $Ramp$  is the standard "ramp function," defined as

$$Ramp(x) = \begin{cases} 0, & x \leq 0 \\ x, & x > 0. \end{cases} \quad (15)$$

Appendix I shows a derivation of this area and its error relative to the total critical area of the bridge.

#### D. Critical Regions for Isolated Spot Defects

Isolated spots form a special case in which a missing or an extra piece of material is present in a layer but it only affects layers other than the one of origin, and, what

is more, their effect is only vertical. A typical example is an isolated missing spot of dielectric oxide in a polysilicon-metal crossing inducing a bridge between both conductors. Another example is an isolated extra spot of polysilicon completely covering a diffusion pattern, such that the "diffusion conductor" is transformed into a parasitic transistor with a floating gate.

Consider a state clause  $\omega \in \Sigma_{tech}$ . Assume an active pattern  $a \subset L_i$ , originating from a partial hard structure  $R_1(\omega) \mid L_i$ . Let the hard structure and the pattern again be depicted as in parts (a) and (b) of Fig. 8. Assume now that an isolated spot defect,  $d^s$ , of  $L_j$ ,  $j \neq i$ , affects the functionality of  $R_1(\omega)$  at pattern  $a$ , and that the size of such a defect is  $\delta$ .

In this case the internal susceptible site  $S_1$ , of Fig. 8(b), is called a vertical lateral susceptible site in  $L_i$  for isolated spot defects of  $L_j$ . The condition, however, for  $S_1$  to be a valid susceptible site is that, in the open rectangle  $S_1$ , no other points of active patterns of the layer where the isolated spot has its origin be allowed. This condition precludes the establishment of redundant susceptible sites, as could be the case of an isolated spot defect of polysilicon over a polysilicon-metal crossing.

The function describing the *failure criterion for isolated spot defects* in  $L_j$  is defined as follows:

$$\Phi_{spot}(S, \sigma_\mu^{ij}) = \begin{cases} 0, & \sigma_\mu^{ij} = 0 \\ \sigma_\mu^{ij} Mag(S), & 0 < \sigma_\mu^{ij} \leq 1 \end{cases} \quad (16)$$

where  $\sigma_\mu^{ij}$  is the sensitivity factor of layer  $L_i$  related to the state clause  $\mu$  and given that  $L_i$  is affected by isolated spot defects originating in  $L_j$ .  $S$  is the associated internal susceptible site where defects take place.

The function is interpreted as follows. For  $0 < \sigma_\mu^{ij} < 1$ , a catastrophic defect size can be less than the magnitude of the susceptible site. As an illustration of this case consider a spot defect of the implant layer, in an NMOS technology, spanning over the gate area of an enhancement transistor in such a magnitude that the transistor is turned into a depletion one. In the extreme case of  $\sigma_\mu^{ij} = 1$ , any defect at least touching the boundary of the susceptible site can be catastrophic. This situation is exemplified by tiny pinholes in the thin oxide of a transistor's gate area such that the gate is shorted to the substrate. For  $\sigma_\mu^{ij} = 0$  the defect size has to be at least the magnitude of the susceptible site in order to be catastrophic.

Replacing  $\Phi_{S_1}$  and  $\Phi_{S_2}$  with  $\Phi_{spot}$  in (6) and (7), the lateral critical region for isolated-spot defects of  $a$  is established if (6) is satisfied, and it is found according to (7). Corner critical regions for isolated-spot defects can be derived from (9) if (8) is satisfied.

A lateral critical region for isolated spot defects is illustrated in Fig. 11 for  $\sigma_\mu^{ij} = 1$  and  $\delta = 1$  unit. The critical area can be computed according to (10).

Isolated spot defects do not need any additional extensions due to the end effects because a defect centered ahead of the critical region will never physically intersect the pattern.

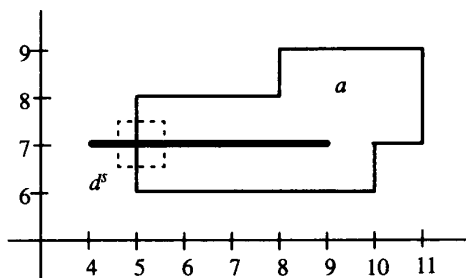


Fig. 11. A lateral critical region for isolated spot defects.

### E. Critical Regions for Intrusion Defects

Unlike isolated spots and protrusion defects, intrusion defects only affect patterns in their layer of origin. Consider some state clause  $\omega \in \Sigma_{\text{tech}}$  and an active pattern,  $a \subset L_i$ , originating from the partial hard structure  $R_1(\omega) \setminus L_i$ . Once more, let the hard structure be depicted as in Fig. 8(a) and the pattern as in Fig. 8(b). Assume now that an intrusion defect,  $d^i$ , capable of functionally affecting  $R_1(\omega)$  at pattern  $a$  is present, and that the size of such a defect is  $\delta$ . In this case the internal susceptible site  $S_1$  of Fig. 8(b) represents a *vertical susceptible site for intrusion defects* in  $L_i$ .

The failure criterion for intrusion defects is defined as

$$\Phi_{\text{intr}}(S, \sigma_\mu^i) = \begin{cases} 0, & \sigma_\mu^i = 0 \\ \sigma_\mu^i \text{Mag}(S), & 0 < \sigma_\mu^i \leq 1 \end{cases} \quad (17)$$

where  $\sigma_\mu^i$  is the sensitivity factor of layer  $L_i$  related to the state clause  $\mu$ , and  $S$  is the associated internal susceptible site where the defect takes place.

The physical meaning of this failure criterion is analogous to that of isolated spot defects. For  $\sigma_\mu^i > 0$ , defects smaller than  $\text{Mag}(S)$  can be catastrophic. This situation appears when the remaining conducting area around the intrusion defect is so small that whenever the current flows through it the area will be blown and the pattern will be cut anyway. For  $\sigma_\mu^i = 0$ , defects are lethal when their size is at least  $\text{Mag}(S)$ .

Replacing  $\Phi_{S_1}$  and  $\Phi_{S_2}$  with  $\Phi_{\text{intr}}$  in (6) and (7), the lateral critical region for intrusion defects of  $a$  is established if (6) is satisfied, and it is found according to (7). Corner critical regions for intrusion defects can be derived from (9) if (8) is satisfied.

For the same reasons as with isolated spots, intrusion defects do not require any additional extensions.

## IV. SYSTEMATIC EXTRACTION OF CRITICAL REGIONS AND COMPUTATION OF CRITICAL AREAS

It has been shown that critical regions can be found geometrically [26]. Under this approach critical regions for bridges are found by expanding each pattern by an amount equal to half the defect size, and then by checking to see whether the expansions intersect. If so, then the (amount of) intersection corresponds to the critical region between the patterns. In the case of critical regions for

cuts every pattern is shrunk by half the defect size, and a critical region is established only, when on shrinking, parallel edges of the same region pass over each other.

The above solution has for bridges a quadratic time complexity; thus it is computationally prohibitive for very large layouts. Also, the expansion of patterns implies that a layout extraction has to be executed for each defect size. For regions sensitive to cuts the problem is simpler since no neighboring patterns need to be considered. Hence, the problem is simply reduced to shrink them. However, an important shortcoming of this method is that critical regions are directly derived from the patterns rather than from the susceptible sites. This action hinders the use of failure criteria because for any susceptible site a separate value for  $\Phi$  can be specified. That is, there may be different values of  $\Phi$  for different portions of the same active pattern. Hence, for a given defect size some critical regions cannot be established for certain multilayer situations.

Fig. 12 shows the overall framework of our system. The four stages are represented by ovals; the input data to each stage is described by rectangles pointing to the ovals, and the output data by rectangles pointed by the ovals. The layout partition stage consists essentially in extracting soft structures from the layout and in determining which defect mechanisms affect them and the manner in which they do so. The susceptible stage locates regions where defect mechanisms can potentially introduce defects in the soft structures. The critical-region stage identifies the regions where spot defects of a known size affect the soft structures. Finally, the area stage computes the total critical area per defect mechanism, and computes also the partial critical area per intersection of critical regions with different fault types and different electric potentials. The former area can be used for yield prediction, and the latter for realistic fault analysis.

By convention, it is assumed in the following subsections that all line segments are of two types. When the interior of the corresponding connected point set lies above (below) the line segment, we say that it is of type *BEGIN* (*END*).

### A. A Spot-Defect Language

A simple language founded on the theory of Section II was created as a user interface. This language provides information about the technology which is going to be used and the defect mechanisms, abstracted at the layout level, that may damage hard structures. Fig. 13 shows its syntax in BNF notation; keywords and variables are identified as boldface and italic words, respectively.

Statements 2 and 3 describe the vector of masks  $\mathbf{M} = (M_1, M_2, \dots, M_{N_{\text{mask}}})$  classified by their conductor/contact properties. Masks which are neither conductor nor contact include implant, p-well, etc. Those state clauses which are meaningless in the technology are specified in statements 6 and 7. Statements 9 to 13 describe the set  $\Omega$  of state clauses associated with mask stacks.

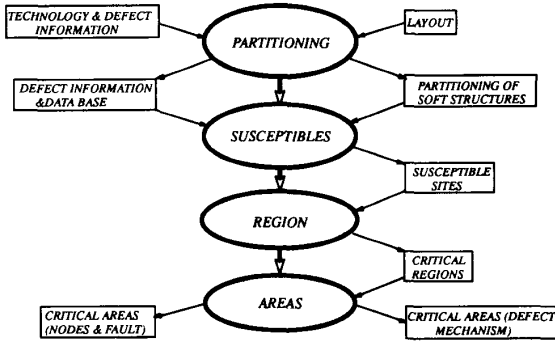


Fig. 12. Overall flowchart of the system for computing multilayer critical areas.

```

1: tech_file      ::= (" TECHNOLOGY tech_name mask_descr ") .
2: mask_descr   ::= (" MASKS {" [masks] "}" ) [invalid_structs] .
3: masks        ::= "<" conductor_mask ">"
                | "$" contact_mask
                | mask_name .
4: conductor_mask ::= mask_name .
5: contact_mask  ::= mask_name .
6: invalid_structs ::= (" SUPPRESS (invalids) )" struct_descr .
7: invalids      ::= (" {" mask_function} " ) .
8: mask_function ::= {" " } mask_name .
9: struct_descr  ::= (" STRUCTURES {structures}+ " ) {defect_descr} .
10: structures   ::= (" struct_name {struct_function}+ " )
                | (" {" struct_name {alternate_struct}+ " } " ) .
11: struct_function ::= {" " } mask_name
                | "<" {grouped_masks} ">" .
12: grouped_masks ::= {" # " } conductor_mask .
13: alternate_struct ::= (" alternate_name {struct_function}+ " ) .
14: defect_descr  ::= (" DEFECTS {" min_size max_size step " }
                {struct_defects} ) .
15: struct_defects ::= (" struct_name {mask_defects}+ " )
                | (" struct_name {alternate_defect}+ " ) .
16: alternate_defect ::= (" {" alternate_name {mask_defects}+ " } " ) .
17: mask_defects  ::= (" mask_name {" defect_type " }+ " ) .
18: defect_type   ::= (" class mask_name sens_factor fault " ) .
19: class         ::= {PROTRUSION | "+"}
                | {INTRUSION | "-"}
                | {ISOLATED | "+"} .
20: fault         ::= fault_name .

```

Fig. 13. Syntax of the spot defect language.

Each state clause, i.e.,  $\mu \in \Omega$ , is specified by a Boolean expression in which the names of the variables are replaced by the mask names. Also, since it is possible to specify a soft structure by more than one state clause, alternate descriptions are possible through statement 10. The value of the mask variable in the definition of a state clause evaluates to “true” when the mask is specified, or evaluates to “false” when it is preceded a tilde ( $\sim$ ). When a mask does not appear it is taken as a “don’t care.”

To give information about the electrical nodes, angle brackets ( $\langle \rangle$ ) are specified to indicate whether the mask remains with its same node or whether two or more masks are electrically merged. If a node is going to be split the symbol “#” preceding its mask is used.

Statements 14 through 20 describe the defect mechanisms that may affect every specified structure. Associated with each defect mechanism is the fault condition that arises together with its sensitivity factor. Each structure which is affected by defects has to specify which layers are sensitive and which defect mechanisms affect each one of the layers. This is explicitly shown in statement 18. If a structure is omitted from the defect specification it is assumed that the structure is insensitive to defects.

## B. Layout Partitioning

The first task in this stage is to parse the technology file in order to create a data base of defect-fault information of each state clause  $\mu \in \Omega$ . This data base is created as an array of  $2^{N_{\text{mask}}}$  elements. Each state clause is specified as a bit vector of masks and assigned to its corresponding entries in the array. Each entry contains information of the defects that affect the soft structure per

- defect mechanism
- individual masks of the state clause
- mask where the defect manifests itself with associated sensitivity factors.

Next, the layout is read and each rectangle is decomposed into horizontal line segments. Let  $\mathcal{R} = \{r_1, \dots, r_n\}$  be the set of horizontal segments sorted lexicographically by  $y$  and  $x$  coordinates.  $T$  is an auxiliary set of line segments which initially is empty, and  $P$  is the set of partitions formed. Each  $r_i \in \mathcal{R}$  has a bit vector such that each bit corresponds to a mask in the mask vector  $M = (M_1, \dots, M_{N_{\text{mask}}})$ . The algorithm sweeps the set  $\mathcal{R}$  by retrieving one line segment at a time. Assume that a line segment  $r$  is retrieved. Then the partitions are formed by constructing rectangular point sets from the comparable sections between  $r$  and each line segment of  $T$  that is below  $r$ . New partitions are stored in  $P$ , noncomparable sections of  $r$  are stored in  $T$ , and each comparable section of the lines stored in  $T$  is split from their corresponding line segments. If  $r$  is of type *BEGIN*, a logic OR operation is performed between the mask and bit vectors of each of these comparable sections and  $r$ . Next, the comparable sections are reinstalled in  $T$  with their bit vectors updated. On the other hand, if  $r$  is of type *END*, an XOR logic operation is carried on. If the result of the XOR is not zero the comparable sections are also inserted in  $T$ ; otherwise they are deleted from their corresponding line segment. After all the partitions are constructed a common node assignment, as is done in layout to circuit extractors, is performed.

## C. Geometrical Construction of Multilayer Susceptible Sites

Susceptible sites are obtained by performing two orthogonal sweeps in the layout. Thus, susceptible sites are found relative to their sweep. Furthermore, each susceptible site is “labeled” according to the sweep in which it was found. Corner susceptible sites are marked as corners. This labeling is necessary because in order to determine the critical regions one must know which coordinates need to be considered, either the abscissas for horizontal sites, the ordinates for vertical sites, or both abscissas and ordinates for corner sites.

Assume now that the vertical sweep is carried on. Let  $T$  be an ordered set containing the horizontal line seg-

ments of each of the masks of the partitions formed in the previous stage. Each line segment has information about the mask to which it belongs, its left, right and pos coordinates, the associated electrical node, and a counter that keeps track of overlapping sections between line segments. Let  $T$  be lexicographically ordered by  $y$  and  $x$  coordinates. Let  $\mathcal{B}[N_{\text{mask}}]$  and  $\mathcal{E}[N_{\text{mask}}]$  be two indexed sets that maintain the scan-line status for *BEGIN* and *END* line segments, respectively. Each of these sets is indexed by the mask to which the line segment belongs relative to its mask position in the mask vector  $\mathbf{M} = (M_1, \dots, M_{N_{\text{mask}}})$ . Both  $\mathcal{B}[N_{\text{mask}}]$  and  $\mathcal{E}[N_{\text{mask}}]$  are initially empty.

The algorithm sweeps the set  $T$  by retrieving one line segment at a time. Every *BEGIN* segment, say  $k \in o, o \subset M_j$ , is installed in  $\mathcal{B}[N_{\text{mask}}]$  indexed by its mask position  $j$  and with its overlap counter initialized to 1. If there are comparable sections between the line segments of  $\mathcal{B}[j]$  and  $k$ , the set  $\mathcal{B}[j]$  is updated in such a way that the comparable sections are split off from their corresponding line segments and reinstalled as independent line segments with their overlap counter incremented by 1. *END* line segments are installed in  $\mathcal{E}[N_{\text{mask}}]$  indexed by their mask position, with their overlap counter initialized to 1, and with the magnitude of the associated internal susceptible site attached.

Assume now an *END* line segment  $k$  of some mask  $M_j$ . Internal lateral susceptible sites are formed from the comparable sections among  $k$  and those line segments installed in every  $\mathcal{B}[i], i = 1, \dots, N_{\text{mask}}$ , whose overlap counter is 1. All comparable sections of  $\mathcal{B}[j]$  are split off from their corresponding line segments, and are reinstalled independently only if after decrementing their overlap counters, the value of the overlap counter is greater than 0. External susceptible sites are constructed after each internal susceptible site is established. The procedure is essentially the same, except that i) instead of using  $k$  as a reference, the *BEGIN* line segments of every internal susceptible site constructed from  $\mathcal{B}[j]$  are used, ii) the set  $\mathcal{E}[N_{\text{mask}}]$  is used to find comparable sections, and iii) external susceptible sites are established only when the associated electrical notes are different. Corner susceptible sites are formed by finding the nearest line segments to the right (left) endpoint of  $k$  until one of those lines has its ordinate bigger than the ordinate of  $k$  or bigger than one of the line segments already found.

Fig. 14 illustrates in a sequence of captions how lateral internal susceptible sites of some mask  $M_j$  are formed. Each caption shows the actions taken at each scan-line position,  $p_i$ , of Fig. 14(a). At scan-line position 1 (Fig. 14(b)) the *BEGIN* line segment is installed in  $\mathcal{B}[j]$ . At position 2 (Fig. 14(b)), the installed line segment is split, the overlap counters are updated, and the new line segment is installed. At position 3 (Fig. 14(d)) the overlap counters are updated. In this case only one susceptible site is made, and their associated *BEGIN* line segment is deleted from  $\mathcal{B}[j]$ . At position 4 (Fig. 14(e)) new susceptible sites are made.

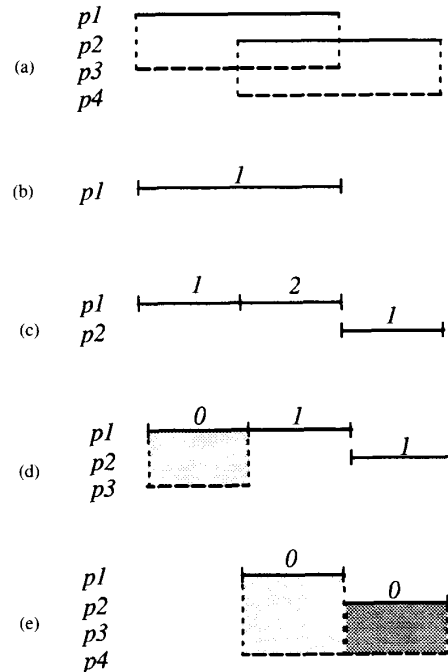


Fig. 14. Construction of lateral internal susceptible sites.  $\mathcal{B}\mathcal{E}\mathcal{G}\mathcal{S}\mathcal{L}$  line segments are at positions  $p_1$  and  $p_2$ .  $\mathcal{E}\mathcal{S}\mathcal{L}$  are at positions  $p_3$  and  $p_4$ .

Next, each susceptible site is processed to determine the possible defect mechanisms that may affect its related soft structures.

**Defect Mechanisms:** In the previous subsection it was described how to obtain susceptible sites. However, these sites are still per mask; furthermore, since there is no knowledge of their related soft structures it is not possible to establish which defect mechanisms are meaningful. In this subsection it will be described how to transform these sites into "multilayer" susceptible sites, and also how to relate them to their corresponding soft structures. The general strategy will be described now, and later the problem of determining whether a multilayer susceptible site is sensitive to defect mechanisms will be addressed.

To construct multilayer internal susceptible sites all the established internal susceptible sites are geometrically intersected among each other to find maximal connected point sets,  $S_{\text{multiple}}$ , that contain subsets of susceptible sites of different masks. External multilayer susceptible sites  $E_{\text{multiple}}(S, S_i)$  (where  $i$  is an index indicating each different internal susceptible) are constructed in the same geometrical way as internal multilayer susceptible sites.

Now establish a state clause  $\mu$  from the result of an OR operation among the masks of a multilayer susceptible site. This state clause is in fact used to represent the related soft structure(s); therefore it is possible to determine the defect mechanisms that affect each of the masks.

As an example of how to construct multilayer internal susceptible sites, consider the case of Fig. 15(a), where

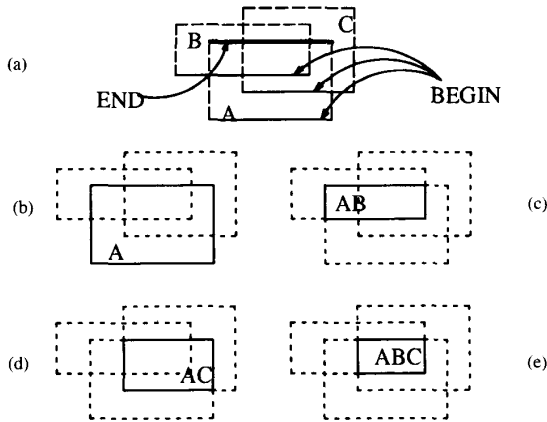


Fig. 15. Geometrical construction of multilayer internal susceptible sites. (a) Three different masks. Multilayer susceptible site for (b) Mask A, (c) masks A and B, (d) masks A and C, and (e) masks A, B, and C.

three *BEGIN* line segments from susceptible sites associated with masks, A, B, and C, and one *END* line segment associated with mask A are shown. Parts (b) through (e) of Fig. 15 display the constructed multilayer susceptible sites after the geometrical intersections take place.

In the following subsections it will be described how to determine whether a multilayer susceptible site is sensitive to defects. Let  $\mathcal{S}_{\text{prot}}[N_{\text{mask}}]$ ,  $\mathcal{S}_{\text{iso}}[N_{\text{mask}}]$ , and  $\mathcal{S}_{\text{intr}}[N_{\text{mask}}]$  be three initially empty sets used to store susceptible sites sensitive to protrusion, isolated, and intrusion defects, respectively. These sets are indexed by the mask where the defect originates relative to its mask position in the mask vector  $\mathbf{M}$ . Each susceptible site in any of these sets will have attached its related electrical nodes, fault types, and label for further processing of critical regions and areas.

*a) Intrusion defects:* Assume a state clause  $\mu \in \Omega$  of some internal susceptible site  $S_{\text{multiple}}$ . For each mask  $M_j$  associated with  $\mu$ , the defect-fault data base is inspected to check if an intrusion defect of that mask creates a fault condition for  $\mu$ . If the fault exists, the sensitivity factor is retrieved, the *Mag* of the susceptible site is calculated, and finally the susceptible site is stored in the set  $\mathcal{S}_{\text{intr}}[j]$ ; otherwise the susceptible site is discarded.

*b) Isolated spot defects:* These defects are checked analogously to intrusion defects. Assume the state clause  $\mu$  of some  $S_{\text{multiple}}$ . For each mask  $M_j$ , in the vector  $\mathbf{M}$ , different from any of the masks related to  $\mu$ , the defect-fault data base is inspected to verify if  $\mu$  is affected by isolated spot defects of  $M_j$ . If two or more masks are affected by the same defect, a valid susceptible site is established either when the faults are different, or when the faults are the same but the electrical nodes are different. If the susceptible site is valid, the associated sensitivity factor is retrieved, the *Mag* of the susceptible site is calculated, and as a last action the site is saved in the set  $\mathcal{S}_{\text{iso}}[j]$ .

*c) Protrusion defects:* For some  $E_{\text{multiple}}(S, S_i)$ , let  $\omega$  and  $\mu$  be the state clauses related to  $S$  and to  $S_i$ , respectively. For each mask associated with  $\mu$ , the defect-fault data base is inspected to verify if a protrusion in that mask affects  $\omega$ . If  $\omega$  is in fact sensitive, a valid susceptible site for protrusion defects is established. Since protrusion defects have a bilateral effect, the process is reversed and now it is checked whether protrusions of  $\omega$  affect  $\mu$ . Susceptible sites for protrusion defects are valid only when the electrical nodes are different. Each new susceptible site is stored in the set  $\mathcal{S}_{\text{prot}}$  indexed by the mask where the defect originates.

#### D. Geometrical Construction of Critical Regions

Critical regions are found by performing geometrical operations of shrinkage–expansion on each susceptible site found. Let  $\mathcal{C}_{\text{prot}}[N_{\text{mask}}][N_{\text{sizes}}]$ ,  $\mathcal{C}_{\text{iso}}[N_{\text{mask}}][N_{\text{sizes}}]$ , and  $\mathcal{C}_{\text{intr}}[N_{\text{mask}}][N_{\text{sizes}}]$  be three initially empty sets used to store critical regions for protrusion, isolated, and intrusion defects, respectively. Let these sets be indexed by the mask where the defect originates relative to its mask position in the mask vector  $\mathbf{M}$  and by the defect size in the given range of defect sizes  $N_{\text{sizes}}$ .

Remember that each susceptible site has information about the associated electrical node, the corner points of the site, the label (vertical, horizontal or corner), the related fault associated with the state clause to which the site belongs, and the respective failure criterion. The procedures that are about to be described are based on (5)–(8).

The algorithm sweeps each set of susceptible sites by retrieving one susceptible site at a time. Assume that  $\mathcal{S}_{\text{intr}}[j]$  is being swept. Then, for each defect size  $\delta$  in the range of defect sizes and for each susceptible site, three possible actions are taken depending on the site's label: **VERTICAL**) The ordinates of the corner points are shrunk by half the defect size plus the failure criterion. If the new shrunk coordinates intersect each other, then the abscissas are expanded by half of the defect size plus the failure criterion. **HORIZONTAL**) The same actions as with vertical sites, except that the shrinkage takes place on the abscissas and the expansion on the ordinates. **CORNER**) Both ordinates and abscissae are shrunk by half the defect size plus the failure criterion. If both ordinates and abscissae intersect each other a valid critical region is formed. Each established critical region is stored in its corresponding  $\mathcal{C}_{\text{intr}}[j][\delta]$ . See Fig. 16 for an illustration of these cases.

#### E. Computation of Critical Areas

Critical areas are computed for each defect size by sweeping the sets of critical regions. Each critical region has information concerning the fault type and the affected electrical nodes. Whenever two critical regions are inter-

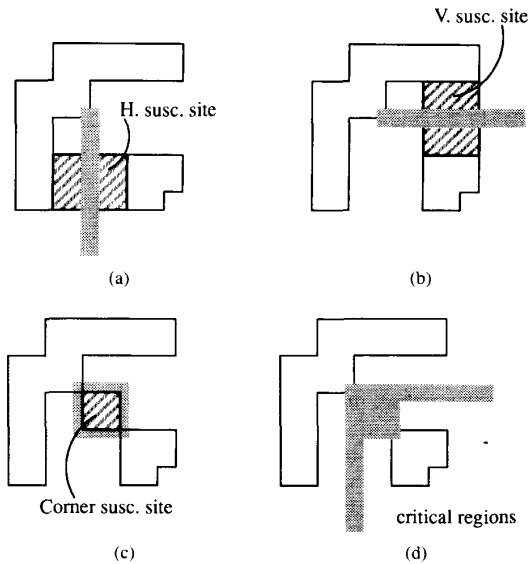


Fig. 16. Geometrical construction of critical regions. (a) From a horizontal susceptible site. (b) From a vertical susceptible site. (c) From a corner susceptible site. (d) All critical regions.

sected, the intersected section will be the critical region for both fault types on all related nodes. This assertion can be illustrated by an example. Assume the three different critical regions  $A$ ,  $B$ , and  $C$  depicted in Fig. 17. Assume that  $A$  has nodes 1 and 2 and fault type "short," that  $B$  has nodes 1 and 3 and fault type "new device," and that  $C$  has nodes 2 and 3 and fault type "new device." Clearly, if the center of the defect falls in region  $A$  only a "short" arises, if it falls in region  $B$  only a "new device" is created, and if it falls in  $ABC$  both short-circuit and "new device" faults are established. Hence, each intersection of critical regions has a different fault significance which can be weighted according to the partial critical area. Therefore, for each distinct defect mechanism, partial critical areas will be computed per fault and related electrical node. The total critical area will simply be obtained by adding up the results of each partial critical area.

Without loss of generality let us denote the set  $\mathcal{C}[N_{\text{mask}}][N_{\text{sizes}}]$  as the set containing the horizontal line segments of each of the critical regions found. Let it be lexicographically sorted by  $y$  and  $x$  coordinates. Take one defect size,  $j$ , and one mask,  $i$ . Each line segment  $c \in \mathcal{C}[i][j]$  has two sets that keep track of the intersection of nodes and faults. Let us denote these sets as  $\text{NODE}$  and  $\text{FAULT}$  and their relationship to  $c$  as  $c.\text{NODE}$  and  $c.\text{FAULT}$ , respectively. Each element of these sets has information of the node number (fault type) and a node counter (fault counter) that keeps track of node (fault) multiplicity in the same line section. Let  $A[2^N][2^F]$  be a matrix used to store the partial area for all possible combinations of nodes and faults, where  $N$  and  $F$  are the total numbers of nodes and types of faults extracted from the layout, respectively. In practice this matrix is too sparse

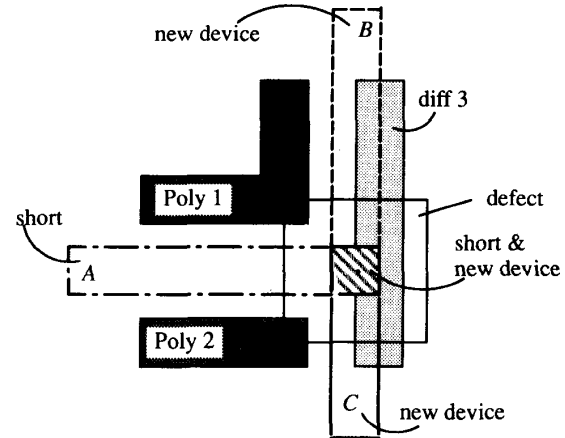


Fig. 17. Electrical significance of the intersection among critical regions.

to be used as such and also it can be very huge; therefore we use a linked list of meaningful elements instead. However, for ease of explanation, the matrix will still be used for the discussion.

The algorithm sweeps the set  $\mathcal{C}[i][j]$  by retrieving one line segment at a time. Let  $T$  be an initially empty auxiliary set maintaining line segments. Assume now that a line segment  $c \in \mathcal{C}[i][j]$  is retrieved. Then for each comparable section  $s$ , obtained from the line segments in  $T$ , the area of the rectangle formed between  $c$  and  $s$  is computed. Next, the sets  $s.\text{NODE}$  and  $s.\text{FAULT}$  are scanned to construct two bit vectors,  $n$  and  $f$ , such that each node and fault in  $s$  are assigned to a bit position. These bit vectors are used to index the matrix  $A[n][f]$  in order to accumulate the partial area for this specific combination of nodes and faults. This partial area is also accumulated to the total critical area. If the type of  $c$  is *BEGIN*, only its noncomparable sections are installed in  $T$ . Every comparable section,  $s$ , is split off from its corresponding line segments and reinstalled with the node and fault sets including the node and fault of  $c$ . If the nodes (faults) of  $c$  and  $s$  are the same, the respective counter is incremented; otherwise they are inserted into the corresponding sets of  $s$  with the respective counter initialized to 1. If the type of  $c$  is *END*, the node and fault counters of each comparable section that has the same node and fault of  $c$  are decremented. If the node or fault counters become 0, the node or fault is removed from its corresponding set. Whenever both fault and node sets are empty the associated line segment is removed from  $T$ .

#### F. Implementation Notes

Scan-line algorithms usually make use of data structures such as balanced trees and segment trees [34]. These data structures are planned for minimizing time of operations such as delete, insert, and search on random accesses to the data structure's elements. However, for the applications explained in the previous sections it becomes

quite difficult and laborious to perform these operations on these data structures. In most cases, one has to deal only with comparable sections rather than whole line segments. Therefore, a simple data structure, named static line array (SLA), was developed. Let  $SLA[N_{SLA}]$  be an array of  $N_{SLA}$  elements, where  $N_{SLA}$  is equal to the maximum abscissa of the layout, or ordinate, minus the minimum corresponding ones. If vertical layout sweeps are performed, the abscissas are used; otherwise the ordinates. Each element of this array represents a section of a line segment of unit 1. Each entry contains a *flag* that indicates whether the slot is occupied or not, the vertical (horizontal) position of horizontal (vertical) line segments, and some extra information which is related to the particular application, i.e., a bit vector of masks, nodes, faults, etc. Insert, delete, and search operations become then quite simple. For instance, if a horizontal line segment ( $pos(\alpha); l(\alpha), r(\alpha)$ ) is going to be inserted, the flag is set ON in all those  $i$  slots such that  $l(\alpha) - MIN \leq i < r(\alpha) - MIN$ , where  $MIN$  is the minimum layout abscissa, and the position in each slot is set to be equal to  $pos(\alpha)$ . Delete operations are obviously done by resetting the flat in the corresponding slots, and search operations are done by finding those slots, in the range of the line segment of reference, whose flat is ON. With the SLA simultaneous operations of insert-delete, insert-split, split-delete, search-split, etc., can be carried out. Fig. 18 shows an example of this static line array.

The performance using this data structure is quite fast. The static line array is based on the fact that most of the line segments in a layout are of length far less than the total length of the layout [2]. So, in most cases the number of iterations is quite small in order to insert, delete, or split a line segment. Yet, the performance can degrade if the average length of the line segments is large. One way to overcome this problem is to adjust the size of the slot to the average line length while maintaining a linked list of line segments in every slot. This last technique resembles the well-known technique of hashing with collision resolution by separate chaining [13].

V. EXPERIMENTAL RESULTS

This section presents timing results of our system and shows results of an exhaustive analysis of defect-fault information based on the faults extracted from the layouts. All previously mentioned algorithms were implemented in C on an HP-9000/835 minicomputer.

As a set of examples a series of benchmarks<sup>1</sup> were implemented in a standard cells place and route approach [43] for an NMOS technology of 6  $\mu\text{m}$  of minimum resolution features. The layout consists of six masks, namely diffusion area (nd), polysilicon (np), buried contact (nb), contact (nc), implantation (ni), and metal (nm). See Appendix II for a description of this technology file, defect mechanisms, and fault types.

<sup>1</sup>Logic benchmarks distributed by Microelectronic Center, NC (MCNC).

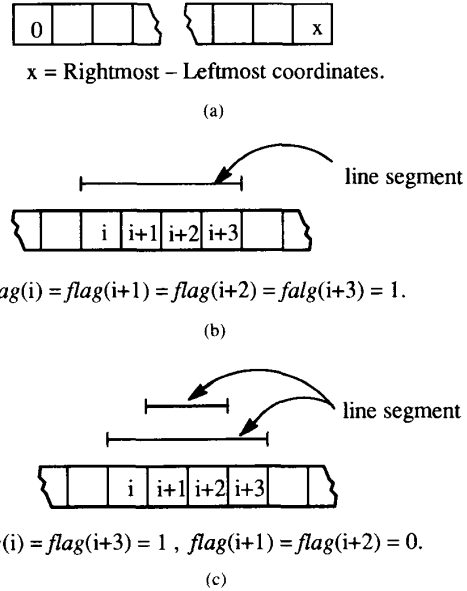


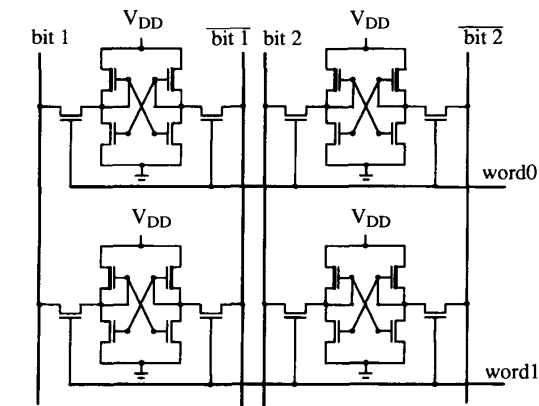
Fig. 18. Static line array. (a) Data structure. (b) INSERT operation. (c) SPLIT-DELETE operation.

TABLE I  
CPU TIME (HP-9000/835)

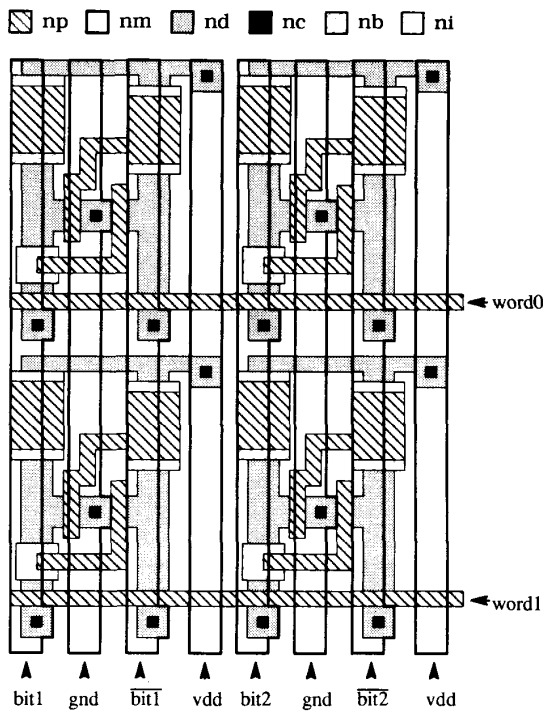
Benchmark	No. Rectangles	No. Transistors	Time (h:min:s)
f2	874	28	1:54.65
rd53	1768	65	3:55.55
radd	3091	91	7:03.28
alu2	5789	175	14:09.48
sao2	11999	281	30:30.94
9sym	15280	368	42:21.37
in6	22396	468	1:03:29.49

One of the advantages of the deterministic approach is the ability to process large layouts, of the order of tens of thousands of rectangles, in a relatively short CPU time. Table I shows the CPU time for each benchmark. Notice that the running time is proportional to the number of rectangles in an almost linear relationship. The examples were run for five different defect sizes, ranging from 7  $\mu\text{m}$  to 19  $\mu\text{m}$  in interval steps of 3  $\mu\text{m}$ . Only the critical area per defect mechanism without partial computation of intersected critical areas per node and fault type were computed. The range of defect sizes gives a good characterization of conditions prevailing in the manufacturing line, provided that the defect sizes obey the  $1/x^3$  [39] defect size distribution. The computed critical areas can further be used for estimating yield on an analytical basis. As another example, the four memory cells shown in Fig. 19 were analyzed for defect sizes ranging from 0  $\mu\text{m}$  to 100  $\mu\text{m}$ . The critical regions for intrusion, protrusion, and isolated defects in polysilicon for a defect size of 10  $\mu\text{m}$  are displayed in Fig. 20. Both vertical and horizontal defect effects can be observed from this figure. For instance, vertical effects in Fig. 20(a) appear in the form of crosses





(a)

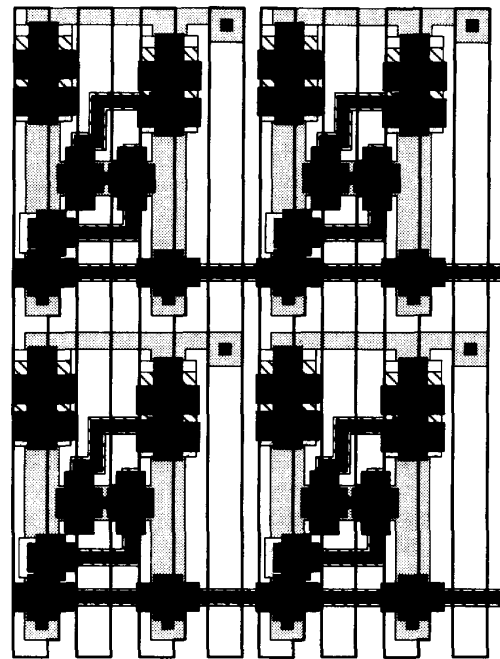


(b)

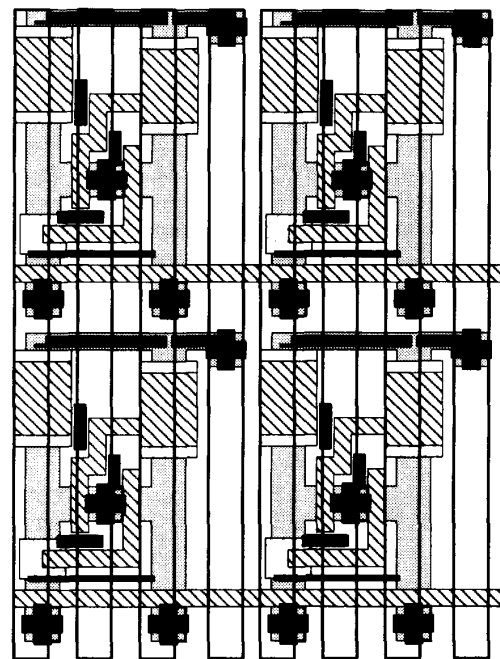
Fig. 19. (a) Schematic diagram of four SRAM cells. (b) Corresponding layout.

owing to vias or to enhancement transistors, and in the form of double crosses in the upper sections of each cell owing to depletion transistors and buried contacts. In Fig. 20(b) the crosses appear when an isolated spot of polysilicon hampers the contact between metal and diffusion; the critical regions in the upper section of each cell are the places where parasitic transistors can be formed.

The design's defect sensitivity for protrusion, intrusion, and isolated spot defects is shown in the histograms of Fig. 21. Worthwhile noticing is that the histograms show that defects smaller than the minimum resolution features can also be catastrophic. These defects appear in



(a)



(b)

Fig. 20. Multilayer critical regions in the poly layer for a defect size of 10  $\mu\text{m}$ . (a) Intrusion defects. (b) Protrusion and isolated spots.

layer crossings, transistor's gate areas, vias, etc. Finally, we selected two cases showing the results of defect-fault diagnosis of the memory cells. The histogram of Fig. 22(a) shows the sensitivity for a short circuit among *bit 1*,  $V_{DD}$ , and ground. This is a case where only one defect

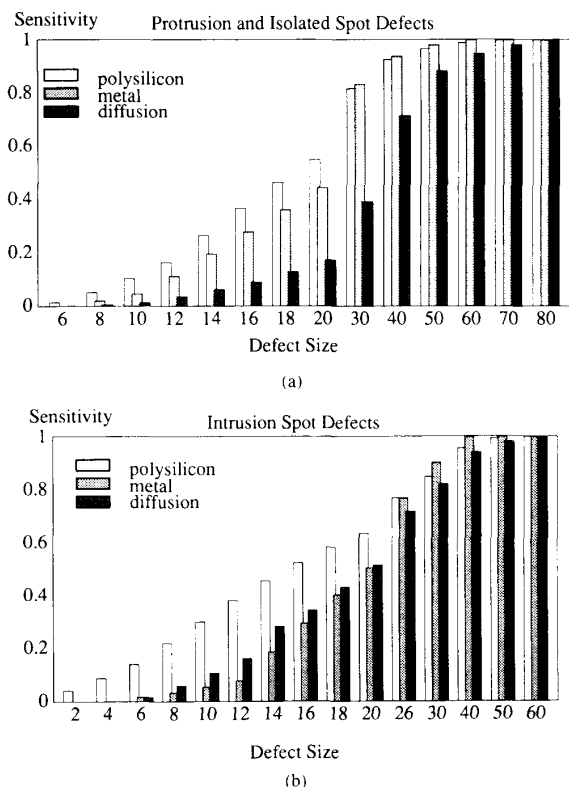


Fig. 21. Defect sensitivity of the SRAM. (a) Protrusion and isolated spot defects. (b) Intrusion defects.

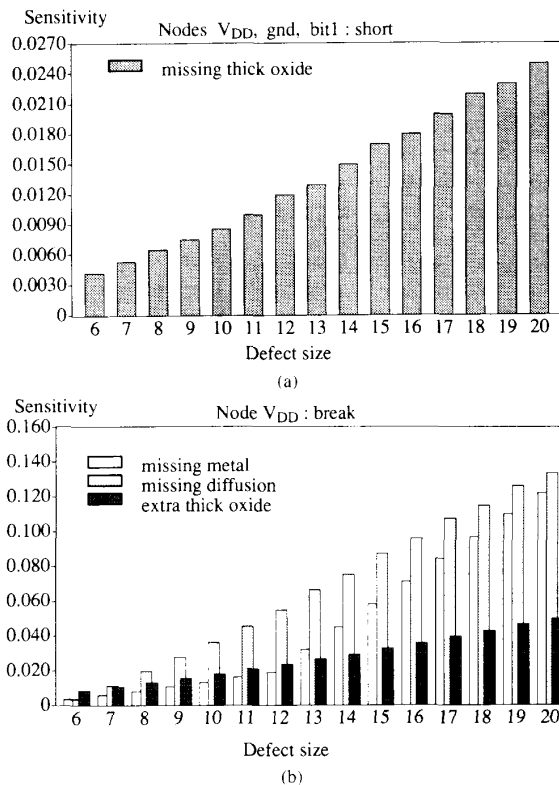


Fig. 22. Defect-fault sensitivity. (a) A short among nodes  $V_{dd}$ , ground and  $bit\ 1$ . (b) A break in node  $V_{dd}$ .

affects several nodes, inducing the same kind of fault. For this particular layout, the fault occurs for the three nodes simultaneously when an intrusion defect of thick oxide appears in the upper left corner of each memory cell. The histogram of Fig. 22(b) shows the sensitivity of a break between the memory cells and power supply. This break occurs when intrusion defects of the metal and diffusion layers, and when isolated spot defects of thick oxide, in the form of extra material, appear simultaneously in the via in the upper right corner of each memory cell. This case is the opposite of the previous one in the sense that three different defect mechanisms induce the same fault.

### VI. SUMMARY AND DISCUSSIONS

Design reliability can largely be improved by measuring the sensitivity of IC designs to spot defects. Smarter strategies for yield improvement can be devised by knowing the defect sensitivity of the design, i.e., module allocation with balanced sensitivities, design rule optimization with defect sensitivity in mind, etc. Furthermore, testing can be improved by knowing a realistic set of faults (induced by spot defects) weighted according to their defect sensitivity in the actual layout. In a similar way, manufacturing diagnosis can also be achieved by characterizing the specific defects with their specific induced faults from actual results of functional fault testing.

This paper described a formal theory to model footprint spot defects. It was shown that by modeling defects as square shaped objects simple and fast algorithms can be derived. Based on a theoretical foundation of defect semantics and technology characterization, a comprehensive theory for multilayer critical area determination was developed. This approach allows us to highlight the defect sensitivity of the circuit (not just of the layout) as a function of the defect models. Hence, the physical meaning of defects is captured not only by its placement in a single layer but rather by means of the effect that they have in several layers.

The timing results of the benchmarks show that solving the problem of finding critical areas still requires a very intensive consumption of CPU resources, even though a deterministic approach was followed. Yet, the problem is largely alleviated compared with Monte Carlo approaches, where even small circuits with only a few tens of transistors require hours. We can state, however, that the running times of our approach remain in the domain of times employed by most layout-analysis tools, such as DRC, ERC, and routers.

An important issue that can be derived from this presentation is that yield can be estimated using defect-sensitivity results in combination with some analytical formula without having to recur to full simulations. This approach is a good compromise between pure simulations

and pure analytical analyses. Furthermore, the defect-fault information and the actual visualization of critical regions on a layout image ease tasks such as manufacturing process diagnosis, design safety improvement, and quality of test pattern generation.

Although in reality every defect is a 3-D object, the majority of defects found in the manufacturing lines have predominantly 2-D effects. The concept of critical areas then becomes inappropriate if we are to model three-dimensional spot defects. Under this situation we encounter three degrees of freedom for modeling defects, namely  $x$ ,  $y$ , and  $z$  coordinates. It would thus be necessary to "re-word" the concept to what perhaps should be called critical volumes.

#### APPENDIX I

##### APPROXIMATION OF CRITICAL AREAS

The critical area and the errors introduced by the bridge model of subsection III-C-2 will be derived here. All terminologies and conventions remain the same. Fig. 10(b) is used as a reference. Solving (14) for  $y$ , the exact critical area is computed as

$$\text{Area} = (L + \delta)w + 2(A_{\text{real}}) \quad (\text{A1a})$$

where

$$A_{\text{real}} = \int_0^f |\sqrt{\Phi_b^2 - x^2} - (-\sqrt{\Phi_a^2 - x^2} + s - \delta)| dx \quad (\text{A1b})$$

and  $w$  is derived as follows:

$$w = \text{pos}(\beta) + \frac{\delta}{2} + \Phi_b - \left( \text{pos}(\alpha) - \frac{\delta}{2} - \Phi_a \right). \quad (\text{A1c})$$

Given that the magnitude of the external site between both patterns is obtained as

$$s = \text{Mag}(E) = \text{pos}(\alpha) - \text{pos}(\beta)$$

(A1c) results in

$$w = \delta - s + \Phi_a + \Phi_b. \quad (\text{A1d})$$

For the computational model of critical areas established in subsection III-C-2, the approximated area is estimated as follows:

$$\text{Area}' = (L + \delta)w + 2(A_{\text{estimated}}) \quad (\text{A2a})$$

where

$$\begin{aligned} A_{\text{estimated}} &= \int_0^{\min(\Phi_a, \Phi_b)} w dx \\ &= \int_0^{\min(\Phi_a, \Phi_b)} (\delta - s + \Phi_a + \Phi_b) dx. \end{aligned} \quad (\text{A2b})$$

The magnitude of the error incurred in this approximation is calculated by

$$\text{error} = \left| \frac{\text{Area} - \text{Area}'}{\text{Area}} \right| = \left| \frac{2(A_{\text{estimated}} - A_{\text{real}})}{(L + \delta)w + 2A_{\text{real}}} \right|. \quad (\text{A3})$$

For  $\Phi_a + \Phi_b = c$ , where  $c$  is a constant, the worst-case error appears when  $\delta \leq s - \max(\Phi_a, \Phi_b)$  and  $\Phi_a = \Phi_b$ , because for certain  $\delta$  and  $s$  satisfying the previous conditions,  $A_{\text{estimated}}$  and  $A_{\text{real}}$  take a maximum and a minimum value, respectively. In order to simplify the manipulation of (A3) the upper bound of the integrals take the value  $\Phi_a$ . In the case of (A1b)  $A_{\text{real}}$  results in an even smaller area. Thus, the error will be even more pessimistic. By substituting  $\Phi_a = \Phi_b$  in (A1a) and (A2b) and after algebraic simplifications, (A3) results in

$$\begin{aligned} \text{error} &= \left| \frac{4 \int_0^{\Phi_a} (\sqrt{\Phi_a^2 - x^2} - \Phi_a) dx}{(L + \delta)w + 2 \int_0^{\Phi_a} (2\sqrt{\Phi_a^2 - x^2} - \Phi_a) dx} \right| \\ &= \left| \frac{(4 - \pi)\Phi_a^2}{(L + \delta)w + (\pi - 2)\Phi_a^2} \right|. \end{aligned} \quad (\text{A4})$$

By substituting the assumptions  $\delta \leq s - \max(\Phi_a, \Phi_b)$  and  $\Phi_a = \Phi_b$  in (A1d) one can see that  $w$  takes values between 0 and  $\Phi_a$ . In order to estimate the error let us observe the effect of  $w$  in (A4). For a very small  $w$  the error is relatively large; however the contribution of the computed area to the total critical area is insignificant. For a large  $w$  the error is simply very small. Also with the assumption that  $L \gg \Phi_a$  (mostly in real layouts it is acceptable), it is easy to conclude that the error introduced is small. Since the error to all intents and purposes can be neglected, we can state that this approximation is a good compromise.

#### APPENDIX II

##### TECHNOLOGY FILE FOR NMOS PROCESS

##### (technology NMOS

##### ( masks

( <nm> \$nc \$nb ni <np> <nd> ) )

{\* nm = metal nc = contact ni = implant

nd = diffusion np = poly nb = buried contact \*}

##### ( suppress

(nc ~nm ~np ~nd ~nb)

(nc ~nm np nd )

(nm nc np nd ~nb)

(nb ~np ~nd ~nm)

(ni ~np ~nd ~nm ~nc ~nb) )

##### ( structures

(poly\_metal <np> <nm> ~nd ~nc)

(dif\_metal ~np <nd> <nm> ~nc)

(poly\_via nc <nm np> ~nd)

(dif\_via nc <nm nd> ~np)

(buried\_via <np nd> nb ~nc)

(pdm\_via <nm nd np> nb nc)

(poly\_track <np> ~nd ~nm)

(dif\_track ~np <nd> ~nm)

(metal\_track ~np ~nd <nm>)

```

(enh_xtor
 (trans_1 ~ni <np #nd> ~nm ~nb ~nc)
 (trans_2 ~ni <np #nd> <nm> ~nb ~nc))
(dep_xtor
 (trans_1 ni <np #nd> ~nm ~nb ~nc)
 (trans_2 ni <np #nd> <nm> ~nb ~nc))
)
(defects (7 19 1)
(poly_metal
 (np (*nc 1.0 short) )
 (nm (*nc 1.0 short) ))
(dif_metal
 (nd (*nc 1.0 short) )
 (nm (*nc 1.0 short) ))
(poly_via
 (np (-np 0.0 break))
 (nc (-nc 0.5 break))
 (nm (-nm 0.0 break)) )
(dif_via
 (nd (-nd 0.0 break) (+np -1.0 float_line) (*np 0.0 float_line))
 (nc (-nc 0.5 break))
 (nm (-nm 0.0 break)) )
(buried_via
 (nd (-nd 0.0 break))
 (nd (-nb 0.5 break))
 (np (-np 0.0 break)) )
(poly_track
 (np (-np 0.0 break) (+np 0.0 short) (+nd -1.0 new_device)))
(dif_track
 (nd (-nd 0.0 break) (+np -1.0 new_device) (*np 0.0 new_device)
 (+nd 0.0 short)))
(metal_track
 (nm (+nm 0.0 short) (-nm 0.0 break)))
((enh_xtor
 (trans_1
 (nd (*nb 0.5 miss_device) (*ni 0.5 new_device))
 (np (*nb 0.5 miss_device) (-np 0.5 miss_device)) )))
((dep_xtor
 (trans_1
 (ni (-ni 0.5 miss_device))
 (nd (*nb 0.5 miss_device))
 (np (*nb 0.5 miss_device) (-np 0.5 miss_device) ) )))
)
)

```

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